Title	**86 W Automotive Power Supply for 800 V Systems Using InnoSwitch™3-AQ INN3949CQ**
Specification	300 VDC – 900 VDC Input; 13.5 V / 6.37 A Output
Application	Auxiliary Equipment Power Supply
Author	Automotive Systems Engineering Department
Document Number	RDR-952Q
Date	February 28, 2025
Revision	A

Summary and Features

- Ultra-compact design for 800 VDC automotive BEV applications
- Low component count (only 62 electrical components)
- Wide-range start-up and operating voltage from 300 VDC to 900 VDC[1]
- Transformer provides 900 V reinforced isolation (IEC-60664-1 and IEC-60664-4 compliant)
- ≥92% full-load efficiency across the input voltage range
- ≤1% line and load regulation
- Secondary-side control without optocouplers
- Ambient operating temperature range: -40 °C to 85 °C
- Comprehensive fault protection, including output current limit and short-circuit
- Uses automotive-qualified AEC-Q surface-mount (SMD) components[2]
- Low profile, 22 mm height

[1] Derated power below 300 VDC input.
[2] AEC-Q200 transformer qualification and AEC-Q qualified SR MOSFET selection belongs to final design.

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No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations, or opinions communicated and any liability for any direct, indirect, or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

1 Introduction

This engineering report describes an 86 W single-output automotive power supply. It is intended for use in 800 V battery powered electric vehicles and supports a wide input range of 300 VDC to 900 VDC. This design uses the 1700 V rated INN3949CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (low-voltage output) sides by complying with creepage and clearance requirements described in IEC-60664 parts 1 and 4.

This document contains the power supply specifications, schematic, printed circuit board (PCB) layout, bill of materials (BOM), specification for the magnetics, and performance data.

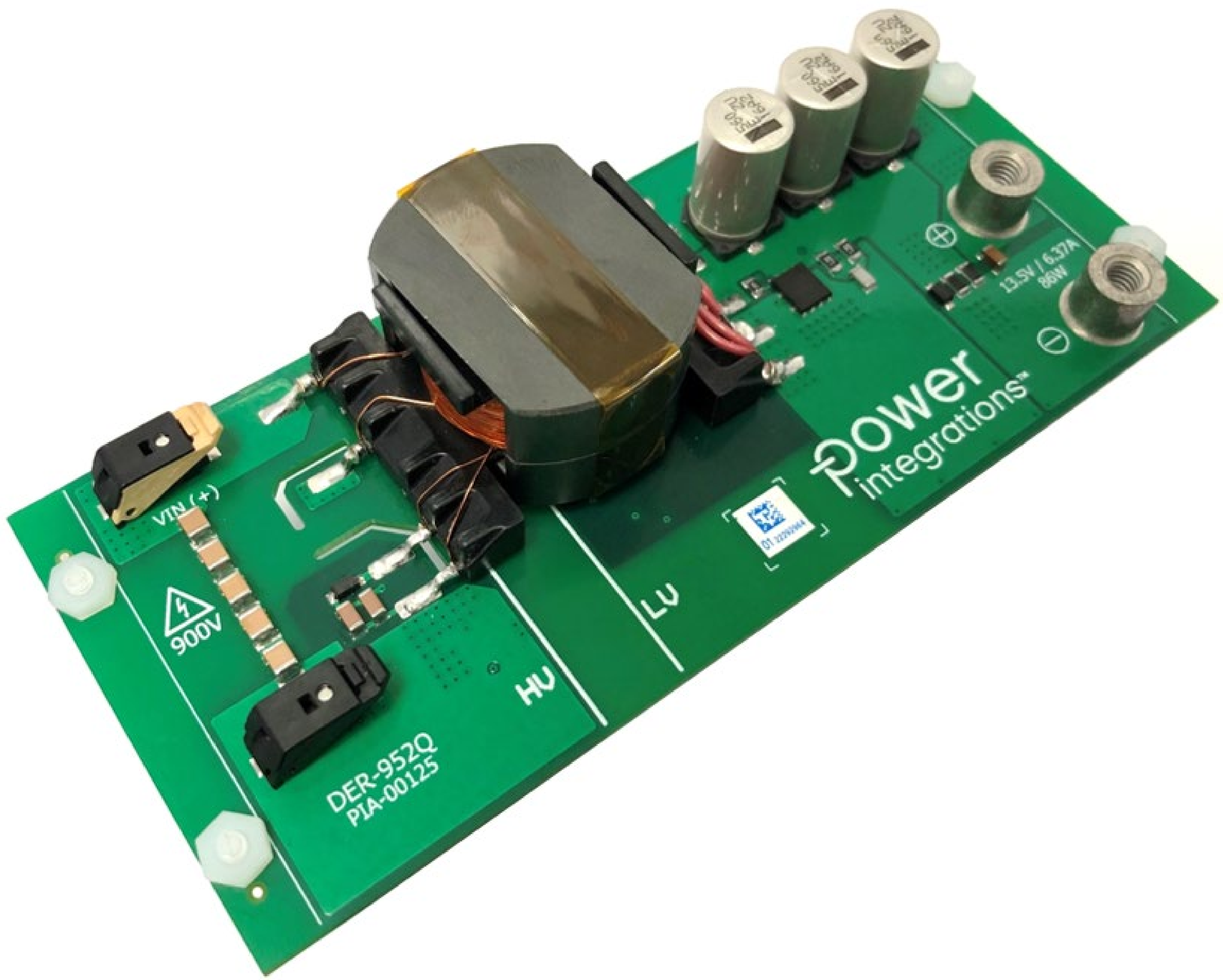


Figure 1 – Populated Circuit Board, Entire Assembly.

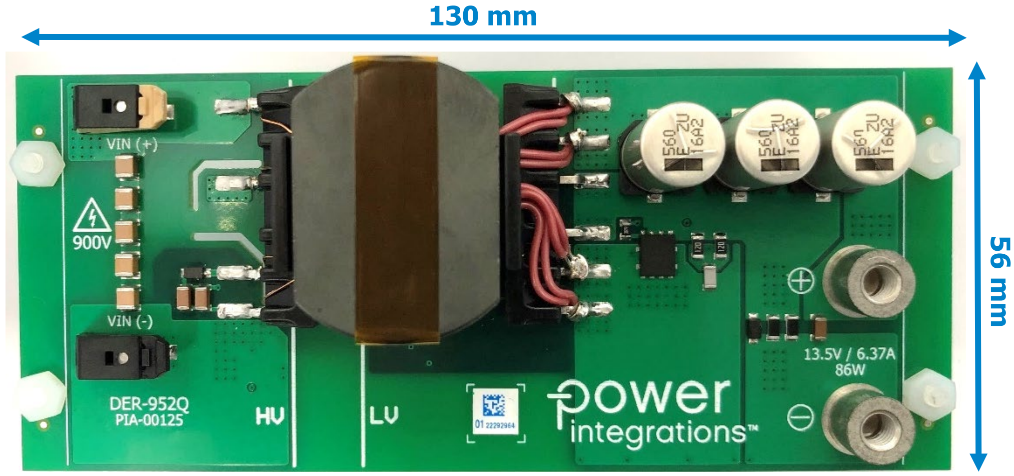


Figure 2 – Populated Circuit Board, Top.

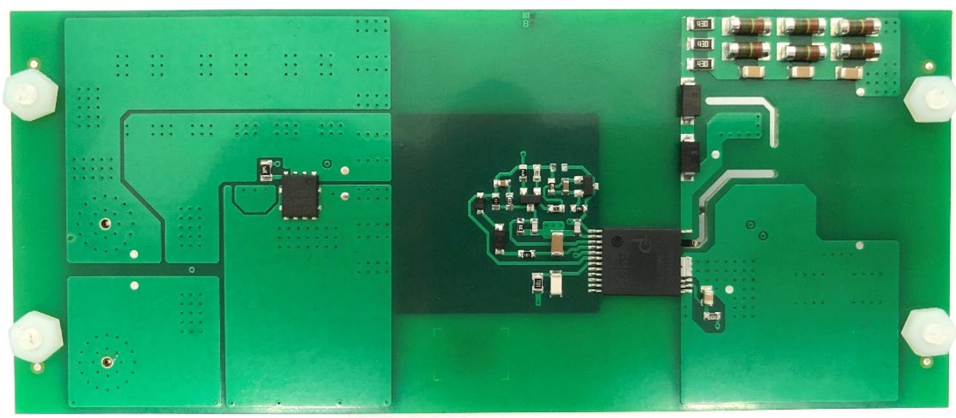


Figure 3 – Populated Circuit Board, Bottom.

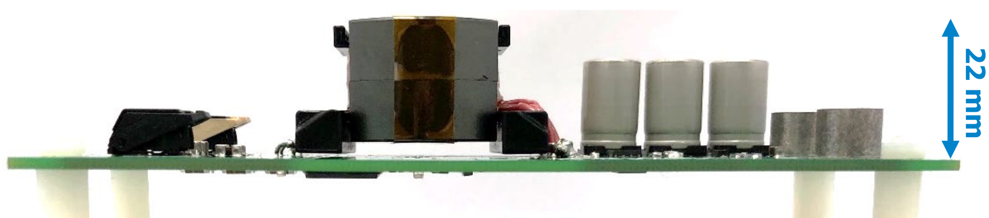


Figure 4 – Populated Circuit Board, Side.

The design can deliver the rated 86 W output power at 85 °C ambient from 300 VDC to 900 VDC input voltage range. The 13.5 V output allows the power supply to replace a vehicle's auxiliary battery to provide power for the vehicle's 12 VDC system.

The InnoSwitch3-AQ IC maintains regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink™ magneto-inductive coupling. The secondary-side controller also provides gate drive for synchronous rectification improving overall efficiency (compared to conventional diode rectifier), thus saving space by eliminating heatsinks.

2 Design Specification

The following tables represent the minimum acceptable performance of the design. Actual performance is listed in the results section.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV**	300	800	900	VDC
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	V_{OUT}	13.4	13.5	13.6	VDC
Output Voltage Load and Line Regulation	V_{REG}	-1		+1	%
Ripple Voltage Measured on Board	V_{RIPPLE}			500	mV
Output Current Parameters					
Output Current	I_{OUT}		6370		mA
Output Power Parameters					
Continuous Output Power at 300 VDC – 900 VDC Input	P_{OUT}		86[3]		W
Output Overshoot and Undershoot During Dynamic Load Condition	ΔV_{OUT}	-5		+5	%
Operating Parameters					
Operating Switching Frequency	f_{SW}	25		38	kHz

Table 1 – Electrical Specifications.

[3] For maximum output power capability at V_{IN} less than 300 V, see Section 13.

2.2 Isolation

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3949CQ	BV_{DSS}			1700	V
System Voltage	V_{SYSTEM}			1370	V
Working Voltage	$V_{WORKING}$			900	V
Pollution Degree	PD			2	
CTI for FR4	CTI	175			
Rated Impulse Voltage	$V_{IMPULSE}$			2.5	kV
Altitude Correction Factor for h_a	c_{ha}	1.59			
Basic Clearance Distance Requirement	CLR_{BASIC}	2.4			mm
Reinforced Clearance Distance Requirement	$CLR_{REINFORCED}$	4.8			mm
Basic Creepage Distance Requirement for PCB	$CPG_{BASIC(PCB)}$	5.4			mm
Reinforced Creepage Distance Requirement for PCB	$CPG_{REINFORCED(PCB)}$	10.8			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60 s	V_{ISO}	3536			V_{RMS}
Partial Discharge Test Voltage	V_{PD_TEST}	1860			V_{PK}

Table 2 – Isolation Coordination[4].

2.3 Environmental Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		85	°C
Altitude of Operation	ha			5500	m
Relative Humidity	Rh			85	%

Table 3 – Environmental Specifications.

[4] Clearance and creepage distances were derived from IEC 60664-1 and IEC 60664-4.

3 Schematic[5]

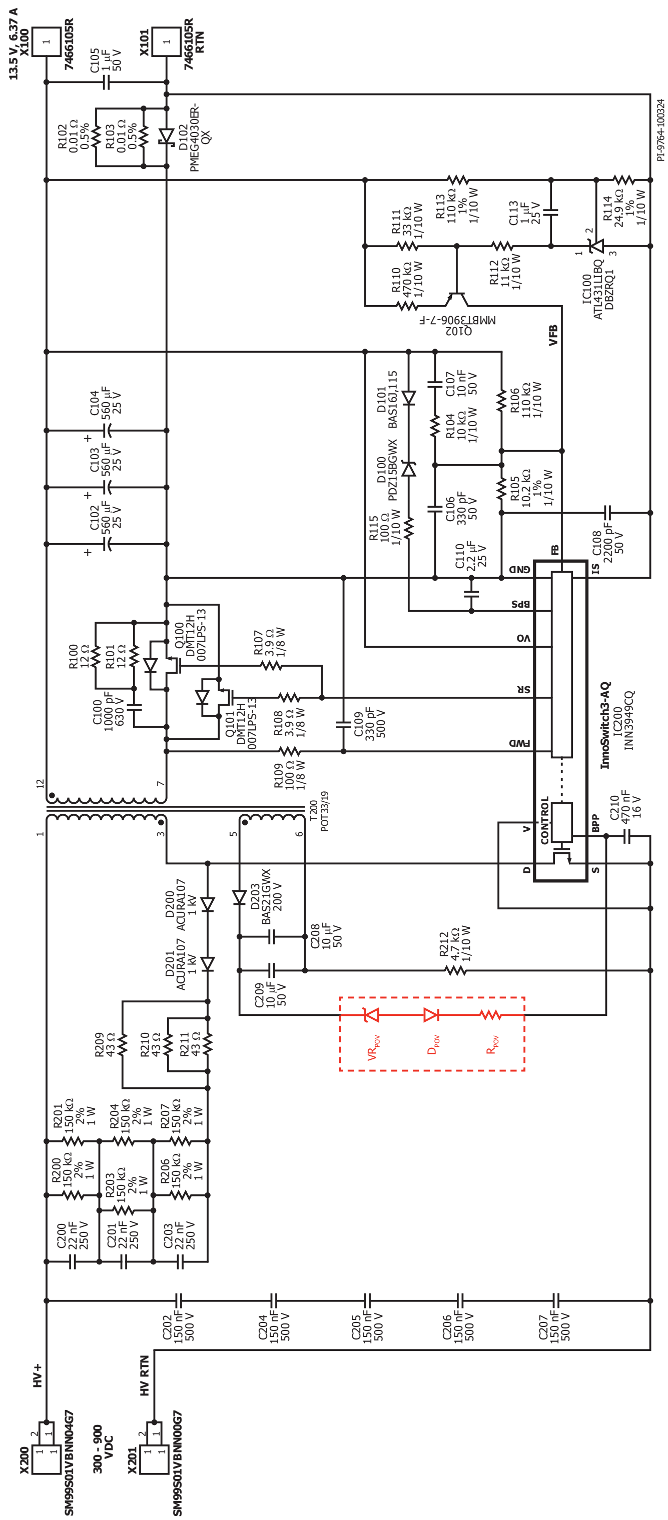


Figure 5 – Schematic.

[5] The primary side overvoltage protection circuit (VR_{POV}, D_{POV}, and R_{POV}) is not included in RDK-952Q board but is recommended for functional safety.

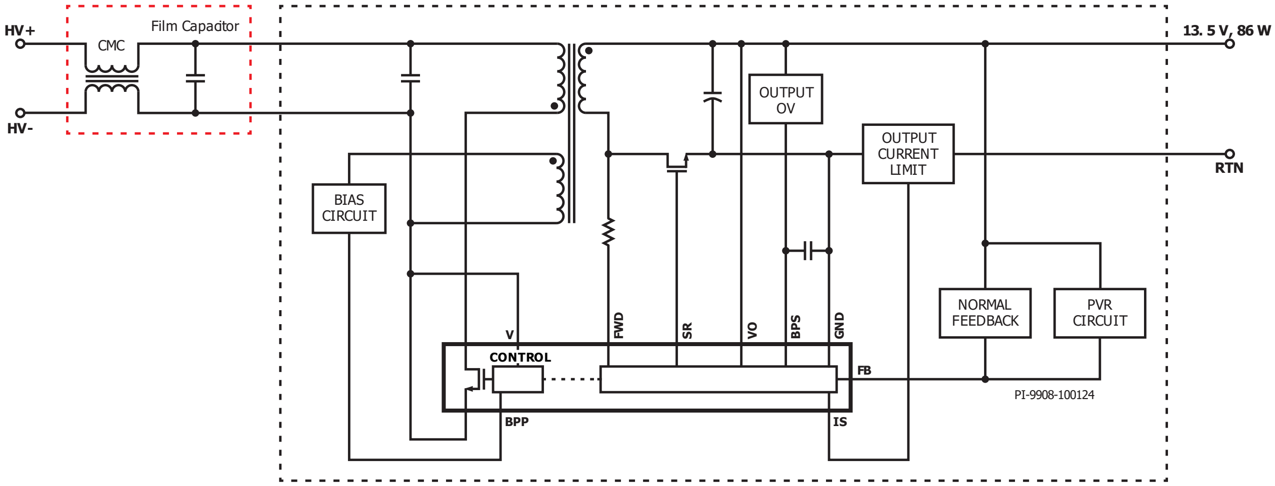


Figure 6 – Application with CMC and Film Capacitor Block Diagram.[6]

[6] Addition of the external CMC and film capacitor is optional. The CMC and film capacitor are only necessary if there is a need to protect the unit from common-mode noise. The film capacitor is added with the CMC to reduce CMC ripple current for lower losses and operating temperature. Filter component values should be calculated based on system application requirements.

4 Circuit Description

4.1 Input Filter

Bypass capacitors C202, C204, C205, C206, and C207 help filter input noise and are used to minimize the primary-side current loop. The capacitors are selected so as not to exceed 65% of their voltage rating as well as to maintain enough pad separation to enable a design that meets creepage and clearance requirements.

4.2 High-Voltage Circuit

The power supply is a flyback converter that provides an isolated low-voltage output from the high-voltage input. The primary winding of the flyback transformer (T200) is connected between the high-voltage DC input and the drain terminal of the integrated 1700 V SiC power switch in the InnoSwitch3-AQ IC (IC200).

An R2CD-type snubber circuit is placed across the primary winding to limit the drain-source voltage peak during turn-off. Two super-fast (or better) surface-mount, AEC-Q qualified diodes (D200 and D201), are placed in series to meet creepage and clearance requirements. This also ensures that the reverse voltage across the diodes will not exceed 70% of their maximum rating. Capacitors C200, C201, and C203 store the energy from the leakage inductance of transformer T200. The capacitors are sized to minimize the voltage ripple across the snubber resistor network and maintain near-constant power dissipation through the switching cycle. Resistors R200, R201, R203, R204, R206, and R207 dissipate the energy stored by the snubber capacitors. The resistor values are selected so that their average voltage will not exceed 80% of their maximum rated voltage and to dissipate less than 50% of their rated power.

The InnoSwitch3-AQ IC (IC200) is self-starting, using an internal high-voltage current source to charge the BPP capacitor, C210. The INN3949CQ IC will operate at 30 V input but can typically start below this level.

The auxiliary winding of transformer T200 provides power to the primary-side during normal operation. This improves efficiency and reduces heating of the InnoSwitch3-AQ IC. The output of the auxiliary winding is rectified and filtered by diode D203 and capacitors C208 and C209. The filtered (DC) voltage is fed to the BPP pin through resistor R212.

In this design, the input UV and OV features are disabled by shorting the V pin to the SOURCE pin.

4.3 Low-Voltage Circuit

The secondary-side of the InnoSwitch3-AQ IC provides output voltage sensing, output current sensing, and gate drive for the synchronous rectification MOSFET (SR FET). SR FETs Q100 and Q101 rectify the voltage across the secondary winding of the transformer T200. The rectified voltage is then filtered by output capacitors C102, C103, C104, and C105. An RC-type snubber formed by resistors R100, R101 and capacitor C100 damps high-frequency ringing across the Drain-Source nodes of the SR FET.

The secondary-side controller inside the InnoSwitch3-AQ IC controls the switching of the SR FETs. Timing is based on the negative edge voltage transition sensed by the FWD pin via resistor R109. Capacitor C109 and resistor R109 form a low-pass filter that reduces voltage spikes seen by the FWD pin and ensures that the maximum rating of 150 V is not exceeded.

In continuous conduction mode operation, the SR MOSFET is turned off just before the secondary-side controller requests a new switching cycle from the primary. In discontinuous conduction mode, the SR MOSFET is turned off when the voltage across it exceeds $V_{SR(TH)}$ (~-3.3 mV). Secondary-side control of both SR MOSFET and primary-side switch prevents cross-conduction and ensures reliable SR operation.

The secondary-side of the InnoSwitch3-AQ IC is powered by either the secondary winding forward voltage (thru R109 and the FWD pin) or by the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C110 via an internal regulator.

Diodes D100, D101, and resistor R115 form the secondary-side output overvoltage protection circuit. During output overvoltage events, the diodes turn on, and current is injected into the BPS pin of InnoSwitch3-AQ IC, triggering AR. This network protect for faults on the secondary when the secondary controller is functional. When the secondary controller is not functional, the primary side BPP pin based output OV function is recommended.

The InnoSwitch3-AQ IC has an internal reference of 1.265 V appearing on the FB pin. Resistors R105, and R106 form the basic voltage divider feedback network for InnoSwitch3-AQ designs. However, for this design, the output voltage set by R105 and R106 is 10 – 15 % higher than the target output voltage to support operation of the Precise Voltage Regulation circuit. Capacitor C106 provides decoupling to eliminate high-frequency noise. Capacitor C107 and R104 form a feedforward network to speed up response time and reduce output ripple.

Output current is monitored via the voltage drop across parallel resistors R102 and R103, filtered by decoupling capacitor C108. This voltage representation of the output current is compared to the ~35 mV threshold of the IS pin (referenced to SECONDARY GROUND pin) to reduce losses. Once the threshold is exceeded, the InnoSwitch3-AQ IC200 will adjust the number of pulses to maintain a fixed current output (CC mode). The IC will enter auto-restart (AR) operation when the output voltage is below 90% of regulation and recover when the load current is reduced below the CC limit. Schottky diode D102 limits the voltage across the IS pin to protect it during output short-circuits.

4.4 Precision Voltage Regulation (PVR) Circuit[7]

The PVR circuit improves output voltage regulation by using an external error amplifier with a high-precision reference voltage (ATL431) to bias the FB pin. The PVR injects a DC

[7] Circuit implementation is optional. Application is only necessary if there is a need for output voltage regulation within 1%.

bias current into the FB pin of InnoSwitch3-AQ IC to reduce the DC error at the output. The ATL431 error-amplifier network is placed after the current sense resistor to also compensate for the voltage drop of the sense resistor.

The ATL431LIBQDBZRQ1 voltage reference IC is selected for its high precision and stability across temperatures. The output voltage is measured via a voltage divider formed by R113 and R114. The resistor values are chosen such that at the rated output voltage, the voltage at the reference pin of the ATL431 IC equals its reference voltage of 2.5 V. The shunt regulator in the ATL431 IC sinks cathode current proportional to the difference between the scaled output voltage and its internal reference. The amplitude of the cathode current controls the amount of current injected into the FB pin of the InnoSwitch3-AQ IC. Capacitor C113 together with resistor R113 forms an integrator to ensure that the PVR circuit only corrects for DC error.

Resistor R111 and R112 provide path for the base current of Q102 and the bias current for IC100. Together with R110, the values of these resistors are chosen such that IC100 and Q102 are kept away from saturation and provide an adequate allowance for the base and cathode currents to swing during transient load events. While operating in the forward active region, Q102 acts as a variable impedance in parallel to the upper feedback resistor R106.

5 PCB Layout

Layers:	Six (6)
Board Material:	FR4
Board Thickness:	1.6 mm
Copper Weight:	1 oz

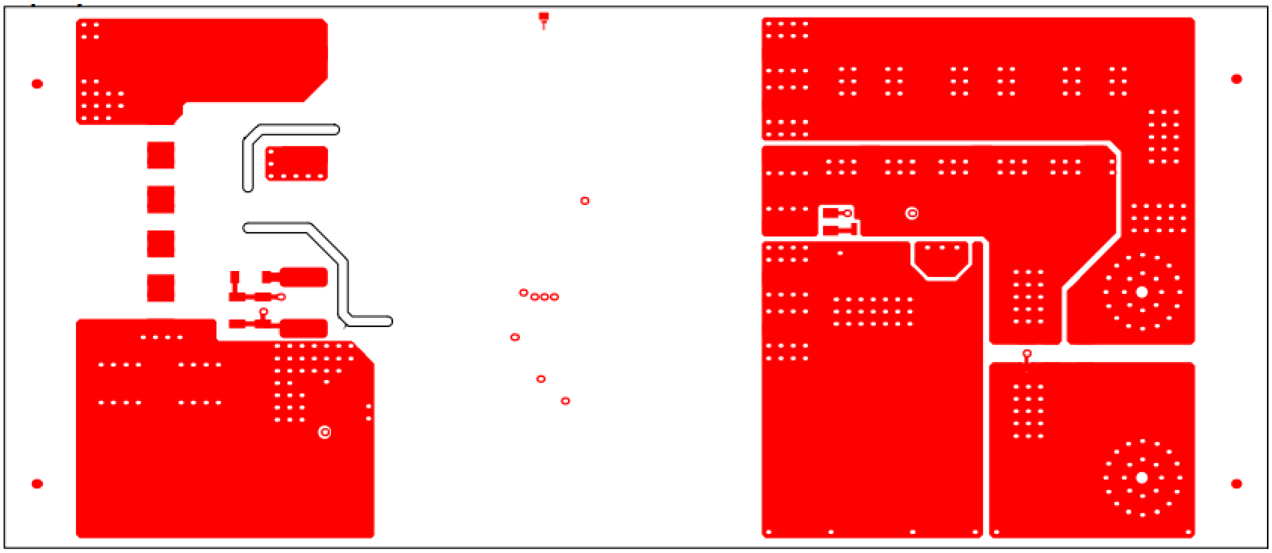


Figure 7 – Top Layer PCB Layout.

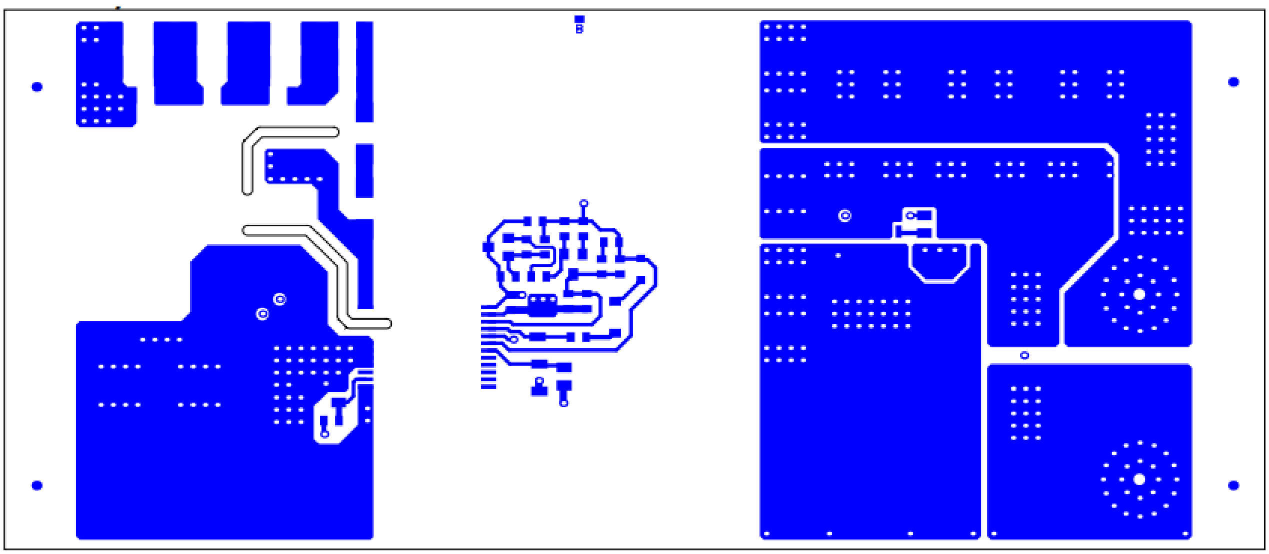


Figure 8 – Bottom Layer PCB Layout.

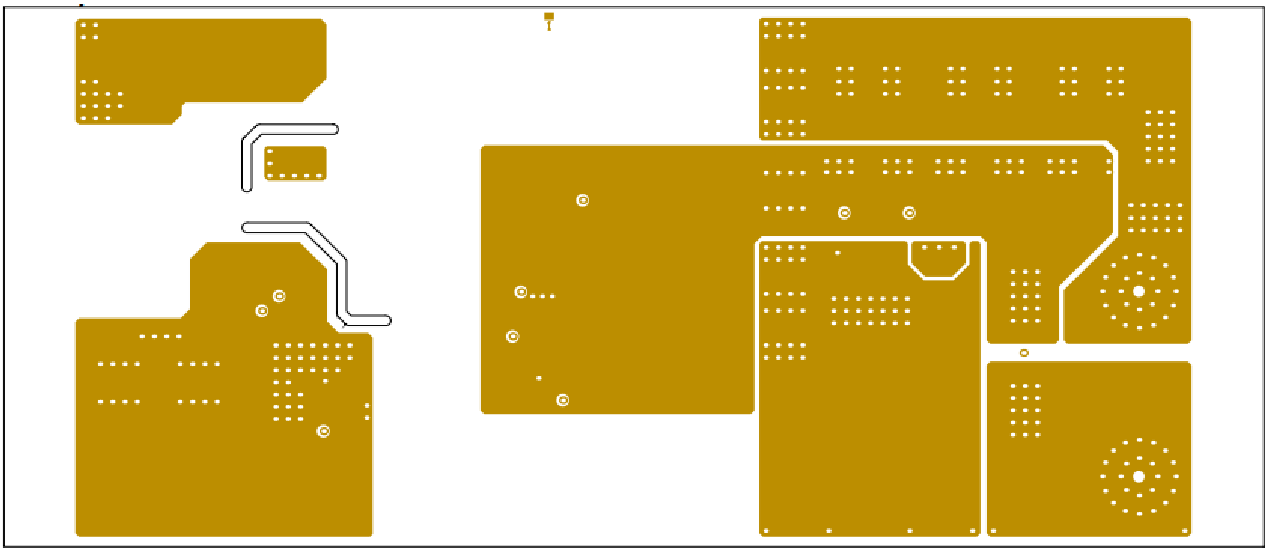


Figure 9 – Mid-Layer 1 PCB Layout

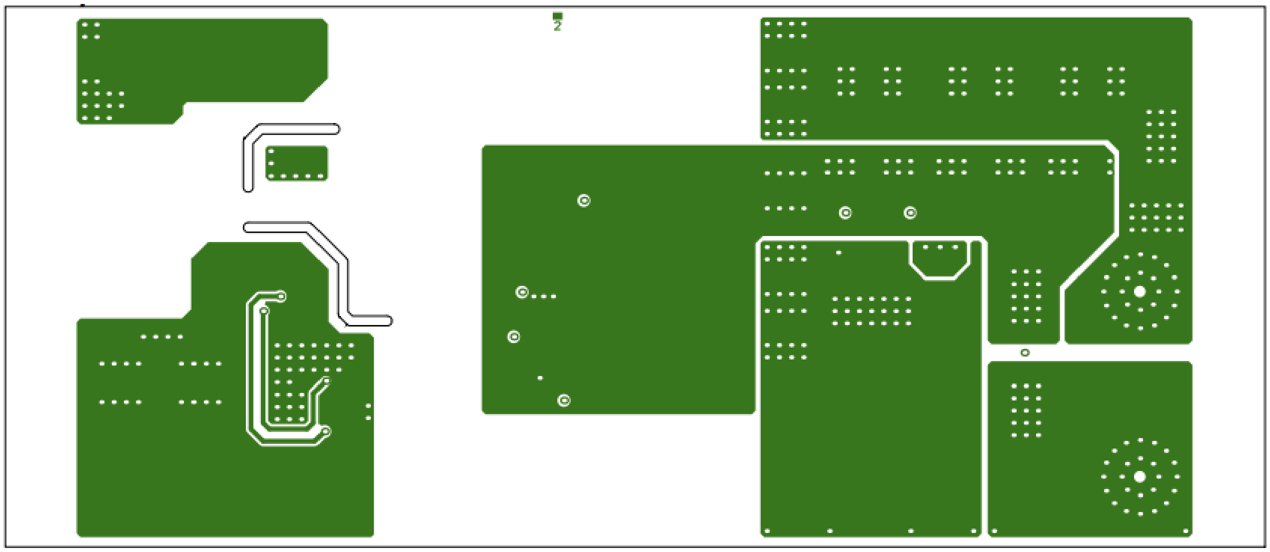


Figure 10 – Mid-Layer 2 PCB Layout.

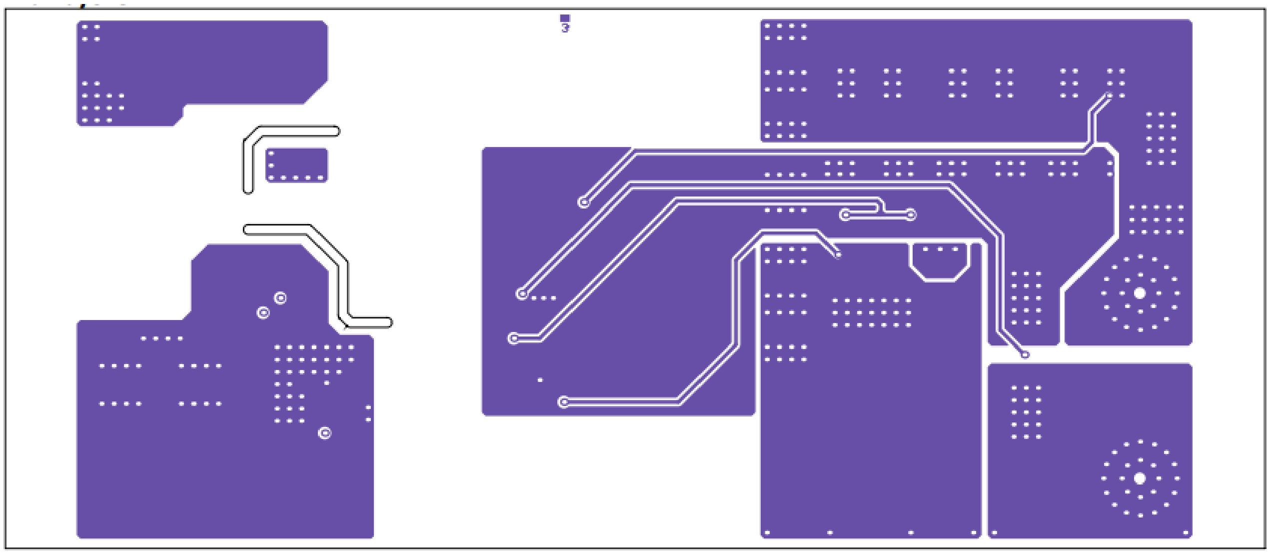


Figure 11 – Mid-Layer 3 PCB Layout.

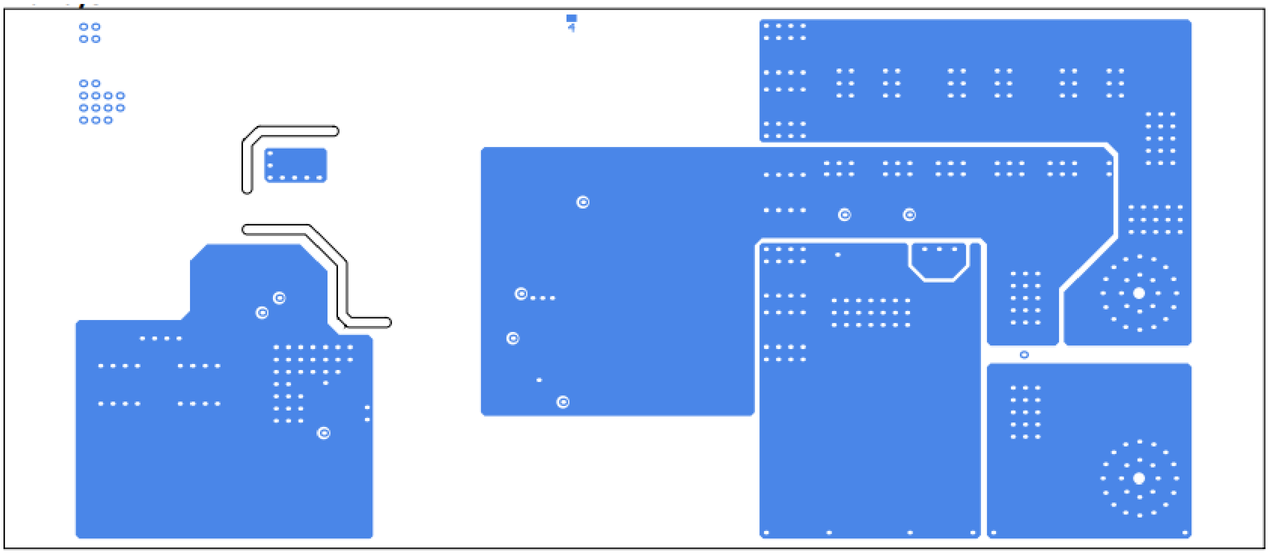


Figure 12 – Mid-Layer 4 PCB Layout.

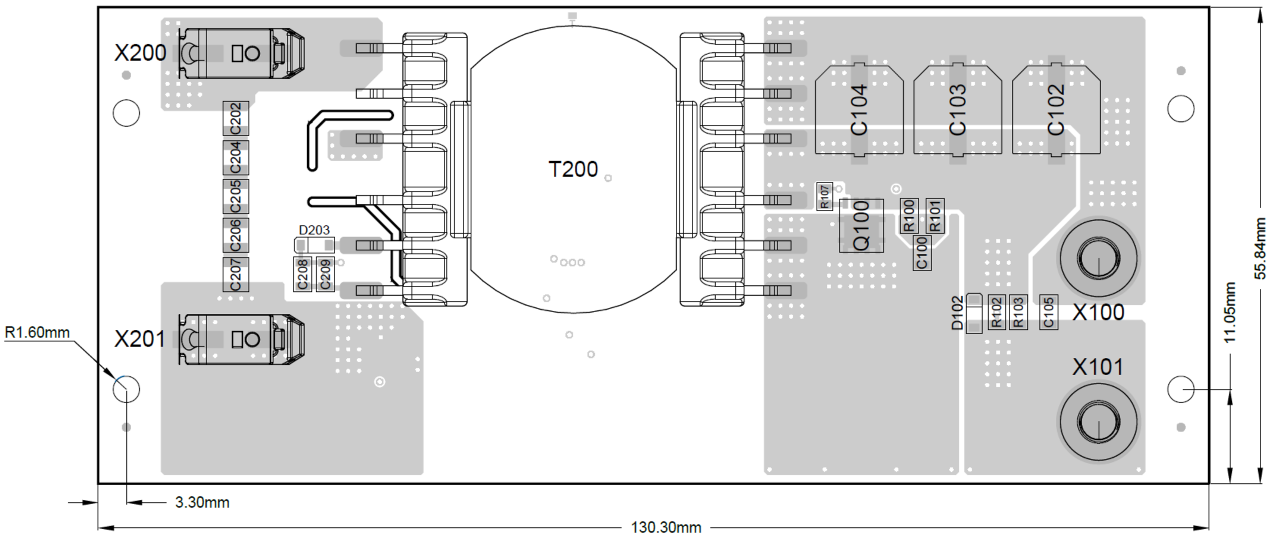


Figure 13 – PCB Assembly (Top).

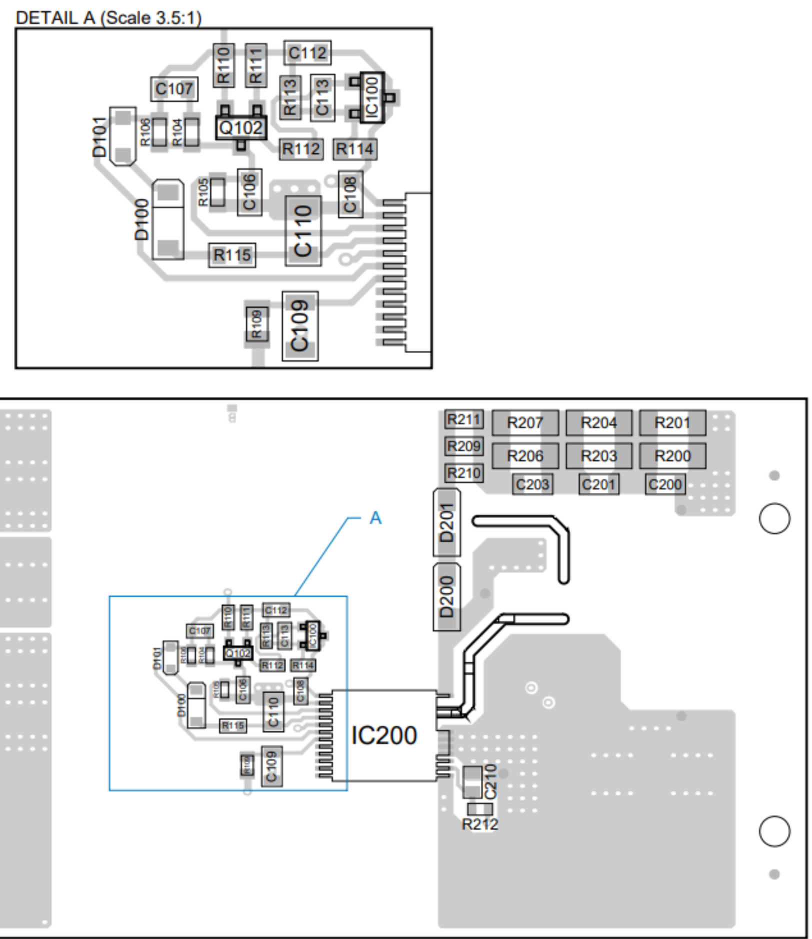


Figure 14 – PCB Assembly (Bottom).

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	1	C100	Ceramic Chip Capacitor 1000 pF C0G 630 V 5% 1206	CGA5F4C0G2J102J085AA	TDK
2	3	C102, C103, C104	Polymer Aluminum Capacitor 560 μF AL 25 V 20% 10.3X10.3mm	EEH-ZU1E561P	Panasonic
3	1	C105	Ceramic Chip Capacitor 1 μF X7R 50 V 10% 1206	CGA5L3X7R1H105K160AE	TDK
4	1	C106	Ceramic Chip Capacitor 330 pF C0G 50 V 5% 0603	CGA3E2C0G1H331J080AA	TDK
5	1	C107	Ceramic Chip Capacitor 10 nF X7R 50 V 10% 0603	C0603C103K5RACAUTO7411	KEMET
6	1	C108	Ceramic Chip Capacitor 2200 pF C0G 50 V 5% 0603	GCM1885C1H222JA16D	Murata
7	1	C109	Ceramic Chip Capacitor 330 pF C0G 500 V 10% 1206	C1206C331KCGACAUTO	KEMET
8	1	C110	Ceramic Chip Capacitor 2.2 μF X7R 25 V 20% 1206	CGA5L2X7R1E225M160AA	TDK
9	1	C113	Ceramic Chip Capacitor 1 μF X7R 25 V 20% 0603	CGA3E1X7R1E105M080AC	TDK
10	3	C200, C201, C203	Ceramic Chip Capacitor 22 nF X7R 250 V 10% 1206	GCJ31BR72E223KXJ1L	Murata
11	5	C202, C204, C205, C206, C207	Ceramic Chip Capacitor 150 nF X7R 500 V 10% 1210	C1210X154KCRACAUTO	KEMET
12	2	C208, C209	Ceramic Chip Capacitor 10 μF X7R 50 V 10% 1206	CGA5L1X7R1H106K160AC	TDK
13	1	C210	Ceramic Chip Capacitor 470 nF X7R 16 V 10% 0805	AC0805KKX7R7BB474	YAGEO
14	1	D100	Zener Diode 15 V 365 mW SOD123	PDZ15BGWX	Nexperia
15	1	D101	Diode Standard 100 V 250 mA SOD-323	BAS16J,115	Nexperia
16	1	D102	Schottky Diode 40 V 3 A SOD-123W	PMEG4030ER-QX	Nexperia
17	2	D200, D201	Diode SCHOTTKY 1 kV 1 A DO-214AC (SMA)	ACURA107-HF	Comchip
18	1	D203	Diode Standard 200 V 225 mA (DC) SMT SOD-123	BAS21GWX	Nexperia
19	1	IC100	Voltage References Automotive, high-bandwidth, low-IQ programmable shunt regulator	ATL431LIBQDBZRQ1	Texas Instruments
20	1	IC200	InnoSwitch3-AQ Vmos InSOP-24D CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3949CQ	Power Integrations
21	2	Q100, Q101	N-Channel MOSFET 120 V 90 A (Ta), 90 A (Tc) 2.9 W (Ta) PowerDI5060-8	DMT12H007LPS-13[8]	Diodes, Inc.
22	1	Q102	40 V / 0.2 A PNP bipolar transistor SOT-23	MMBT3906-7-F	Diodes, Inc.
23	2	R100, R101	Thick Film Chip Resistor 12 Ω 0.25 W 200 V 5% 1206	AC1206JR-0712RL	YAGEO
24	2	R102, R103	Current Sense Resistor 0.01 Ω 0.25 W 200 V 0.5% 1206	WSL1206R0100DEA	Vishay
25	1	R104	Thick Film Chip Resistor 10 kΩ 0.1 W 75 V 5% 0603	AC0603JR-0710KL	YAGEO
26	1	R105	Thick Film Chip Resistor 10.2 kΩ 0.1 W 150 V 1% 0603	RMCF0603FT10K2	Stackpole
27	1	R106	Thick Film Chip Resistor 110 kΩ 0.1 W 150 V 5% 0603	RMCF0603JT110K	Stackpole
28	2	R107, R108	Thick Film Chip Resistor 3.9 Ω 0.125 W 150 V 5% 0805	RMCF0805JT3R90	Stackpole
29	1	R109	Thick Film Chip Resistor 100 Ω 0.125 W 150 V 5% 0805	RMCF0805JT100R	Stackpole
30	1	R110	Thick Film Chip Resistor 470 kΩ 0.1 W 150 V 5% 0603	RMCF0603JT470K	Stackpole
31	1	R111	Thick Film Chip Resistor 33 kΩ 0.1 W 150 V 5% 0603	RMCF0603JT33K0	Stackpole
32	1	R112	Thick Film Chip Resistor 11 kΩ 0.1 W 150 V 5% 0603	RMCF0603JT11K0	Stackpole
33	1	R113	Thick Film Chip Resistor 110 kΩ 0.1 W 150 V 1% 0603	RMCF0603FT110K	Stackpole
34	1	R114	Thick Film Chip Resistor 24.9 kΩ 0.1 W 150 V 1% 0603	RMCF0603FT24K9	Stackpole
35	1	R115	Thick Film Chip Resistor 100 Ω 0.1 W 5% 0603	RMCF0603JT100R	Stackpole
36	6	R200, R201, R203, R204, R206, R207	MELF Resistors 150 kΩ 1 W 200 V 2% MELF 0207	CMB02070X1503GB200	Vishay
37	3	R209, R210, R211	Thick Film Chip Resistor 43 Ω 0.25 W 5% 1206	RMCF1206JT43R0	Stackpole
38	1	R212	Thick Film Chip Resistor 4.7 kΩ 0.1 W 150 V 5% 0603	RMCF0603JT4K70	Stackpole
39	1	T200	86 W Power Transformer		Power Integrations

[8] DMT12H007LPS-13 is not AEC-Q qualified.

40	2	T200-Core	SSP-95A POT/3319 Ferrite Core		Sunshine
41	1	T200-Bobbin	Customized bobbin		Power Integrations
42	2	X100, X101	1 Pin Screw Terminal, Power Tap M5 Surface Mount	7466105R	Würth
43	1	X200	TERM BLOCK 1POS SIDE ENTRY SMD RED	SM99S01VBNN04G7	METZ CONNECT
44	1	X201	TERM BLOCK 1POS SIDE ENTRY SMD BLACK	SM99S01VBNN00G7	METZ CONNECT

Table 4 – Bill of Materials[9].

[9] All components are AEC-Q qualified except the SR MOSFET, connectors, and transformer.

7 Transformer Specification (T200)

7.1 Electrical Diagram

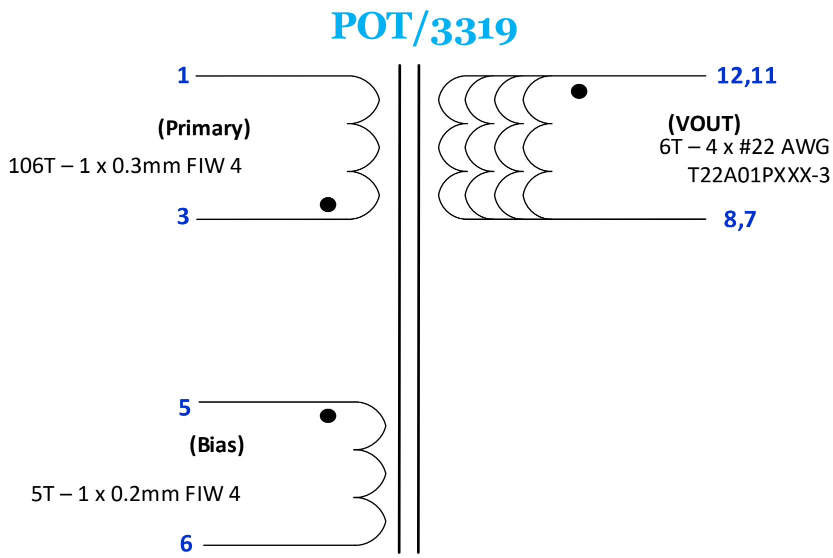


Figure 15 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			86	W
Input voltage VDC	Flyback topology	300	800	900	V
Switching frequency	Flyback topology			38	kHz
Duty cycle	Flyback topology	13.2		44.5	%
Np:Ns			17.7		
Rdc	Primary-side		1.7		Ω
Rdc	Secondary-side		6.0		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 3 to pin 7, with pins 1 - 3 shorted and pins 7 - 12 shorted at 25°C			137	pF
Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 3, with all other windings open at 25 °C		2660		μH
Part to part tolerance	Tolerance of Primary Inductance	-5.0		5.0	%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.			26.6	μH

Table 5 – Transformer (T200) Electrical Specifications.

7.3 Transformer Build Diagram

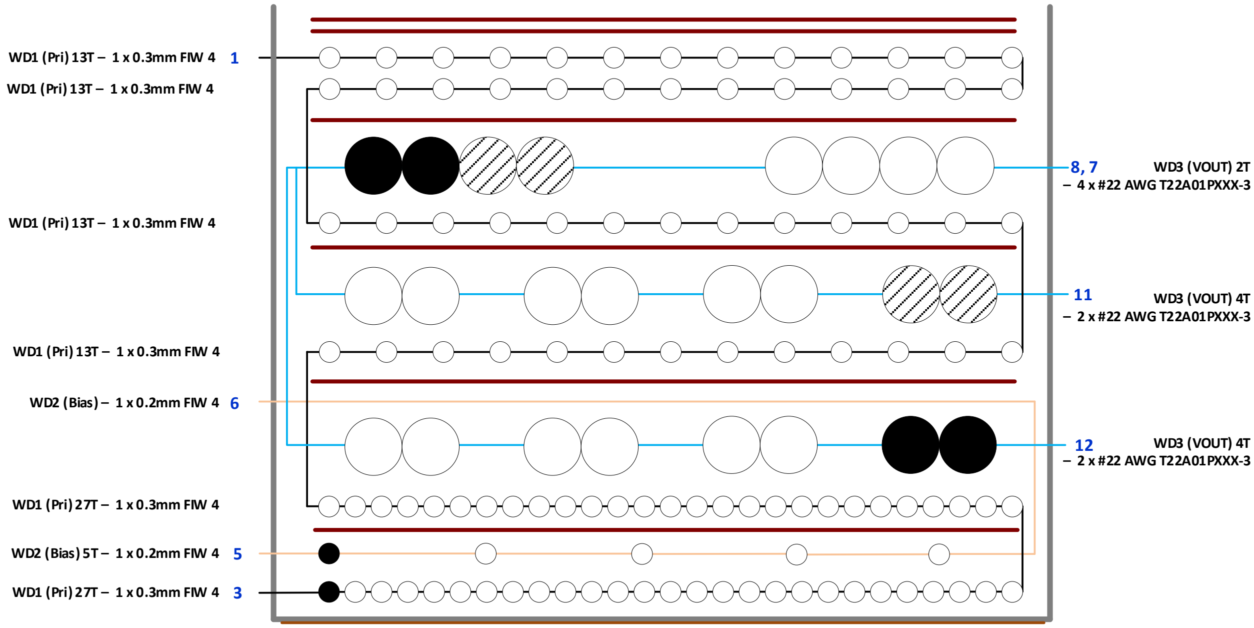


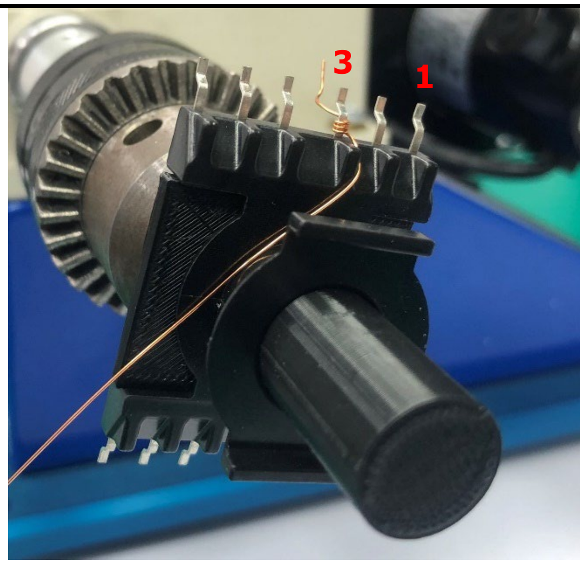
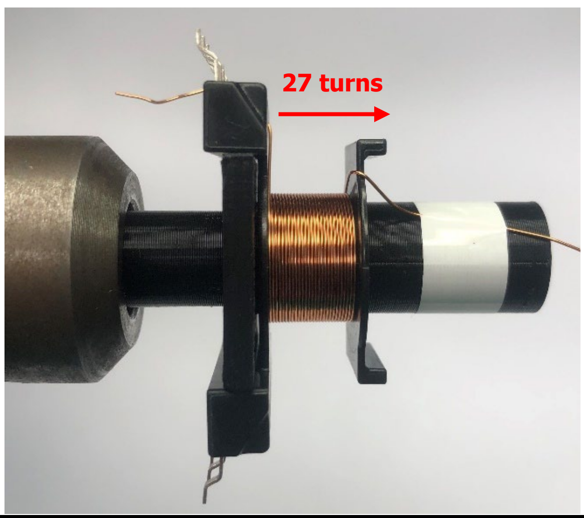
Figure 16 – Transformer Build Diagram.

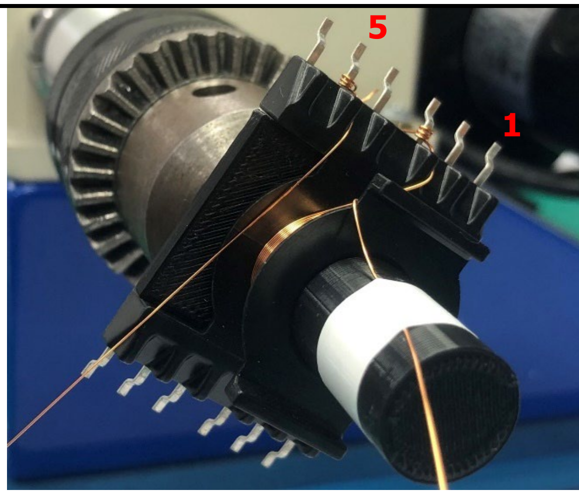
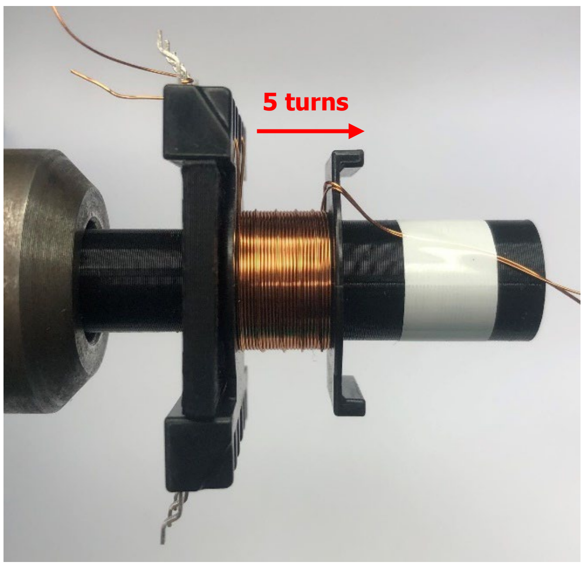
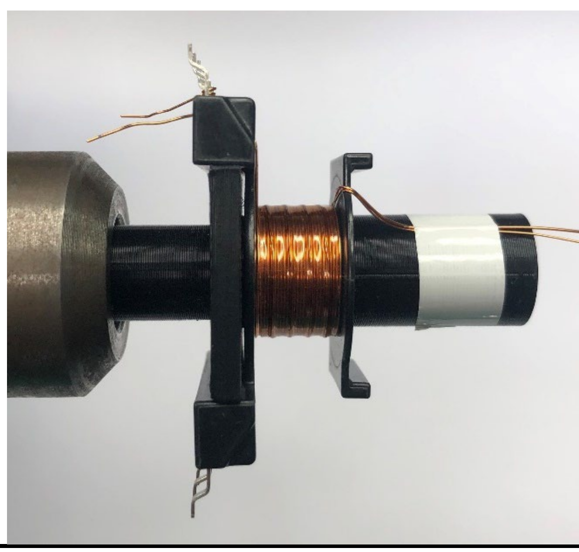
7.4 Material List

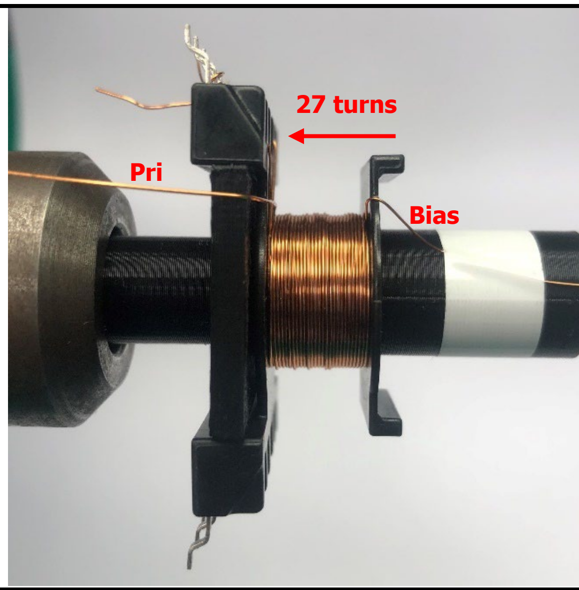
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: MCT-POT3301	1	PC	Phenolic	MyCoilTech
[2]	Core: POT33/19	2	PCS	SSP-95A (or equivalent)	Sunshine
[3]	WD1 (Pri): 0.30 mm FIW 4, Class F	6250	mm	Copper Wire	Elektrisola
[4]	WD2 (Bias): 0.20 mm FIW 4, Class F	300	mm		Elektrisola
[5]	WD3 (VOUT): T22A01PXXX-3, AWG #22 PFA .003”	1800	mm		Rubadue
[5]	3M Polyimide Film Tape 5413, width: 0.38 in (9.65 mm)		mm	3M 5413 0.38" X 36YD (or equivalent)	3M

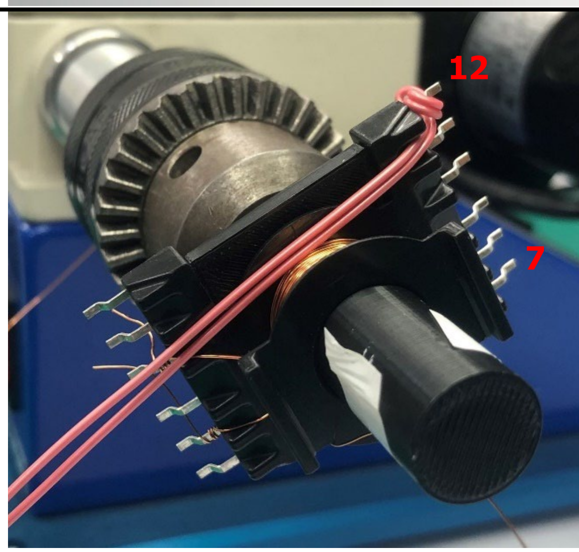
Table 6 – Transformer (T200) Material List.

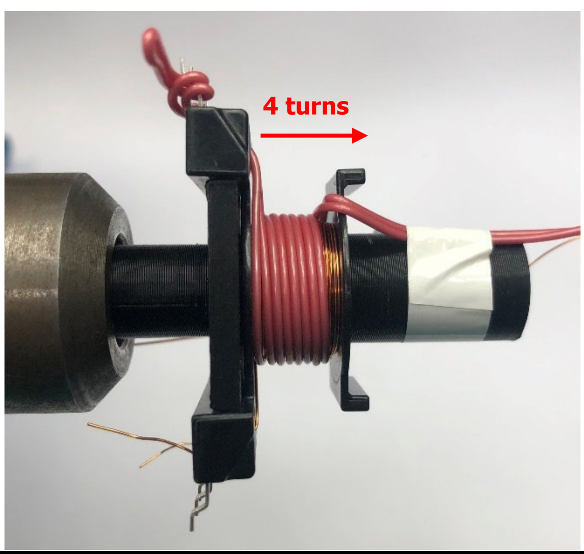
7.5 Winding Instructions

WD1 (Primary)		Use 0.3 mm FIW4 wire. Start on PIN 3. Wind the primary winding's first layer, 27 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.

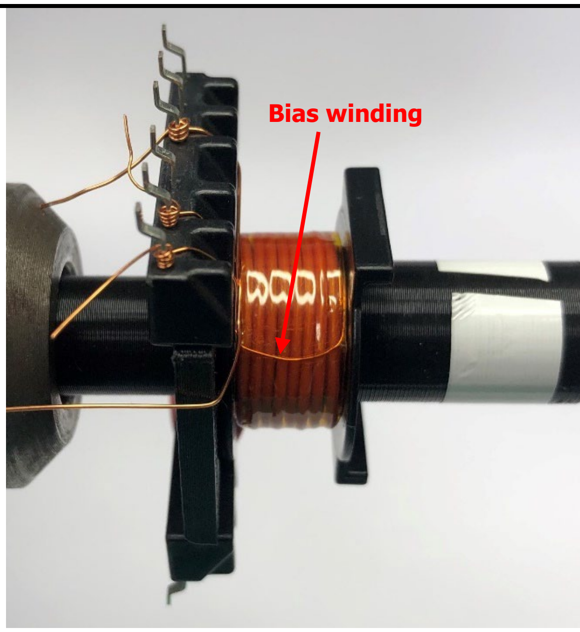
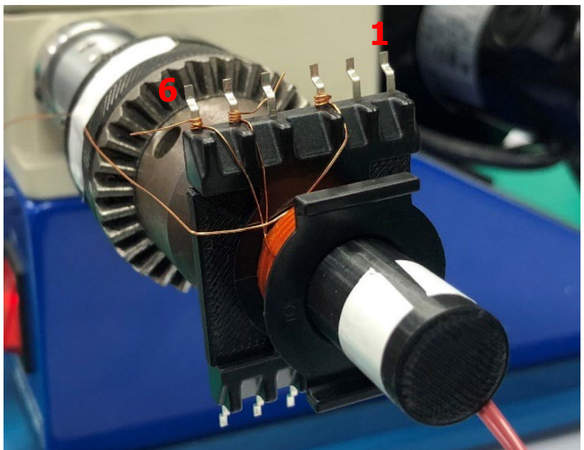
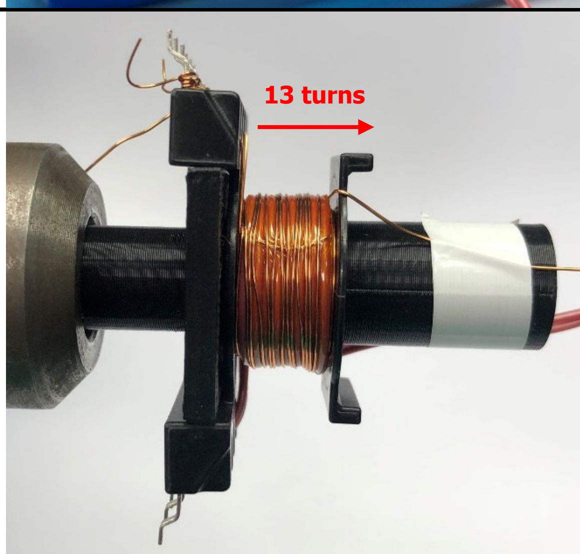
WD2 (Bias)	  	Use 0.2 mm FIW4 wire. Start on PIN 5. Wind the bias winding, 5 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet. Secure the winding using 1 layer of tape.

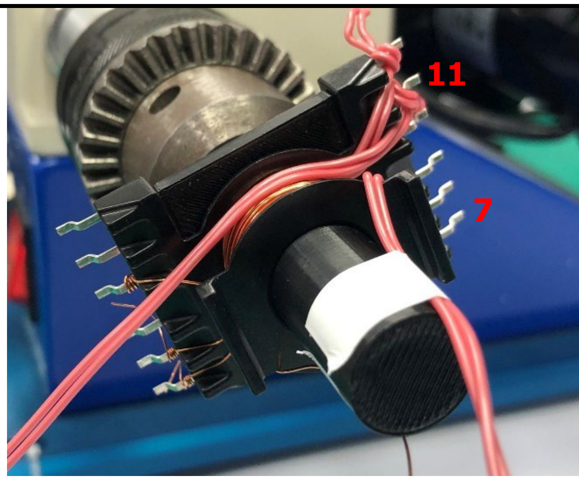
<table>
<tr>
<td>WD1
(Primary)</td>
<td>
</td>
<td>Continue winding the primary wire.

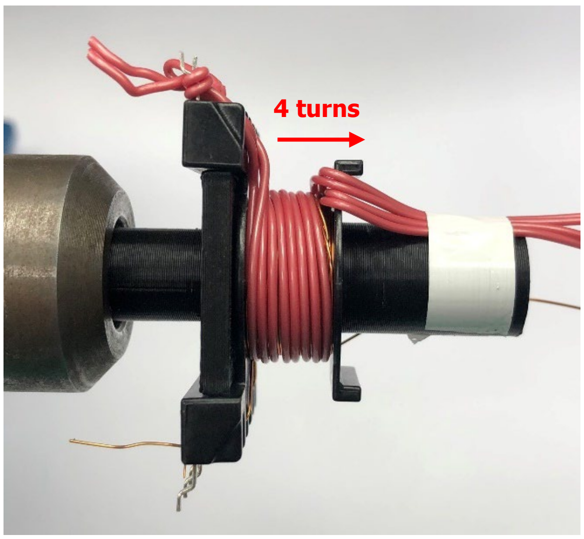
Wind the primary winding’s second layer, 27 turns from right to left. Spread the winding evenly along the bobbin’s width.
Do not terminate yet.</td>
</tr>
<tr>
<td>WD3
(VOUT)</td>
<td>

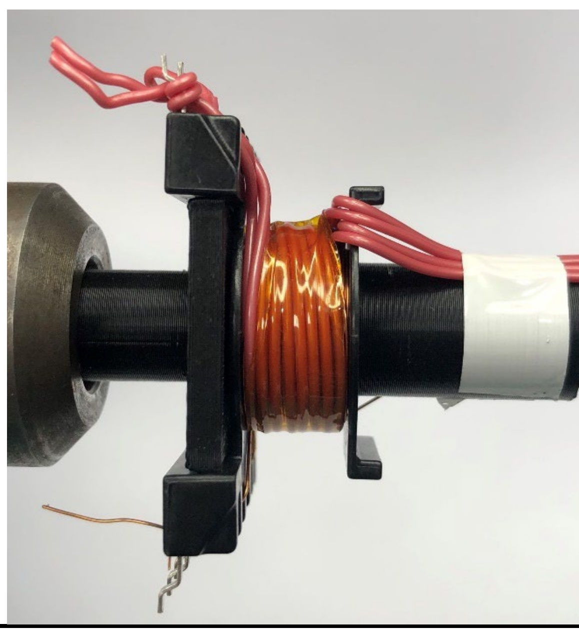

</td>
<td>Use 2 x #22 AWG T22A01PXXX-3.
Start on PIN 12.

Wind the secondary winding’s first layer,
4 turns from left to right. Spread the winding evenly along the bobbin’s width.
Do not terminate yet.</td>
</tr>
</table>

WD2 (Bias)		No additional turns. Terminate bias winding at PIN 6 by laying it flat across the bobbin's width. Secure using 1 layer of tape.
WD1 (Primary)		Continue winding the primary wire. Wind the primary winding's third layer, 13 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.

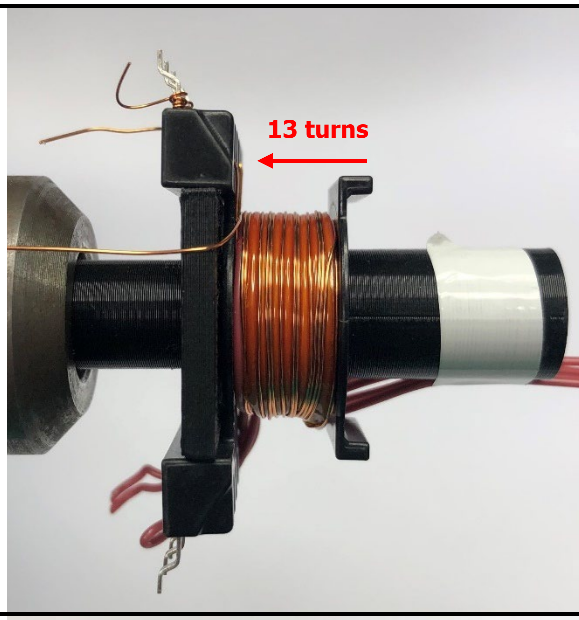
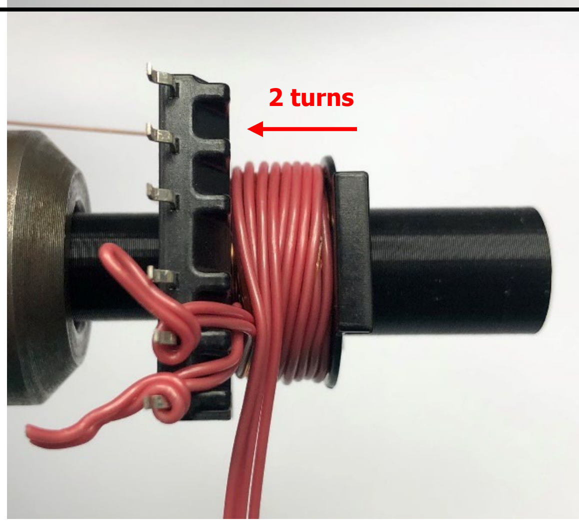
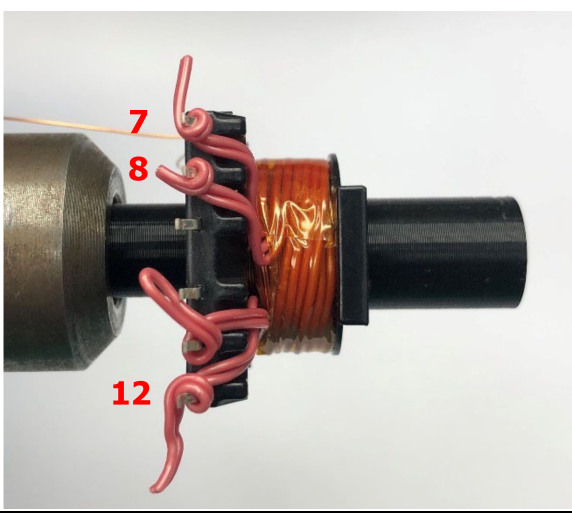
<table>
<tr>
<td>WD3
(VOUT)</td>
<td>

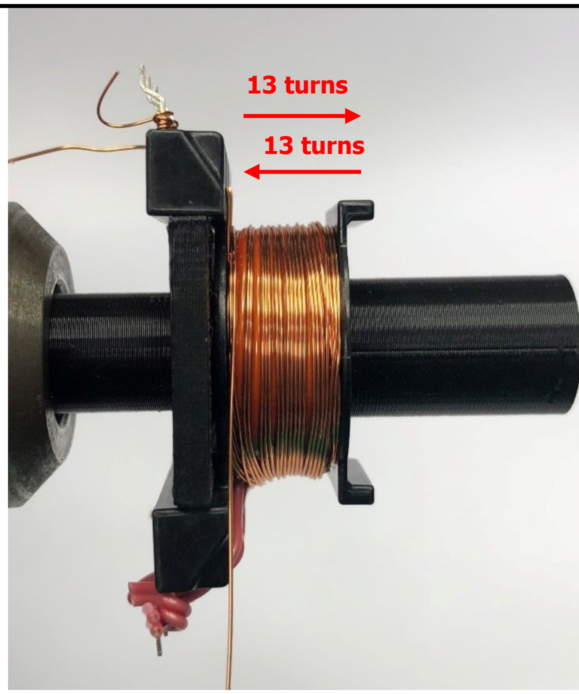
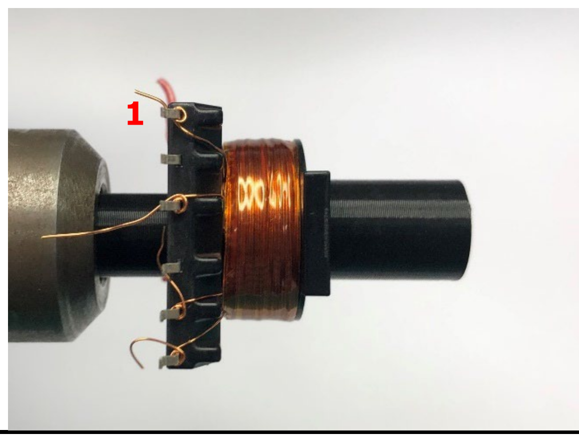


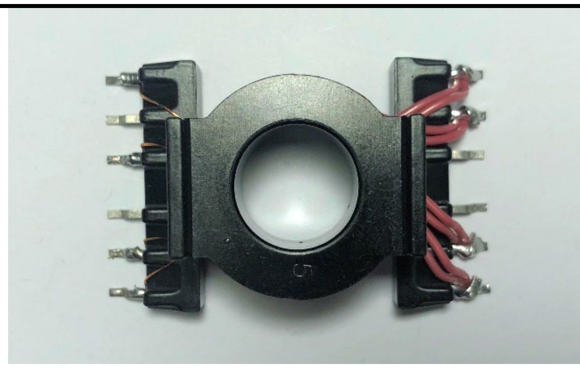
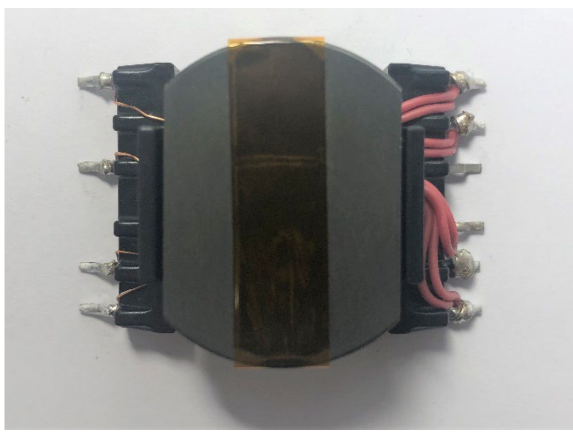
</td>
<td>Use another 2 x #22 AWG T22A01PXXX-3.
Start on PIN 11

Wind the additional secondary winding layer, 4 turns from left to right. Spread the winding evenly along the bobbin’s width. Do not terminate yet.

Secure using 1 layer of tape.</td>
</tr>
</table>

WD1 (Primary)		Continue winding the primary wire. Wind the primary winding's fourth layer, 13 turns from right to left. Spread the winding evenly along the bobbin's width. Do not terminate yet.
WD3 (VOUT)	 	Continue winding the secondary wire. Combining the 4 wires of the secondary winding, wind 2 turns from right to left. Spread the winding evenly along the bobbin's width. Secure using 1 layer of tape. Terminate secondary winding at PINs 7 and 8. *PIN 7 and 8 can be interchanged since they are shorted on the PCB*

WD1 (Primary)	 	Continue winding the primary wire. Wind the primary winding's fifth layer, 13 turns from left to right. Spread the winding evenly along the bobbin's width. Continue winding the primary wire for the final layer, 13 turns from right to left. Spread the winding evenly along the bobbin's width. Secure using 2 layers of tape. Terminate the primary winding at PIN 1.

Finishing	  	Cut and solder the wires. Mount the gapped core using glue (a 0.375” polyester film electrical tape can be used as an alternative). Remove pins 2 and 4.

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	13.50		13.50	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	900.00		900.00	V	Input DC voltage 1
6	IOUT1	6.370		6.370	A	Output current 1
7	POUT1		Info	86.00	W	The device is capable of delivering 70 W at the specified input voltage. Verify thermal performance.
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	300.00		300.00	V	Input DC voltage 3
13	IOUT2	6.370		6.370	A	Output current 3
14	POUT2		Info	86.00	W	The device is capable of delivering 70 W at the specified input voltage. Verify thermal performance.
15	EFFICIENCY2			0.85		Converter efficiency for output 3
16	Z_FACTOR2			0.50		Z-factor for output 3
69	**PRIMARY CONTROLLER SELECTION**					
70	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
71	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X9		Device selection
73	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25 °C
76	RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125 °C
77	ILIMIT_MIN			1.767	A	Primary switch minimum current limit
78	ILIMIT_TYP			1.900	A	Primary switch typical current limit
79	ILIMIT_MAX			2.033	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.34	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1170	V	Peak drain voltage on the primary switch during turn-off
85	**WORST CASE ELECTRICAL PARAMETERS**					
86	FSWITCHING_MAX	35000		35000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	240.0		240.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			1.025		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.439		Primary switch duty cycle
91	TIME_ON_MIN			4.09	μs	Minimum primary switch on-time
92	TIME_ON_MAX		Info	14.37	μs	Maximum primary switch on-time is greater than 11.75 μs: Increase the controller switching frequency or increase the VOR
93	TIME_OFF			16.29	μs	Primary switch off-time
94	LPRIMARY_MIN			2530.7	μH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			2663.9	μH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			2797.1	μH	Maximum primary magnetizing inductance
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			0.312	A	Primary switch average current
101	IPEAK_PRIMARY			1.575	A	Primary switch peak current

102	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			1.575	A	Primary switch ripple current
104	IRMS_PRIMARY			0.573	A	Primary switch RMS current
108 **109**	**TRANSFORMER CONSTRUCTION PARAMETERS** **CORE SELECTION**					
110	CORE	POT33/19		POT33/19		Core selection
111	CORE NAME			POT33/19-JP95		Core code
112	AE			147.4	mm^2	Core cross sectional area
113	LE			51.0	mm	Core magnetic path length
114	AL			5500	nH	Ungapped core effective inductance per turns squared
115	VE			7517	mm^3	Core volume
116	BOBBIN NAME			POT33/19		Bobbin name
117	AW			49.4	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
118	BW			10.50	mm	Bobbin width
119	BH			4.70	mm	Bobbin height
120	MARGIN			0.0	mm	Bobbin safety margin
122	**PRIMARY WINDING**					
123	NPRIMARY			106		Primary winding number of turns
124	BPEAK			3725	Gauss	Peak flux density
125	BMAX			2756	Gauss	Maximum flux density
126	BAC			1378	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			237	nH	Typical gapped core effective inductance per turns squared
128	LG			0.748	mm	Core gap length
130	**SECONDARY WINDING**					
131	NSECONDARY	6		6		Secondary winding number of turns
133	**BIAS WINDING**					
134	NBIAS			5		Bias winding number of turns
138 **139**	**PRIMARY COMPONENTS SELECTION** **LINE UNDERVOLTAGE/OVERVOLTAGE**					
140	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
141	**UNDERVOLTAGE PARAMETERS**					
142	BROWN-IN REQUIRED	30.00		30.00	V	Required DC bus brown-in voltage threshold
143	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
144	VZ			9.10	V	Zener diode reverse voltage
145	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
146	ILKG			2.00	μA	Zener diode maximum reverse leakage current
147	BROWN-IN ACTUAL			22.99 - 29.55	V	Actual brown-in voltage range using standard resistors
148	BROWN-OUT ACTUAL			19.76 - 26.44	V	Actual brown-out voltage range using standard resistors
149	**OVERVOLTAGE PARAMETERS**					
150	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
151	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
152	VF				V	OV diode forward voltage
153	VRRM				V	OV diode reverse voltage
154	PIV				V	OV diode peak inverse voltage
155	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
156	**DC BUS SENSE RESISTORS**					
157	RLS_H			0.70	MΩ	Connect five 140 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold

158	RLS_L			261	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
161	**BIAS WINDING**					
162	VBIAS			9.00	V	Rectified bias voltage
163	VF_BIAS			0.70	V	Bias winding diode forward drop
164	VREVERSE_BIASDIODE			51.45	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
165	CBIAS			22	μF	Bias winding rectification capacitor
166	CBPP			0.47	μF	BPP pin capacitor
170 **171**	**SECONDARY COMPONENTS SELECTION** **FEEDBACK COMPONENTS**					
172	RFB_UPPER			100.00[10]	kΩ	Upper feedback resistor (connected to the output terminal)
173	RFB_LOWER			10.20	kΩ	Lower feedback resistor
174	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
178 **179**	**MULTIPLE OUTPUT PARAMETERS** **OUTPUT 1**					
180	VOUT1			13.50	V	Output 1 voltage
181	IOUT1	6.370		6.370	A	Output 1 current
182	POUT1			86.00	W	Output 1 power
183	IRMS_SECONDARY1			11.306	A	Root mean squared value of the secondary current for output 1
184	IRIPPLE_CAP_OUTPUT1			9.340	A	Current ripple on the secondary waveform for output 1
185	NSECONDARY1			6		Number of turns for output 1
186	VREVERSE_RECTIFIER1			64.44	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
187	SRFET1	DMT12H007LPS-13		DMT12H00 7LPS-13		Secondary rectifier (Logic MOSFET) for output 1
188	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
189	VBREAKDOWN_SRFET1			120	V	SRFET breakdown voltage for output 1
190	RDSON_SRFET1			14	mΩ	SRFET on-time drain resistance at 25 degC and VGS = 4.4 V for output 1
218	PO_TOTAL			86.00	W	Total power of all outputs

Table 7 – PIXls Spreadsheet.

[10] Actual value implemented on the unit is 110 kΩ as requirement for implementing the Precision Voltage Regulator circuit.

9 Performance data

Note: 1. Measurements were taken with the unit-under-test mounted inside a thermal chamber in a high-voltage (HV) safety room.

Figure 17 – Set-up for High-Voltage Test.

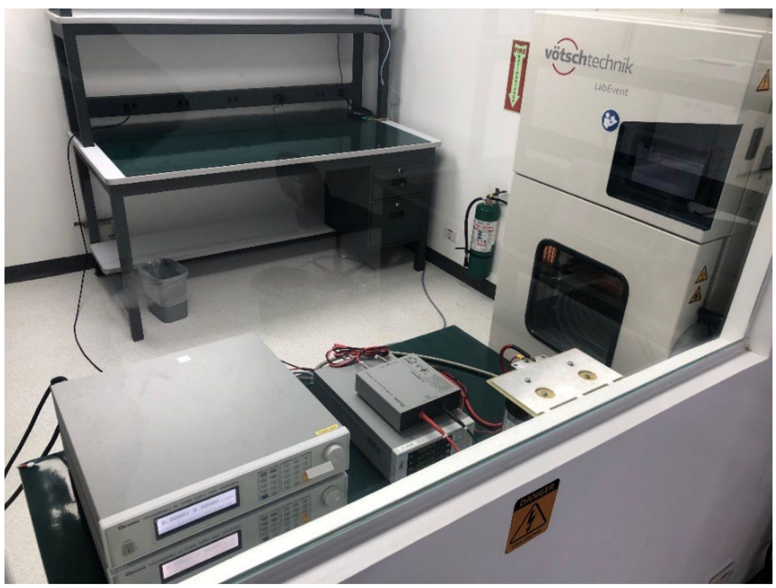


Figure 18 –Set-up for Test Inside the High-Voltage Room.

2. The RDK-952Q board was placed in a box within the thermal chamber to eliminate the effects of airflow.

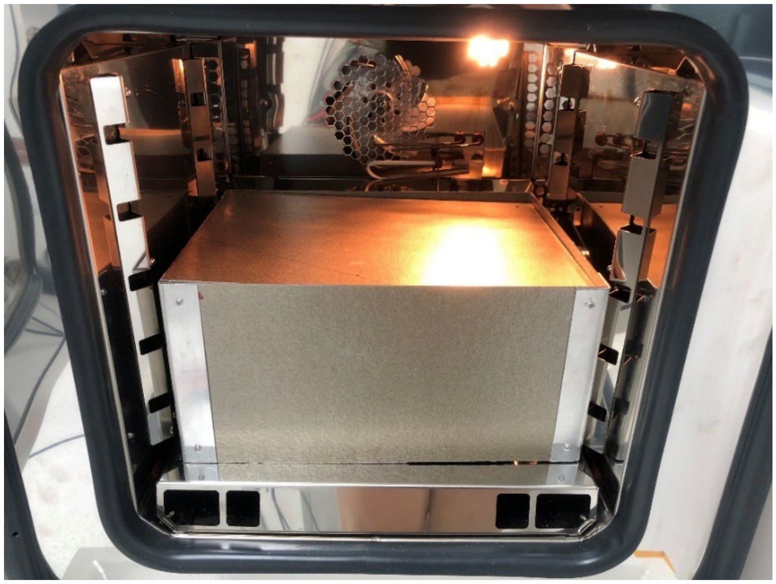


Figure 19 – Unit Under Test Placed Inside a Box to Eliminate the Effect of Airflow.

3. The unit was soaked for 5 minutes at full load at the start of each test sequence. For each loading condition, the RDK-952Q test board was allowed to stabilize for at least 1 minute before measurements were taken.

4. List of equipment used for testing

Equipment Type	Model Number	Specifications	Manufacturer
Power Supply	62024P-600-8	600 V/8 A/2400 W DC PSU	Chroma
Power Supply	HP20 757 152	2 kV/750 mA/1.5 kW	Iseg
Electronic Load	DL3021	150 V/40 A/200 W DC ELOAD	Rigol
Electronic Load	PEL-2020A	80 V/20 A/100 W DC ELOAD	GW Instek
Power Meter	66205	600 V/30 A 10 kHz Digital Meter	Chroma
Power Meter	WT310E	600 V/20 A 100 kHz Digital Meter	Yokogawa
Current Meter	DMM-4050	Precision Multimeter	Tektronix
High Voltage Measurement	TT-SI 9010A	70 MHz 7000 V Differential Probe	Testec
High Voltage Measurement	TT-SI 9110	100 MHz 1400 V Differential Probe	Testec
Low Voltage Measurement	701937	500 MHz 600 V Passive Probe	Yokogawa
Output Current Measurement	701928	100 MHz 30 A_{rms} Current Probe	Yokogawa
Component Current Measurement	CWTUM/015/B	30 MHz 30 A_{peak} Rogowski Coil	CWT
Component Current Measurement	CWTUM/06/R	30 MHz 120 A_{peak} Rogowski Coil	CWT
Thermocouple Measurement	GL840	20 channel Data Logger	Graphtec
Thermal Image	TiX580	1000 °C Thermal Imagin Camera	Fluke
Oscilloscope	DLM5058	2.5GS/s 500 MHz Mixed Signal	Yokogawa

9.1 No-Load Input Power

Figure 20 shows the schematic for the no-load input power measurement. The voltmeter was placed before the ammeter; this was done to prevent the voltmeter bias current from affecting the input current measurement. A Chroma Digital Power Meter 66205 was used to measure both the current and voltage.

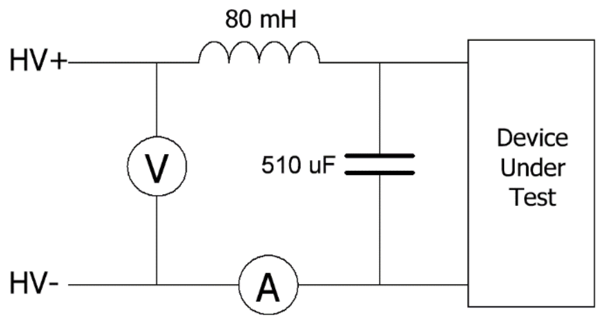


Figure 20 – No-Load Input Power Measurement Diagram.

Before starting data averaging, the unit was allowed to stabilize for 10 minutes. The leakage current through the DC-Link capacitor was measured before testing and subtracted from the no-load input current measurement. The voltage across the inductor was assumed to be negligible due to the inductor's very low DCR (40 mΩ) and low input current. AC losses in the inductor were also assumed to be negligible since the input current was DC.

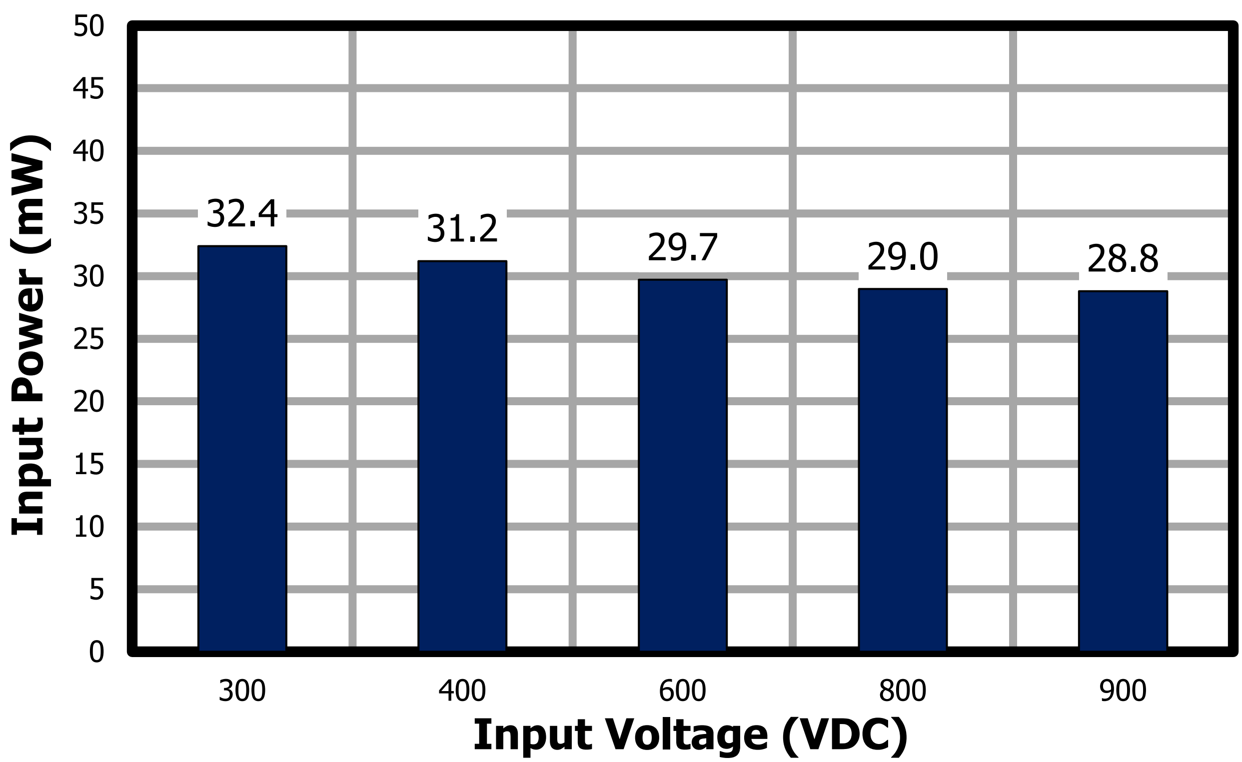


Figure 21 – No-Load Input Power vs. Input Voltage (25 °C Ambient).

9.2 Efficiency

9.2.1 Efficiency Across Line

Efficiency across line describes how input voltage affects the unit's overall efficiency. The points in the graph were taken at 100% load conditions.

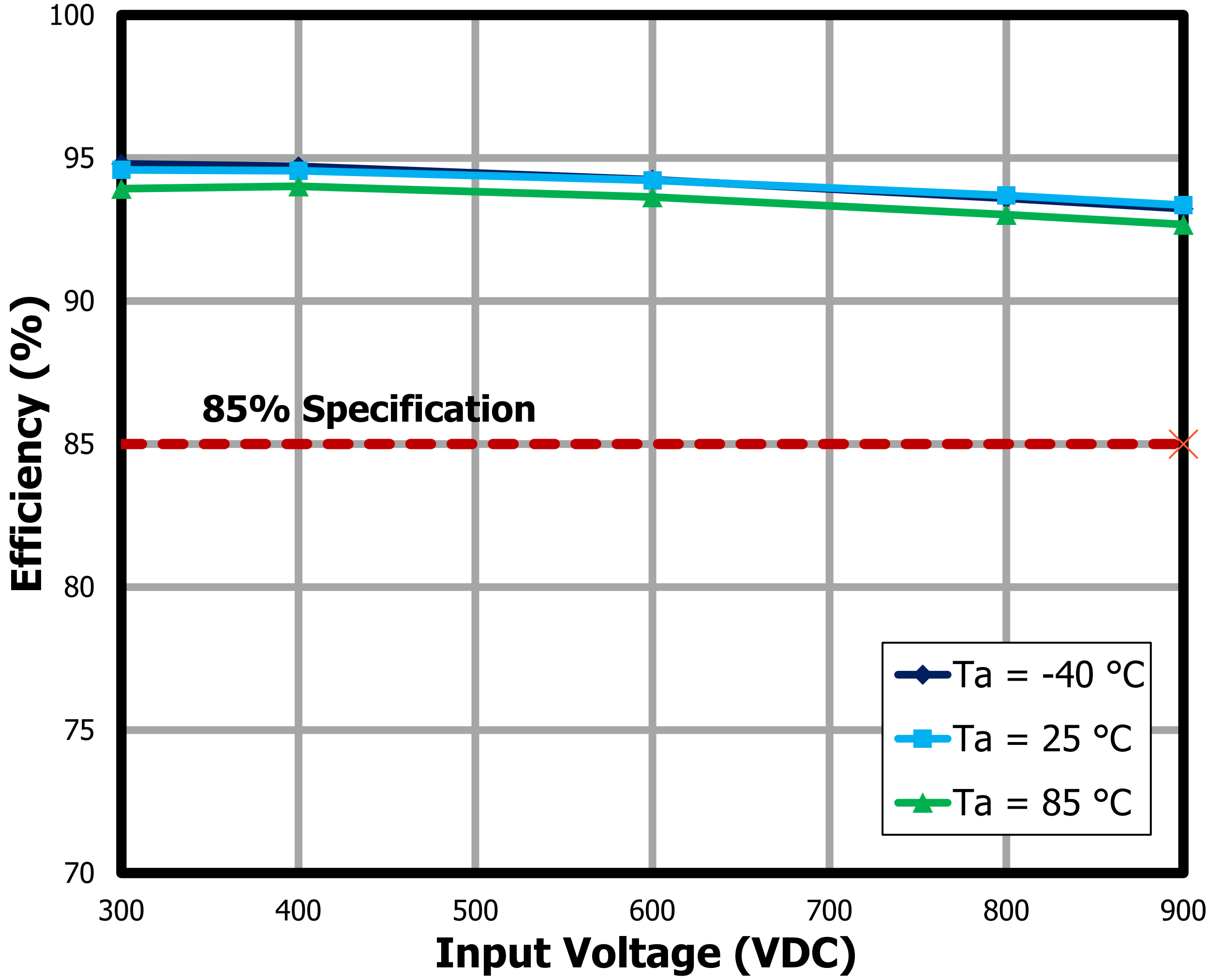


Figure 22 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Efficiency Across Load

Efficiency across load describes how the change in output loading conditions affects the unit's overall efficiency.

9.2.2.1 Efficiency Across Load at 85 °C Ambient

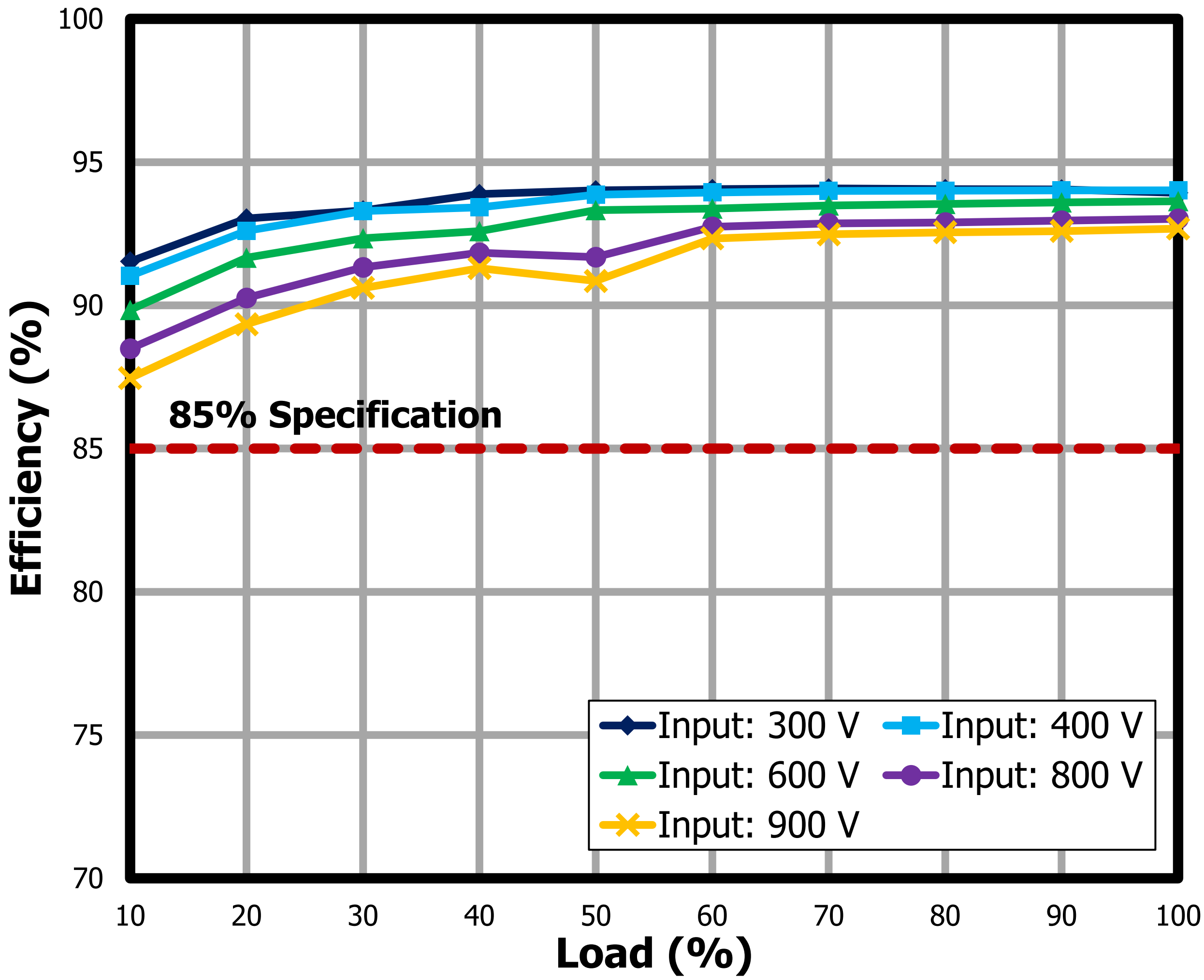


Figure 23 – Efficiency vs. Load at Different Input Voltages (85 °C Ambient).

9.2.2.2 Efficiency Across Load at 25 °C Ambient

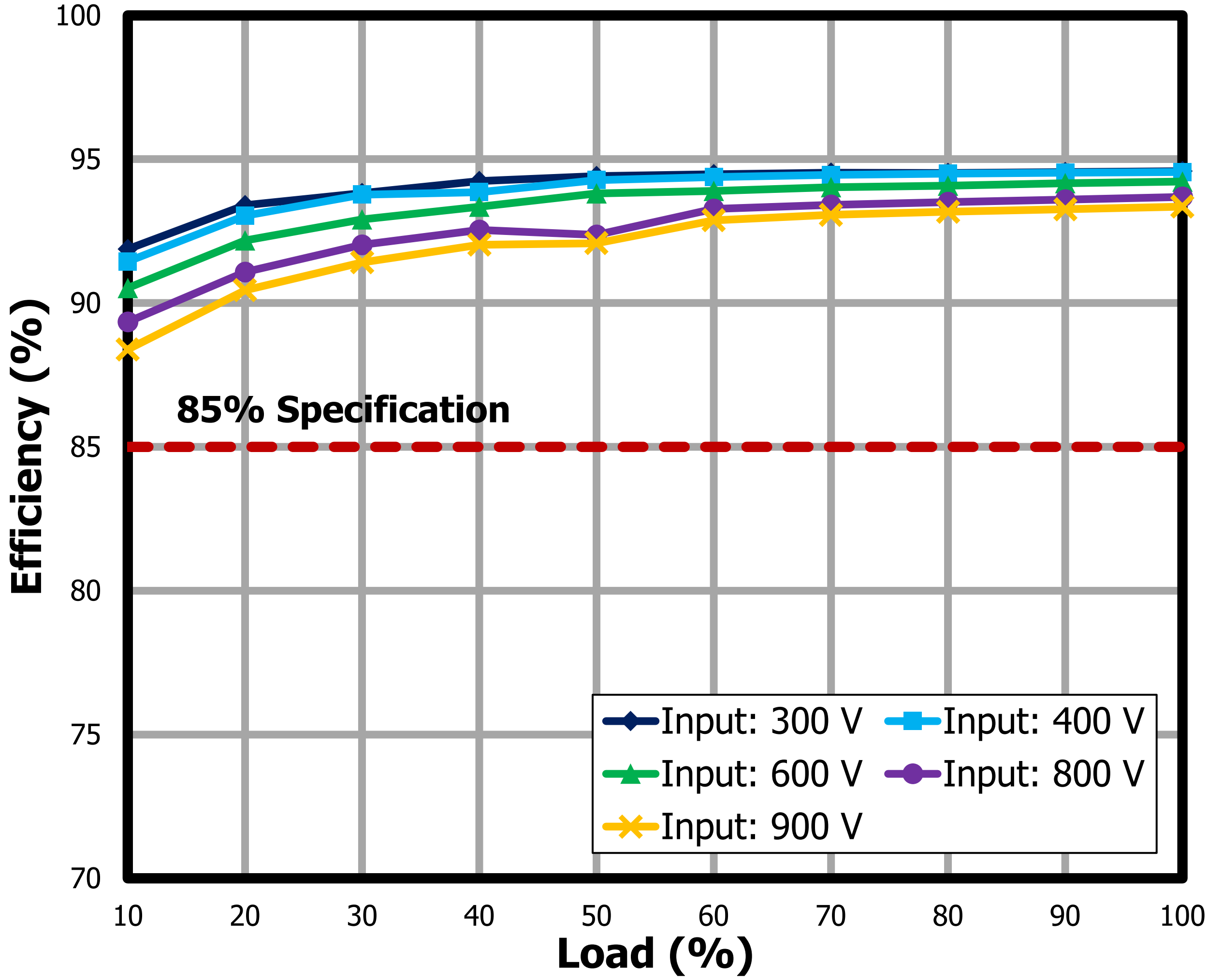


Figure 24 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).

9.2.2.3 Efficiency Across Load at -40 °C Ambient

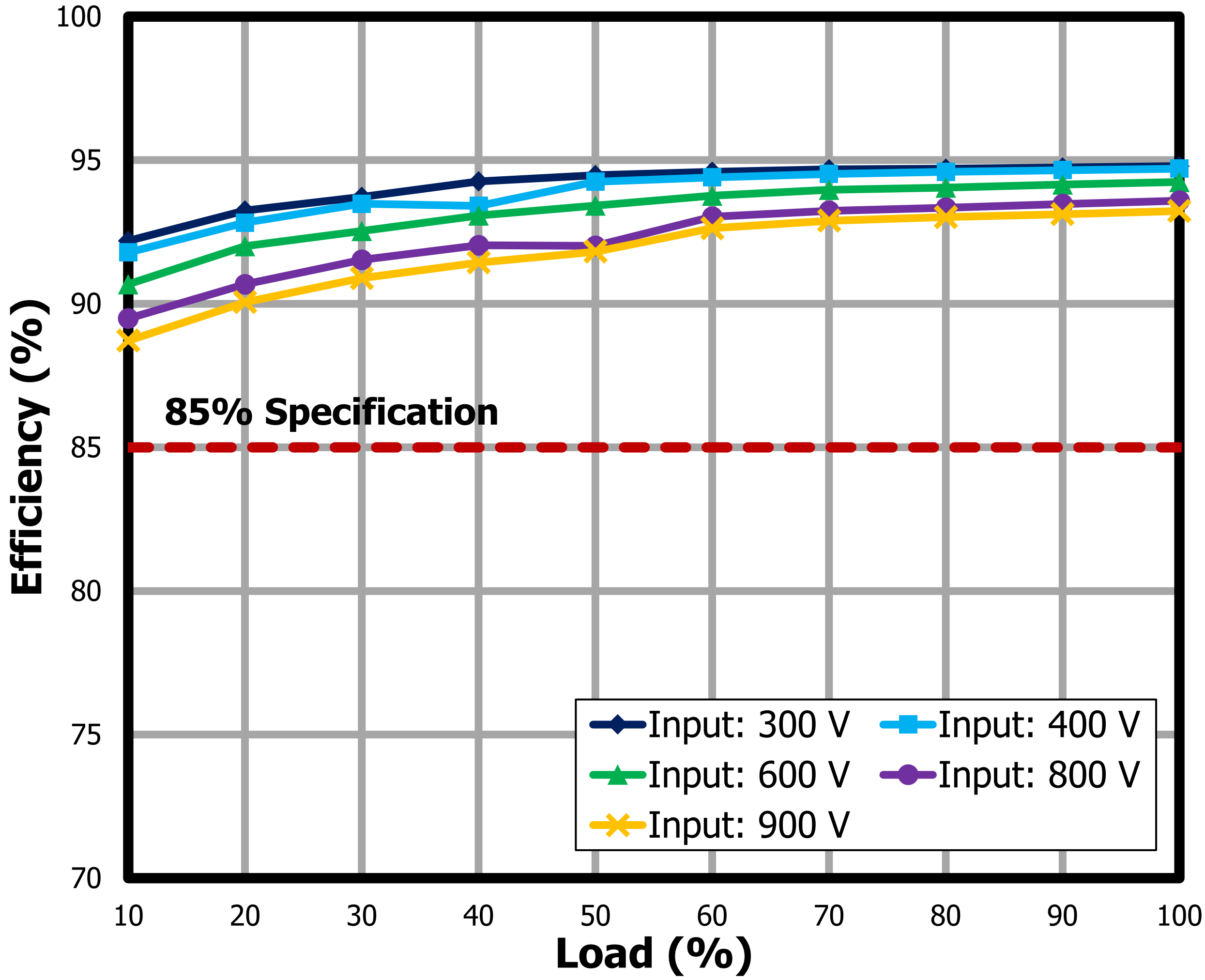


Figure 25 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).

9.3 Line and Load Regulation

9.3.1 Load Regulation

Load regulation describes how a change in load affects output voltage.

9.3.1.1 Load Regulation at 85 °C Ambient

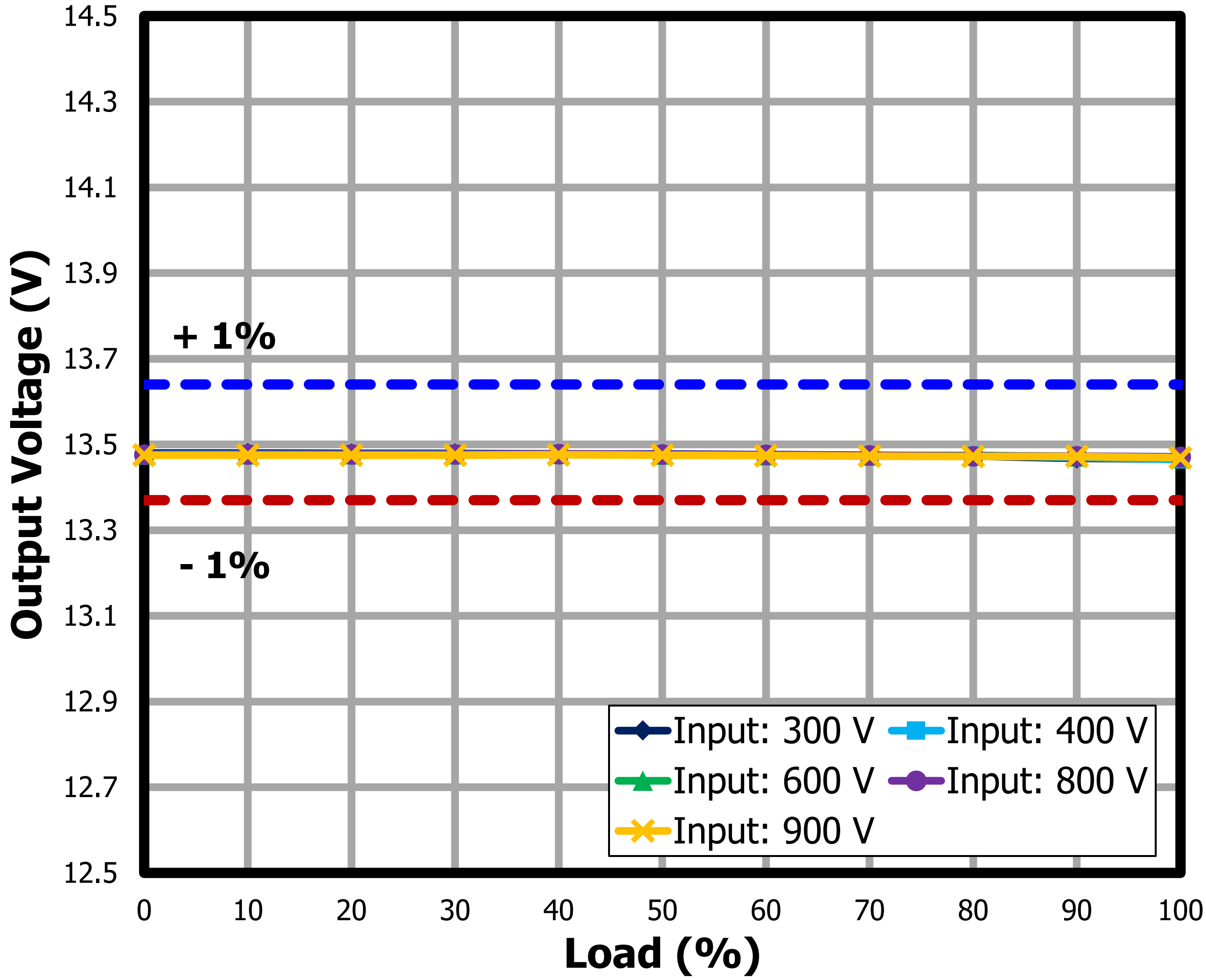


Figure 26 – Output Regulation vs. Load at Different Input Voltages (85 °C Ambient).

9.3.1.2 Load Regulation at 25 °C Ambient

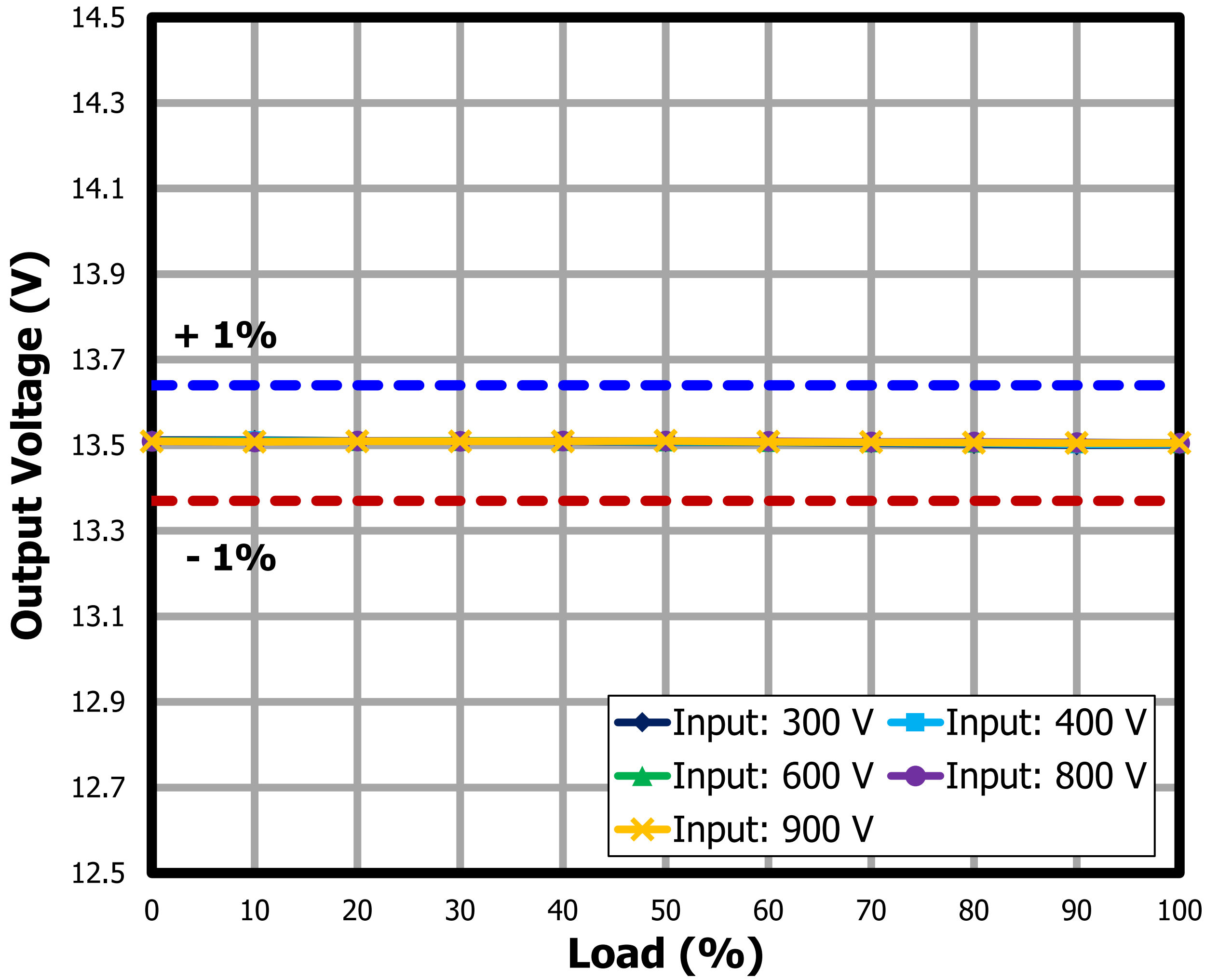


Figure 27 – Output Regulation vs. Load at Different Input Voltages (25 °C Ambient).

9.3.1.3 Load Regulation at -40 °C Ambient

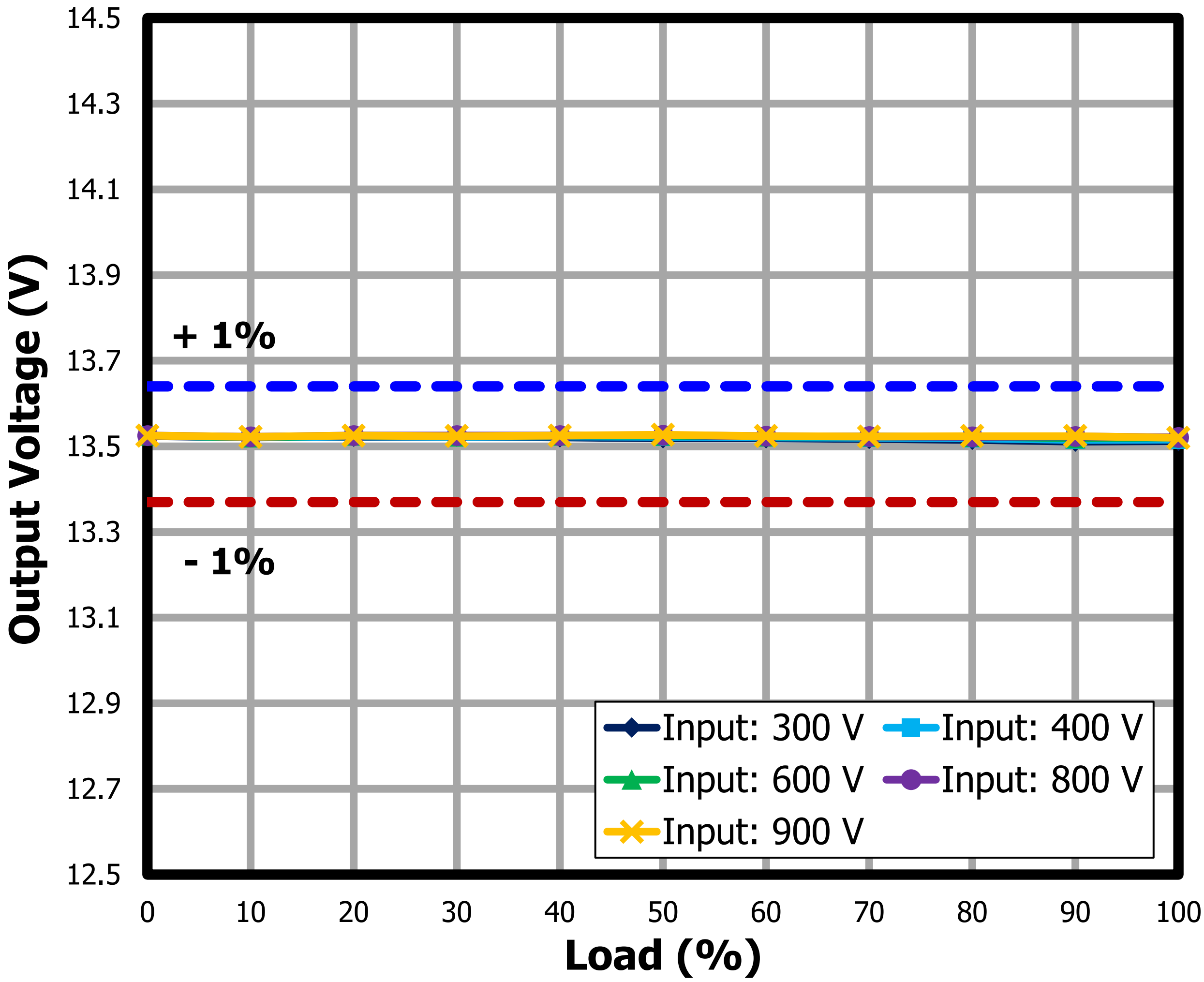


Figure 28 – Output Regulation vs. Load at Different Input Voltages (-40 °C Ambient).

9.3.2 Line Regulation

Line regulation describes how the change in input voltage affects the average output voltage of the unit. The points in the following graph were taken at 100% load.

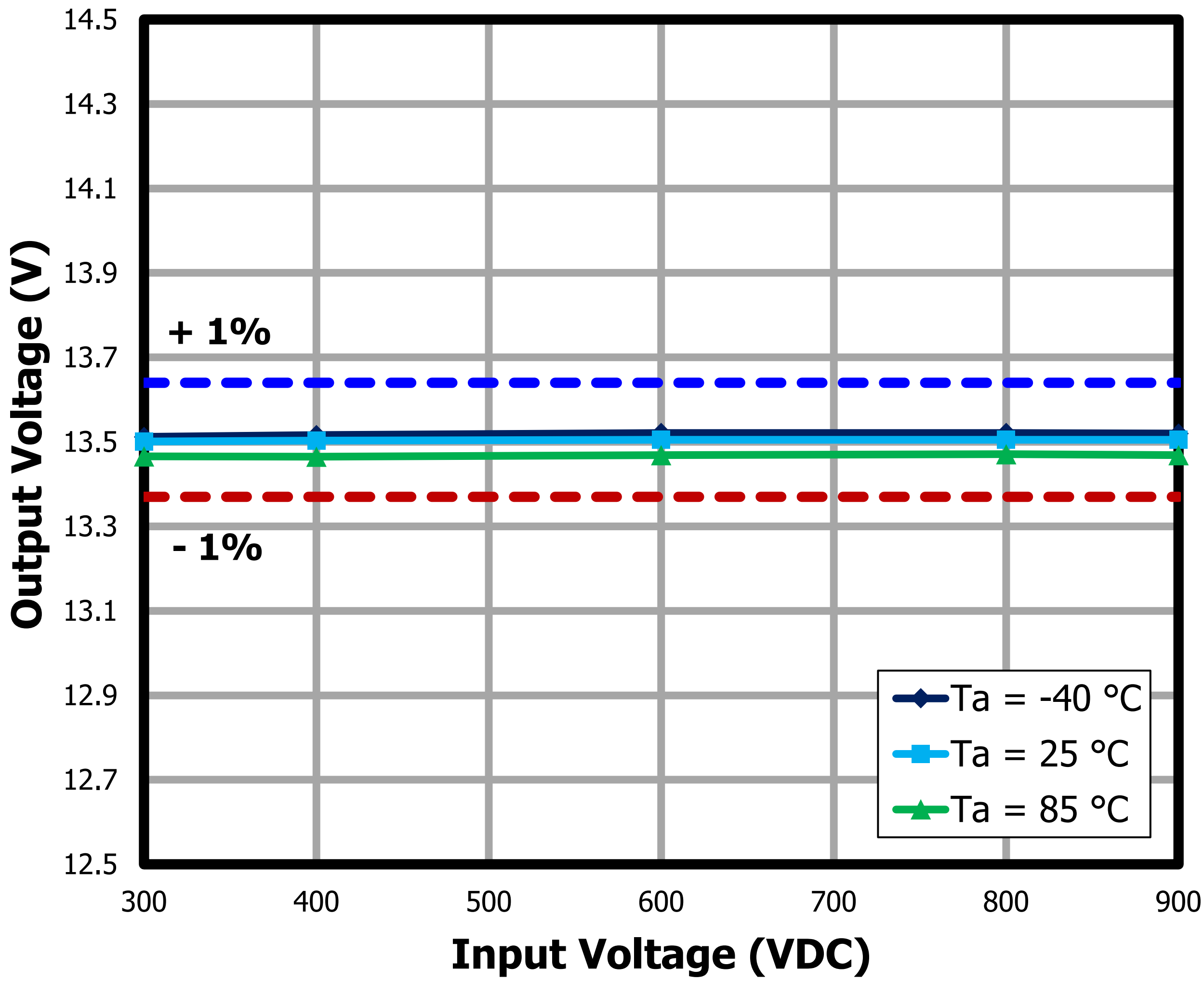


Figure 29 – Output Voltage vs Input Voltage at Full Load.

10 Thermal Performance

10.1 Thermal Data at 85 °C Ambient

The unit was placed inside a thermal chamber and allowed to stabilize for 1 hour. Figure 19 shows the test setup for thermal measurement.

Critical Components	Temperature (°C)		
	300 V	800 V	900 V
InnoSwitch3-AQ (IC200)	107	115	119
Primary Snubber Resistor (R207)	111	110	110
Transformer Winding (T200)	134	138	139
Transformer Core (T200)	125	131	131
SR MOSFET (Q101)	109	112	112
SR MOSFET (Q100)	110	112	112
Secondary Snubber Resistor (R101)	103	105	105
Output Capacitor (C104)	101	103	102

Table 8 – Thermal Data at 85 °C at Different Input Voltages (V).

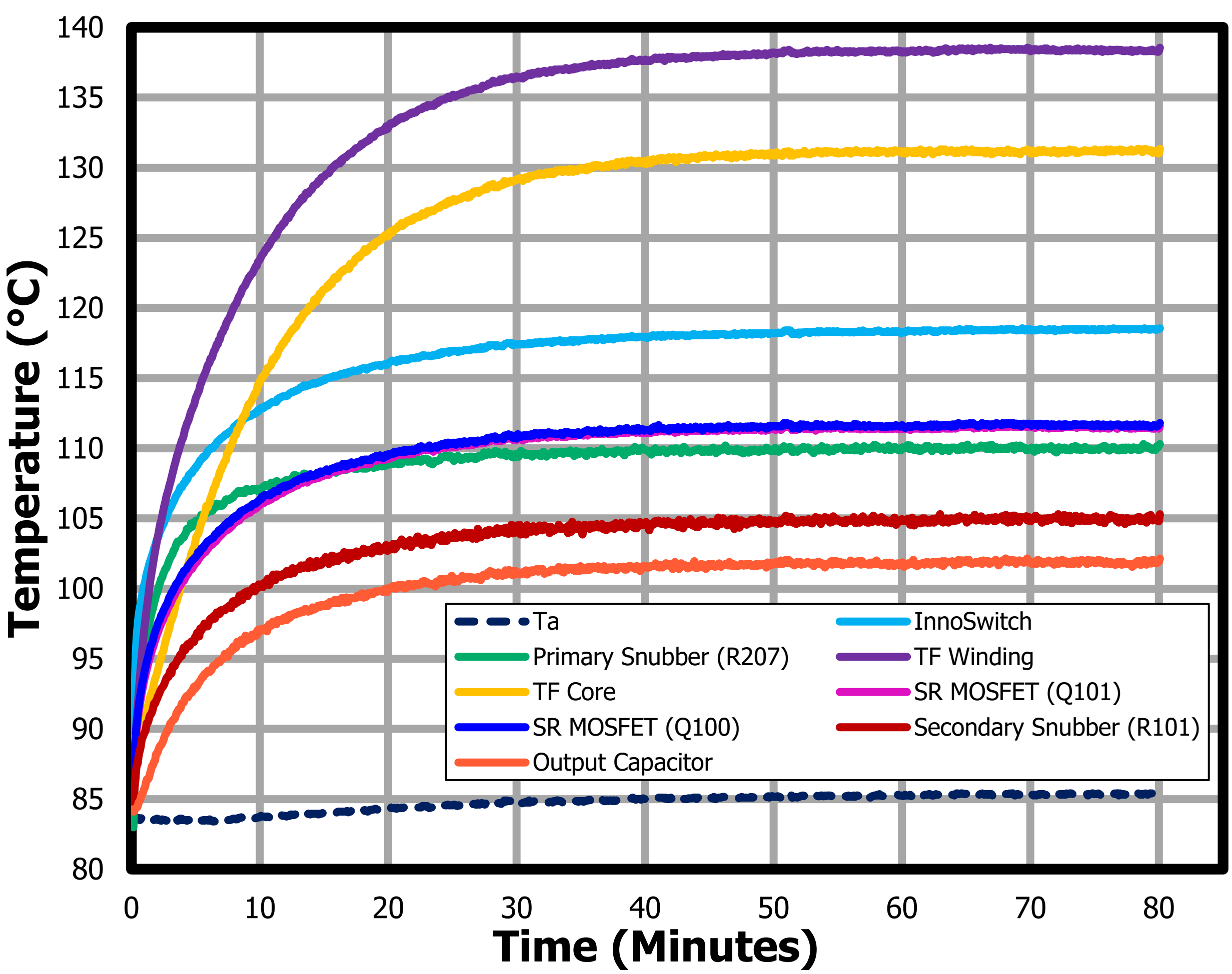


Figure 30 – Component Temperatures at 85 °C Ambient, 900 V Input.

10.2 Thermal Image Data at 25 °C Ambient

The following thermal scans were captured using a Fluke thermal imager after soaking for 1 hour in an enclosure that minimized the effect of airflow.

Critical Components	Temperature (°C)		
	300 V	800 V	900 V
InnoSwitch3-AQ (IC200)	48.2	58.4	62.1
Primary Snubber Resistors	57.4	56.8	56.3
Transformer (T200)	63.6	68.7	70.5
SR MOSFET (Q101)	52.3	54.8	54.3
SR MOSFET (Q100)	50.7	53.0	54.1
Secondary Snubber Resistor (R101)	45.4	48.3	49.7
Output Capacitor (C104)	45.0	45.7	46.8

Table 9 – Thermal Data at 25 °C at Different Input Voltages (V).

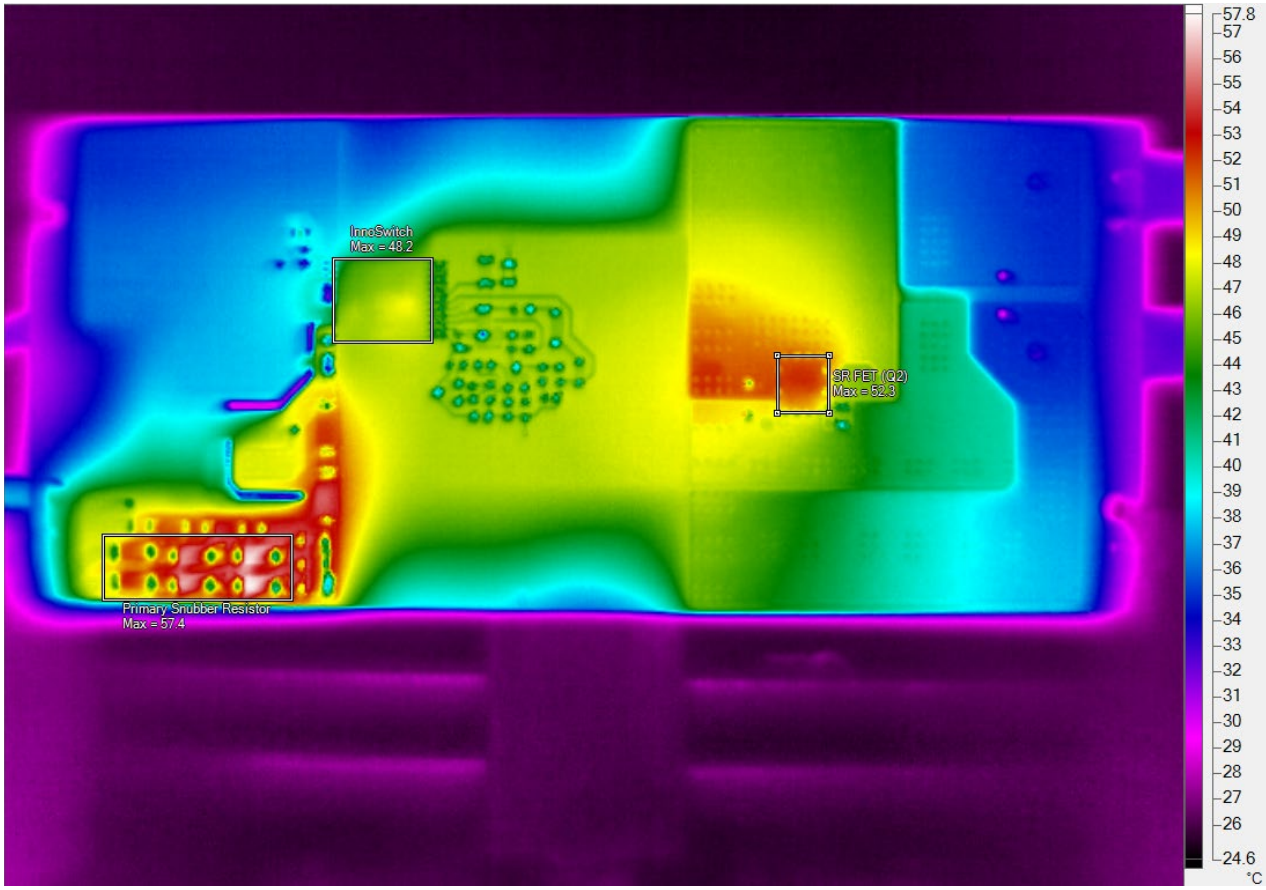


Figure 31 – Thermal Scan of the Bottom of the PCB at 300 V Input.

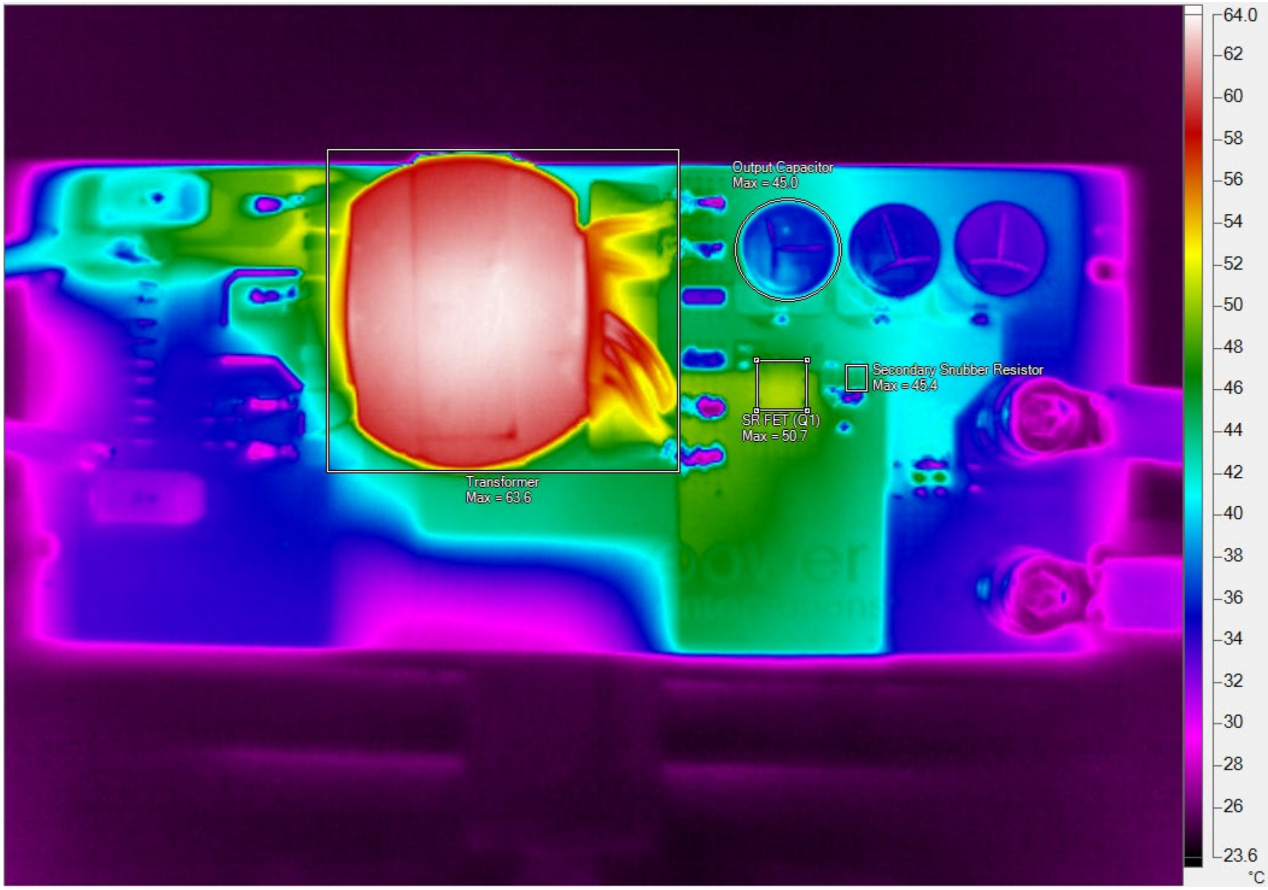


Figure 32 – Thermal Scan of the Top of the PCB at 300 V Input.

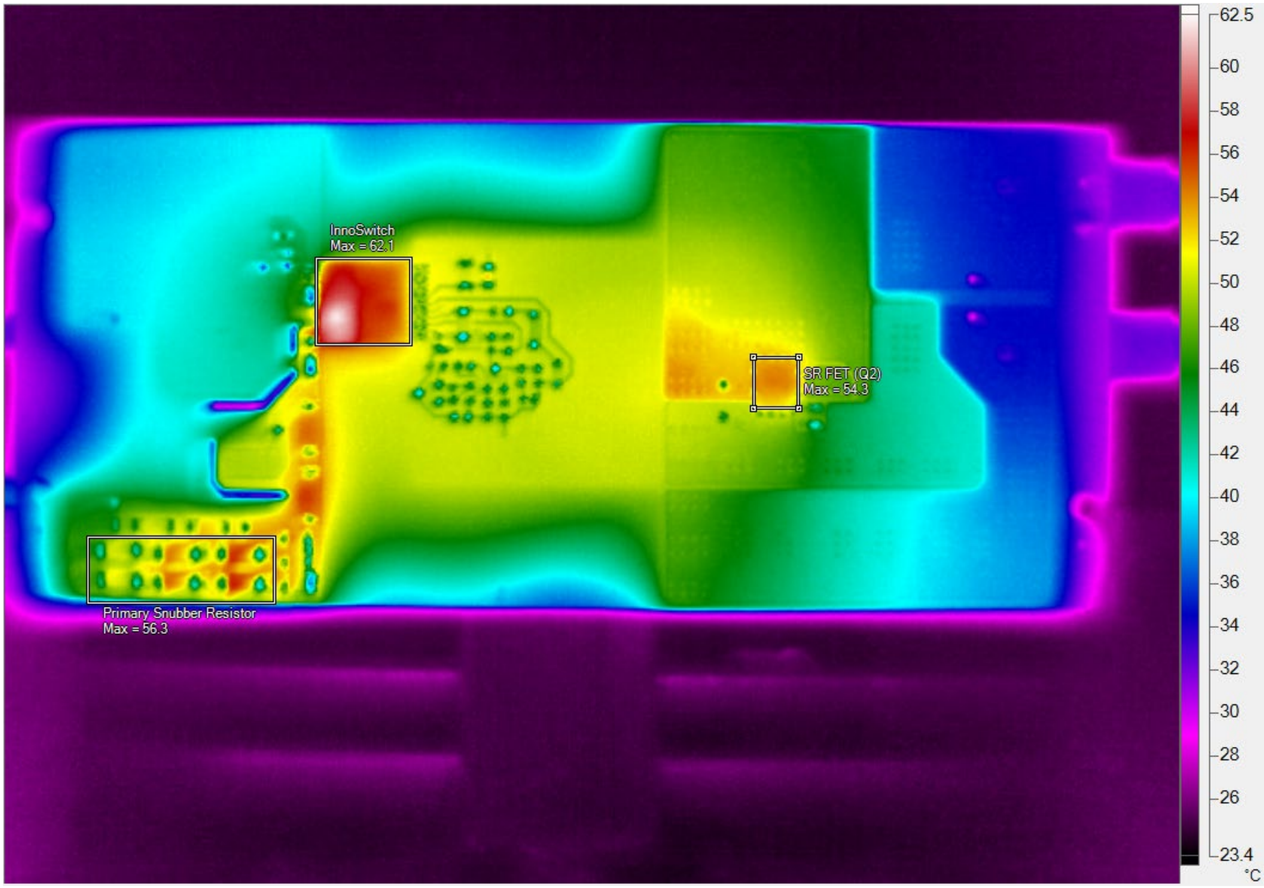


Figure 33 – Thermal Scan of the Bottom of the PCB at 900 V Input.

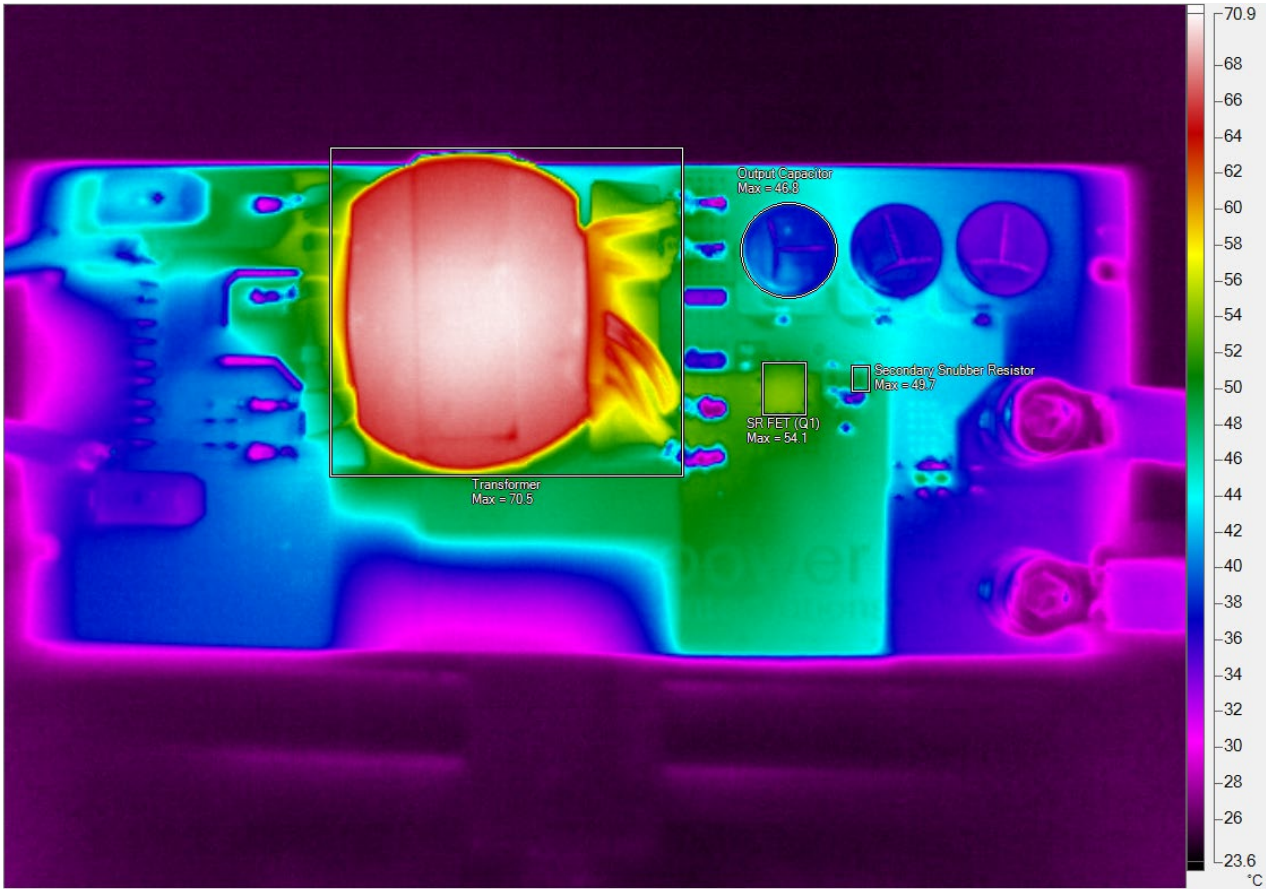


Figure 34 – Thermal Scan of the Top of the PCB at 900 V Input.

11 Waveforms

11.1 Start-Up Waveforms

The following measurements were taken by connecting the unit-under-test to a DC-link capacitor charged [11] to different test input voltages. A constant resistance load configuration was used for all start-up tests.

11.1.1 Output Voltage and Current at 25 °C Ambient[12,13]

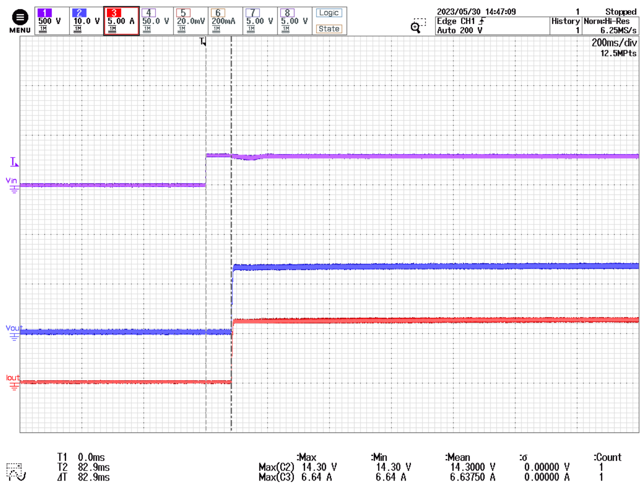


Figure 35 – Output Voltage and Current.
300 VDC, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

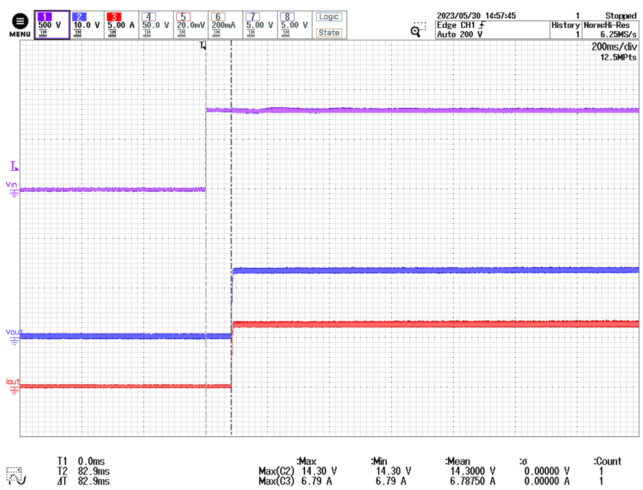


Figure 36 – Output Voltage and Current.
800 VDC, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

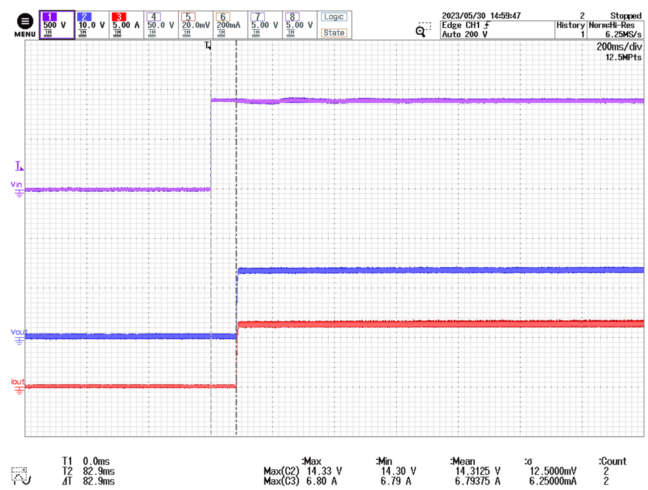


Figure 37 – Output Voltage and Current.
900 VDC, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

[11] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[12] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.
[13] Current waveforms were measured using a Yokogawa current probe.

11.1.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient[14,15]

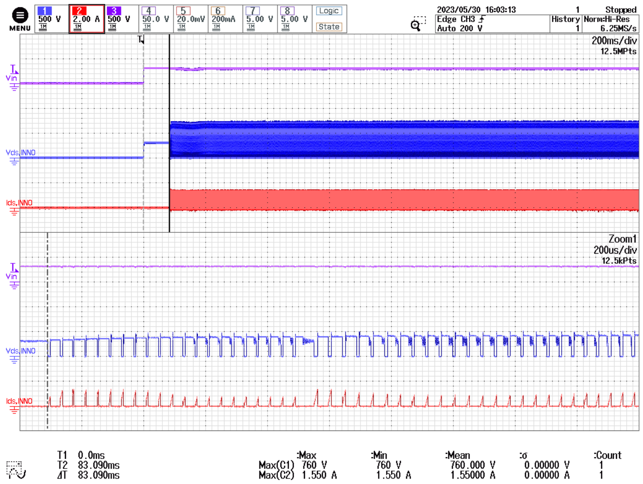


Figure 38 – INN3949CQ Drain Voltage and Current.
300 VDC, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

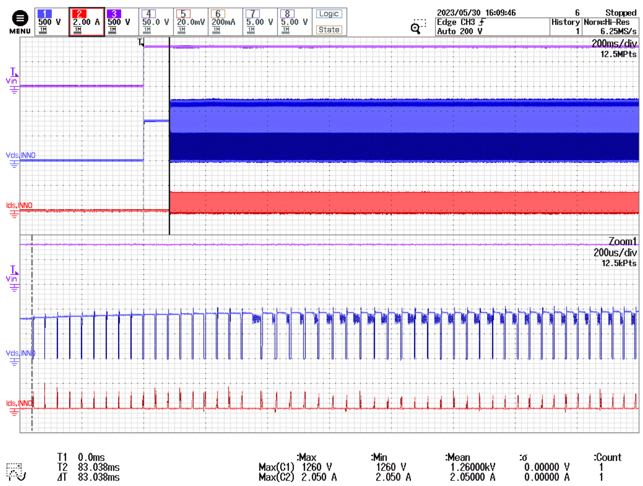


Figure 39 – INN3949CQ Drain Voltage and Current.
800 VDC, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

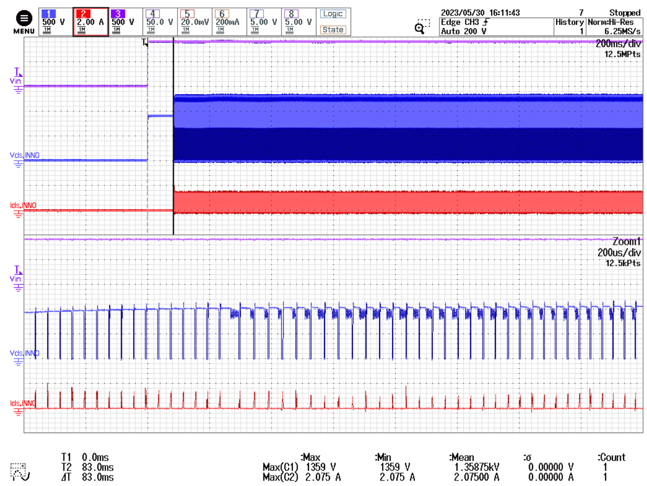


Figure 40 – INN3949CQ Drain Voltage and Current.
900 VDC, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[14] The time between when V_{IN} turned on and the InnoSwitch starts switching was due to the additional t_{AR} delay of InnoSwitch3.
[15] Current waveforms were measured using a Yokogawa current probe.

11.1.3 SR FET Drain Voltage and Current at 25 °C Ambient[16,17]

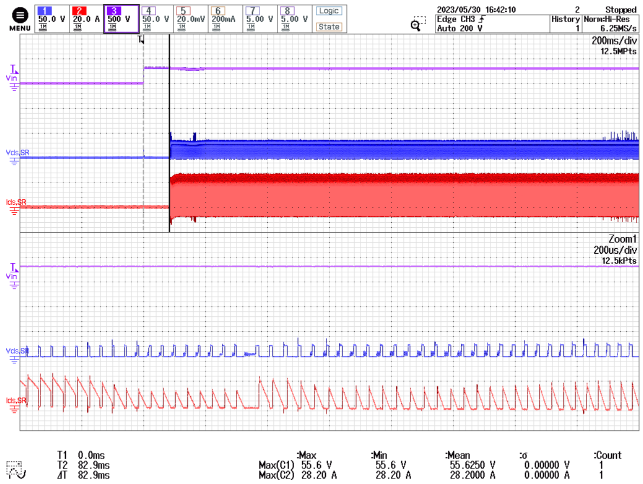


Figure 41 – SR FET Drain Voltage and Current.
300 VDC, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

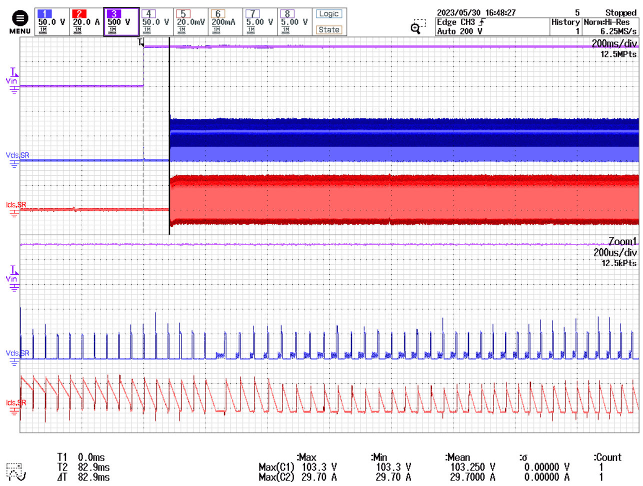


Figure 42 – SR FET Drain Voltage and Current.
800 VDC, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

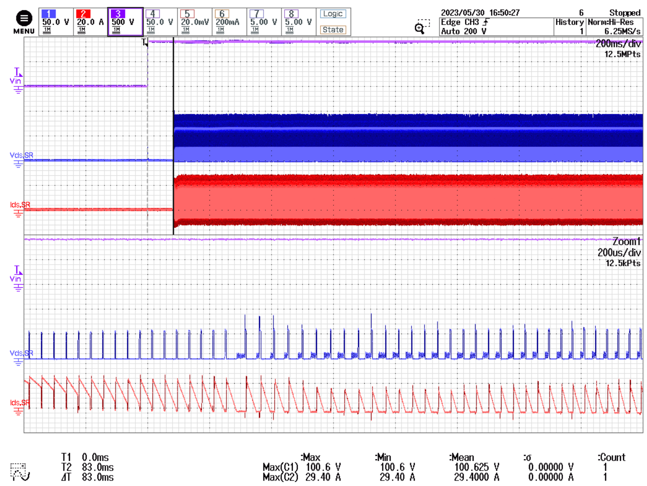


Figure 43 – SR FET Drain Voltage and Current.
900 VDC, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

16 The time between when V_{IN} turned on and the SR FET starts switching was due to the additional t_{AR} delay of InnoSwitch3.
17 Current waveforms were measured using a Yokogawa current probe.

11.1.4 Output Voltage and Current at -40 °C Ambient[18,19]

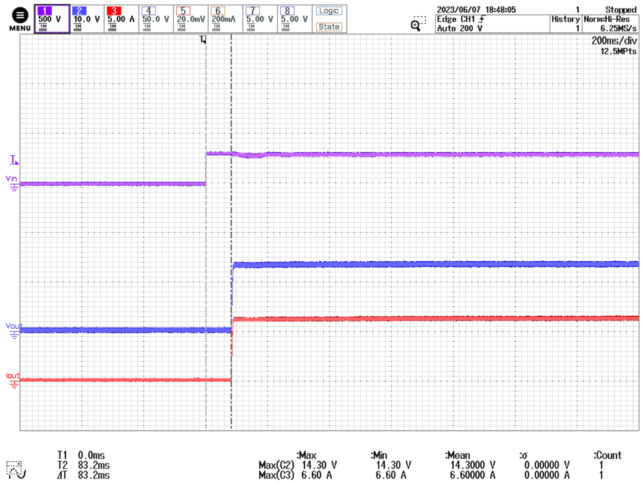


Figure 44 – Output Voltage and Current.
300 VDC, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

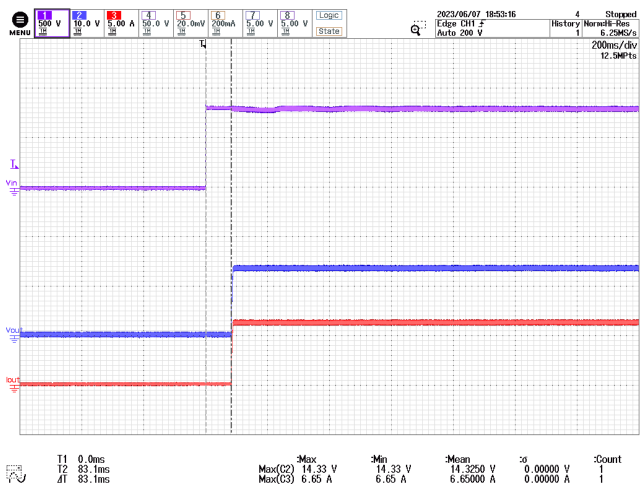


Figure 45 – Output Voltage and Current.
800 VDC, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

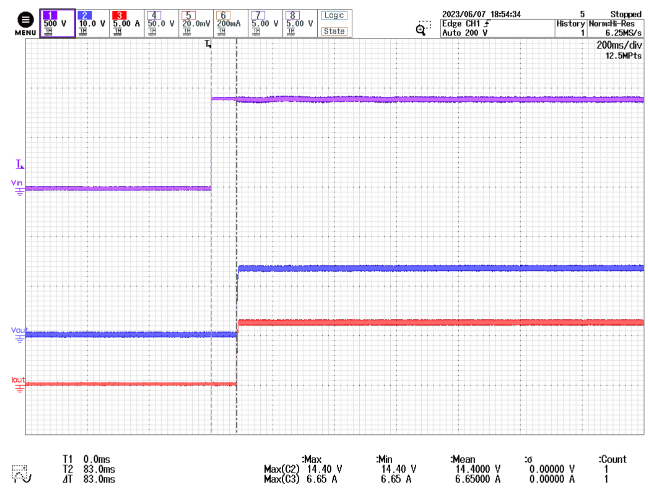


Figure 46 – Output Voltage and Current.
900 VDC, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

[18] Voltage dip on the V_{IN} waveform was due to the effective line impedance from the DC link capacitor to the unit under test.
[19] Current waveforms were measured using a Yokogawa current probe.

11.1.5 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient[20,21]

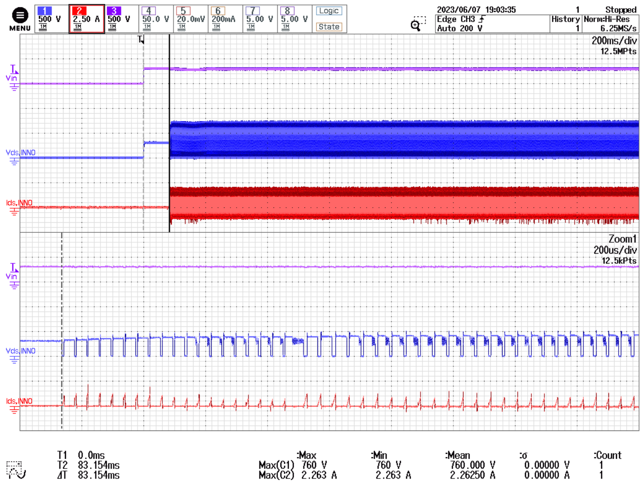


Figure 47 – INN3949CQ Drain Voltage and Current.
300 VDC, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

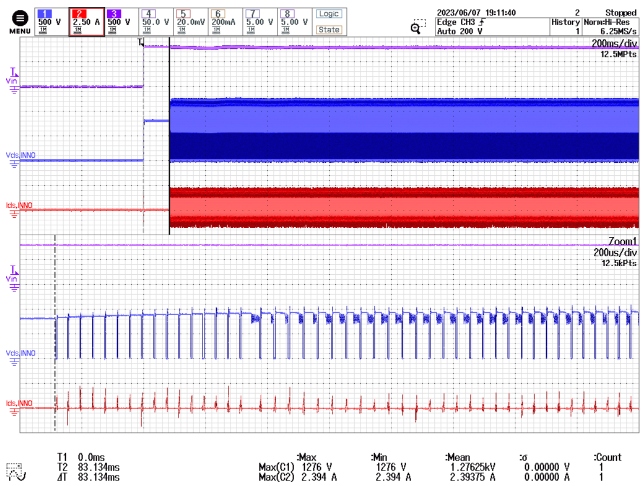


Figure 48 – INN3949CQ Drain Voltage and Current.
800 VDC, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

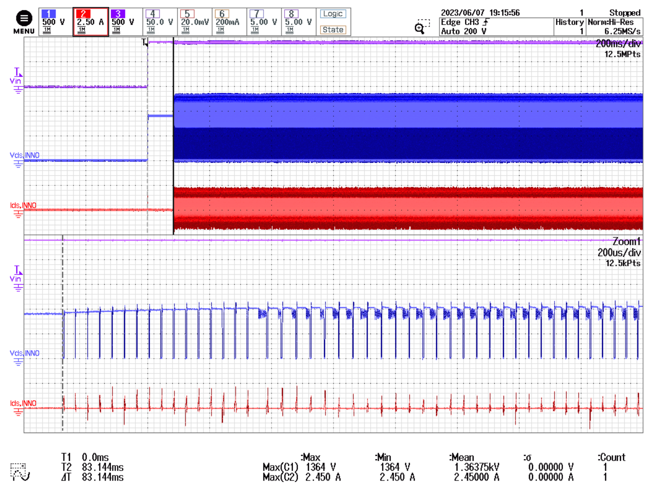


Figure 49 – INN3949CQ Drain Voltage and Current.
900 VDC, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[20] The time between when V_{IN} turned on and the InnoSwitch starts switching was due to the additional t_{AR} delay of InnoSwitch3.
[21] Current waveforms were measured using a Rogowski coil.

11.1.6 SR FET Drain Voltage and Current at -40 °C Ambient[22,23]

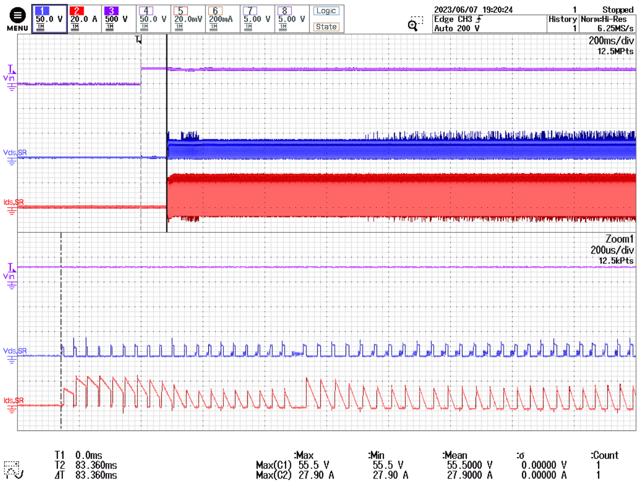


Figure 50 – SR FET Drain Voltage and Current.
300 VDC, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

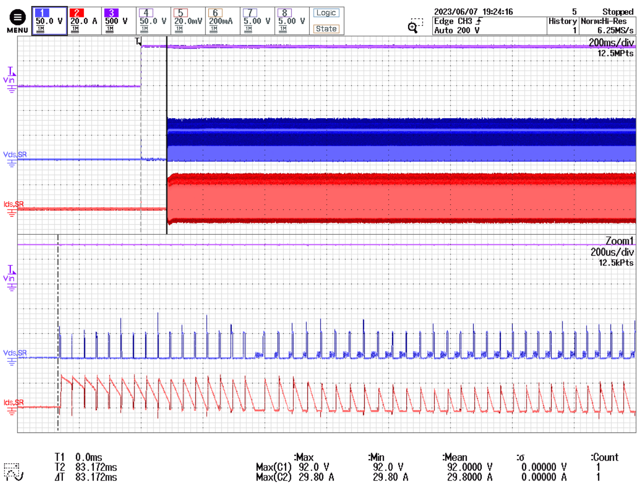


Figure 51 – SR FET Drain Voltage and Current.
800 VDC, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

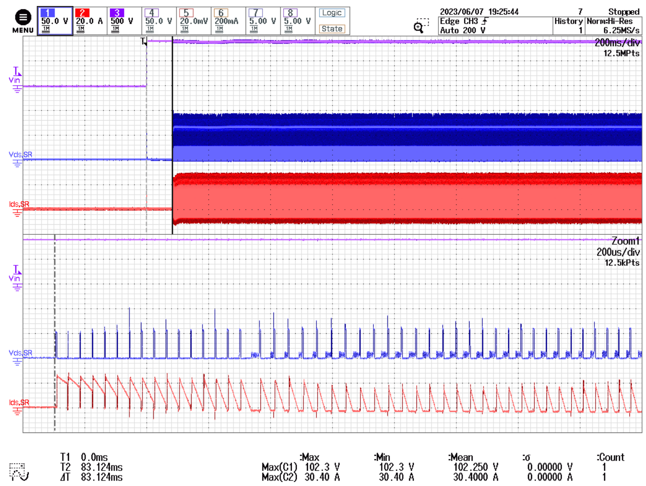


Figure 52 – SR FET Drain Voltage and Current.
900 VDC, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

22 The time between when V_{IN} turned on and the SR FET starts switching was due to the additional t_{AR} delay of InnoSwitch3.

23 Current waveforms were measured using a Rogowski coil.

11.2 Steady-State Waveforms

11.2.1 Switching Waveforms at 85 °C Ambient

11.2.1.1 Normal Operation Component Stress

	Steady-State Switching Waveforms 85 °C Ambient, Full Load					
Input	INN3949CQ			SR FETs		
V_{IN} (V)	I_D (A_{PK})	V_{DS} (V_{PK})	V_{STRESS} (%)	I_D (A_{PK})[24]	V_{DS} (V_{PK})[25]	V_{STRESS} (%)
300	1.63	740	43.5	34.4	57.6	48.0
600	1.33	1070	62.7	35.0	67.0	55.8
800	1.40	1270	74.5	33.8	87.9	73.3
900	1.50	1360	80.1	34.0	98.0	81.7

Table 10 – Summary of Critical Component Voltage Stresses at 85 °C Ambient.

[24] SR FET current is the sum of Q100 and Q101 currents.
[25] SR FET voltage was taken from Q101.

11.2.1.2 InnoSwitch3-AQ and SR FET[26] Drain Voltage at 85 °C Ambient

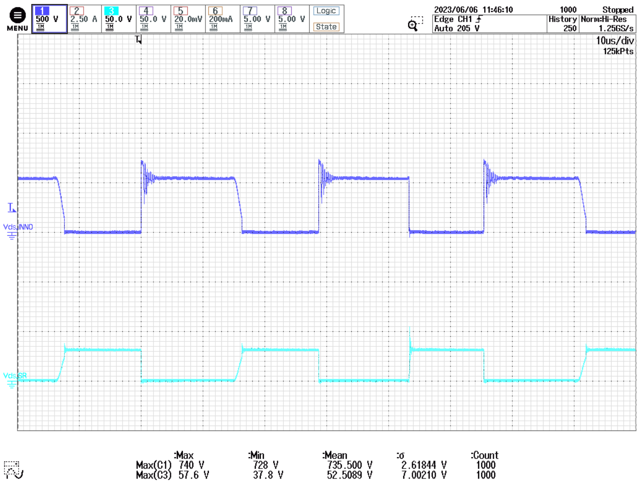


Figure 53 – InnoSwitch3-AQ and SR FET Drain Voltage.[27]
300 VDC, 6.37 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 10 µs / div.

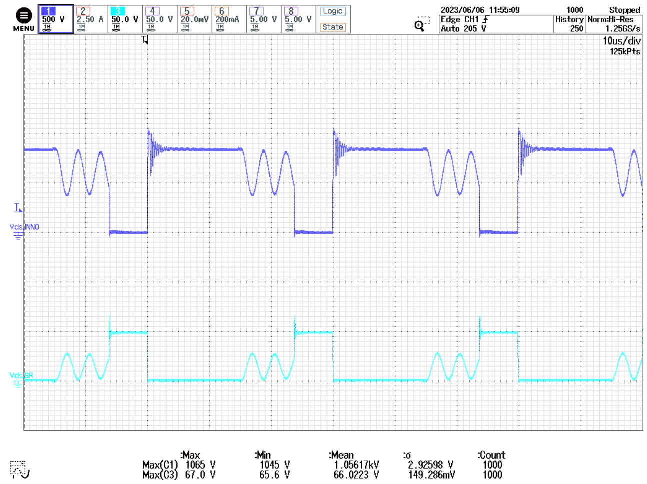


Figure 54 – InnoSwitch3-AQ and SR FET Drain Voltage.
600 VDC, 6.37 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 10 µs / div.

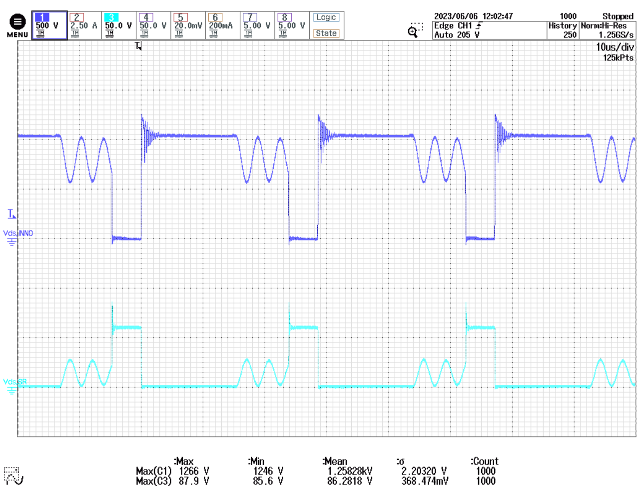


Figure 55 – InnoSwitch3-AQ and SR FET Drain Voltage.
800 VDC, 6.37 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 10 µs / div.

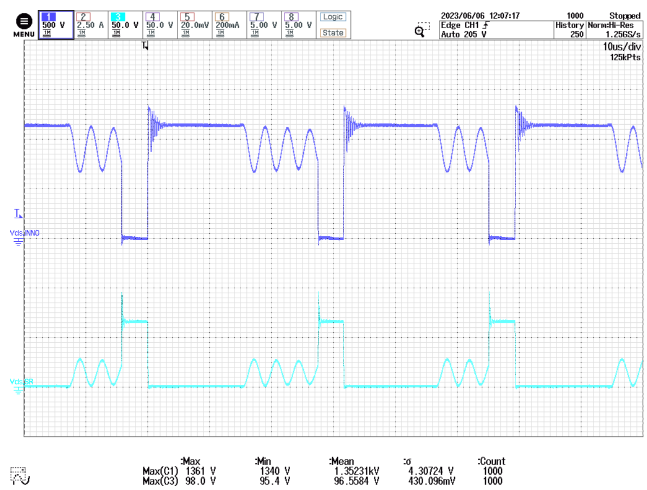


Figure 56 – InnoSwitch3-AQ and SR FET Drain Voltage.
900 VDC, 6.37 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 10 µs / div.

[26] SR FET voltage waveform was taken from Q101.
[27] Intermittent spikes on the SR FET V_{DS} waveform were due to the unit operating intermittently in CCM at 300 V_{IN}.

11.2.2 Switching Waveforms at 25 °C Ambient

11.2.2.1 Normal Operation Component Stress

	Steady-State Switching Waveforms 25 °C Ambient, Full Load					
Input	**INN3949CQ**			**SR FETs**		
V_{IN} (V)	**I_D (A_{PK})**	**V_{DS} (V_{PK})**	**V_{STRESS} (%)**	**I_D (A_{PK})[28]**	**V_{DS} (V_{PK})[29]**	**V_{STRESS} (%)**
300	1.54	770	45.3	33.2	38.0	31.7
600	1.56	1060	62.4	33.0	68.0	56.7
800	1.56	1270	74.7	33.4	87.5	72.9
900	1.72	1370	80.6	33.8	97.1	80.9

Table 11 – Summary of Critical Component Voltage Stresses at 25 °C Ambient.

[28] SR FET current is the sum of Q100 and Q101 currents.
[29] SR FET voltage was taken from Q101.

11.2.2.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient

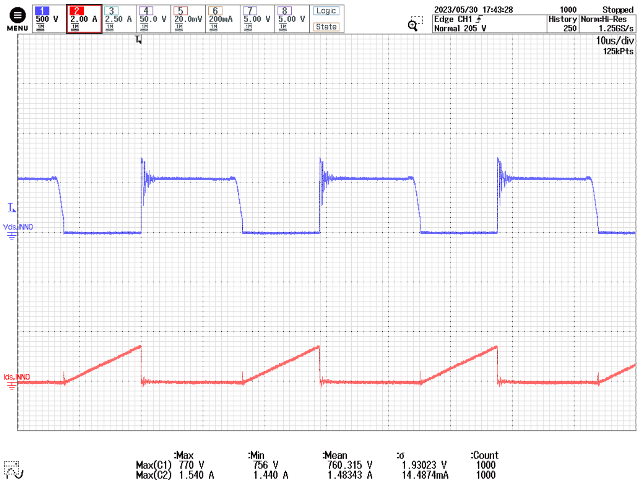


Figure 57 – InnoSwitch3-AQ Drain Voltage and Current.
300 VDC, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
Time: 10 μs / div.

Figure 58 – InnoSwitch3-AQ Drain Voltage and Current.
600 VDC, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
Time: 10 μs / div.

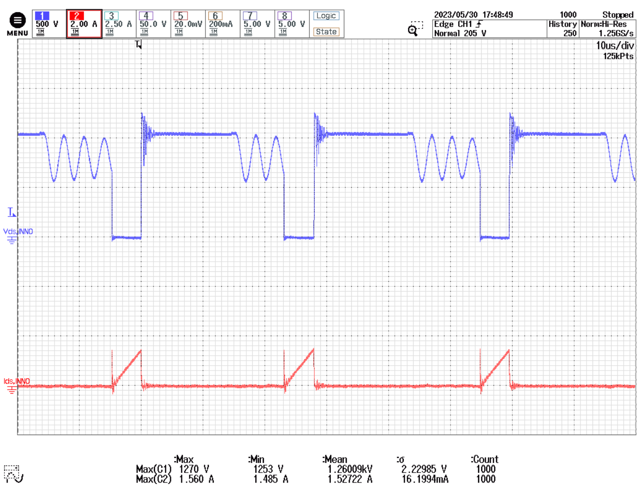


Figure 59 – InnoSwitch3-AQ Drain Voltage and Current.
800 VDC, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
Time: 10 μs / div.

Figure 60 – InnoSwitch3-AQ Drain Voltage and Current.
900 VDC, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
Time: 10 μs / div.

11.2.2.3 SR FET Drain Voltage and Current at 25 °C Ambient[30]

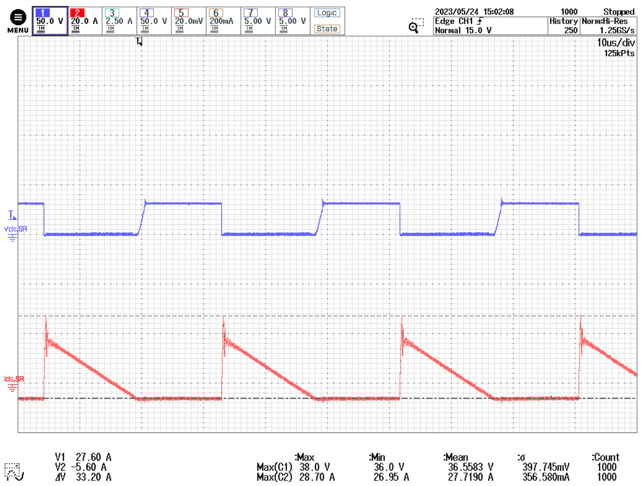


Figure 61 – SR FET Drain Voltage and Current.
300 VDC, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
Time: 10 µs / div.

Figure 62 – SR FET Drain Voltage and Current.
600 VDC, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
Time: 10 µs / div.

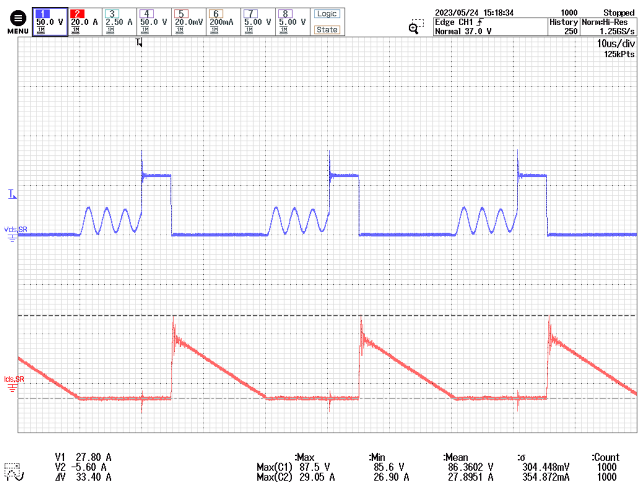


Figure 63 – SR FET Drain Voltage and Current.
800 VDC, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
Time: 10 µs / div.

Figure 64 – SR FET Drain Voltage and Current.
900 VDC, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
Time: 10 µs / div.

30 SR FET voltage waveform was taken from Q101.

11.2.2.4 Short-Circuit Response

The unit was tested by applying an output short-circuit during normal operation and then removing the short-circuit to see if the unit would recover and operate normally. The expected response during short-circuit is for the unit to go to auto-restart (AR) mode and attempt recovery every 1.70 to 2.11 seconds. Full load is at 2.12 ohms constant-resistance.

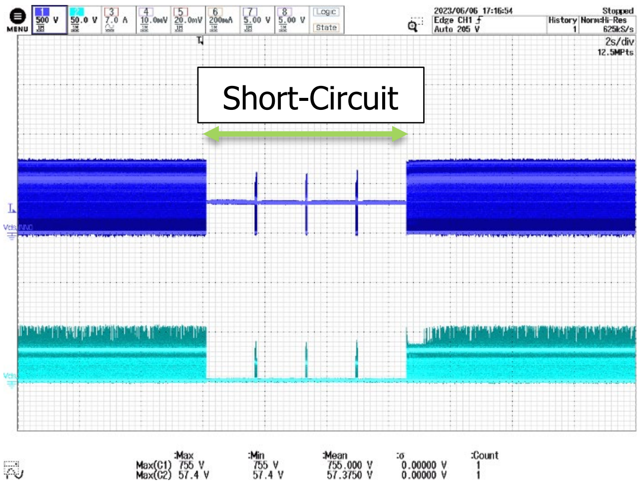


Figure 65 – InnoSwitch3-AQ and SR FET Drain Voltage.
300 VDC, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 2 s / div.

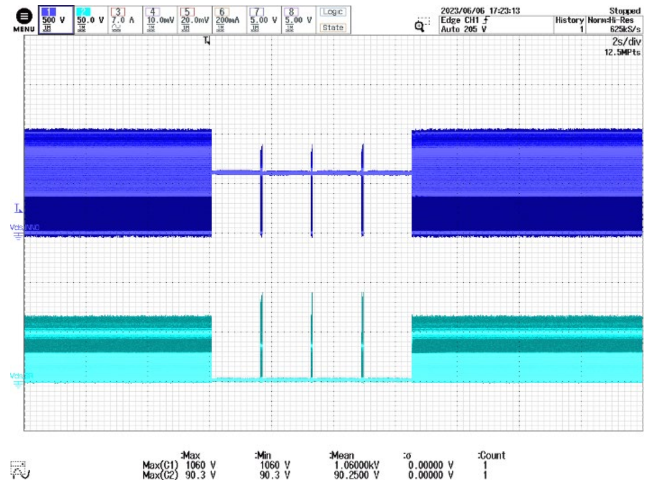


Figure 66 – InnoSwitch3-AQ and SR FET Drain Voltage.
600 VDC, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 2 s / div.

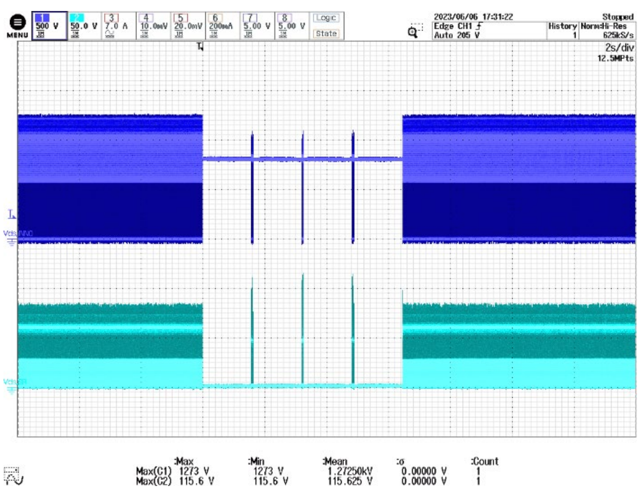


Figure 67 – InnoSwitch3-AQ and SR FET Drain voltage.
800 VDC, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 2 s / div.

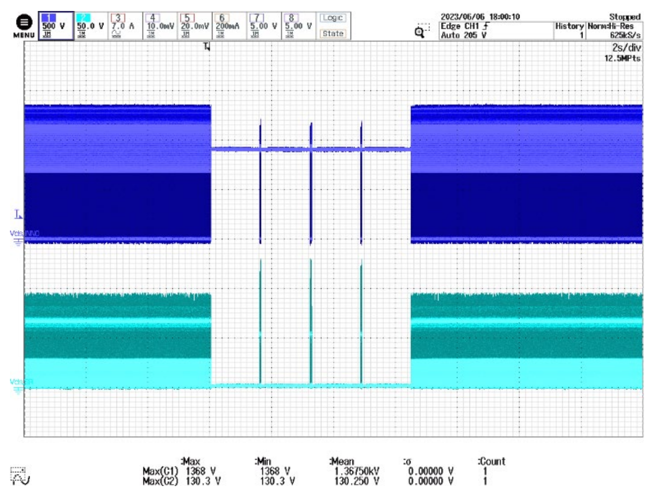


Figure 68 – InnoSwitch3-AQ and SR FET Drain voltage.
900 VDC, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 2 s / div.

11.3 Load Transient Response

The output voltage waveform was captured during a dynamic load transient from 0% to 50%, 50% to 100%, and 10% to 90%. The duration for each load point was set to 100 ms with a load slew rate of 100 mA / μs. The test was performed at 85 °C ambient.

Dynamic Load Settings	V_{IN} (V)	$V_{OUT(MAX)}$ (V)	$V_{OUT(MIN)}$ (V)
0% to 50%	300	13.6	13.3
	600	13.7	13.4
	800	13.7	13.3
	900	13.7	13.3
50% to 100%	300	13.8	13.2
	600	13.7	13.2
	800	13.7	13.3
	900	13.7	13.3
10% to 90%	300	13.7	13.2
	600	13.7	13.3
	800	13.7	13.3
	900	13.7	13.3

Table 12 – Load Transient Response.

11.3.1 Output Voltage Ripple with 0% to 50% Transient Load at 85 °C Ambient

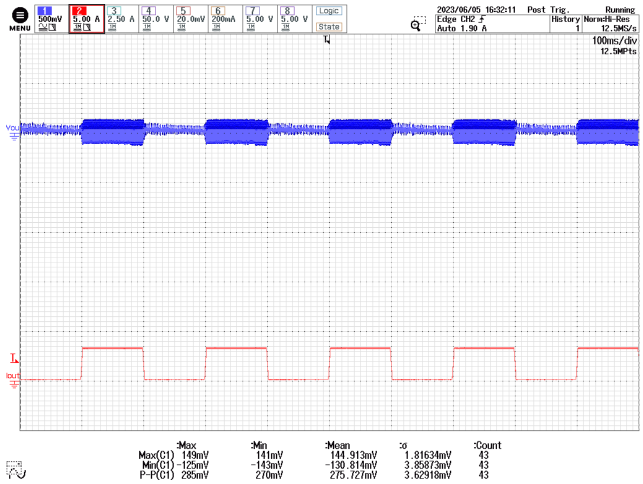


Figure 69 – Output Voltage and Current.
300 VDC, 0 A to 3.19 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

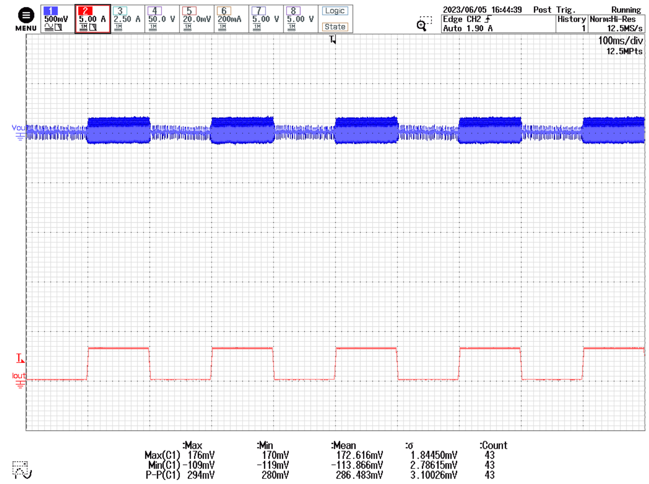


Figure 70 – Output Voltage and Current.
600 VDC, 0 A to 3.19 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

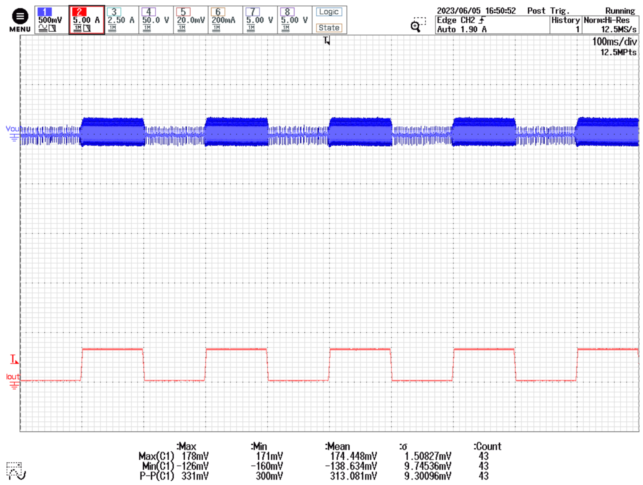


Figure 71 – Output Voltage and Current.
800 VDC, 0 A to 3.19 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

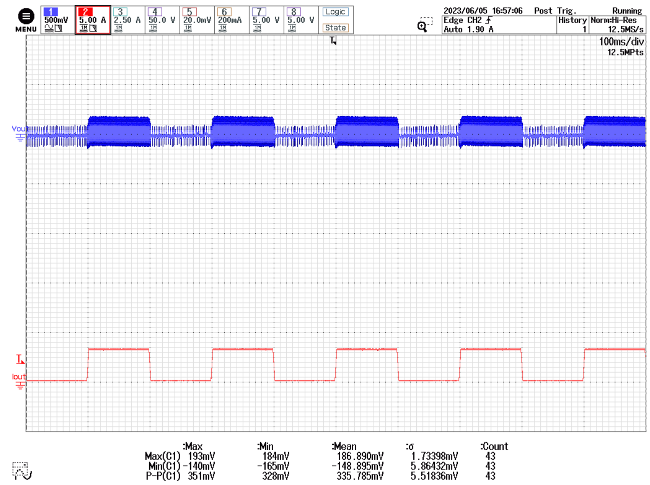


Figure 72 – Output Voltage and Current.
900 VDC, 0 A to 3.19 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

11.3.2 Output Voltage Ripple with 50% to 100% Transient Load at 85 °C Ambient

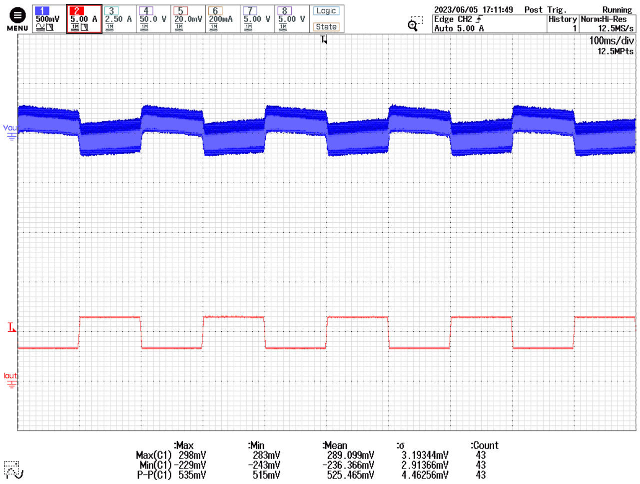


Figure 73 – Output Voltage and Current.
300 VDC,
3.19 A to 6.37 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

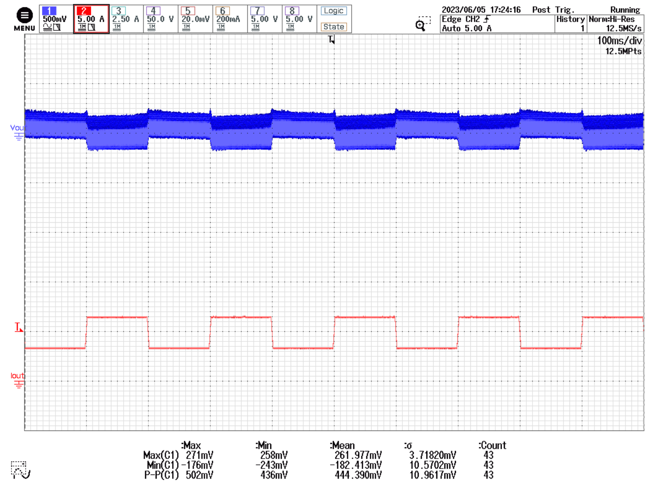


Figure 74 – Output Voltage and Current.
600 VDC,
3.19 A to 6.37 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

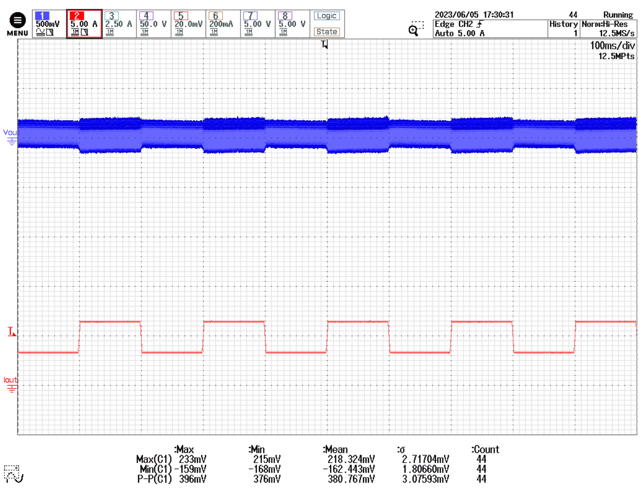


Figure 75 – Output Voltage and Current.
800 VDC,
3.19 A to 6.37 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

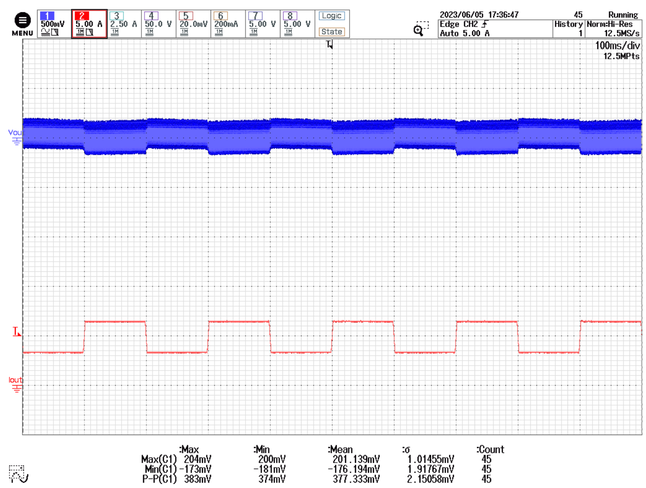


Figure 76 – Output Voltage and Current.
900 VDC,
3.19 A to 6.37 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

11.3.3 Output Voltage Ripple with 10% to 90% Transient Load at 85 °C Ambient

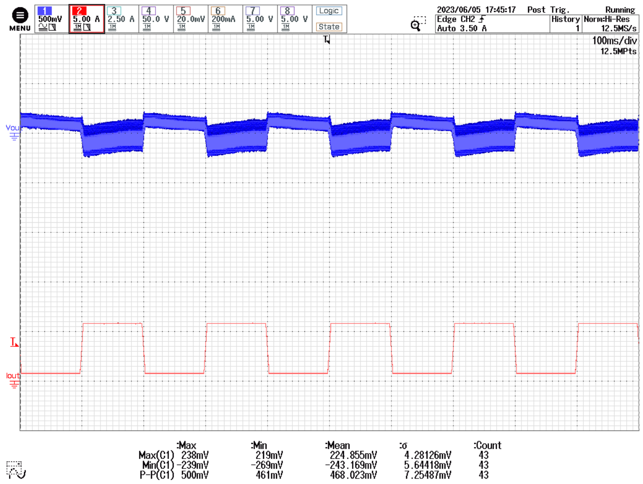


Figure 77 – Output Voltage and Current.
300 VDC,
637 mA to 5.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

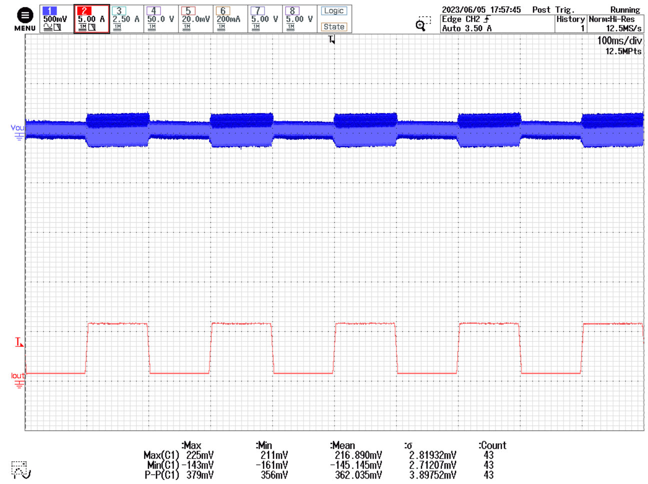


Figure 78 – Output Voltage and Current.
600 VDC,
637 mA to 5.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

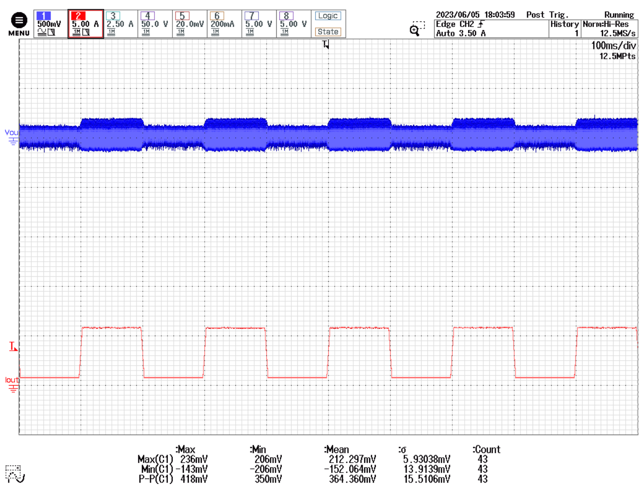


Figure 79 – Output Voltage and Current.
800 VDC,
637 mA to 5.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

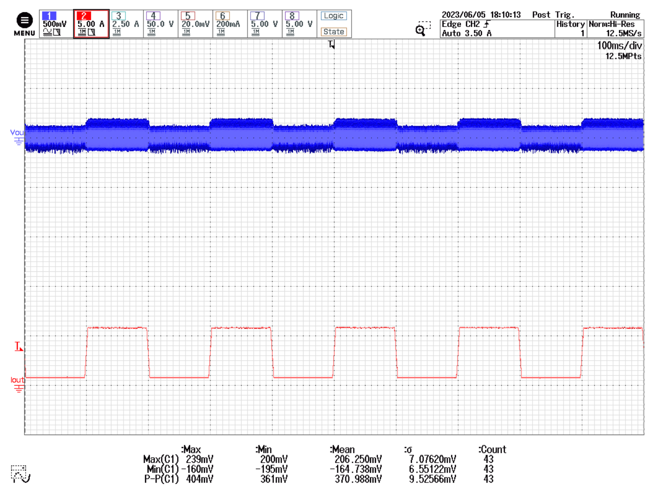


Figure 80 – Output Voltage and Current.
900 VDC,
637 mA to 5.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

A modified oscilloscope test probe was used for output voltage ripple measurements to reduce spurious signals due to pick-up. Details of the probe modification were provided in Figure 81 and Figure 82 below.

A CT2708 probe adapter was affixed with a 1 μF / 50 V ceramic capacitor placed in parallel between the probe tip and GND terminal. A twisted pair of wires, kept as short as possible, was soldered directly between the probe and the output terminals.

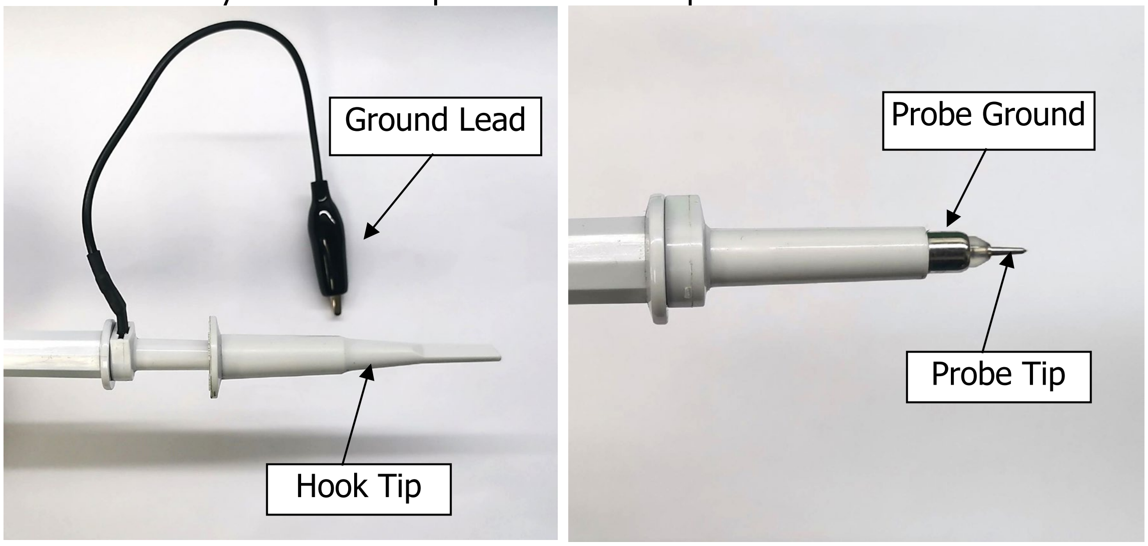


Figure 81 – Oscilloscope Probe Prepared for Ripple Measurement. (Hook Tip and Ground Lead Removed.)

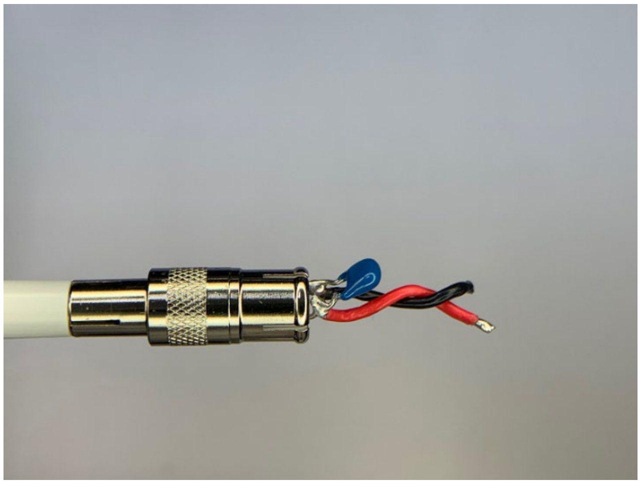


Figure 82 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement, and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the output terminals using the ripple measurement probe with a decoupling capacitor.

11.4.2.1 Output Voltage Ripple at 85 °C Ambient with Constant Full Load[31]

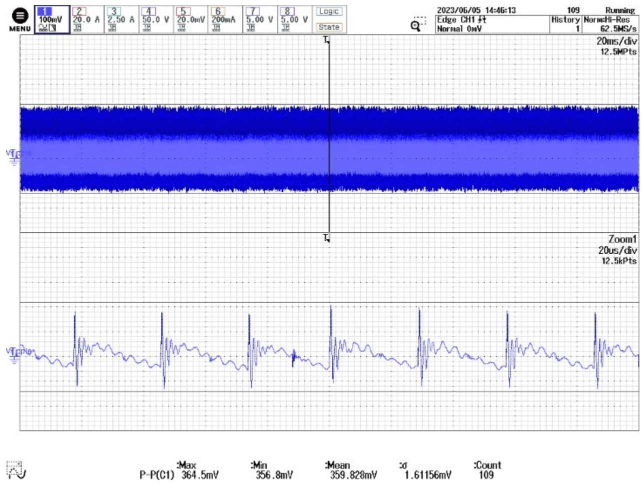


Figure 83 – Output Voltage Ripple.
300 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 360 mV.

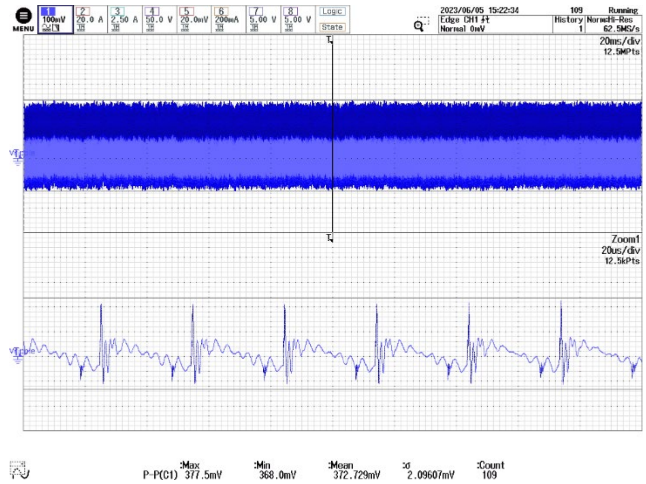


Figure 84 – Output Voltage Ripple.
600 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 373 mV.

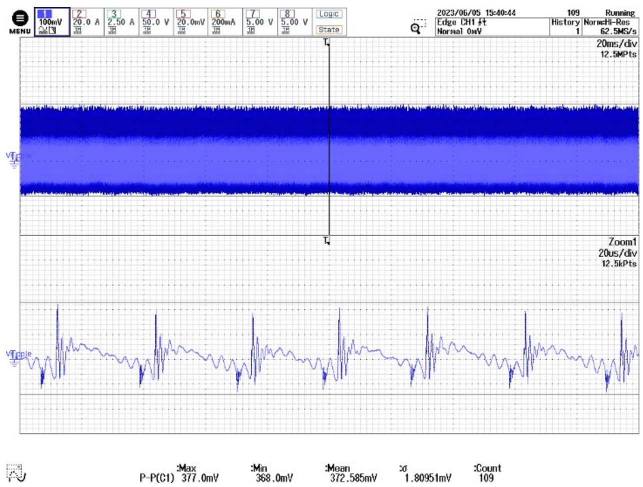


Figure 85 – Output Voltage Ripple.
800 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 373 mV.

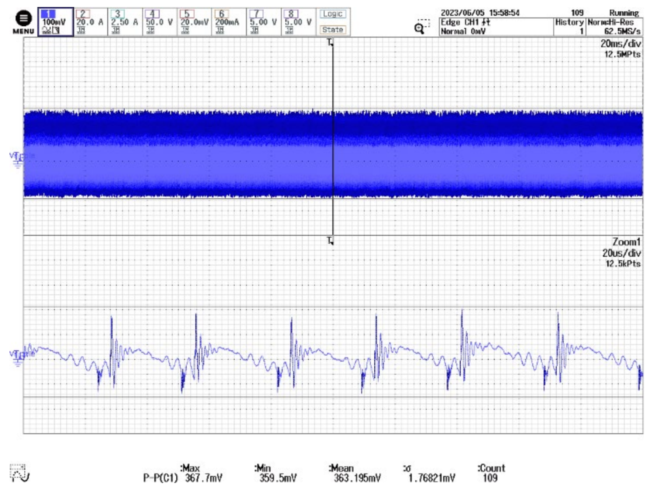


Figure 86 – Output Voltage Ripple.
900 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 363 mV.

[31] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at 25 °C Ambient with Constant Full Load[32]

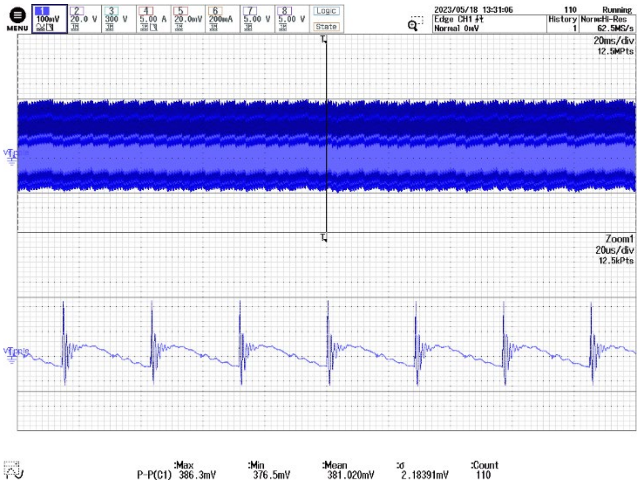


Figure 87 – Output Voltage Ripple.
300 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 381 mV.

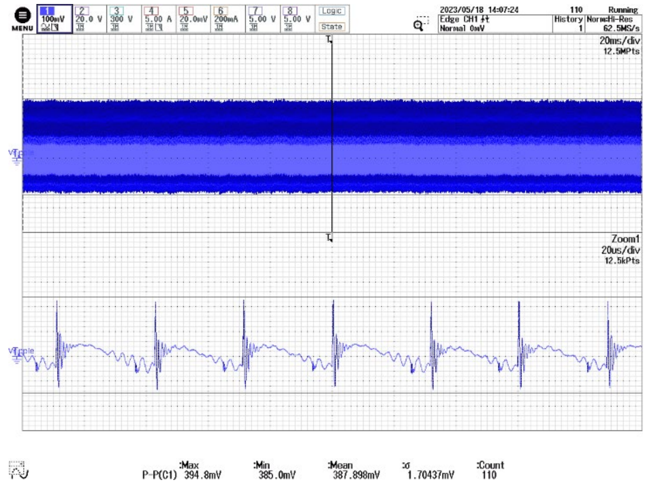


Figure 88 – Output Voltage Ripple.
600 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 388 mV.

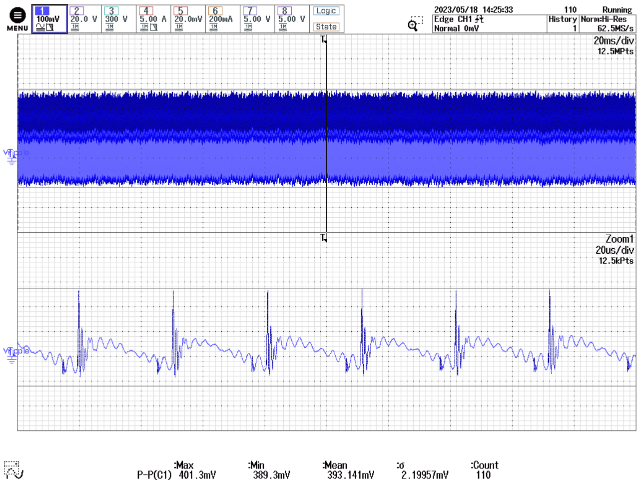


Figure 89 – Output Voltage Ripple.
800 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 393 mV.

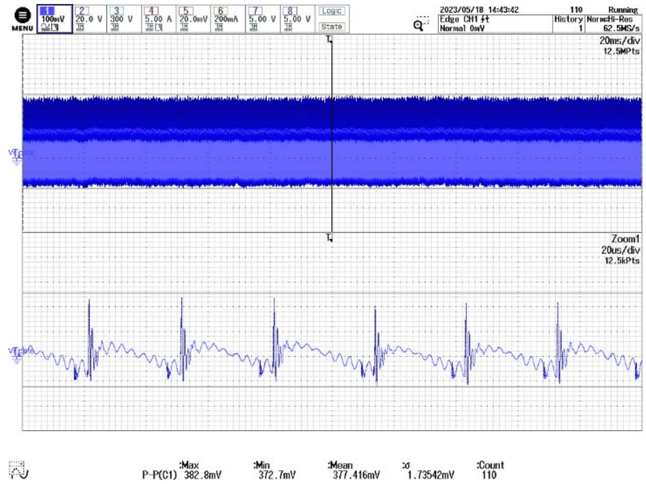


Figure 90 – Output Voltage Ripple.
900 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 377 mV.

[32] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at -40 °C Ambient with Constant Full Load[33]

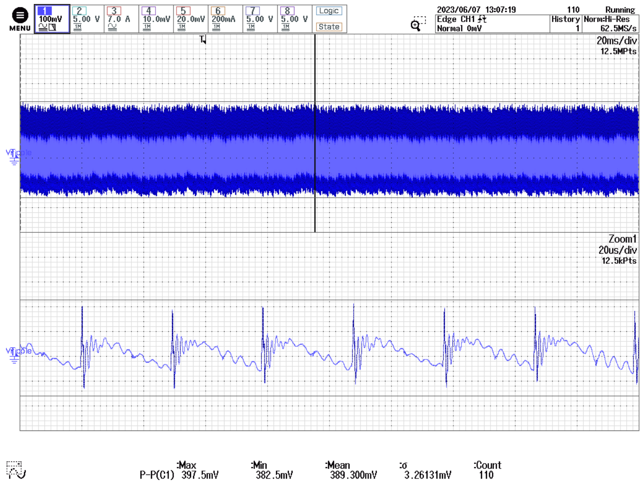


Figure 91 – Output Voltage Ripple.
300 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 389 mV.

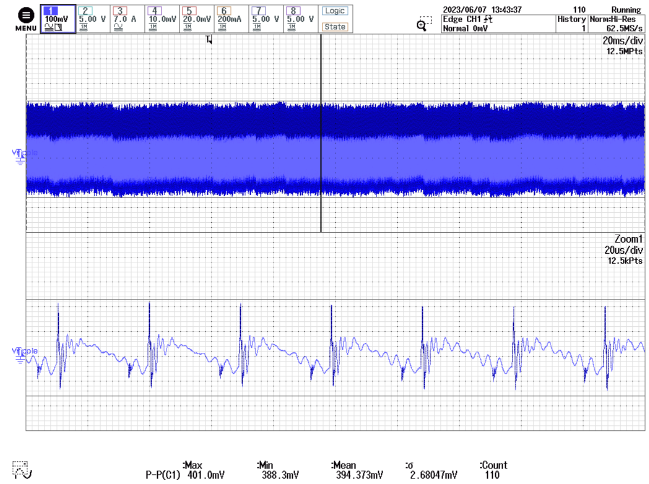


Figure 92 – Output Voltage Ripple.
600 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 394 mV.

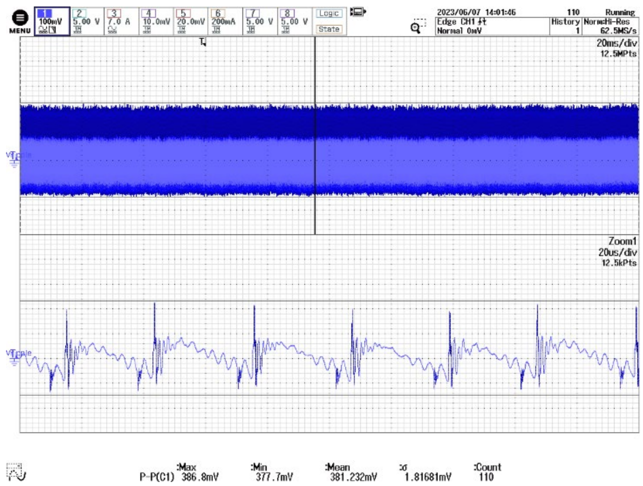


Figure 93 – Output Voltage Ripple.
800 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 381 mV.

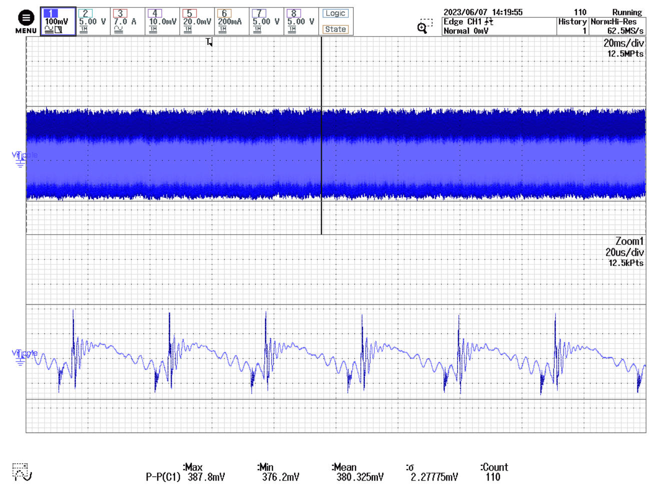


Figure 94 – Output Voltage Ripple.
900 VDC, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 380 mV.

[33] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 85 °C Ambient

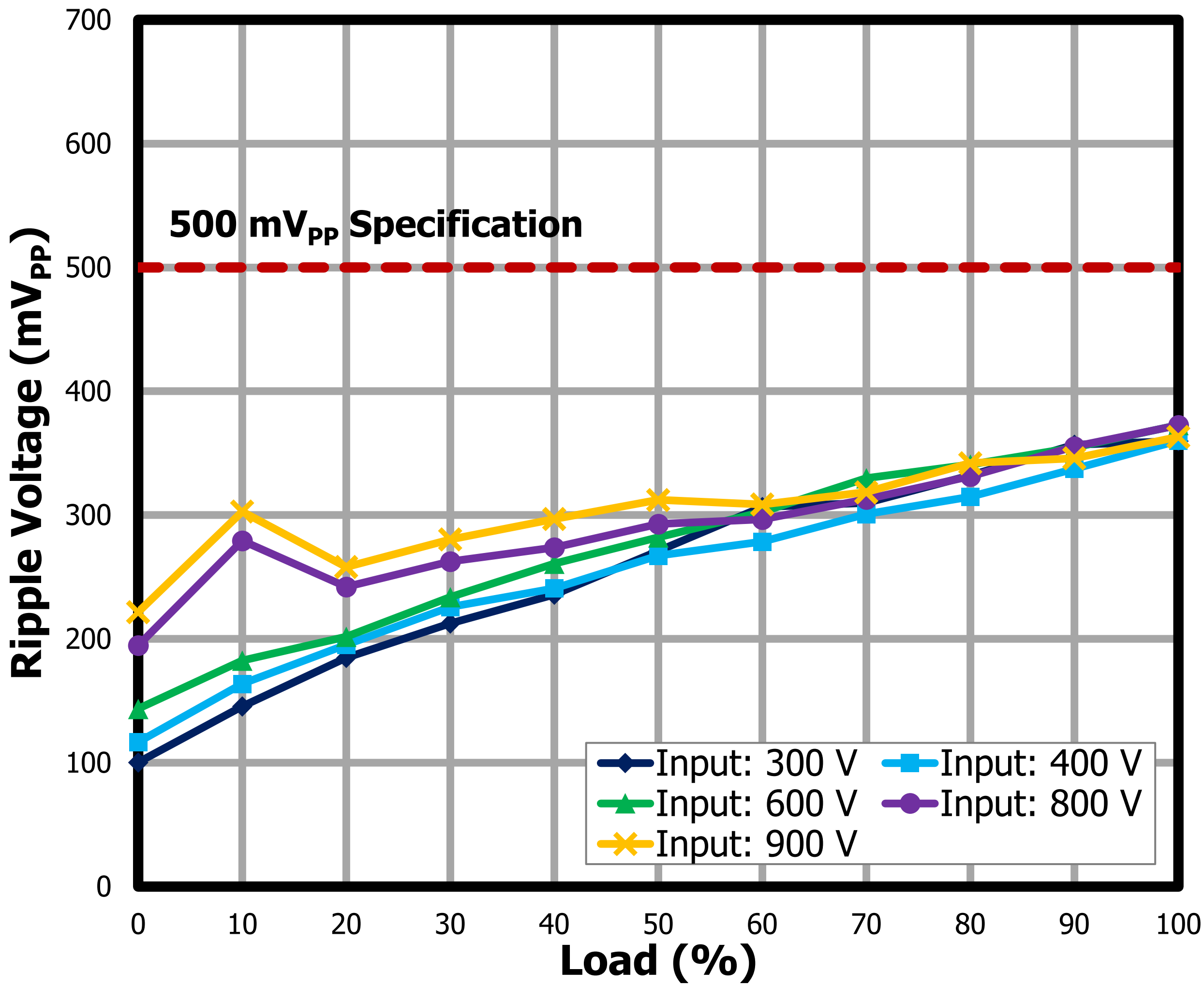


Figure 95 – Output Ripple Voltage Across Full Load Range (85 °C Ambient).

11.4.3.2 Output Ripple at 25 °C Ambient

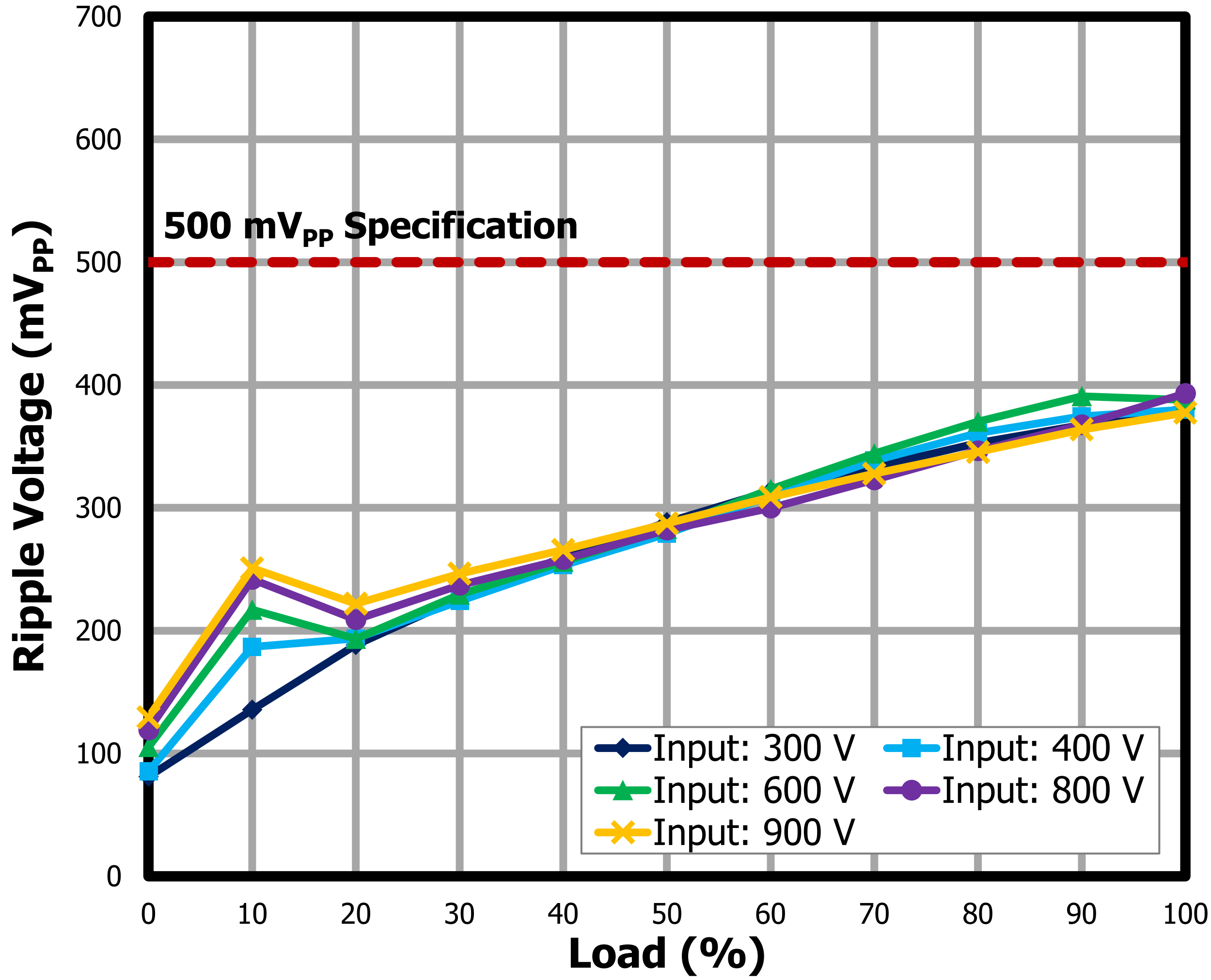


Figure 96 – Output Ripple Voltage Across Full Load Range (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C Ambient

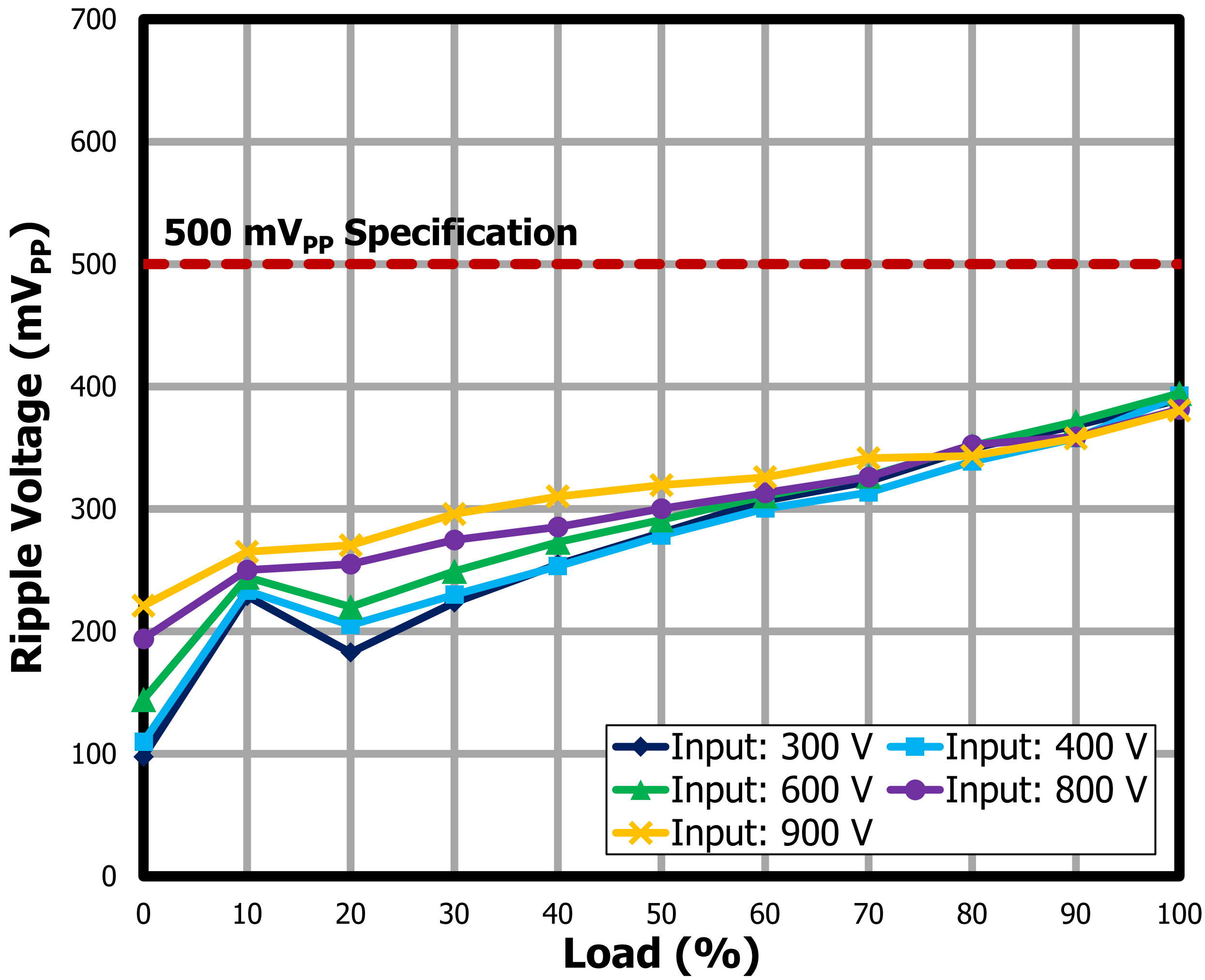


Figure 97 – Output Ripple Voltage Across Full Load Range (-40 °C Ambient).

12 Output Overload

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C and allowed to stabilize for 30 minutes before turning on the unit under test. The unit was allowed to stablize for 20 minutes after each change in input voltage. For every loading condition, the unit under test was allowed to settle for 60 seconds before output voltage and current measurements were taken.

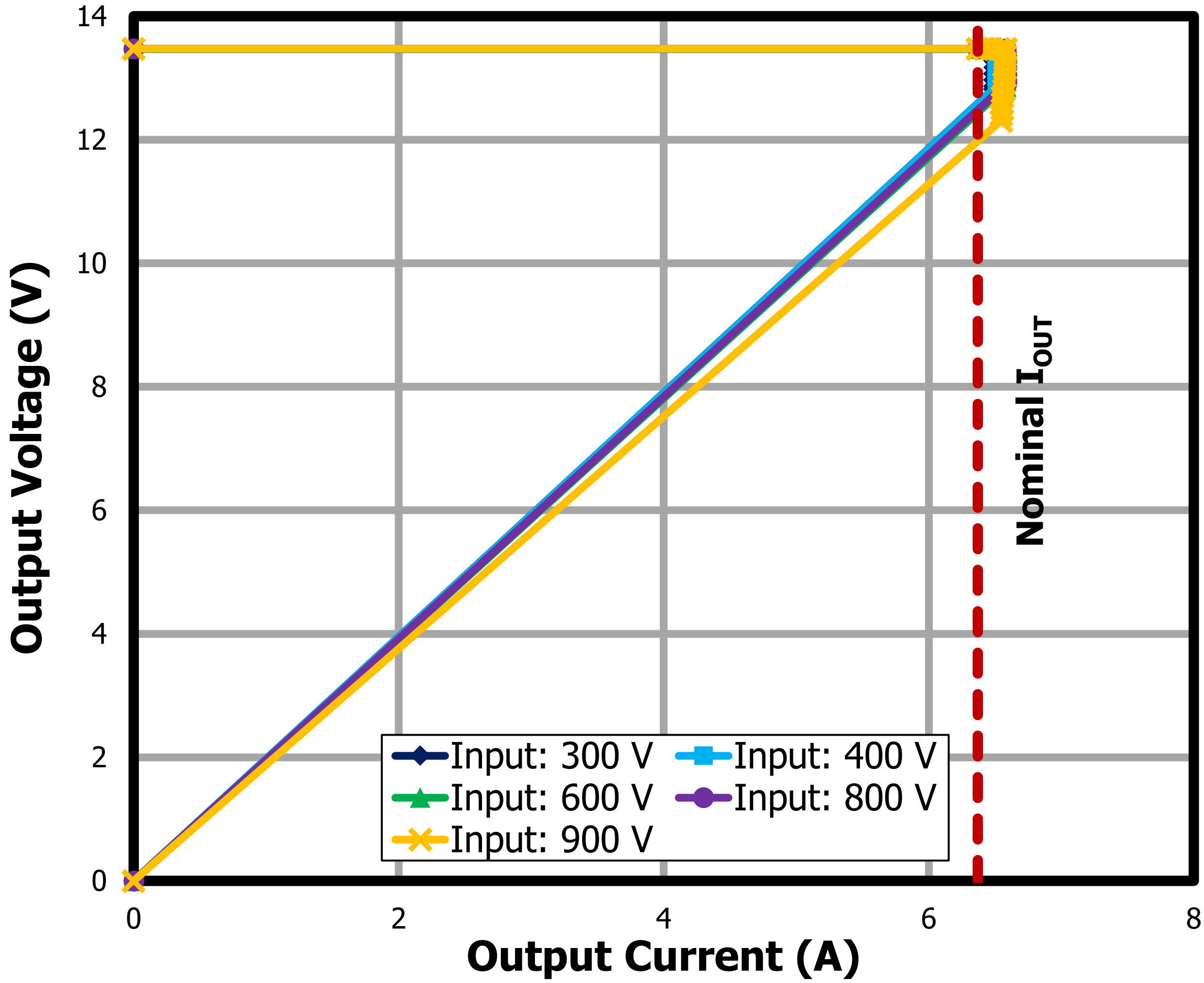


Figure 98 – Output Overload Curve at 85 °C Ambient.

13 Maximum Output Power

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C and allowed to stabilize for 30 minutes before the unit under test was turned on. To allow component temperatures to settle, the unit was loaded for 30 minutes before each test was started. Maximum output power at each given input voltage was determined by finding the maximum loading condition at which the unit did not enter auto-restart (AR) or trigger any overtemperature protection. Case temperature for critical components was also considered when determining the maximum output power capability of the power supply.

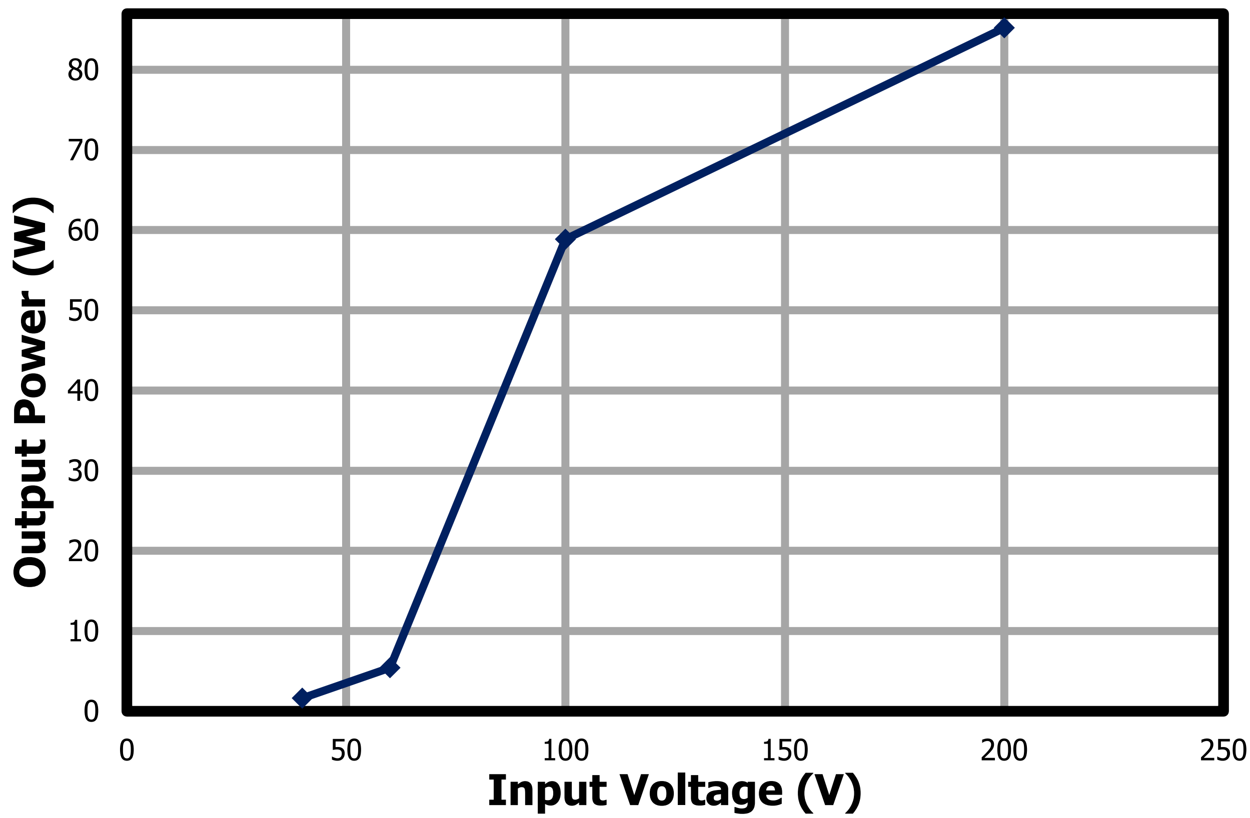


Figure 99 – Maximum Output Power Curve at 85 °C Ambient.

Input Voltage (V)	PIXls Calculated Maximum Output Power[34] (W)	Measured Maximum Output Power (W)	Limiting Factor for Measured Maximum Output Power	Value
200	86.0	86.0	Design maximum output power reached	86.0 W
100	86.0	58.9	Transformer winding temperature	134 °C
60	5.1	5.4	InnoSwitch3-AQ power limit	-
40	2.1	1.6	InnoSwitch3-AQ power limit	-

Table 13 – Maximum Output Power Capability Limiting Factor.

[34] Calculated maximum output power was only determined by using the PIXls "Input Voltage Set-Points Analysis" feature. Component thermal calculations were not included in this column.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
28-Feb-25	JS	A	Initial Release.	Apps & Mktg

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