HiperLCS-2 Chipset

Off-Line LLC Switcher ICs with Integrated 600 V Half-Bridge Synchronous Rectification and FluxLink Feedback

Product Highlights

Highly Integrated, Compact Footprint

- Up to 98.1% efficiency
- Very low component count and small footprint package
- Up to 1650 W with heat sink
- Self-powered start-up
- 600 V Half-Bridge, rugged fast recovery body diode, auto dead time, hard switch detect, current sense and thermal detect
- HB auto dead time and hard switch detect
- Selectable center frequency (90, 120, 180, 240 kHz)
- Secondary-side sensing and feedback control with fast transient response
- Synchronous rectification driver
- Integrated FluxLink™, HIPOT-isolated control link

EcoSmart™ – Energy Efficient

- As low as 65 mW no-load including line sense
- Output always in regulation, 0-100% load step
- Easily meets all global energy efficiency regulations

Advanced Protection / Safety Features

- HB and SR shoot-through protection
- Power-up pin open/short check
- System short-circuits, thermal, HB OCP, FB open, fast input line UV/OV and PMAX protection

Scalable Power Delivery

- 80 W – 1440 W for adapter (free convection)
- 520 W – 1650 W open frame (forced air)

Optional Features

- Auto-restart or latching fault response for output OVP/UVP
- Latching or hysteretic primary over-temperature protection
- External faults detect and remote on/off
- Inrush-relay drive output pin
- Provides start-up bias for PFC stage

Full Safety and Regulatory Compliance

- Reinforced isolation, isolation voltage >4000 VAC
- UL1577 isolation voltage 4000 VAC (max), CQC and TUV (EN62368-1) safety approved

Applications

- High efficiency power supplies up to 1650 W continuous
- Consumer electronics – TV, PC, e-bike, EV 2-/3-wheeler and tool chargers

Description

The HiperLCS™-2 chipset achieves high efficiency and compact size in power supplies up to 220 W with no heat sink and 1650 W with heat sink. This IC chipset simplifies the design and manufacture of LLC resonant power converters. The LCS726x primary-side devices incorporate 600 V FREDFET in a half-bridge arrangement with control, level shifting, drive and self-powered start-up. The LSR2000C master controller device provides reinforced isolated feedback, output sensing and SR management.

HiperLCS-2 chipset incorporates multiple protection features including line over and undervoltage protection, output overvoltage and over-temperature shutdown. Device fault response options support common combinations of latching and auto-restart behaviors required by applications such as chargers, adapters, consumer electronics and industrial systems.

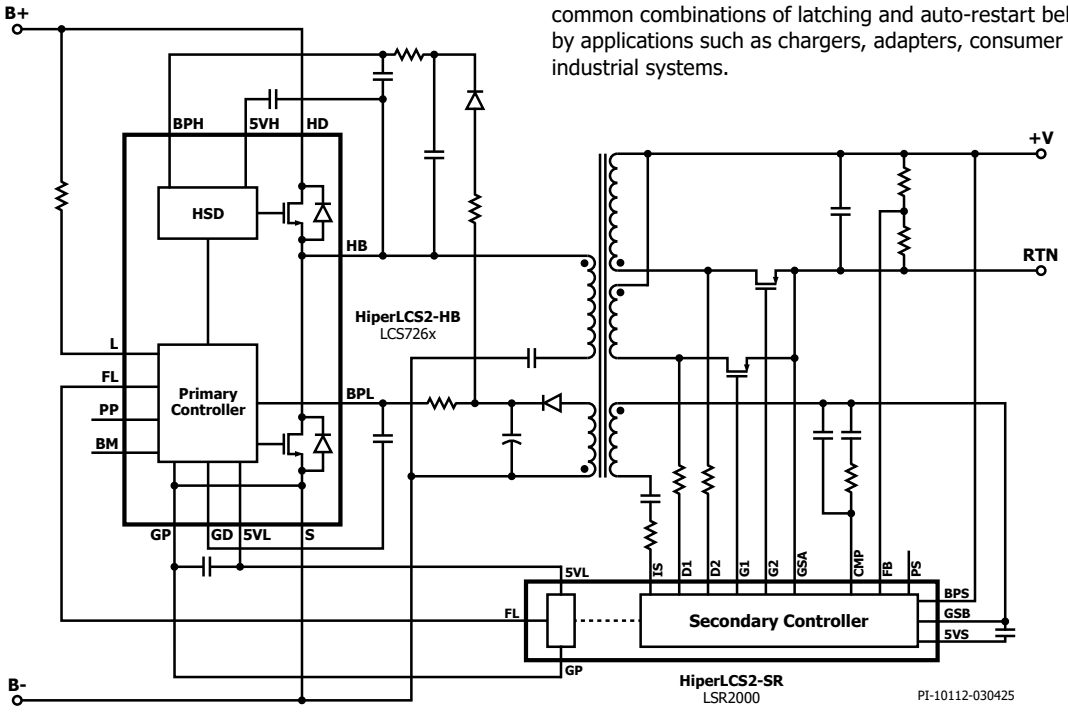


Figure 1. Typical Application Schematic.

Output Power Table

Power Device	Safety Isolation Device	385 VDC ±5%		
		Adapter[1]	Forced Air Cooled[2]	Peak Power[3]
LCS7260C	**LSR2000C**	80 W	N/A	135 W
LCS7262C		120 W	N/A	205 W
LCS7265C		220 W	N/A	375 W
LCS7265Z		460 W	520 W	780 W
LCS7268Z		720 W	830 W	1225 W
LCS7269Z		1440 W	1650 W	2450 W

Table 1. Output Power Table.

Notes:

1. Power Device: Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient. Max output power is dependent on the design, with condition that T_J <110 °C.
2. Forced air cooled: With combination of heat sink and airflow, sufficient to maintain T_J < 110 ºC
3. Power Device: Minimum peak power capability (not thermally limited).
   Where Duty (Pk) = P(pk 50 ms) / P(adapter) < = 170%.

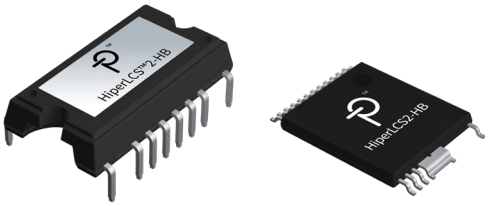


Figure 2. Primary-Side Packages.
(Left) POWeDIP-20B
(Right) InSOP-24C
Top View.

Figure 3. HiperLCS2-SR.
Safety Isolation Package,
InSOP-24D Top View.

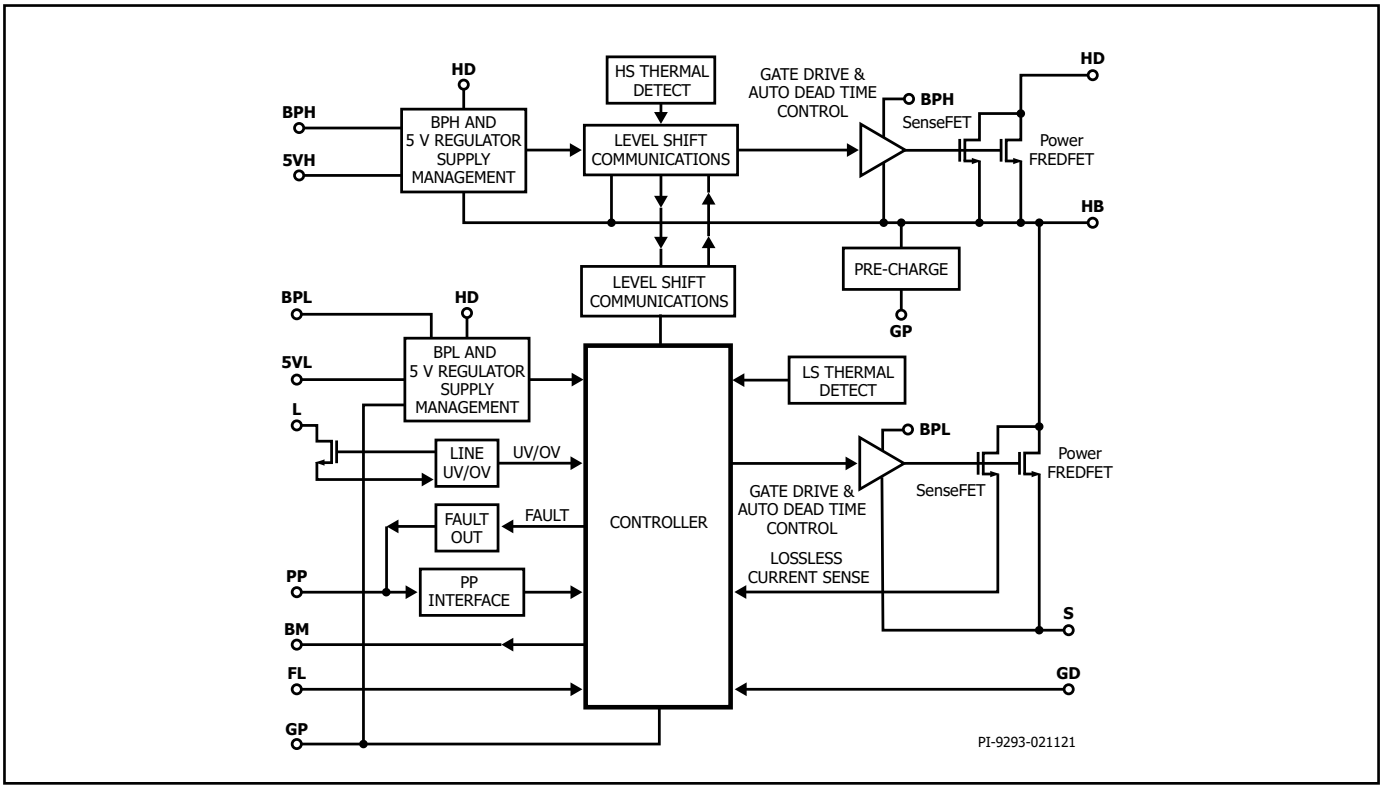


Figure 4. Primary Controller (Low-Side and High-Side), Block Diagram.

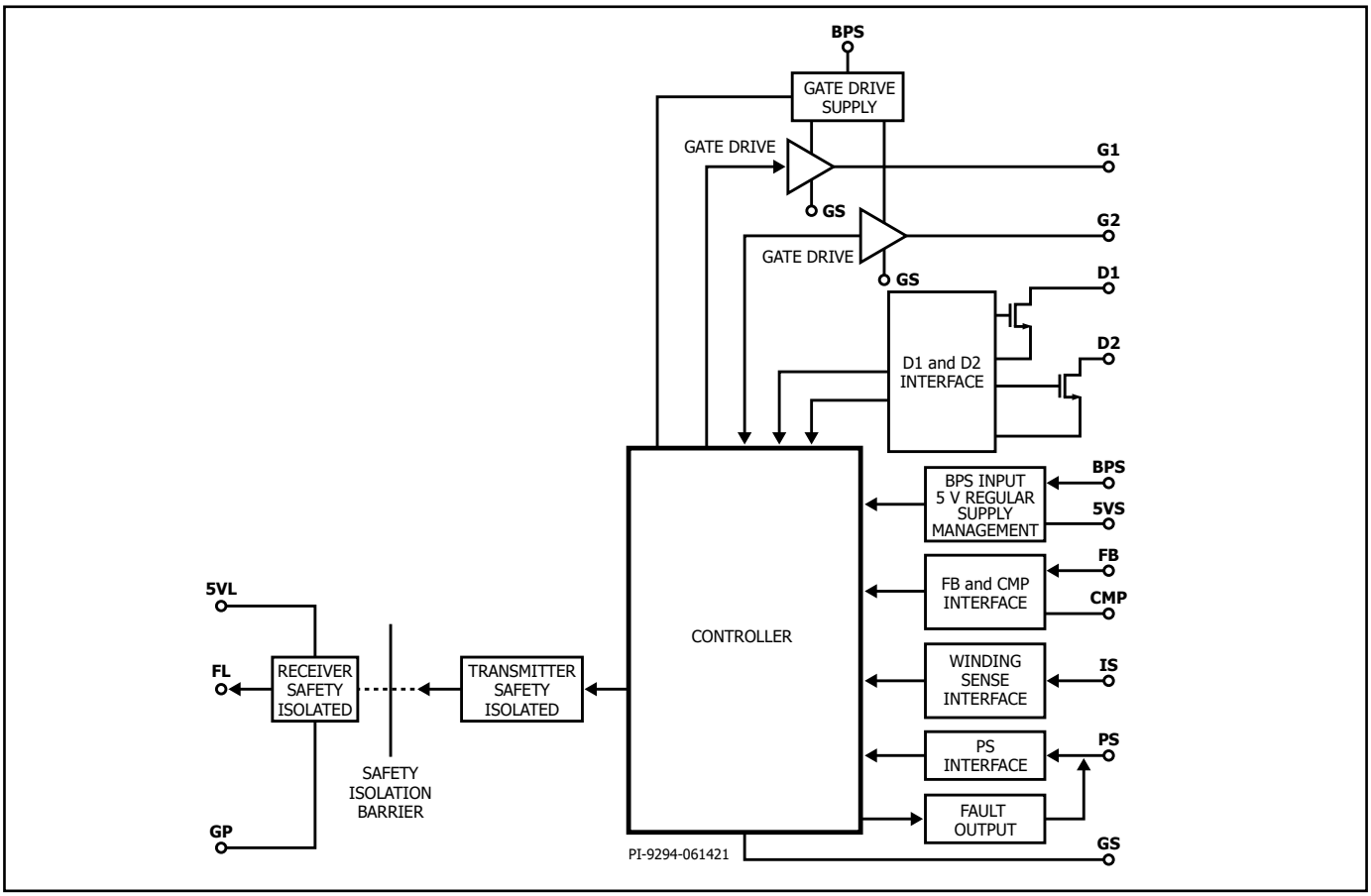


Figure 5. Safety Isolation and Secondary Controller Block Diagram.

Pin Functional Description – Primary-Side Device LCS726xC

Low-Side

PRIMARY GROUND (GD) (Pin 1)
Primary gate-drive ground. Should be capacitively decoupled to primary supply pin (BPL).

BURST MODE (BM) (Pin 2)
Small signal output indicating deep burst mode operation. Can be coupled to control external primary-side circuits.

PRIMARY GROUND (GP) (Pin 3)
Small signal primary ground. Should be capacitively decoupled to primary 5 V (5VL) pin.

NO CONNECTION (NC) (Pin 4)
Pin not connected. Leave open.

BYPASS LOW-SIDE (BPL) (Pin 5)
Power supply pin for primary low-side device. Should be capacitively decoupled to primary gate-drive ground (GD) pin.

PRIMARY LOW-SIDE 5 V (5VL) (Pin 6)
Primary low-side small signal 5 V IC-supply pin. Also provides bias power to the Primary-side of the Isolation device (LSR2000). 5VL should be capacitively decoupled to primary small signal ground (GP).

FLUXLINK INPUT (FL) (Pin 7)
Small signal input for FLUX LINK signal.

PROGRAM PRIMARY (PP) (Pin 8)
Small signal connection for customer configuration selection components. Also used in some configurations as small signal current input to receive power-good (remote on/off), signal to command device activation. Likewise used in some configurations as small signal current input for external fault. This pin also outputs logic level error code during fault conditions.

NO CONNECT (NC) (Pin 9)
Pin not connected. Leave open.

PRIMARY GROUND (GP) (Pin 10)
Small signal primary ground. Should be capacitively decoupled to primary 5 V (5VL) pin.

NO CONNECT (NC) (Pin 11)
Pin not connected. Leave open.

LINE SENSE (L) (Pin 12)
High-voltage small signal current input pin. Used to detect line-input voltage. Also used in some configurations as small signal input to receive power-good (remote on/off) signal to command device activation.

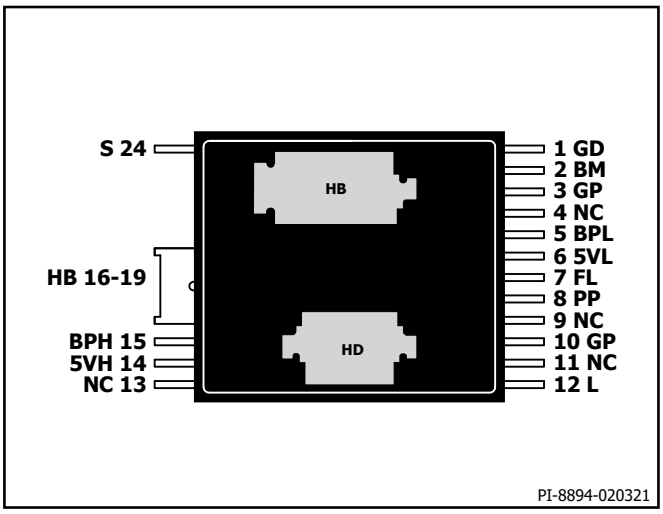


Figure 6. HiperLCS2 Primary-Side LCS726XC, InSOP-24C (Bottom View.)

High-Side

NO CONNECT (NC) (Pin 13)
Pin not connected. Leave open.

HIGH-SIDE 5 V (5VH) (Pin 14)
Primary high-side small signal 5 V IC-supply pin. Should be capacitively decoupled to half-bridge (HB). NOTE: this pin floats on the half-bridge switching voltage, can be at high-voltage with respect to primary grounds.

BYPASS HIGH-SIDE (BPH) (Pin 15)
Power supply for primary high-side device. Should be capacitively decoupled to half-bridge (HB) pin. NOTE: this pin floats on the half-bridge switching voltage, can be at high-voltage with respect to primary grounds.

HALF-BRIDGE (HB) (Pins 16-19 and Back Side HB Pad)
High-voltage and high current connection point for low-side MOSFET DRAIN and high-side MOSFET SOURCE. The half-bridge node typically switches between primary ground and primary input bus (HD).

SOURCE (S) (Pin 24)
High current Power ground return for half-bridge switch current. Also, at same potential as other small-signal primary grounds.

HD (Pin Back-Side Solder Pad)
High current, high-side MOSFET Drain and connection to system high-voltage input bus.

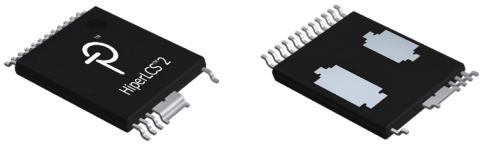


Figure 7. Primary-Side Packages.
(Right Upper), InSOP-24C Top View
(Right Lower), InSOP-24C Bottom View

Pin Functional Description – Primary-Side Device LCS726xZ

Low-Side

NO CONNECT (NC) (Pin 1)
Pin not connected. Leave open.

LINE SENSE (L) (Pin 2)
High-voltage small signal current input pin. Used to detect line-input voltage. Also used in some configurations as small signal input to receive power-good (remote on/off) signal to command device activation.

NO CONNECT (NC) (Pin 3)
Pin not connected. Leave open.

PRIMARY GROUND (GP) (Pin 4)
Small signal primary ground. Should be capacitively decoupled to primary 5 V (5VL) pin.

PROGRAM PRIMARY (PP) (Pin 5)
Small signal connection for customer configuration selection components. Also used in some configurations as small signal current input to receive power-good (remote on/off), signal to command device activation. Likewise used in some configurations as small signal current input for external fault. This pin also outputs logic level error code during faults.

FLUXLINK INPUT (FL) (Pin 6)
Small signal input for FLUX LINK signal.

PRIMARY LOW-SIDE 5 V (5VL) (Pin 7)
Primary low-side small signal 5 V IC-supply pin. Also provides bias power to the Primary-side of the Isolation device (LSR2000). 5VL should be capacitively decoupled to primary small signal ground (GP).

BYPASS LOW-SIDE (BPL) (Pin 8)
Power supply pin for primary low-side device. Should be capacitively decoupled to primary gate-drive ground (GD).

BURST MODE (BM) (Pin 9)
Small signal output indicating deep burst mode operation. Can be coupled to control external primary-side circuits.

PRIMARY GROUND (GD) (Pin 10)
Primary gate-drive ground. Should be capacitively decoupled to primary supply pin (BPL).

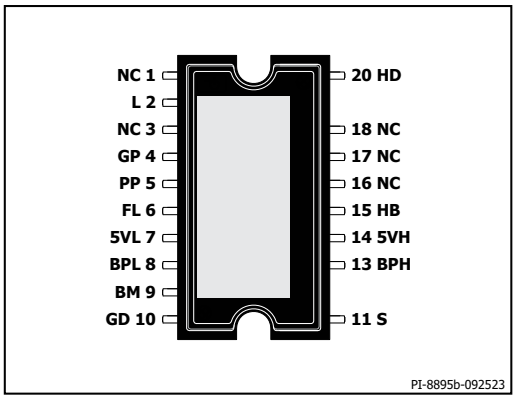


Figure 8. HiperLCS2 Primary-Side LCS726xZ, POWeDIP-20B (Top View.)

High-Side

SOURCE (S) (Pin 11)
High current Power ground return for half-bridge switch current. Also, at same potential as other small-signal primary grounds.

BYPASS HIGH-SIDE (BPH) (Pin 13)
Power supply for primary high-side device. Should be capacitively decoupled to half-bridge (HB) pin. NOTE: this pin floats on the half-bridge switching voltage, can be at high-voltage with respect to primary grounds.

HIGH-SIDE 5 V (5VH) (Pin 14)
Primary high-side small signal 5 V IC-supply pin. Should be capacitively decoupled to half-bridge (HB). NOTE: this pin floats on the half bridge switching voltage, can be at high-voltage with respect to primary grounds.

HALF-BRIDGE (HB) (Pins 15)
High-voltage and high current connection point for low-side MOSFET DRAIN and high-side MOSFET SOURCE. The half-bridge node typically switches between primary ground and primary input bus (HD).

NO CONNECT (NC) (Pin 16-18)
Pin not connected. Leave open.

HD (Pin Back-Side Solder Pad) (Pin 20)
High current, high-side MOSFET Drain and connection to system high-voltage input bus.

BACKSIDE PAD
This thermal pad on the back-side of the POWeDIP package, is not electrical conductive. The provides functional electrical isolation from internal switching voltages. The POWeDIP package can be directly connected to a metallic heat sink without need for additional electrical isolation.

UPPER and LOWER SCREW HOLES
The upper and lower screw holes on the POWeDIP package are intended for use with M2 screws. The screws should be torqued according to recommended settings:

POWeDIP Mounting Instructions:
Use thermal grease between package & heat sink.
Use M2 x 0.4 screws with M2 metal washers.
Loosely assemble package to heat sink with two screws, making sure package is centered:

1. Tighten first screw lightly until "snug"
2. Tighten second screw until "snug"
3. Tighten first screw again to 1.0 in-lb maximum
4. Tighten second screw again to 1.0 in-lb maximum

Figure 9. POWeDIP-20B Package LCS726xZ.

Pin Functional Description – Safety Isolation and Secondary-Side Device LSR2000C

SECONDARY 5 V (5VS) (Pin 1)
Connection point for an external decoupling capacitor for the secondary IC supply. Should be capacitively decoupled to secondary ground (GSB).

SECONDARY GROUND (GSB) (Pin 2)
Small signal ground for secondary-side (5VS, IS, CMP, FB, PS).

WINDING SENSE (IS) (Pin 3)
Secondary-side, small signal current input connection to an external resistor and capacitor.

COMPENSATION (CMP) (Pin 4)
Secondary-side, small signal connection to external frequency compensation resistor capacitor network.

FEEDBACK (FB) (Pin 5)
Secondary-side, small signal feedback signal to secondary control.

PROGRAM SECONDARY (PS) (Pin 6)
Secondary-side, small signal connection for customer configuration selection components. This pin also outputs logic level fault code during fault conditions.

SECONDARY BYPASS (BPS) (Pin 7)
Secondary-side power supply pin for secondary device.

SR GATE2 DRIVE (G2) (Pin 8)
Secondary-side, output for driving secondary synchronous rectifier (SR) MOSFET for first output phase.

SR GATE1 DRIVE (G1) (Pin 9)
Secondray-side, output for driving secondary synchronous rectifier (SR) MOSFET for second output phase.

SR DRAIN2 SENSE (D2) (Pin 10)
Secondary-side, medium voltage small signal input for sensing SR DRAIN/SOURCE voltage.

SR DRAIN1 SENSE (D1) (Pin 11)
Secondary-side, medium voltage small signal input for sensing SR DRAIN/SOURCE voltage.

SECONDARY GROUND (GSA) (Pin 12)
Power ground for secondary-side (BPS, G1, G2, D1, D2).

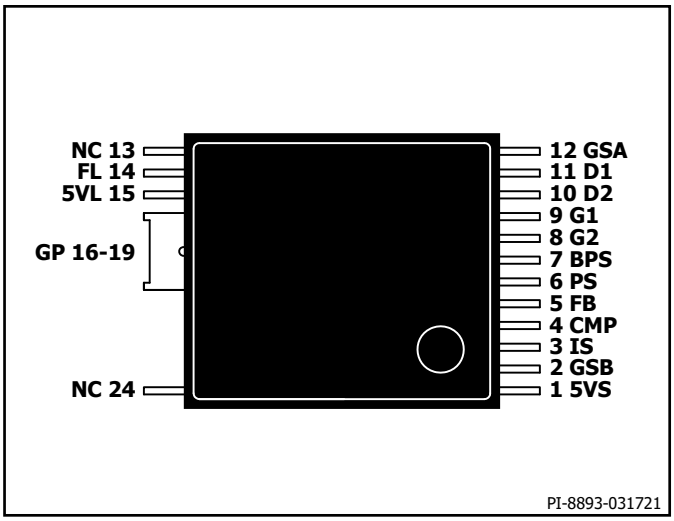


Figure 10. HiperLCS-2 Safety Isolation and Secondary-Side LSR2000C, InSOP-24D (Top View).

NO CONNECT (NC) (Pin 13)
No connection. Leave open.

FLUXLINK (FL) (Pin 14)
Primary-side small signal output is the FluxLink primary output pin.

PRIMARY 5V (5VL) (Pin 15)
Primary-side connection point for an external primary decoupling capacitor for the primary IC supply. Should be capacitively decoupled to primary ground (GP).

PRIMARY GROUND (GP) (Pins 16-19)
Primary-side ground reference for primary BYPASS pin.

NO CONNECT (NC) (Pin 24)
No connection. Leave open..

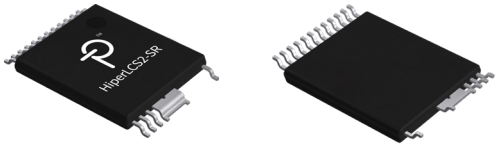


Figure 11. HiperLCS2–SR, Safety Isolation Package. InSOP-24D (Top View), InSOP-24D (Bottom View).

HiperLCS-2 Basic Operation

The HiperLCS-2 is designed for half-bridge LLC converters, which are high-efficiency resonant ZVS, variable frequency converters.

HiperLCS-2 comes as a chipset with two devices: the power-device, and the isolation device. The power-device (LCS726x) is on the primary side of the isolation barrier and includes an LLC controller with built-in high-side and low-drivers and half-bridge power-MOSFETs. The isolation-device (LSR2000) straddles the isolation barrier to facilitate communications to the power-device (primary device). The isolation-device also includes the secondary controller and SR-driver. The HiperLCS-2 is able to operate with nominal frequencies of up to 240 kHz. It offers extremely high conversion efficiency coupled with low-component count and rugged protection features.

HiperLCS-2 Primary-Side Power-Device Operation

Start-Up Self-Bias

The HiperLCS-2 provides self-powered start-up. This means that the system provides a high-voltage bus to the HD pin and the HiperLCS-2 device will take care the rest. Self-powering is accomplished using internal high-voltage current sources. The first current source is connected between HD and the BPL pin. When voltage is applied to HD, the BPL will begin to charge any capacitance connected to this pin. There is a low pre-charge current which allows initial charging voltage to be established, and then as BPL voltage increases, this charge current is stepped to a much higher level allowing faster start-up times. This higher current capability of the BPL charging also allows the HiperLCS-2 to provide bias power to a PFC stage and allow the PFC to begin switching prior to the HiperLCS-2. Once the BPL self-charge reaches the target voltage it will enter hysteretic control. The internal current source is disabled during normal operation once an external bias (from a transformer bias winding), becomes active. The BPH pin is charged in very similar way to BPL, but the charge current from HD to BPH is lower. The BPH pin internal charge current will likewise be disabled once external bias becomes available.

In order to begin switching of an LLC converter ideally, we would prefer the half-bridge and resonant capacitor voltages to be in a known condition (preferably close to zero). The HiperLCS-2 achieves this using a high-voltage current source connected to the HB pin. This HB current source pre-conditions the resonant tank components pulling current to ground (return), prior to beginning switching. Doing this means that at initial start or restart, the HiperLCS-2 always starts with known tank conditions. The result is that the HiperLCS-2 can achieve resonant switching on the second switch edge. The pre-condition HB-current source is active prior to switching while the high-side device is below UV condition.

After all the charging conditions are complete and all undervoltage conditions are cleared, HiperLCS-2 begins switching with the high-side power-MOSFET first.

Start-Up Primary Soft-Start

The HiperLCS-2 begins primary switching at a frequency approximately 1.5x the maximum of the selected switching frequency range. The switching frequency is ramped down quickly to build current in the resonant tank. Once the resonant tank achieves target current ($I_{HB(IOVL)}$), the frequency is then indirectly regulated to maintain tank current at this level. The result at the system output capacitor, is equivalent to a very high-power current source. This results in a monotonic rise at the voltage on the output capacitor. The positive slew rate of the output voltage-rise will be a function of resonant tank and output capacitor values. There are two selectable thresholds, $I_{HB(OVL)}$ and $I_{HB(IOVL-)}$. The higher level $I_{HB(OVL)}$, is the default value, selected by using L pin for input voltage UV/OV functions. The lower level $I_{HB(IOVL-)}$ is selected by grounding L pin and using PP pin PG function instead. Selecting $I_{HB(IOVL-)}$ will slow the output voltage positive start-up slope and minimizes magnitude of output overshoot. Selecting $I_{HB(IOVL-)}$ is recommended for systems using an active PFC boosted input bus and requires the PFC boost to provide a power-good (PG) signal to the PP pin. Engagement of arbitrary output loads will slow the output voltage-rise but will not change the polarity of the output voltage slope. Primary control of switching continues until the output voltage reaches close to regulation at which point the secondary will take control of switching.

Auto Dead Time

The LLC-converter has a structure where positive and return voltages connect sequentially via power-MOSFET's to the mid-point or half-bridge node. The half-bridge connects to a resonant-tank network which is then series connected to typically power-return (ground) and coupled to output load. The high-side power-MOSFET and low-side power-MOSFET are driven sequentially (i.e., neither MOSFET is on at the same time). During on-time the resonant-tank delivers some energy to the output and stores the remaining energy. When the first power-MOSFET turns-off, there is a period of dead time before the second power-MOSFET turns on. During dead time some of the remaining stored energy in the resonant tank, continues to circulate current in the lumped half-bridge capacitance, causing the half-bridge voltage to slew towards the next switch. The half-bridge voltage slew continues until either the voltage is clamped by a MOSFET body-diode (ZVS), or the tank runs out of energy (non-ZVS). The goal for the LLC-converter is to always run in ZVS (zero-voltage-switching), operation. This is where the voltage across the next power-MOSFET is close to zero prior to turning on the power-MOSFET. This results in near zero capacitive (COSS) MOSFET losses. After the first power-MOSFET turns-off, the HiperLCS-2 auto-dead time function holds off second power-MOSFET until the controller detects either the end of half-bridge voltage-slew or abnormally reaches maximum dead time. Following this the second power MOSFET will turn-on. The dead time of a given LLC-converter may vary with input voltage and output load. The HiperLCS-2 will automatically adjust dead times in the range from ~90-500 ns (except for LCS7269Z where dead-time is fixed at 150 ns).

Frequency Range	Min	Nom	Max	Start	Unit
0	23	90	135	167	kHz
1	30	120	183	227	kHz
2	45	180	270	333	kHz
3	60	240	366	455	kHz

Table 2. Table of Primary and Secondary Frequency Ranges Selections. Primary Device Frequency Range Selection via PP Pin Resistor (see data table). Secondary Device Frequency Range Selection by Part Number.

Primary Protection and Fault Response

If secondary controller does not wake up within 32 ms of primary switching start, then the power device will declare fault. If hand over to secondary control does not occur within a further 32 ms after secondary wake-up, then the primary will declare a fault. As with all faults, the primary is the master of fault management. When a fault is declared (primary or secondary), the device will go into either latching (off) or non-latching fault handling.

For non-latching faults the primary device will initiate auto-restart. Auto-restart has two responses a short fault response and a long response (see Table 2).

Short fault auto-restart occurs for fault events that are detected while operating in secondary control. This auto-restart off-period is approximately 250 ms. All faults that trigger during primary control result in analog auto-restart response where the off-time is around 5 seconds.

The short-auto-restart event allows quick restart for occasional faults. The long auto-restart ensures that repetitive auto-restart maintains a very low auto-restart-attempt versus auto-restart-off-time ratio. This in turn ensures that the persistent fault does not create excess electrical nor thermal stress on the part.

The primary includes many layers of device self-protection to achieve rugged performance in the event of faults.

At power-up the device completes FMEA checks (failure-mode effect analysis) on device pins. If faults are observed the device will not start switching. Note that such an FMEA fault will not report an error code on the PP pin if it occurs prior to switching. Fault reporting messages on the PP pin are only generated for faults which occur after switching has started.

Primary half-bridge current is internally sensed during low-side MOSFET on-time. This is used for both primary start-up and also for safety current limits during secondary mode.

The primary device also includes (high-side controller) over-temperature protection. This protects against excessive power dissipation in the primary package. The device also has ambient (low-side controller) thermal protection, which prevents restart until the temperature has lowered sufficiently to allow restart. This prevents thermal temperature built up which might otherwise occur in the event of immediate restart for repeat fault conditions. Thermal fault triggers either latching or non-latching response (PP pin select).

The L pin detects input voltage for undervoltage and overvoltage protection. The input voltage is coupled via a resistor connected to L pin. The L pin is polled during burst operation to reduce system consumption. During continuous switching (non-burst) the L pin is continuously monitored. Overvoltage and undervoltage both have hysteresis to prevent chatter. On exiting undervoltage the device goes through a restart. However, for overvoltage the device switching is blocked while the condition persists but allowed to continue when condition is removed. Note: that the L pin detects at power-up whether the pin is connected to ground or if there is a resistor between the HD pin and L pin. If the L pin is connected to ground then the PP pin power-good input function is used instead to indicate line-UV/OV conditions.

The BPL pin provides main supply voltage into the low-side driver and controller. This voltage is internally regulated to provide 5 V at 5VL pin. Note: the 5VL pin is not intended to provide power to any external devices other than the isolation device. The BPH and 5VH pins provide similar functions on the high-side driver. Both must be externally decoupled to ground with a capacitor.

The BPL, 5VL, BPH and 5VH pins are monitored for undervoltage condition. At start-up the device will not begin switching until all are above their respective UV thresholds. The pins are also monitored during normal switching and UV will trigger auto-restart. Please note that unlike faults, a UV-condition on BPL, 5VL, BPH, 5VH will force a restart but will not output a fault to the PP pin.

Miscellaneous Primary Functions

At power-up, the PP pin is used to read customer configuration (resistor) settings (see Table 2), which select for the primary start-up frequency range (90, 120, 180, 240 kHz), and latching/non-latching fault handling. The PP pin may also be used to receive a power-good input signal from an external system (such as PFC controller) when the L pin is connected to ground. As mentioned previously, when PP pin (PG) function is used, the start-up current is set to the lower value of $I_{HB(IOVL-)}$. This is intended only for PFC-boost applications where the $I_{HB(IOVL-)}$ slows the output voltage rise and reduces output overshoot. The same PP pin (PG) signal could be used for remote on/ off. The PP pin can also receive an external fault signal to disable device under fault or other conditions. During fault conditions the PP pin is also used to output device error codes to help with debug. The error code is output as a binary non-return-to-zero (NRZ) bit stream.

Primary Device PP Pin Error Fault Codes

Bit	Hex Code	Fault Action	PP Pin Error Fault Name	Description
31:28	X	I	1111	Fixed Pre-amble.
27:20	X	I	000 0000 0	Fixed Pre-amble.
19	X	N	x	
18:16	X	N	xxx	
15	8000h	A/L	HSD_OT	High-side MOSFET over-temperature fault. Prevents start-up switching while fault is activated and then monitored again after hand over to secondary control mode.
14	4000h	A/L	AMB_OT	Low-side controller ambient over temperature fault. Prevents start-up switching while fault is activated and then monitored again after hand over to secondary control mode.
13	2000h	I	BPH_UVN	High-side BPH undervoltage. Prevents start-up switching while fault is activated. Not monitored in secondary control.
12	1000h	I	L_OV	Line overvoltage – activation of this fault L = OV+ causes device to stop switching and restart occurs when fault clears L = OV-. Fault monitored in all switching modes. Fault when active will instantaneously halt HB-switching. However if Fault is sustained for more than a few LLC periods, other faults may trigger and cause device auto-restart.
11	800h	A/L	L_UV	Line undervoltage. Prevents start-up switching while fault is activated. Fault monitored in all switching modes.
10	400h	L	EXT_FAULT	External Fault on PP pin. External circuit required to trigger this fault. Often used for secondary V_{OUT} OV detection.
9	200h	I	REM_OFF	Remote-off on PP pin (note: when L pin not used REM_OFF also generated concurrently at EXT_FAULT). Prevents start-up switching while fault is activated.
8	X	N	x	
7	80h	A/L	LOST_FL_FAULT	Lost FluxLink is monitored after start-up and hand over to secondary control mode and only when not in burst-mode. This occurs after XXXus of observing an unchanged/static FL signal while no in burst-mode. This fault can often be triggered when secondary bias is lost (BPS_UV), and secondary device stops operating.

Bit	Hex Code	Fault Action	PP Pin Error Fault Name	Description
6	40h	A/L	100MS_FL_FAULT	Lost FluxLink in burst_off (in super light load). A burst packet should occur a minimum of every 50 ms. This fault is activated if the burst packet doesn't arrive by 100 mS. This fault can often be triggered when secondary bias is lost (BPS_UV), and secondary device stops operating.
5	20h	A/L	START_FAULT	Primary mode switch frequency reached FMIN. Reaching FMIN during start-up is very uncommon. This fault may indicate resonant LLC tank frequency problem or incorrect PP pin frequency-range selection.
4	10h	A/L	PCD_SS_FAULT	Start-up problem. From start of primary switching, secondary should send wake-up command within 32 ms and hand over should occur to secondary control within 64 ms. Also during start-up frequency confirmation received signal should be received. If any of these do not occur, then error will be activated. May indicate excessive C_{OUT}, excessive load, or insufficient power delivery.
3	8h	A/L	SEC_FAULT	Secondary control fault is registered on the primary controller, when ALL secondary faults declared by the secondary control. For details of secondary fault see PS pin fault error code table.
2	4h	A/L	SCD_2PULSE_FAULT	Secondary sending 2 pulse message unexpectedly in secondary control. Three messages required to trigger the fault. This fault is usually caused by grounding issues on primary ground, or magnetic coupling from the LLC transformer to the LSR2000C.
1	2h	A/L	I_SAFETY_LIM	Safety current limit fault in low-side MOSFET.
0	1h	A/L	FREQ_FAULT	Frequency confirmation failure fault. The primary control (PP selected), frequency-range, does not match frequency code received from the secondary controller. May be wrong PP pin resistor, or wrong secondary controller device.

Fault Action:
A/L = auto-restart or latch-off (depending on PP-selection Table 5), L = latch-off, I = information only, N = not used (ignore).

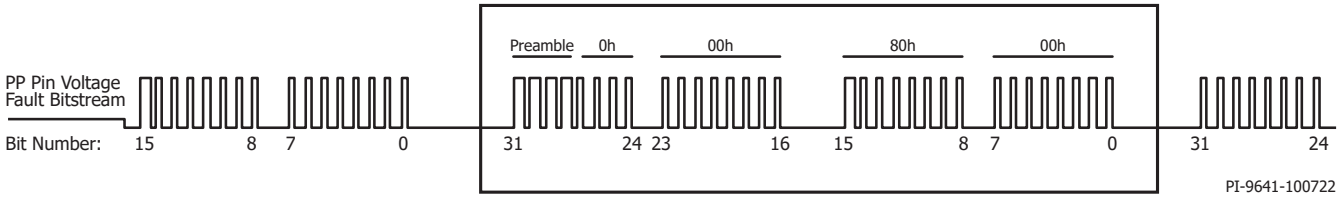
Table 3. LCS726x – Primary-Side PP Pin Error Fault Reporting.

LSR2000C – Primary PP Pin and Secondary PS Pin Error Fault Bitstream

Note1: The below PP pin error fault-code bit stream message may include multiple (concurrent) fault bits. The Fault bit stream is repetitively sent out PP pin during fault-off period. Message initially starts and bit-15 and continues to bit0. Then repeats continuously starting with MSB (Bit 31) pre-amble and ending with LSB (Bit 0). For a bit period of T, logic-1 (high for 2/3.T, low for 1/3.T), and logic-0 (high for 1/3.T, low for 2/3.T).

Note2: Similarly, the PS pin error fault-code bit stream message may include multiple (concurrent) fault bits. The Fault bit stream is repetitively sent out PS pin during fault-off period. Message initially starts and bit-15 and continues to bit0. Then repeats continuously starting with MSB (Bit 31) pre-amble and ending with LSB (Bit 0). For a bit period of T, logic-1 (high for 2/3.T, low for 1/3.T), and logic-0 (high for 1/3.T, low for 2/3.T).

Below example shows primary-side PP pin bitstream during high-side over-temperature fault (HSD_OT).



Error Code = 0008000h : HSD_OT (high-side over-temperature fault)

Secondary Device PS Pin Error Fault Codes

Bit	Hex Code	Fault Action	PS Pin Error Fault Name	Description
31:28	X	I	1111	Fixed Pre-amble.
27:24	X	I	0000	Fixed Pre-amble.
23:18	X	N	xxxxxx	
17:16	X	I	FREQ_MODE_INFO	Information only: read-out of the Secondary device internal Frequency Range 0-3 value. Helpful for debugging frequency confirmation faults (FREQ_FAULT), reported on the primary device.
15:14	X	N	xx	
13	2000h	P	BPS UV FLT	BPS undervoltage fault. This causes the secondary controller to stop operating and enter power-up state.
12	1000h	A/L	SEC_IS_CLK_FLT	Secondary fault triggered when slew is not detected on IS-pin signal. Often this fault will be caused when primary fault occurs and HB stops switching. Fault may indicate incorrect IS-pin components.
11	800h	I	SEC_FB_OV_FLT	FB pin overvoltage fault. Note: this fault is only active after hand over to secondary control.
10	400h	N	x	
9	200h	N	x	
8:7	X	N	xx	
6	40h	A/L	SEC_OT_FAULT	Secondary controller over-temperature fault. Device switching stops while fault is active.
5	20h	I	SEC_PHINV_FAULT	Phase inversion fault is only active after start-up and hand over to secondary control mode. The V_{IS} clock is compared to the internal FL clock. If the two clocks are out of phase during 800 µs fault timer, the fault is asserted. Cumulative switching cycles with phase inversion are required. A single switching cycle without phase inversion resets the fault timer.
4:3	X	N	x	
2	4h	A/L	VOUT_UV_FLT	Output UV Fault become active after start-up and hand over to secondary mode. Fault is activated if FB pin remains below $V_{FBBSTN(TH)}$ for 64 ms. This fault is disabled in CC mode (PPsel6, PPsel7).
1	X	N	x	
0	1h	A/L	VFB_START_FLT	Secondary start-up fault. From end of frequency confirmation (before hand over), secondary output voltage (monitored by FB pin), if output does not reach regulation within 64 ms, the fault is activated. This fault is disabled in CC mode (PPsel6, PPsel7).

Fault Action:
A = auto-restart or latch-off (depending on PP-selection Table 5), P = power-up reset stage, I = information only, N = not used (ignore).

Table 4. LSR2000C – Secondary-Side PS Pin Error Fault Reporting.

PP Pin Selection	Frequency Range	Fault Response
0	0	Auto-on
1	1	Auto-on
2	2	Auto-on
3	3	Auto-on
4	0	Latch-off
5	1	Latch-off
6	2	Latch-off
7	3	Latch-off
PP External Fault	All	Latch-off

Table 5. Table of Primary-Side PP Pin Functionality Selections. See Data Table for PP Pin Selection Resistor Values.

The BM pin is used to signal that the HiperLCS-2 is operating at low load. Amongst its uses, this signal can be used to turn-on/off an inrush bypass relay. It could also be used to change the set-point of the PFC boost voltage.

The FL pin input is used to receive secondary communications, such as regulation, burst modes and faults. This input receives a digital 0-5 V signal from the FL-output of the isolation device.

HiperLCS-2 Secondary-Side Isolation-Device Operation

Communications to Primary-Device

As mentioned earlier the primary device will autonomously start-up and begin switching, with primary remaining in control until the output voltage reaches close to regulation. At this point the secondary will take control (primary will hand over control to secondary) and all further switching is then controlled from the secondary side controller.

The secondary-device communicates to the primary-device via the FluxLink isolated communications. Communication commands include hand over (i.e., secondary taking control), half-bridge switching, burst mode and declaration of fault condition.

The isolation-device FL-output is connected to the primary FL-input.

Secondary Fault Handling

After hand over the secondary remains in control until either: a UV-event occurs (primary or secondary), or until a fault occurs (primary or secondary). Under either of these conditions UV or fault, the control reverts back to primary control. Also, under either of these conditions the primary would enter auto-restart. For auto-restart, the device has two functionalities, either latch (off-condition), or non-latching (i.e., auto-restart).

After auto-restart off-time, the primary restart is the same as for first power-up as described earlier in primary control section.

Note that the primary is the device which handles all system level fault events. Any secondary fault is reported to the primary and ultimate system level fault response comes from the primary.

Secondary Control

The secondary takes control of switching as the output voltage approaches regulation. Once in secondary control, the secondary device uses 3 signals to achieve closed loop control. The FB pin signal is coupled via resistor divider from the output voltage. This FB pin voltage represents a scaled version of the output voltage. The FB pin generates an error signal with respect to an internal 3.75 V DC reference. The error signal is output via an OTA, operational trans-conductance (voltage input to current output) amplifier in the form of an error current signal to the CMP pin. The gain of the OTA amplifier is dependent on the magnitude of the error signal. Low gain (e.g., 1x.), is used for small errors, but once error exceeds a threshold the gain is increased to high gain (e.g. 4x.). This non-linear amplification (NLA) allows for extremely fast large-signal transient response.

The CMP pin is coupled to an external resistor capacitor compensation network (two poles one zero). This compensation network is tailored to achieve good phase-gain response. The error current signal is integrated and filtered by the compensation network. When the system is in regulation the error-current-signal should be extremely small, thus a small current causing very small variations in the CMP voltage (compensation network). Both leakage and magnetizing signals.

The IS pin senses the winding voltage from the transformer. The sense winding is coupled to the primary of the transformer (both leakage and magnetizing signals), generating a voltage whose magnitude is similar in scale to that of the main output voltage winding. The IS pin has internal clamping at 2.5 V. The sense winding voltage is AC coupled (via capacitor) and then converted to a current using a resistor into the IS pin. The magnitude of the current is low, below 35 μA, thus causing minimal system loss.

Internally the IS pin AC-coupled current signal is compared against the CMP pin voltage. When the two cross this indicates the end of a half-cycle.

The IS pin signal contains, amongst other things, information about primary input current. This means that the overall system implements a current mode control. The control system does not directly control frequency, but instead controls half-cycle by half-cycle in time-domain. However, the frequency is an indirect function of the control loop, thus in steady state the frequency will be stable and a function of resonant tank, input voltage and output power, etc.

PS Pin Selection	Burst Threshold (%) **
0	15
5	~2

Table 6. Table of Secondary-Side PS Pin Functionality Selections. Selected via PS Pin Resistor (see data table). **Approximate Burst Percentage of Maximum Continuous System Output Power. For resistor values see LSR2000 data-table Page 38.

Burst Mode

The CMP pin voltage changes inversely with respect to average primary input current. The CMP voltage is used to determine when the system should enter burst mode. The CMP burst threshold is compensated for input voltage, such that the burst-entry point should be at relatively similar power levels over the entire input voltage range.

For the HiperLCS-2 the burst mode is used for more than one reason. The first reason for burst is to maintain system efficiency. In full frequency mode the system efficiency naturally drops significantly below 10% load. So, the first goal is to enter burst mode before 10%. The regulation is achieved by switching less often but continuing to deliver the equivalent of about 10% power per switched half-cycle.

The second goal once in burst is to maintain output regulation. This is achieved using three modes of burst regulation.

The third goal once in burst is to maintain the switching frequency envelope well below the audio resonant frequency of the LLC transformer. The audio/mechanical resonance LLC-transformers is typically in the 7-12 kHz range. Thus, in burst the HiperLCS-2 intends to maintain switching frequency envelope below approximately 1 kHz. Being well below the audio resonance of the transformer means that there will be little or no noise from the transformer.

The fourth goal is to maintain ability to satisfy 0-100% load step without losing regulation. To help achieve the goals above, the HiperLCS-2 uses 3 modes of operation when in burst.

On entering burst, the highest power burst mode is called intermediate mode (IM-burst). In this mode the system is still in closed loop analog control via the CMP pin. The IM-burst works by forcing off-time at a 1.5 ms repeat period. The IM-mode off-time is terminated once the output voltage decays to a minimum value (V_{OUT}MIN). At this point switching begins again and the analog control loop closes to reach regulation. Regulation is then maintained until the off-to-off timer again reaches the 1.5 ms period. Then the next IM-mode off-time begins.

The next level down in terms of output power, is the light-load LL-mode burst. During this mode the CMP is no longer used. Instead, an internal VCMP_BURST is used, where VCMP_BURST corresponds to the equivalent of 10% load. The LL-mode burst switching begins when output voltage reaches V_{OUT}MIN. The switching continues, terminating when output voltage exceeds V_{OUT}MAX. The device enters LL-off-time until the voltage again reaches V_{OUT}MIN. During the LL-burst switching each half-cycle delivers equal power (determined by internal VCMP_BURST) and approximately equal to 10% load.

The lowest level of burst in terms of output power is super-light SL-burst. During this mode the switching occurs after a maximum off-time of 50 ms. The start SL-burst switching depends on the 50 ms off-time only. If the output voltage drops as far as V_{OUT}MIN then the device will move back to LL-burst. During SL-burst switch, the burst switches until either it reaches V_{OUT}MAX or reaches 60 μs of total switching time.

With the burst modes of the HiperLCS-2 the device is able to achieve exceptional system no-load performance. Unlike other systems though it can still accommodate a full 0-100% load step without dropping out of regulation. The burst mode also intrinsically manages audio noise. The output ripple during burst is also entirely bounded by the V_{OUT}MIN and V_{OUT}MAX of the system. The device achieves 1% system regulation, internally the FB pin V_{OUT}MAX and V_{OUT}MIN thresholds are fixed at ±0.65% of V_{OUT}REG.

SR (Synchronous Rectifier) Control

The D1 and D2 pins monitor the drain voltage of the SR MOSFET's. When D1 and D2 go below ground this indicates the potential start of SR conduction. Pins D1 and D2 require a small series resistor to prevent excessive substrate current when below ground voltage. Under certain conditions, there may be ringing on D1 and D2, and the ring may temporarily go below ground only to rise back above ground. The HiperLCS-2 therefore employs a learning engine to ignore the ringing. Therefore, when the ring-filtered value of D1 (or D2) goes below a turn-on threshold, the associated SR MOSFET is then activated. Once activated the D1 (or D2) signals then monitor the on-state Drain-Source voltage across the SR MOSFET. This gives an indication of conduction current. For an LLC-converter in discontinuous conduction mode (DCM), the rectified output current (i.e., power delivered to the secondary), will reach zero before the end of the half-cycle. In discontinuous mode (DCM) LLC operation, the detected D1 (or D2) will terminate the SR-conduction when current approaches zero. The secondary controller turns off the SR MOSFET before reverse conduction. For an LLC-converter operating in continuous conduction mode (CCM), the current will not reach zero prior to the end of the half-cycle. Therefore, to prevent reverse SR MOSFET current, the HiperLCS-2 will terminate SR-conduction prior to half-bridge switching. This can be done because the half-bridge switching signal is originated at the secondary controller. Thus, the secondary control can turn off the SR MOSFET at exactly the latest possible moment to guarantee no shoot-thru in CCM mode. This is something that allows the HiperLCS-2 to safely operate in CCM-mode with maximum SR conduction. Note: that in CCM mode, the primary and secondary rms currents are reduced vs. DCM mode. Therefore, being able to operate safely in CCM mode generally results in higher system efficiency.

SR Driver Voltage Clamp

The G1 and G2 pins respectively drive the SR MOSFET's for each phase of the LLC secondary. The BPS pin voltage supplies drive current to the G1 and G2 gate-drive outputs. However, the BPS pin is able to accommodate a voltage range of up to 24 V. This would exceed the maximum gate withstand for most SR MOSFETs. Also, most SR MOSFET's are fully enhanced at voltages well below that. In order to limit the SR-MOSFET gate-charge/discharge energy, the HiperLCS-2 provides an internal voltage clamp to limit the maximum voltage output on the G1 and G2 SR-drive pins. The gate-drive voltage is internally controlled to a maximum of either 11.5 V or 6.5 V. The maximum voltage depends on the selected frequency range of the device. Frequency ranges 0,1 (90, 120 kHz), receive 11.5 V whereas higher frequency ranges 2,3 (180, 240 kHz) receive 6.5 V drive limits. Limiting the SR MOSFET drive voltage limits the gate-charge/discharge losses. Typically, higher frequency SR MOSFET's are structurally optimized to have lower V_{GS} turn-on thresholds and thus fully enhanced at lower voltages.

Layout Connections and Recommended Values

During PC-board layout, it is important to understand the current return pin for each signal, so that correct routing paths can be implemented. The following table shows that information along with generic recommended external component values. Obviously for all designs component values may change or be optimized to suit specific conditions, however the recommended values are given as a good starting point.

Isolation Barrier	Device	Pin	Most Sensitive	Returned to Pin	Recommended Value	Notes
Primary Low-Side Control						
Primary	LCS726x	BM		GP		
Primary	LCS726x	BPL		GD	1 µF / 35 V SMD right at pin. Usually also 47 µF further from pin	The gate-drive energy comes from this pin. Large BPL pin capacitance will also be needed away from pin.
Primary	LCS726x	5VL		GP	1 µF / 10 V SMD right at pin	
Primary	LCS726x	FL	**	GP (LSR2000 device)		There is a connection from isolation device LSR2000 to LCS726x. The 5VL, GP and FL pins of both devices should be directly connected.
Primary	LCS726x	PP		GP	RPP at pin	See data table for selection values.
Primary	LCS726x	L	**	GP	4 MΩ	Split resistance into at least 3 SMD resistors. Ensure that all resistors are located close to L pin.
Primary High-Side Control						
Primary	LCS726x	BPH		HB	1 µF / 35 V SMD right at pin. Usually also 10 µF further from pin	
Primary	LCS726x	5VH		HB	220 nF / 10 V SMD right at pin	
Primary	LCS726x	Heat Sink		S		If heat sink used ensure that it is grounded to S pin.
Primary FluxLink						
Primary	LSR2000	5VL		GP(LSR2000)		There is a connection from isolation device LSR2000 to LCS726x. The 5VL, GP and FL pins of both devices should be directly connected.
Primary	LSR2000	GP		GP(LCS726x)		There is a connection from isolation device LSR2000 to LCS726x. The 5VL, GP and FL pins of both devices should be directly connected.
Primary	LSR2000	FL	**	GP(LCS726x)		There is a connection from isolation device LSR2000 to LCS726x. The 5VL, GP and FL pins of both devices should be directly connected.

Isolation Barrier	Device	Pin	Most Sensitive	Returned to Pin	Recommended Value	Notes
Secondary Control						
Secondary	LSR2000	D1	**	GSA	499 ohm	Switch signal hence pay attention to layout/coupling.
Secondary	LSR2000	D2	**	GSA	499 ohm	Switch signal hence pay attention to layout/coupling.
Secondary	LSR2000	G1		GSA	4.7 ohm	High current gate-drive. Wider PC-board trace to limit inductance.
Secondary	LSR2000	G2		GSA	4.7 ohm	High current gate-drive. Wider PC-board trace to limit inductance.
Secondary	LSR2000	BPS		GSA	1 μF / 35 V SMD right at pin. Usually also 47 μF further from pin	
Secondary	LSR2000	5VS		GSB	10 μF / 10 V SMD right at pin	Note: this pin also has high internal current spikes, hence larger capacitor right at the pin.
Secondary	LSR2000	IS	**	GSB	RIS resistor + 470 pF / 200 V capacitor	Note: the RIS resistor is typically split into two series resistors to share the voltage rating. Series resistors are placed as close as possible to the IS pin to limit external noise coupling.
Secondary	LSR2000	CMP		GSB	Initial values (150k + 2.2 nF) // 100 pF. All components at pin	Compensation components may require modification to optimize phase-gain response.
Secondary	LSR2000	FB	**	GSB	10 k lower resistor value, at pin	The resistor divider 10 kΩ low-side resistor is used to give a good balance between no-load consumption and noise rejection. Lower values will give more noise immunity but will also increase no-load consumption.
Secondary	LSR2000	PS		GSB	RPS at pin	See data table for selection values.

Table 7. Data Sheet Body Table.

Basic Layout Guidelines

The HiperLCS-2 is a high-frequency power device and requires careful attention to circuit board layout in order to achieve maximum performance. The bypass capacitors need to be positioned and laid out carefully to minimize trace lengths to the pins they serve. Surface mount (SMD) components are recommended for minimum component and PC-board stray inductance.

The HiperLCS-2 has several sensitive pins, used for sensing analog signals. Good device performance can be achieved by paying special attention to the layout at and around these pins.

On the primary-side control, both the FL pin and L pin may be sensitive to layout.

The FL pin output is essentially a digital output, so for this pin the issue is to ensure that the GP, FL and 5VL are all directly connected between the primary and isolation devices. If the grounding is not done correctly this can lead to potential noise pickup.

For the L pin this is a sensitive analog input pin. The L pin senses input voltage via a resistor (typically 4 MΩ). The resistor is typically made of a series of SMD resistors. Splitting the resistance into several devices will minimize the voltage stress on each resistor. There are two different examples of how to connect the L pin to VIN. The first (incorrect) would be to place all the resistors close to VIN and then run a long PC-board trace to the L pin. This is incorrect since the node from resistor to L pin is high-impedance and a long PC-board trace would allow noise pickup injected into the L pin. The second (correct) method would be to place ALL the resistors close to the L pin and run a long PC-board trace to VIN. This method is correct since the node from resistor to VIN is very low-impedance and thus very unlikely to pick-up noise. On the secondary-side control, the FB, CMP, IS and D1/D2 pins may be sensitive to layout.

The FB pin is a high impedance voltage input pin. It is connected to V_{OUT} via a resistor divider (R_{UPPER}, R_{LOWER}). V_{OUT} is a low-impedance node, so this may be the long PC-board connection. The node from R_{UPPER} to R_{LOWER}, is high impedance and should be placed as close and tightly coupled as possible to the FB and GSB pins. The general recommendation for R_{LOWER} is ~20 kΩ, which is a good compromise between no-load consumption and noise immunity. Further reducing R_{LOWER} would increase noise immunity but increase no-load consumption. Note that any noise injected into the FB pin could be observed as duty-cycle and/or frequency variation.

The CMP pin is a high impedance current output and voltage-input pin. The compensation network of one-resistor and two capacitors' is should be place as closely and tightly coupled as possible to the CMP and GSB pins. Any noise injected to the CMP pin could be observed as duty-cycle and/or frequency variation.

The IS pin is a current input, with a forced voltage on the pin. The IS pin signal passes from the winding-sense pin of the transformer through series capacitor CIS and resistor RIS connected to the IS pin. The transformer winding signal pin should first be connected to the CIS capacitor and then in series to the RIS resistor. The RIS resistor should be split into two SMD resistors, the last of which should be terminated right at the IS pin of the HiperLCS-2 device. The transformer should have both a winding sense signal pin and also a winding-sense small signal ground pin. The winding sense small signal transformer ground pin should be connected to the GSB pin of the HiperLCS-2. The winding sense transformer signal pin is a low-impedance node and therefore this may be the long PC-board connection. This trace however is carrying a large magnitude (medium voltage) AC coupled signal. Thus, care needs to be taken to keep these signals away from other small signal sensitive inputs of the device.

The D1/D2 pins are both high impedance voltage inputs. The D1/D2 are connected via a low-value resistor (typically 499 Ω), to the respective Drain of the SR MOSFET with respect to GSA pin. The SR MOSFET Drain point is a low-impedance node so may be the long PC-board connection. This trace however is carrying a large magnitude (medium voltage) AC coupled signal. Thus, care needs to be taken to keep these signals away from other small signal sensitive inputs of the device.

Transformer T1 is a source of both high di/dt signals and dv/dt noise. The high di/dt can couple magnetically (PC-board loop signal loop area coupling), to sensitive circuitry. The high dv/dt inject noise via electrostatic (stray capacitive), coupling. Electrostatic noise coupling can be reduced by grounding the transformer core, but it is not economically feasible to reduce the stray magnetic field around the transformer without drastically reducing its efficiency. Where possible, sensitive signal paths and components should be located away from the transformer to avoid noise pickup. The secondary transformer main output windings should be twisted together prior to winding. Twisting the wires together will minimize differences in secondary leakage and will enhance current balance between the windings. Also as importantly please ensure that all secondary wires are twisted together prior to termination on the transformer pin. Twisting the terminate wires will minimize wire-loop area and minimize the ability of the windings to couple stray flux to other system signals.

HiperLCS-2 primary-side power pins are the S, HB and HD pins. Unlike some designs, the HiperLCS-2 is intended for use with a single resonant capacitor. This is typically connected to primary-return (primary ground). However the device will also work if used with split resonant capacitor. Also the system can be used with C_{RES} clamp diodes (from ground to HB and HB to input buss). Clamp diodes limit the excursion C_{RES} voltage and in the process also impose a lower converter power limit. The HB pin is connected to the LLC transformer and the transformer to the resonant capacitor, this path length of PC-board connection should be minimized. Care should be taken to minimize return path (primary-ground) between the resonant capacitor and S pin of the HiperLCS-2 and the PC-board connection between resonant capacitor and device. The HD pin connection should also include a local decoupling capacitor from HD to primary ground (S pin potential). The goal of the local decoupling capacitor is to reduce the path length for high magnitude switched currents.

The GP ground is for small-signal circuits is used as a reference for external small-signal circuits connected to the primary device. The GP ground should NOT be connected to the bulk capacitor ground, instead GP is connected internally to HiperLCS-2 S pin ground. The S pin is connected primary-side power ground. Also the primary bias winding return and the first bias winding capacitor are also connected to power ground. The GD ground is used only to connected to the BPL decoupling capacitors, which provides gate drive power for the internal switch power MOSFETs. GD ground should NOT be connected to the bulk capacitor ground, instead it is internally connected to S pin ground.

Note:
HiperLCS-2 secondary-side only has one power pin and this is the GSA pin. The GSA pin should be tightly connected to the SOURCE of both SR MOSFETs (SR1 and SR2). Both SR MOSFETs should be co-located as close as possible with a shared Source connection point. The GSA pin should be connected at the mid-point between

SR1 and SR2 SOURCE pin connections. The G1 and G2 secondary gate-driver pins do drive substantial gate current and so should be kept to a short (and equal) length(s). The D1 and D2 DRAIN sense pins, should also be kept to equal lengths. The location of the GSA pin connection to SR MOSFET source, will determine the accuracy of D1/D2 detection. This can affect the current-sensed turn-off point for SR1 and SR2 when operating in DCM (discontinuous) mode. If fine tuning is required, moving the GSA connection point closer to one of the two MOSFETs can change the relative turn-off points for SR1 and SR2. Also, fine tuning of both turn-off points can be achieved by changing the resistor (RD1 or RD2), in series with D1 or D2 pins. The resistor is typically 499 Ω, but may be adjusted in the range 200 – 1.5 kΩ. These small changes will adjust the turn-off current of SR1 or SR2 (larger resistor increases current at which SR will turn-off).

Key Design Details

The LLC can be optimized for different criteria. The HiperLCS-2 has four frequency ranges of operation with nominal frequencies of 90, 120, 180, 240 kHz. For highest possible efficiency, lower frequency designs generally give marginally better results. However high frequency designs are very close in efficiency. High-frequency design may yield smaller magnetic size and smaller resonant capacitor. For most designs litz wire is recommended. For a given design the optimal diameter and number of strands is automatically calculated by Power Integrations design tools (PIXIS HiperLCS-2 Spreadsheet), that assist with the entire design process.

For most designs low-loss ferrite cores lower the magnetizing losses and a recommended for best efficiency. Likewise, the maximum flux-density also has strong effect on hysteretic magnetic losses. Lowering maximum flux-density (i.e., increasing secondary turns), can often give a higher efficiency design (especially at higher frequencies).

For nominal input voltage and 100% load, it is recommended that the magnetizing inductance (LM) is adjusted to give a half-bridge slew rate of approximately 250 ns at 380 VDC (except for LCS7269Z where slew should be ~120 ns). Such a design should achieve ZVS operation for all load and input voltage conditions. Lowering the magnetizing inductance beyond this target, will result in higher circulating currents and higher resistive losses. For all HiperLCS-2 designs, the goal is for the resonant tank to still be able to achieve ZVS operation at the FMAX limit for the chosen frequency range. This is important since when the converter sees a load transient (when load is say stepped to zero), the frequency may temporarily reach FMAX limit prior to entering burst mode. For this reason, it is important to choose the frequency range that offers the appropriate range of frequencies needed for the operational scope of the converter. Note the FMIN limit of the chosen frequency range will become active at lowest input voltage and highest load. Typically, the FMIN limit is only reached under fault conditions.

The resonant inductance LRES (or often referred to as leakage inductance), should be designed to provide maximum overload power. For the HiperLCS-2, it is recommended that the design be optimized for operation at resonance, CRM at nominal input voltage and 50% load. At higher input voltages the converter may enter continuous mode, CCM operation. For some converters this may present a risk of shoot-through, but the HiperLCS-2 is uniquely designed to allow the system to enter continuous conduction mode, CCM without risk of shoot-through or other anti-social converter behavior.

Application Example 1

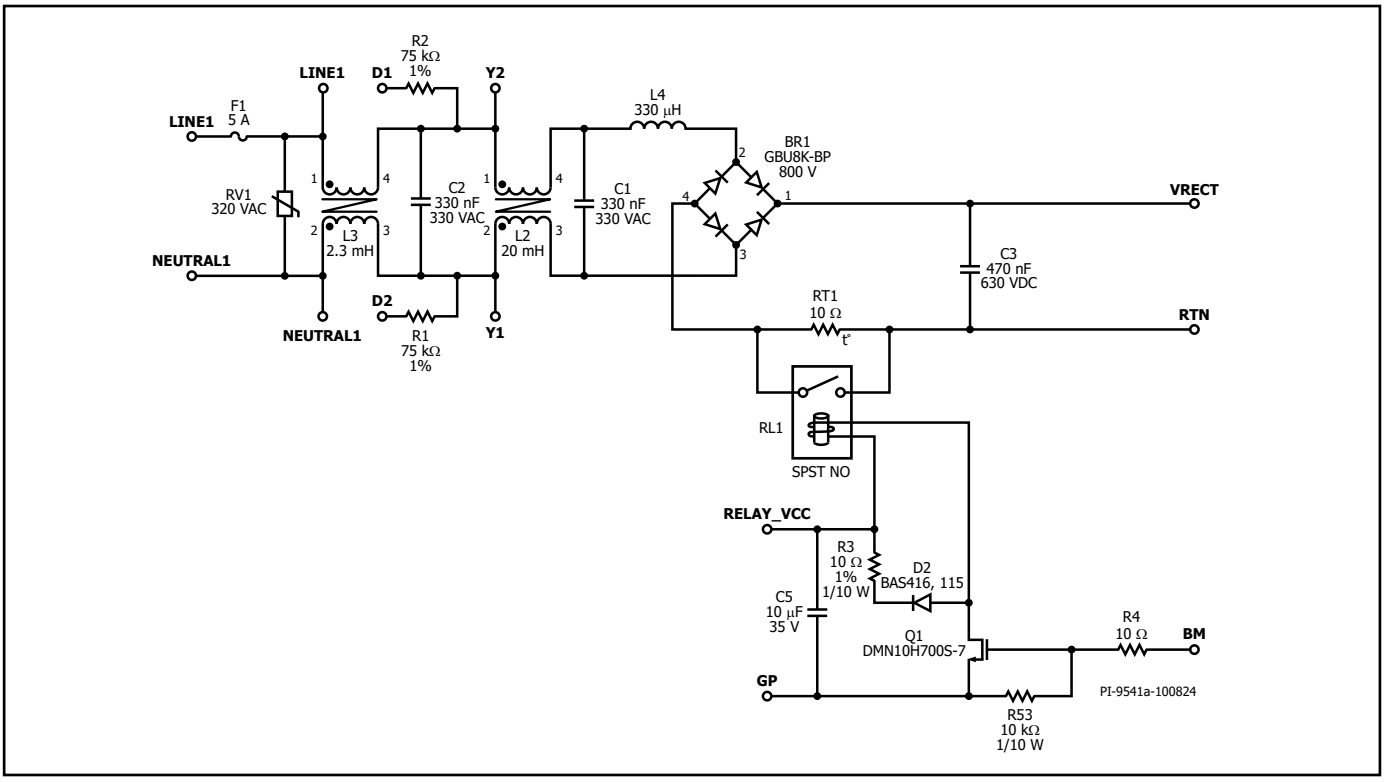


Figure 12. EMI Section 220 W, 24 V.

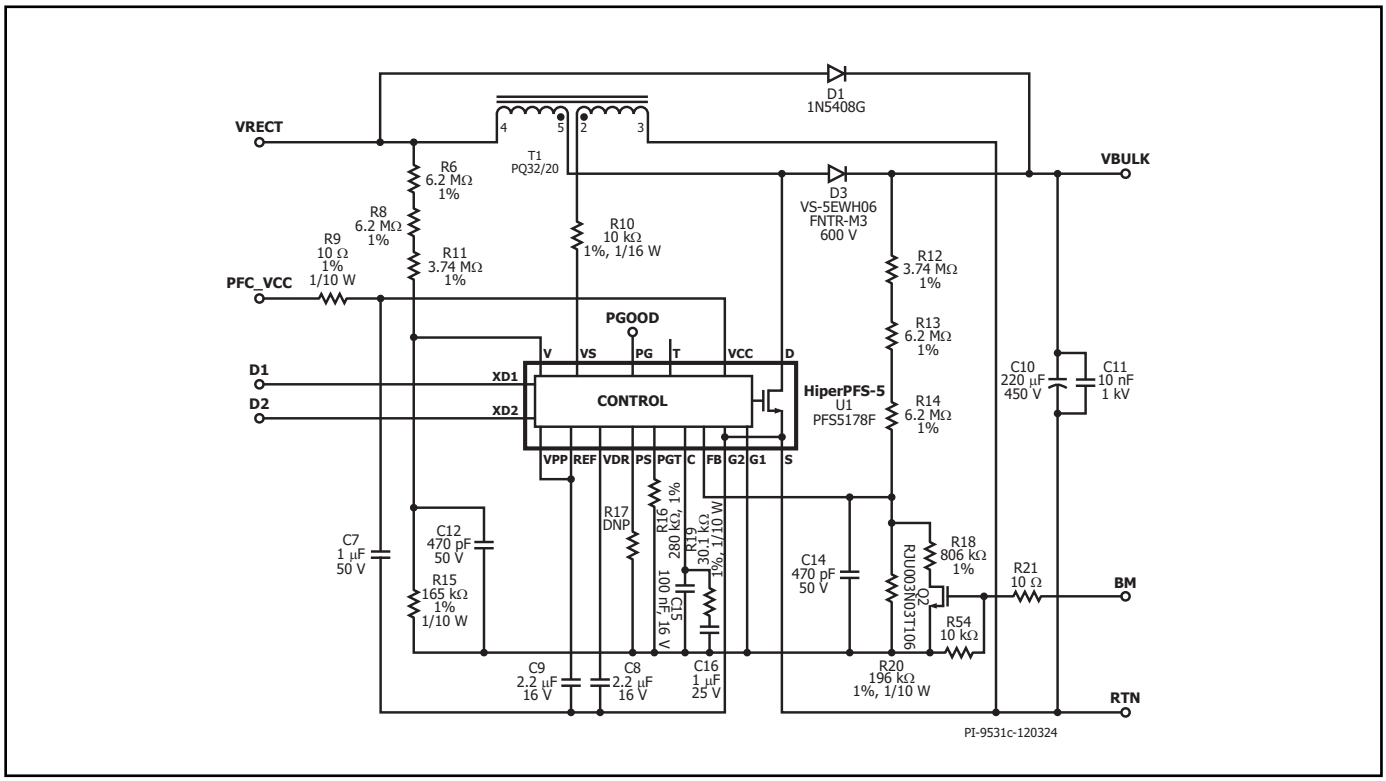


Figure 13. Hiper-PFS5 PFC Section 220 W, 24 V.

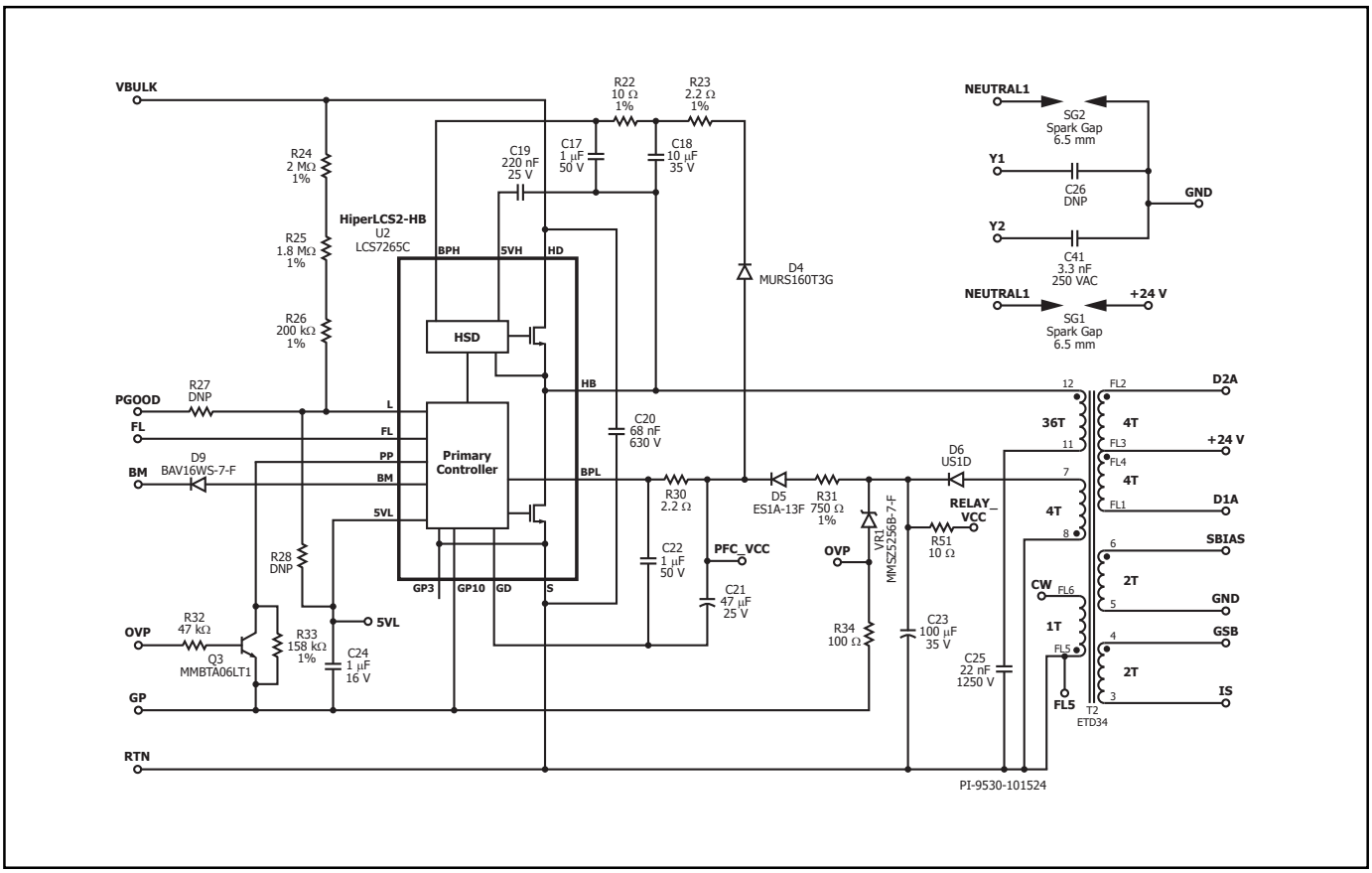


Figure 14. HiperLCS-2 Primary-Side 220 W, 24 V LCS7265C.

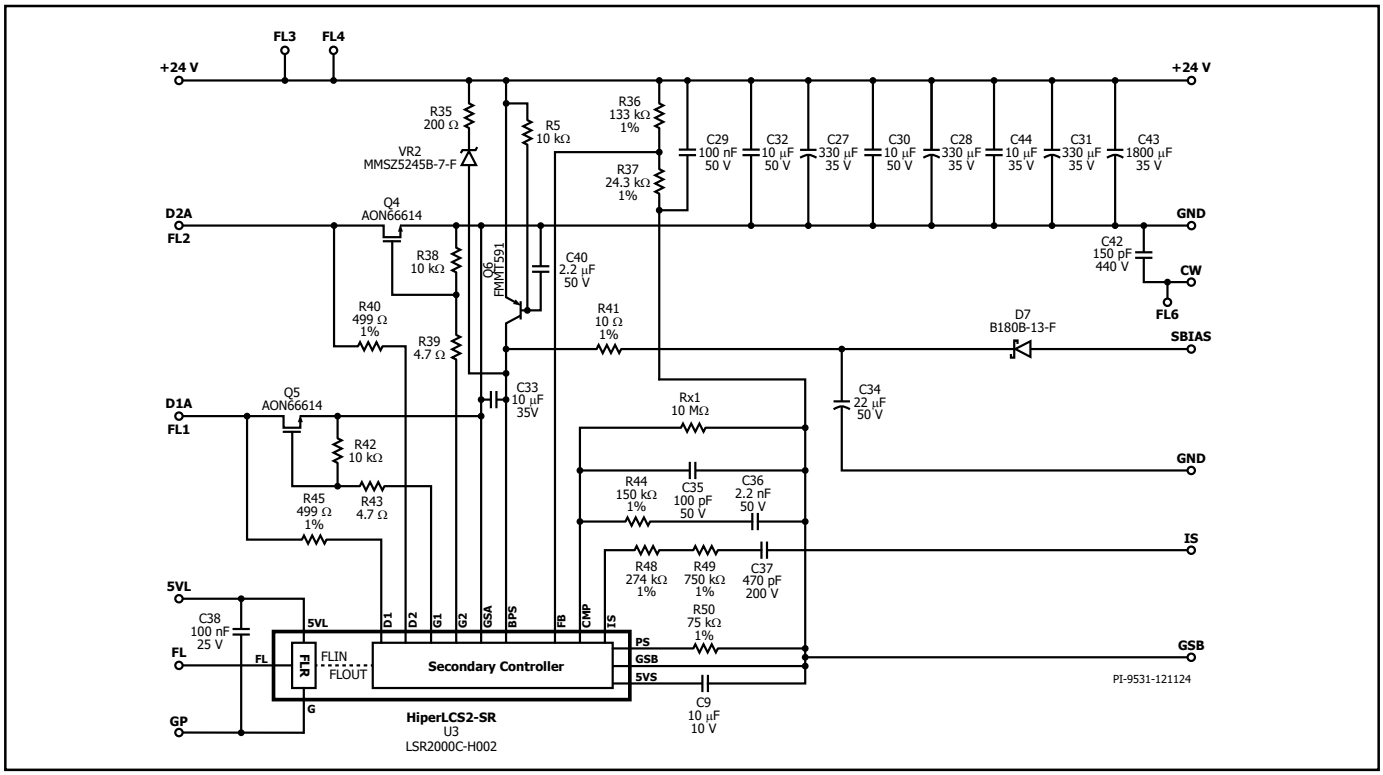


Figure 15. HiperLCS-2 Isolation and Secondary-Side 220 W, 24 V LSR2000C.

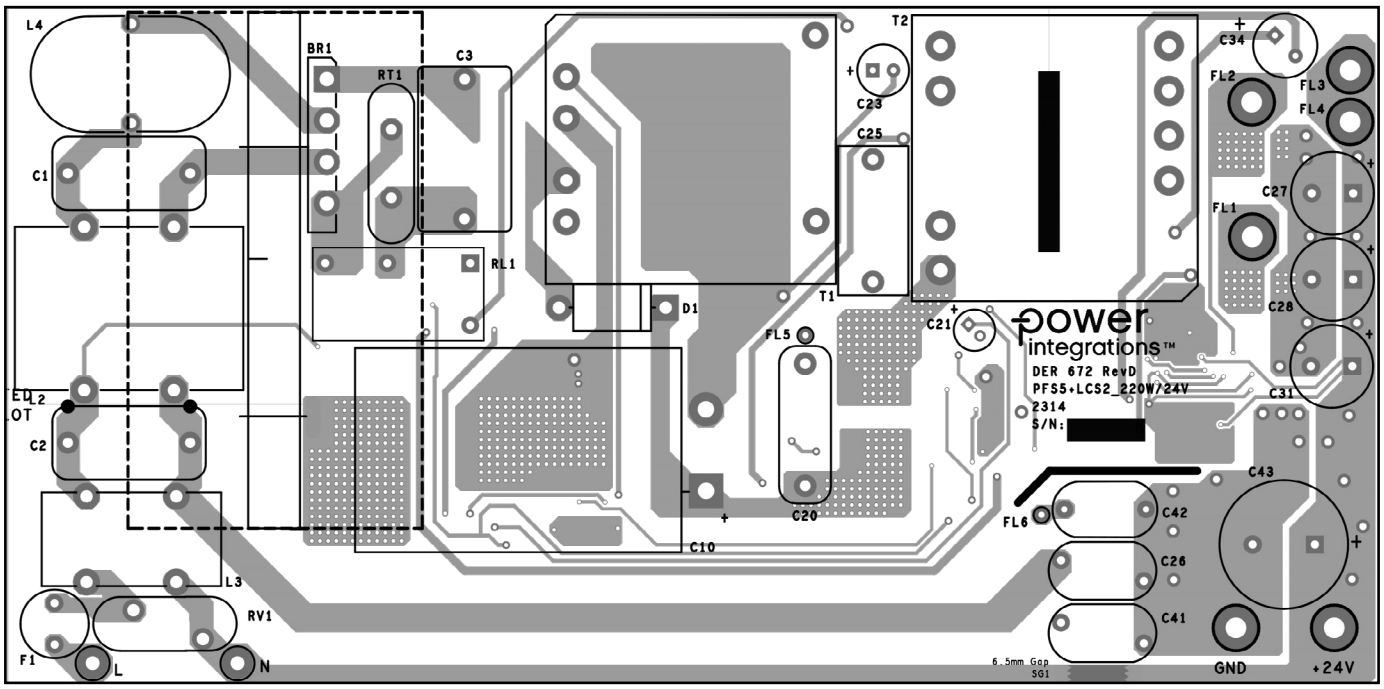


Figure 16. PCB Layout 220 W / 24 V (Top View).

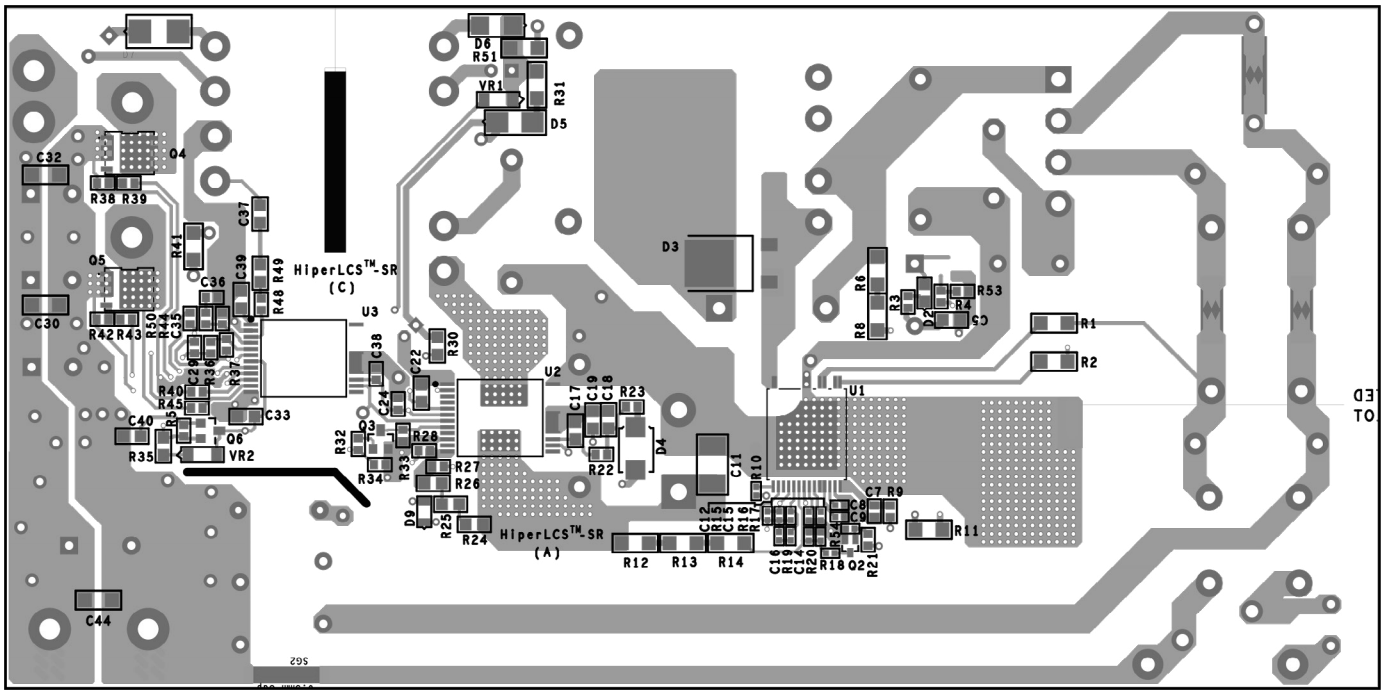


Figure 17. PCB Layout 220 W / 24 V (Bottom View).

LLC Primary Schematic (220 W / 24 V)

This section describes primary-side schematics in Figures 12, 13 and 14. The high-voltage input-bus is filtered through capacitor C1 and C7. Line sense (L pin) detects input bus voltage via resistors (R24, R25, and R26). The LCS2-HB (U2) will initiate soft-start when L pin detects UVplus threshold. Primary-side detected output overvoltage is sensed from the primary bias-winding (pins 7 and 8 of transformer T2), via Zener diode VR1 and resistor R34 and coupled to the PP pin via resistor R32 and transistor Q3. When overvoltage occurs, Zener VR1 conducts and current will be pulled from PP pin to ground via transistor Q3. Resistor R33 programs the PP pin primary frequency range and fault-response. Diode D9 may couple from BM pin to control an external in-rush relay drive circuit and/or change PFC voltage as a function of light-load. Note BM transitions to low state when in light load burst mode.

Capacitors C24 and C22, decouple the 5VL and BPL respectively to GP (small signal primary ground). The primary return power-ground (RTN) is connected to S pin (SOURCE), primary-bias winding and capacitor C23. The RTN ground is kelvin connected to the negative-pin of bulk-capacitor C1 and C7. From a layout point of view, it is very important to keep the small signal GP ground, separate from system power-ground (RTN). Note: the RTN power-ground is intended to offer the low-impedance path for system noise events, whereby secondary coupled noise currents can be safely delivered to RTN/bulk-capacitor ground without disturbing primary small-signal ground (GP).

Diode D6 rectifies primary bias winding voltage and capacitor C23 decouples to RTN ground. Capacitor C22 provides local high-frequency cycle-to-cycle decoupling (to GD ground) at the BPL pin. Before switching the BPL pin charges both capacitor C22, and C21 (via resistor R30). Capacitor C21 provides sufficient energy storage to sustain start-up switching prior to primary bias winding contribution. Capacitor C21 is sized to also provide boot-strap energy to the LCS-2 high-side bias via diode-D4 and resistor R23. Capacitor C21 also provides start-up bias to external PFC stage. Capacitor C21 should be sized to provide sufficient bias energy during startup and also for boot-strap, the capacitance of C21 should be greater than 5x the capacitance of high-side bias capacitor C18.

Resistor R30 limits output current from BPL in the event of a large current draw from external PFC stage. Diode D5 is used as blocking diode, to block BPL charge current to C23 prior to bias-winding activation. During normal operation the (U2) bias current comes from the bias winding to capacitor C23. The BPL pin has an internal shunt regulator to limit BPL voltage. Resistor R31 limits the BPL shunt-current when BPL shunt-voltage-clamping is active. This in turn limits the power-dissipation in the BPL during this condition. Note: pay careful attention to the steady-state bias-winding voltage. If voltage is above BPL clamp threshold, this may lead to additional unnecessary dissipation in the BPL circuit and thereby risk unintentional thermal shutdown of LCS-2 (U2). Note that the bias winding voltage may vary over a 25% range from zero to full output load. For best no-load performance, the bias winding is intended to deliver a minimum of 15 V to the bias winding at zero load conditions, while the shunt will engage if the bias winding grossly exceeds 21 V at the BP pin. High-side bootstrap is charged via diode D4, then resistor R23 into capacitor C18 during low-side power MOSFET-on period. During the first few switching cycles at start-up, capacitor C18 typically starts with no charge and resistor R23 limits the bootstrap current into capacitor C18. During bootstrap, the C18 charge current flows through the low-side power MOSFET, so the removal of resistor R23 may result in safety current limit being triggered under start-up conditions. Resistor R22 and capacitor C17 provide further low-frequency filtering to the BPH pin. High-side 5VH is decoupled via capacitor C19. Note that all high-side decoupling is with reference to HB pin.

Resonant tank inductor components T2 pins 11/12 (integrated transformer includes resonance inductance LR and magnetizing inductance LM), are connected from HB in series through resonant capacitor C25 to primary return RTN (primary power ground). Capacitor C42 (coupled to RTN), is a safety Y capacitor used to couple an inverted primary winding signal from an auxiliary winding to the secondary ground to cancel out common mode noise across the isolation barrier which helps lower conducted EMI emissions.

LLC Secondary (220 W / 24 V)

This section describes the secondary schematic in Figure 15. The HiperLCS2-SR (U3) has isolated primary side pins. Pin 5VL receives 5VL voltage from LCS2-HB. Pin GP couples to primary small signal ground (GP). Capacitor C38 provides local decoupling to the 5VL and GP pins of U3. The FL pin provides a FluxLink signal to the primary HiperLCS2-HB.

Transformer output pins T2 FL3/FL4 provide the positive output voltage, which is rectified and filtered by capacitors C27, C28, C29 C30, C31, C32, C43, and C44. These capacitors combine to provide low ESR which mostly defines the output ripple of the system, and their combined capacitance should be chosen to match the desired burst off-time. These capacitors are decoupled to secondary power ground (GND). Transformer output pins T2 FL1/FL2 respectively provide the transformer return path via synchronous rectifier MOSFETs Q4 and Q5. The secondary power path is from T2 FL3/FL4 through capacitors C27, C28, C29, C30, C31, C32, C43, and C44 and the return path via MOSFETs Q4 and Q5 to transformer T2 FL1/FL2. Note: for best matching of the two secondary power-phases, it is important to equalize the secondary power path such that path-lengths via Q4 and Q5 are equal.

Capacitor C33 decouples the BPS to GSA (secondary SR-drive ground). Capacitor C39 decouples 5VS to GSB (secondary small signal ground). Diode D7 and capacitor C34, rectify and filter the secondary bias winding T2 pin 6 (with respect to output power ground GND). Resistor R41 forms an additional high-frequency filter to capacitor C33.

At start-up the LCS2-HB primary side controls switching until the LCS2-SR (U3) secondary takes control. During primary control the output voltage will continue to rise. There is a period of time (T_{WAKE}), from when the secondary BPS voltage exceeds UV-plus, to when the LCS2-SR is ready to take system control. In some applications the BPS (bias winding voltage) rises more slowly than V_{OUT} (+24 V) which allows V_{OUT} to exceed regulation prior to secondary control. To avoid this situation, components Q6, R5 and C40 form a start-up circuit to provide fast initial bias to BPS directly from V_{OUT} prior to secondary bias winding activation. In some designs, Zener Diode VR2 and R35 may be required to provide a small pre-load to ensure output maintains regulation during no load conditions.

Small signal secondary ground GSB is used for feedback and compensation. Output voltage is sensed via resistor R36 and R37 with local capacitor decoupling C29 to GSB (small-signal secondary ground), to remove any high-frequency noise.

Compensation is provided between CMP and GSB, via components R44, C35 and C36 which provide a pole (C36) and zero (R44, C35) and a final pole (C35). The transformer IS winding T2 pin 3 (T2 pin 4 grounded to GSB secondary small signal-ground), provides a high frequency medium voltage small-signal which is capacitor coupled via C37 and then via resistors R48 and R49 to the IS pin.

Synchronous MOSFET Q4 and Q5 drive are coupled from G1 and G2 pins via resistors R39 and R43. The drive resistors are optional and intended to limit super high-frequency MOSFET drive ring. In the case of FMEA open-connection condition from G1 and G2 to Q1 and Q2 gate, local pull-down resistors R38 and R42 are present to ensure the MOSFET Q4 and Q5 remain off. SR-ground GSA is used to return SR-gate-drive. The D1 and D2 pins sense the synchronous rectifier Q4 and Q5 drain voltages via resistors R40 and R45, respectively. The resistors are required to limit below-ground sensing current into the D1 and D2 pins. These resistor values can be increased to offer adjustment to SR turn-off threshold. Increasing resistor value will cause SR to turn off at higher SR current. Note: the D1 and D2 signal paths, are from Pins D1 and D2 to resistors R40 and R45 and through the SR-MOSFETs (Q4, Q5) to and back to GSA. The total path length D1 ,R45, Q5, GSB and D2, R40, Q4, GSB should be equal, to ensure optimal SR functionality.

The PS pin resistor R50 programs secondary-side user selection such as burst threshold option.

Application Example 2

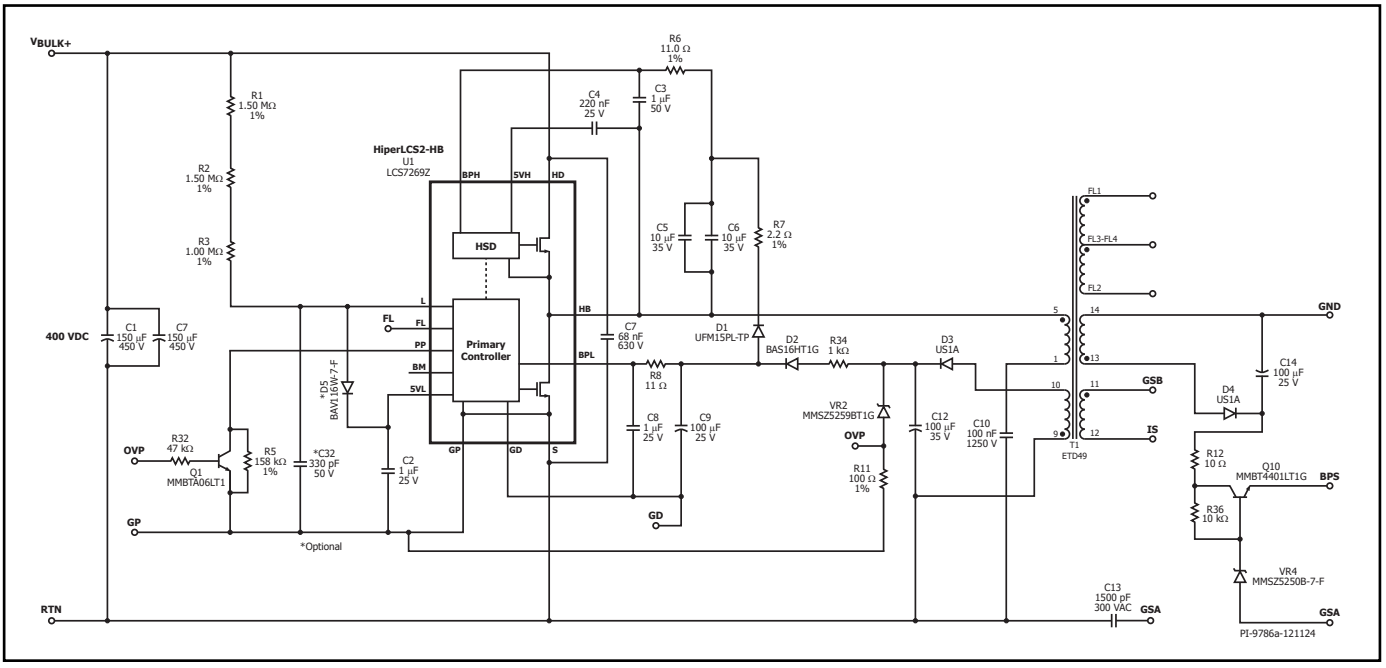


Figure 18. HiperLCS-2 Primary-Side 1650 W, 60 V LCS7269Z.

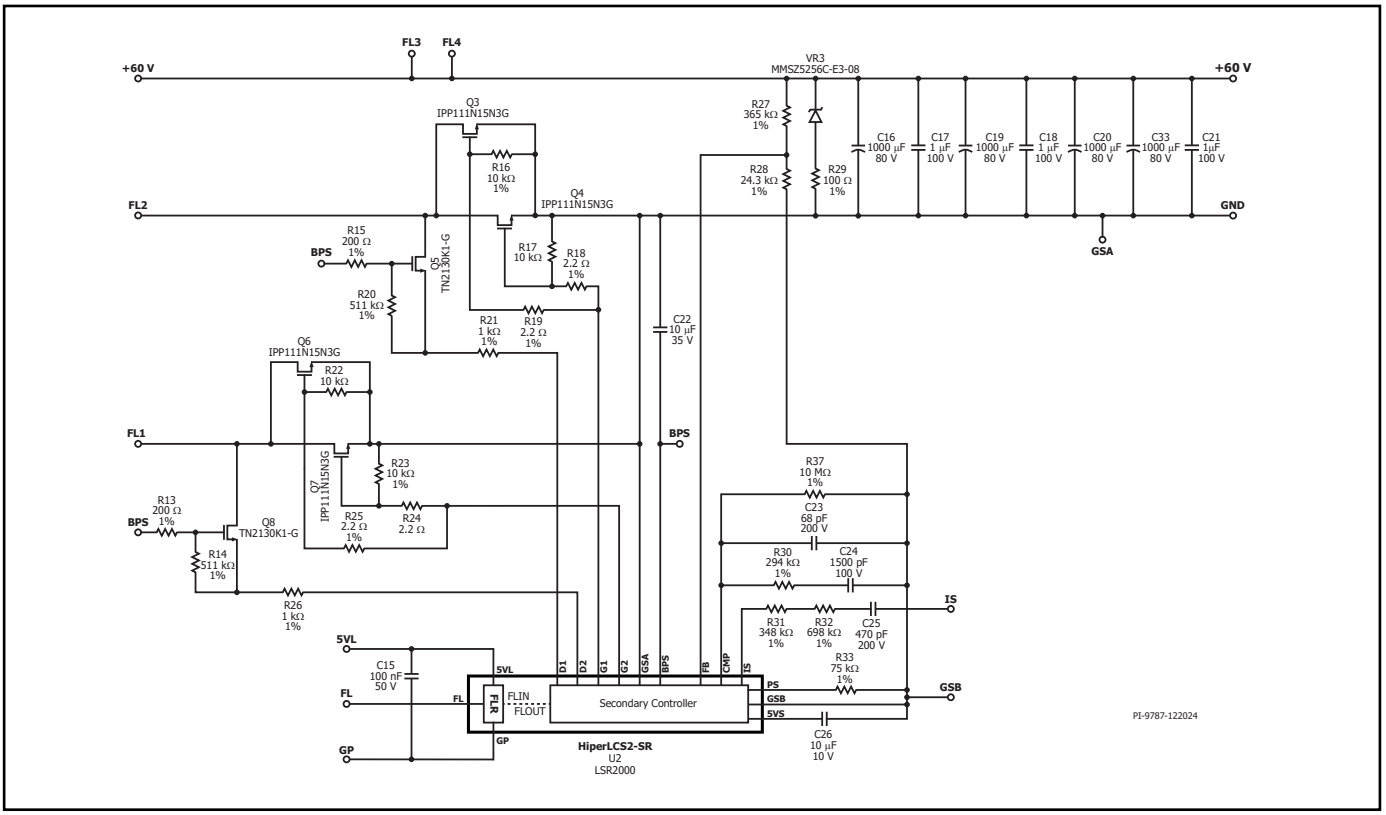


Figure 19. HiperLCS-2 Isolation and Secondary-Side 1650 W, 60 V LSR2000C.

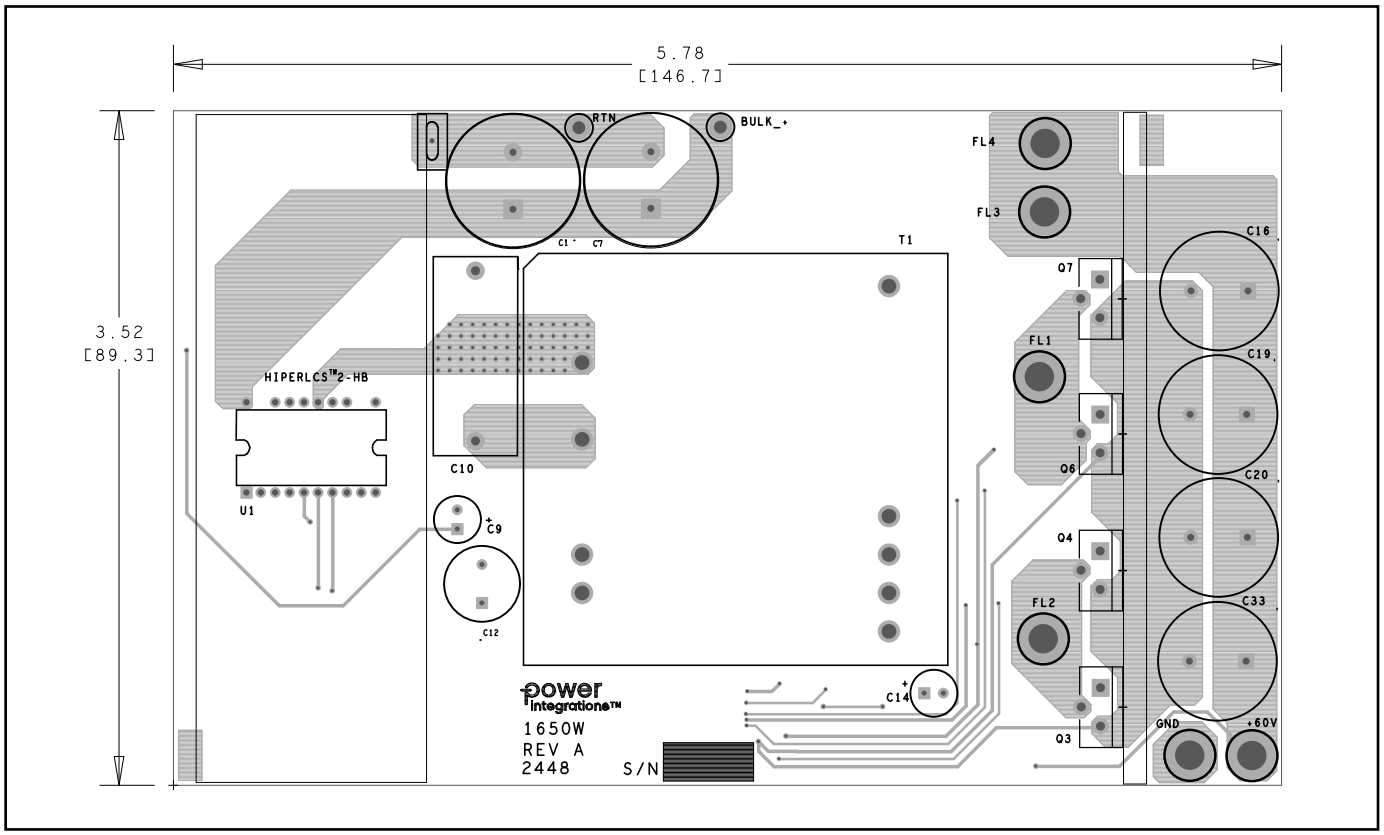


Figure 20. PCB Layout 1650 W / 60 V (Top View).

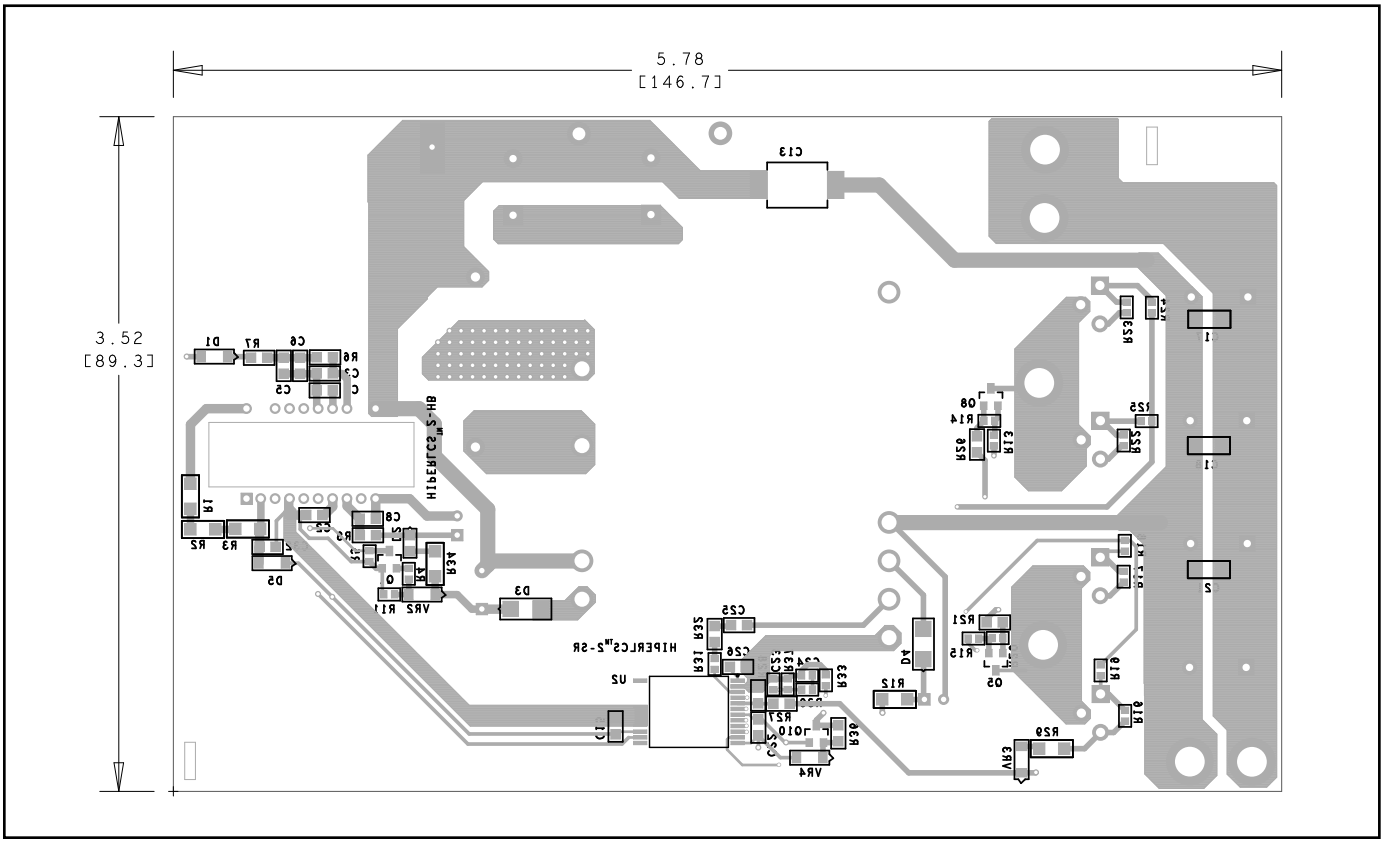


Figure 21. PCB Layout 1650 W / 60 V (Bottom View).

LLC Primary Schematic (1650 W / 60 V)

This section describes primary schematic Figure 18. The high-voltage input bus is filtered through capacitor C1 and C7. Line sense (L pin), detects the input bus voltage via resistors R1, R2 and R3. HiperLCS2-HB (U1), will initiate soft-start when L pin goes above UV+ threshold. Primary-side detected output overvoltage is sensed from the primary bias-winding (pins 9 and 10 of transformer T1), via Zener diode VR2 and resistor R11 and coupled to the PP pin via resistor R4 and transistor Q1. When overvoltage occurs, Zener VR2 conducts and current will be pulled from PP pin to ground via transistor Q1. Resistor R5 programs the PP pin primary frequency range and fault-response. The BM pin may couple to control an external in-rush relay drive circuit and/or to change PFC voltage as a function of light-load. Note BM transitions to low state when in light load burst mode.

Capacitors C2 and C8, decouple the 5VL and BPL respectively to GP (small signal primary Capacitor C2 and C8 decouple the 5VL and BPL pins respectively to GP (small signal primary ground). The primary return power-ground (RTN) is connected to S pin (SOURCE), primary-bias winding and capacitor C12, and the ground is kelvin connected to the negative pin of bulk-capacitor C1 and C7. From a layout point of view it is very important to keep the small signal GP ground, separate from system power-ground (RTN). Note: the RTN power-ground is intended to offer the low-impedance path for system noise events, whereby secondary coupled noise currents can be safely delivered to RTN/bulk-capacitor ground without disturbing primary small-signal ground (GP). Diode D3 rectifies primary bias winding voltage and capacitor C12 decouples to RTN ground. Capacitor C8 provides local high-frequency cycle-to-cycle decoupling to GD ground at the BPL pin. Before switching during start-up charge, the BPL pin charge both capacitor C8 and C9 (via resistor R8). Resistor R8 limits output current from BPL in the event of a large current draw from external PFC stage. Capacitor C9 provides storage to sustain start-up prior to primary bias winding contribution. Capacitor C9 is sized to also provide boot-strap energy to the LCS-2 high-side bias via diode-D1 and resistor R6. Capacitor C9 also provides bias to external PFC stage. Capacitor C9 should be sized to provide sufficient bias during startup and also for boot-strap, the capacitance of C9 should be greater than 5x the capacitance of high-side bias capacitors (C5+C6). Diode D2 is used as blocking diode to prevent initial BPL charge current at start-up from draw to charge capacitor C12 prior to bias winding activation. During normal operation the (U1) bias current comes from the bias winding to capacitor C12. The BPL pin has an internal shunt regulator to limit BPL voltage. Resistor R34 limits the BPL shunt-current when BPL shunt-voltage-clamping is active. This in turn limits the power-dissipation in the BPL during this condition. Note: pay careful attention to the steady-state bias-winding voltage. If voltage is above BPL clamp threshold, this may lead additional dissipation in the BPL circuit and may lead to unintentional thermal shutdown of LCS-2 (U1). Note that the bias winding voltage may vary over a 25% range from zero to full output load. For best no-load performance, the bias winding is intended to deliver a minimum of 15 V to the bias winding at zero load conditions, while the shunt will engage if the bias winding grossly exceeds 21 V at the BPL pin.

High-side bootstrap is charged via diode D1, then resistor R7 into capacitors C5 and C6 during low-side power MOSFET-on period. During the first few switching cycles at startup, capacitor C5 and C6 typically starts with no charge and resistor R7 limits the current into capacitors C5 and C6 if the capacitors voltage are fully-depleted. During initial bootstrap C5 an C6 charge current flows through the low-side power MOSFET, so the removal of resistor R7 may result in safety current limit being triggered under worst-case conditions.

Resistor R6 and capacitor C3 provide further low-frequency filtering to the BPH pin. High-side 5VH is decoupled via capacitor C4. Note that all high-side decoupling is with reference to HB pin. Resonant tank inductor components T1 pins 1/5 (integrated transformer includes resonant inductor LR and magnetizing inductance LM), are connected from HB in series through resonant capacitor C10 to primary return RTN (primary power ground).

LLC Secondary Schematic (1650 W / 60 V)

This section describes secondary schematic Figure 19. The HiperLCS2-SR (U2) has isolated primary-side pins. Pin 5VL receives 5VL voltage from LCS2-HB (U1). Pin GP couples to primary small signal ground (GP). Capacitor C15 provides local decoupling to the 5VL and GP pins of U2. The FL pin provides a FluxLink signal to the primary HiperLCS2-HB.

Transformer output pins T1 FL3/FL4 provide the positive output voltage, which is rectified and filtered by capacitors C16, C17, C18, C19, C20, C21 and C33. These capacitors combine to provide low ESR, which mostly defines the output ripple of the system and their combined capacitance should be chosen to match the desired burst off-time. These capacitors are decoupled to secondary power ground (GND).

Transformer output pins T1 FL1/FL2 respectively provide the return path for synchronous rectifier MOSFETs Q3, Q4, Q6 and Q7. The secondary power path is from T1 FL3/FL4 through capacitors C16, C17, C18, C19, C20, C21 and C33 and the return path via MOSFETs Q3, Q4, Q6 and Q7 to transformer T1 FL1/FL2. Note: for best matching of the two secondary power-phases, it is important to equalize the secondary power path such that path-lengths via Q3,Q4 and Q6,Q7 are equal.

Transformer T1 pin 13 feeds a diode D4 and capacitor C14 to rectify and filter the secondary bias winding and returns to T1/14 and secondary power ground (GND). Components R12, R36, Q10 and VR4 form a voltage regulator to provide a limited bias voltage to BPS. VR4 is returned to secondary SR-drive ground (GSA).

Capacitor C22 decouples the BPS to GSA (secondary SR-drive ground). Capacitor C26 decouples 5VS to GSB (secondary small signal ground).

Transformer T1 pin 13 feeds a diode D4 and capacitor C14 to rectify and filter the secondary bias winding and returns to T1/14 and GND (secondary power ground). Components R12, R36, Q10 and VR4 (connected to GSA secondary SR-drive ground), form a voltage regulator to provide a limited bias voltage to BPS. This is helpful for designs where the desired bias winding number of turns is in between discrete steps. Zener Diode VR3 and R29 may be required to provide a small pre-load to ensure the output maintains regulated during no load conditions. Output voltage is sensed via resistor R27 and R28 and returned to GSB (secondary small signal ground). Note: a local small value capacitor decoupling to GSB may help remove any high-frequency noise

Small signal secondary ground GSB is used for feedback, compensation and also as ground for IS pin signals. SR-ground GSA is used to return SR-gate-drive. Compensation is provided between CMP and GSB, via components R30 and C24 and C23 to provide a pole (C24, R30) and zero (R30, C23) and a final pole (C23). The transformer IS winding T2 pin 12 (T2 pin 11 grounded to GSB), provides a high frequency medium voltage small-signal which is capacitor coupled via C25 and then via resistors R32 and R31 to the IS pin.

The D1 and D2 pins sense the synchronous rectifier Q3, Q4, Q6 and Q7 drain voltages via resistors R21 and R26. The resistors are required to limit below-ground sensing current into the D1 and D2 pins. These resistor values can be increased to offer adjustment to SR turn-off threshold. Increasing resistor value will cause SR to turn off at higher SR current.

MOSFETs Q5 and Q8 acts as blocking FETs during SR turn-off, to limit the maximum voltage of V(R21) and V(R26) to approximately BPS (BPS + Q5,Q8 threshold) voltage. The normal maximum voltage on V(D1) and V(D2) is approximately 2 x V_{OUT}. The maximum pin voltage rating of D1 and D2 pins is 150 V (or ~120 with 80% derating).

This Q5, Q8 voltage limiting circuit is recommended for designs where 2 x V_{OUT} > = 120 V.

Synchronous MOSFET Q3, Q4, Q6 and Q7 drive is coupled from G1 and G2 pins via resistors R18, R19, R24 and R25. The drive resistors are optional and intended to limit super high-frequency MOSFET drive ring. In the case of FMEA open-connection condition from G1 and G2 to Q3, Q4, Q6 and Q7 gate, local pull-down resistors R16, R17, R22 and R23 are present to ensure the MOSFET Q3, Q4, Q6 and Q7 remain off.

The PS pin resistor R33 programs secondary-side user selection such as burst threshold.

Absolute Maximum Ratings[1,2] – LCS726xC and LCS726xZ

HD Pin Voltage[2]	-1.3 V to 600 V
HB Pin Voltage[2]	-1.3 V to 600 V
HB Pin Peak Current[4,5]: LCS7260C	2.9 A
LCS7262C	5.8 A
LCS7265C	10.9 A
LCS7265Z	10.9 A
LCS7268Z	17.5 A
LCS7269Z	34.8 A
BPH Pin Voltage[3,5]	-0.3 V to 27 V
BPL Pin Voltage[5]	-0.3 V to 27 V
BPL Pin Current	50 mA
5VH Pin Voltage[3]	-0.3 to 6 V
5VL Pin Voltage	-0.3 to 6 V
FL, PP Pin Voltage	-0.3 to 6 V
BM Pin Voltage	-0.3 to 6 V
BM Pin Current	10 mA
L Pin Voltage	-0.3 V to 600 V
L Pin Current	1 mA
S Pin to GP or GD Pin Voltage	±0.33 V
Junction Temperature[5]:	
FREDFET	-40 °C to 160 °C
Driver	-40 °C to 150 °C
Storage Temperature	-65 °C to 150 °C
Ambient Temperature	-40 °C to 105 °C
Lead Temperature	260 °C

Notes:
1. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
2. All voltages referenced to low-side Source S and signal ground GP, GD except noted otherwise, T_A = 25 °C.
3. Referenced to Half-bridge Connection HB, T_A = 25 °C.
4. Continuous DC output current per FREDFET calculated at 25 °C case and 125 °C junction temperature.
5. Normally limited by internal circuitry.

Thermal Resistance

Thermal Resistance: InSOP-24C Package	
LCS7260C (θ_{JA})	74 °C/W[1], 59 °C/W[2]
LCS7262C (θ_{JA})	68 °C/W[1], 53 °C/W[2]
LCS7265C (θ_{JA})	63 °C/W[1], 51 °C/W[2]
POWeDIP-20B Package	
LCS7265Z ($\theta_{JC(HB\ or\ HD)}$)	1.8 °C/W[3]
LCS7268Z ($\theta_{JC(HB\ or\ HD)}$)	1.3 °C/W[3]
LCS7269Z ($\theta_{JC(HB\ or\ HD)}$)	0.9 °C/W[3]

Notes:
1. Individual exposed pad (HB or HD), soldered to 0.36 sq. in. (232 mm²), 2 oz. (610 g/m²) copper clad.
2. Individual exposed pad (HB or HD), soldered to 1.0 sq. in. (645 mm²), 2 oz. (610 g/m²) copper clad.
3. Maximum thermal resistance junction to case (POWeDIP), $\theta_{JC(HB\ or\ HD)}$ measured underneath each HB or HD switch. The combined package $\theta_{JC(TOTAL)}$ is parallel combination of both HB or HD switches and can be calculated $\theta_{JC(TOTAL)} = \theta_{JC(HB\ or\ HD)} / 2$. POWeDIP mounted using M2 x 0.4 screws and M2 metal washers. Use thermal grease between POWeDIP package and heat sink. Make sure package is centered and assemble package to heat sink using the following sequence:
   a. Tighten first screw lightly until 0.3 in-lb.
   b. Tighten second screw until 0.3 in-lb.
   c. Tighten first screw again to 1.0 in-lb maximum.
   d. Tighten second screw again to 1.0 in-lb maximum.

Parameter	Symbol	Conditions T_{JC} = 0 °C to 100 °C BP = BPH = 18 V (Unless Otherwise Specified)		Min	Typ	Max	Units
Primary High-Side Controller/Driver							
BPH Pin							
BPH-HB Undervoltage Start Threshold	$V_{BPH(UV+)}$			12.4	13.2	14	V
BPH-HB Undervoltage Stop Threshold	$V_{BPH(UV-)}$			10.15	10.8	11.3	V
BPH-HB Start/Stop Hysteresis	$V_{BPH(UV)(HYST)}$				2.4		V
BPH (HD) Charge Output Current	$I_{BPH(CH)}$				-1.3		mA
BPH-HB UV to Shunt Spacing	$V_{BPH(SHGAP)}$	See Note D			9		V
BPH-HB Shunt Onset Voltage	$V_{BPH(SHON)}$	I_{BPHSH} = 250 µA		23.00	24.48	26.35	V
BPH-HB Shunt Max Voltage	$V_{BPH(SHMX)}$	I_{BPHSH} = 26 mA		23.50	24.55	27	V
BPH Shunt Current	$I_{BPH(SH)}$			0		26	mA
BPH Pin Current Consumption Switching	$I_{BPH(SW)}$	F_{SW} = 208 kHz	LCS7260C	1.4	1.7	2.0	mA
			LCS7262C	1.9	2.2	2.5	mA
			LCS7265C	3.0	3.3	3.6	mA
			LCS7265Z	2.7	3.10	3.4	mA
			LCS7268Z	3.9	4.45	5.1	mA
			LCS7269Z	6.7	8.00	10	mA
BPH Pin Current Non-Switching Consumption	$I_{BPH(NSW)}$	No switching $V_{BPH} > V_{BPH(UV+)}$		90	115	150	µA
5VH Pin							
5VH-HB Power-Up Threshold	$V_{5VH(UV+)}$	See Note A		4.85	4.9	4.99	V
5VH-HB Power-Up Threshold	$V_{5VH(UV-)}$	See Note A		4.45	4.55	4.7	V
5VH-HB Power-Up Hysteresis	$V_{5VH(UV)(HYST)}$	See Note A		0.3	0.35	0.4	V
5VH-HB Output Voltage	V_{5VH}	I_{5VH} = 0 mA			5.17		V
Primary Low-Side Controller/Driver							
BPL Pin							
BPL Undervoltage Start Threshold	$V_{BPL(UV+)}$			13	13.7	14.3	V

Parameter	Symbol	Conditions T_{JC} = 0 °C to 100 °C BP = BPH = 18 V (Unless Otherwise Specified)		Min	Typ	Max	Units
Primary Low-Side Controller/Driver (cont.)							
BPL Undervoltage Stop Threshold	$V_{BPL(UV-)}$			10.4	11.4	12	V
BPL Start/Stop Hysteresis	$V_{BPL(UV)(HYST)}$				2.3		V
BPL (HD) Low Charge Current	$I_{BPL(CH)LO}$	V_{HB} = 50 V, V_{BP} = 0 V		-2.5	-1.9	-1.55	mA
BPL (HD) Charge Output Current	$I_{BPL(CH)}$	V_{HB} = 50 V, V_{BP} = 10 V		-10	-7.7	-4.2	mA
BPL UV to Shunt Spacing	$V_{BPL(SHGAP)}$	See Note D			9		V
BPL Shunt Onset Voltage	$V_{BPL(SHON)}$	I_{BPLSH} = 500 µA		20	21.61	23	V
BPL Shunt Max Voltage	$V_{BPL(SHMX)}$	I_{BPLSH} = 26 mA		20	21.83	23.50	V
BPL Pin Current Switching Consumption	$I_{BPL(SW)}$	F_{SW} = 208 kHz	LCS7260C	2.4	2.7	3.2	mA
			LCS7262C	3	3.3	3.6	mA
			LCS7265C	4.1	4.5	5.0	mA
			LCS7265Z	3.6	4.2	6.2	mA
			LCS7268Z	5.3	6	7	mA
			LCS7269Z	8	10.9	13.7	mA
BPL Pin Current Non-Switching Consumption	$I_{BPL(NSW)}$	No switching V_{BPL} > $V_{BPL(UV+)}$		600	780	950	µA
5VL Pin							
5VL Power-Up Threshold	$V_{5VL(UV+)}$	C5VL = 1 µF / 10 V ceramic See Note A		4.85	4.9	4.99	V
5VL Power-Up Threshold	$V_{5VL(UV-)}$	C5VL = 1 µF / 10 V ceramic See Note A		4.45	4.55	4.70	V
5VL Power-Up Threshold	$V_{5VL(HYST)}$	C5VL = 1 µF / 10 V ceramic See Note A		0.30	0.35	0.40	V
5VL Output Voltage	V_{5VL}	I_{5VL} = 0 mA			5.15		V
BM Pin							
BM – On Trigger Period (no FL)	$T_{BM(ON)}$	See Note A			5		ms
BM – On Trigger Debounce	$T_{BM(DB)}$	See Note A			5		sec
BM – Off Trigger Period (FL present)	$T_{BM(OFF)}$	See Note A			2		ms
BM – Current Source	$I_{BM(SRC)}$	BM Driving High, V_{BM} = 0 V See Note A, C			-19		mA
BM – Current Sink	$I_{BM(SNK)}$	BM Driving Low, V_{BM} = V_{5VL} See Note A			24		mA
BM – On-Output Voltage	$V_{BM(ON)}$	I_{BM} = - 2 mA		4.2	4.65		V
BM – Off-Output Voltage	$V_{BM(OFF)}$	I_{BM} = + 2 mA			0.005	0.1	V

Parameter	Symbol	Conditions T_{JC} = 0 °C to 100 °C BP = BPH = 18 V (Unless Otherwise Specified)	Min	Typ	Max	Units
Primary Low-Side Controller/Driver (cont.)						
FL Pin						
FL – Logic 1 Input High-Voltage	$V_{FL(IH)}$			3.2	4.2	V
FL – Logic 0 Input Low-Voltage	$V_{FL(IL)}$		1.2	1.5		V
L Pin						
L Pin Breakdown Voltage	$V_{L(BV)}$	L Pin Disabled (Burst Off-State)	600			V
L Pin UV Stop Threshold Current	$I_{L(UV-)}$		44	49	54	µA
L Pin UV Restart Threshold Current	$I_{L(UV+)}$		58	63.5	69	µA
L Pin OV Restart Threshold Current	$I_{L(OV-)}$		98	108	118	µA
L Pin OV Stop Threshold Current	$I_{L(OV+)}$		110	123	135	µA
L Pin UV Hysteresis Current	$I_{L(UV)(HYST)}$		12.0	14.6	17.2	µA
L Pin OV Hysteresis Current	$I_{L(OV)(HYST)}$		12.5	15.2	18.2	µA
L Pin Sink Current	$I_{L(SNK)}$	See Note A, C	200			µA
L Pin Sink Voltage UV Stop	$V_{L(SNK)(UV-)}$	$I_{L(SNK)} = I_{L(UV-)}$		1.6		V
L Pin Sink Voltage UV Start	$V_{L(SNK)(UV+)}$	$I_{L(SNK)} = I_{L(UV+)}$		1.7		V
L Pin Sink Voltage OV Start	$V_{L(SNK)(OV-)}$	$I_{L(SNK)} = I_{L(OV-)}$		2.0		V
L Pin Sink Voltage OV Stop	$V_{L(SNK)(OV+)}$	$I_{L(SNK)} = I_{L(OV+)}$		2.1		V
PP Pin						
PP Pin Remote-Off Threshold	$I_{PP(REM-)}$		-17	-13.5	-10	µA
PP Pin Remote-On Threshold	$I_{PP(REM+)}$		-47	-39	-32	µA
PP Pin Remote-On/Off Hysteresis	$I_{PP(REM)(HYST)}$		20	25.5	31	µA
PP Pin Remote-On Voltage	$V_{PP(REM+)}$			0.81		V
PP Pin Remote-Off Voltage	$V_{PP(REM-)}$			0.86		V
PP Pin Fault Clear Threshold	$I_{PP(FLT-)}$		-93	-79	-66	µA
PP Pin Fault Assert Threshold	$I_{PP(FLT+)}$		-95	-81	-68	µA

Parameter	Symbol	Conditions T_{JC} = 0 °C to 100 °C BP = BPH = 18 V (Unless Otherwise Specified)		Min	Typ	Max	Units
Primary Low-Side Controller/Driver (cont.)							
PP Pin Remote-On/Off Hysteresis	$I_{PP(FLT)(HYST)}$				1		µA
PP Pin Fault Assert Voltage	$V_{PP(FLT+)}$				0.75		V
PP Pin Selection0 Resistor	$R_{PP(SEL0)}$	Required Resistor 1% E96 series			59		kΩ
PP Pin Selection1 Resistor	$R_{PP(SEL1)}$	Required Resistor 1% E96 series			158		kΩ
PP Pin Selection2 Resistor	$R_{PP(SEL2)}$	Required Resistor 1% E96 series			226		kΩ
PP Pin Selection3 Resistor	$R_{PP(SEL3)}$	Required Resistor 1% E96 series			316		kΩ
PP Pin Selection4 Resistor	$R_{PP(SEL4)}$	Required Resistor 1% E96 series			412		kΩ
PP Pin Selection5 Resistor	$R_{PP(SEL5)}$	Required Resistor 1% E96 series			536		kΩ
PP Pin Selection6 Resistor	$R_{PP(SEL6)}$	Required Resistor 1% E96 series			715		kΩ
PP Pin Selection7 Resistor	$R_{PP(SEL7)}$	Required Resistor 1% E96 series			1020		kΩ
HB MOSFET							
HB-S Breakdown Voltage Rating	$V_{HBS(BV)}$			600			V
HB-S Reverse Voltage Rating	$V_{HBS(BV)}$	See Note A		-1.5			V
HB Start-Up PreCharge Current to S Pin	$I_{HB(PRE)}$				2		mA
HB $R_{DS(ON)}$	$R_{DS(ON)}$	I_{HB} = 0.8 A, T_{JS} = 25 ºC, 400 µs Single Pulse	LCS7260C		1.49		Ω
		I_{HB} = 1.6 A, T_{JS} = 25 ºC, 400 µs Single Pulse	LCS7262C		0.73		Ω
		I_{HB} = 3.2 A, T_{JS} = 25 ºC, 400 µs Single Pulse	LCS7265C		0.41		Ω
		I_{HB} = 3.2 A, T_{JS} = 25 ºC, 400 µs Single Pulse	LCS7265Z		0.41		Ω
		I_{HB} = 4.8 A, T_{JS} = 25 ºC, 400 µs Single Pulse	LCS7268Z		0.26		Ω
		I_{HB} = 9.8 A, T_{JS} = 25 ºC, 400 µs Single Pulse	LCS7269Z		0.13		Ω

Parameter	Symbol	Conditions T_{JC} = 0 °C to 100 °C BP = BPH = 18 V (Unless Otherwise Specified)		Min	Typ	Max	Units
Primary Low-Side Controller/Driver (cont.)							
HB MOSFET							
Combined HB Q_{oss} (0 .. 480 VDC)	$Q_{HBOSS(480V)}$	V_{GS} = 0 V, V_{DS} = 0 - 480 V, See Note D	LCS7260C	40	50	60	nC
			LCS7262C	81	100	120	nC
			LCS7265C	153	189	225	nC
			LCS7265Z	153	189	225	nC
			LCS7268Z	245	302	360	nC
			LCS7269Z	490	604	720	nC
HB Safety Current Limit	$I_{HB(SFTY)}$	See Note C	LCS7260C		2.7		A
			LCS7262C		5.4		A
			LCS7265C		10.1		A
			LCS7265Z		10.1		A
			LCS7268Z		16.2		A
			LCS7269Z		32.4		A
HB Start-Up Current Limit	$I_{HB(IOVL)}$	See Note C	LCS7260C		1.9		A
			LCS7262C		3.7		A
			LCS7265C		7.0		A
			LCS7265Z		7.0		A
			LCS7268Z		11.2		A
			LCS7269Z		22.3		A
HB Start-Up Reduced Current Limit	$I_{HB(IOVL-)}$	See Note C, D	LCS7260C		0.66		A
			LCS7262C		1.29		A
			LCS7265C		2.43		A
			LCS7265Z		2.43		A
			LCS7268Z		3.89		A
			LCS7269Z		7.74		A

Parameter	Symbol	Conditions T_{JC} = 0 °C to 100 °C BP = BPH = 18 V (Unless Otherwise Specified)		Min	Typ	Max	Units
Primary Low-Side Controller/Driver (cont.)							
HB Diode							
HB Diode Forward Voltage	$V_{HB(F)}$	I_F = 1.0 A, V_{GS} = 0 V, T_J = 100 °C See Note D	LCS7260C		1.13		V
			LCS7262C		0.9		V
			LCS7265C		0.8		V
			LCS7265Z		0.8		V
			LCS7268Z		0.74		V
			LCS7269Z		0.66		V
HB Diode Reverse Recovery Current	$I_{HB(RRM)}$	I_F = $I_{HB(RRM)}$ A, di/dt = 200 A/µs, V_R = 400 V, T_J = 125 °C See Note D	LCS7260C		4.0		A
			LCS7262C		5.6		A
			LCS7265C		8		A
			LCS7265Z		8		A
			LCS7268Z		10.2		A
			LCS7269Z		20.4		A
HB Diode Reverse Recovery Time	$T_{HB(RR)}$	I_F = $I_{HB(RRM)}$ A, di/dt = 200 A/µs, V_R = 400 V, T_J = 125 °C See Note D	LCS7260C		110		ns
			LCS7262C		170		ns
			LCS7265C		200		ns
			LCS7265Z		200		ns
			LCS7268Z		200		ns
			LCS7269Z		200		ns
HB Diode Reverse Recovery Charge	$Q_{HB(RR)}$	I_F = $I_{HB(RRM)}$ A, di/dt = 200 A/µs, V_R = 400 V, T_J = 125 °C See Note D	LCS7260C		220		nC
			LCS7262C		480		nC
			LCS7265C		840		nC
			LCS7265Z		840		nC
			LCS7268Z		1200		nC
			LCS7269Z		2400		nC

Parameter	Symbol	Conditions T_{JC} = 0 °C to 100 °C BP = BPH = 18 V (Unless Otherwise Specified)	Min	Typ	Max	Units
Primary Low-Side Controller/Driver (cont.)						
HD Pin						
HD-S Breakdown Voltage	$V_{HDS(BV)}$		600			V
HD-HB Breakdown Voltage Rating	$V_{HBHD(BV)}$		600			V
HD-HB Reverse Voltage Rating	$V_{HBS(BV)}$	See Note A	-1.5			V
Half-Bridge Over-Temperature Stop	$HB_{(OT)(STOP)}$	See Note A	131	139	147	°C
Half-Bridge Over-Temperature Hysteresis	$HB_{(OT)(HYST)}$	See Note A	10	14	18	°C
LS Controller Over-Temperature Stop	$LS_{(OT)(STOP)}$	See Note A	115	125	135	°C
LS Controller Over-Temperature Start	$LS_{(OT)(START)}$	See Note A	66	78	90	°C

NOTES:
A. Not tested parameter. Guaranteed by design.
B. In typical LLC application circuit.
C. Normally limited by internal circuitry.
D. Not tested parameter. Based on device characterization.

Absolute Maximum Ratings[1,2] – LSR2000C

BPS Pin Voltage ..... -0.3 V to 25 V
BPS Pin Current ..... 2 A
D1, D2 Pin Voltage ..... -1.5 V to 150 V
FB Pin Voltage ..... -0.3 V to 6 V
CMP Pin Voltage ..... -0.3 V to 6 V
G1, G2 Pin Voltage ..... -0.3 V to 20 V
IS Pin Voltage ..... -0.3 V to 5 V
5VS Pin Voltage ..... -0.3 V to 6 V
5VL Pin Voltage (wrt GP) ..... -0.3 V to 6 V
FL Pin Voltage (wrt GP) ..... -0.3 V to 6 V
Junction Temperature[3] ..... -40 to 150 °C
Storage Temperature ..... -65 °C to 150 °C
Ambient Temperature ..... -40 °C to 105 °C
Lead Temperature[4] ..... 260 °C

Notes:
1. All voltages referenced to GSA, GSB unless otherwise stated T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Absolute maximum voltage for less than 500 msec is 3 V.

Thermal Resistance

Thermal Resistance: InSOP-24D
(θ_{JA}) ..... 90 °C/W[1]

Notes:
1. Pins 2 and 12 soldered to a shared 0.36 sq. inch (232 mm^2) 2 oz. (610 g/m^2) copper clad.

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Secondary-Side Power Rating	TAMB = 25 °C See Note A	820	mW
Secondary-Side Power Rating	TAMB = 105 °C	300	mW
Secondary-Side Current Rating	TAMB = 25 °C See Note A	34	mA
Package Characteristics			
Clearance		11.35	mm (min)
Creepage		11.35	mm (min)
Distance Through Insulation (DTI)		0.4	mm (min)
Transient Isolation Voltage		6	kV (min)
Comparative Tracking Index (CTI)		600	-

Note A: Remark regarding UL testing: the secondary side Pin 7 BPS power the IC internal controller on the secondary side and functioned as a constant current load. The pin is intended to accept a voltage in the 8-24 VDC range, which is shown on the spec, and drew 818 mW max at the high end of the voltage range.

Parameter	Symbol	Conditions BPS = 12 V T_J = 0 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Secondary-Side of Safety Isolation Barrier							
Frequency Pin							
FMIN Frequency Range 0	$F_{MIN(FR0)AUTO}$	See Note A	LSR2000C H001	21	23	24	kHz
FMIN Frequency Range 1	$F_{MIN(FR1)AUTO}$		LSR2000C H002	28	30	32	kHz
FMIN Frequency Range 2	$F_{MIN(FR2)AUTO}$		LSR2000C H003	41	45	47	kHz
FMIN Frequency Range 3	$F_{MIN(FR3)AUTO}$		LSR2000C H004	55	60	63	kHz
			LSR2000C H005				
FMAX Frequency Range 0	$F_{MIN(FR0)LATCH}$		LSR2000C H001	123	135	141	kHz
FMAX Frequency Range 1	$F_{MIN(FR0)LATCH}$		LSR2000C H002	167	183	191	kHz
FMAX Frequency Range 2	$F_{MIN(FR0)LATCH}$		LSR2000C H003	246	270	282	kHz
FMAX Frequency Range 3	$F_{MIN(FR0)LATCH}$		LSR2000C H004	334	366	383	kHz
			LSR2000C H005				
BPS Pin							
BPS Undervoltage Shutdown Threshold	$V_{BPS(UV-)}$			7.0	7.25	7.5	V
BPS Above UV Start Threshold	$V_{BPS(UV+)}$			7.3	7.55	7.8	V
BPS Start/Stop Hysteresis	$V_{BPS(UV)(HYST)}$				0.29		V
BPS Pin Current in Burst	$I_{BPS(BURST)}$	Operating in super light load switching G1, G2 floating, See Note D			600		µA
BPS Pin Current Consumption	$I_{BPS(SW)}$	Device with G1,G2 floating, V_{BPS} = $V_{BPS(UV+)}$	Frequency Range0 (90 kHz)		9.9		mA
			Frequency Range1 (120 kHz)		12.5		mA
			Frequency Range2 (180 kHz)		17.6		mA
			Frequency Range3 (240 kHz)		23.2		mA
5VS Pin							
5VS Secondary Power-Up Threshold	$V_{5VS(UV+)}$	C_{5VS} = 1 µF / 10 V Ceramic See Note A		4.25	4.30	4.37	V
5VS Secondary Power-Down Threshold	$V_{5VSU(V-)}$	C_{5VS} = 1 µF / 10 V Ceramic See Note A		4.15	4.2	4.25	V
5VS Hysteresis	$V_{5VS(HYST)}$	C_{5VS} = 1 µF / 10 V Ceramic See Note A		0.08	0.1	0.12	V
5VS Output Voltage	V_{5VS}	I_{5VS} = 0 mA, See Note A			5.18		V
IS Pin							
IS Pin Input Common Mode Voltage	$V_{IS(CM)}$				2.8		V
IS Pin Input Impedance	$R_{IS(IN)}$			3.2	3.7	4.3	kΩ
IS Pin Input Current Clip Threshold	$I_{IS(CLP)}$			-44	-39	-32	µA
IS Pin Gain	$G_{IS(CMP)}$			-74	-72	-70	kV/A
IS Pole	$F_{IS(CMP)}$	See Note A		2.1	3.3	4.4	MHz

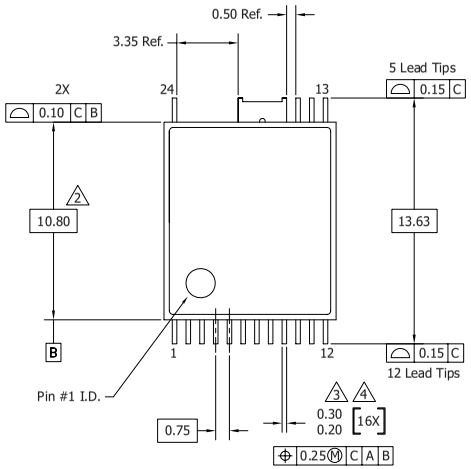
Parameter	Symbol	Conditions BPS = 12 V T_J = 0 °C to 100 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary-Side of Safety Isolation Barrier (cont.)						
CMP Pin						
CMP Pin Max Output Current	$I_{CMP(OUT)(MAX)}$	$V_{FB} = V_{FB(STOP)(TH)}$ See Note D	50	80	140	µA
CMP Pin Burst Off 2.5 V Pull	$R_{CMP(PULL)(2V5)}$	During burst-off condition See Note A		1		MΩ
FB Pin						
FB Pin REF Threshold	$V_{FB(REF)}$	V_{FB} when ICMP = 0	3.7	3.75	3.8	V
FB Pin Stop Plus Threshold	$V_{FBSTOP(TH)}$		3.91	3.96	4.01	V
FB Pin Stop – VFBREF	$V_{FBSTOP(DIFF)}$	Difference $V_{FBSTOP(TH)} – V_{FBREF}$	194	210	226	mV
FB Pin Max Threshold	$V_{FB(MAX)(TH)}$		3.72	3.77	3.81	V
FB Pin Max – VFBREF	$V_{FB(MAX)(DIFF)}$	Difference $V_{FBMAX(TH)} – V_{FBREF}$	6	19	32	mV
FB Pin Min Threshold	$V_{FB(MIN)(TH)}$		3.69	3.73	3.77	V
FB Pin Min – VFBREF	$V_{FBMIN(DIFF)}$	Difference $V_{FBMIN(TH)} – V_{FBREF}$	-32	-19	-6	mV
FB Pin REG Threshold	$V_{FBREG(TH)}$		3.7	3.75	3.8	V
FB Pin REG – VFBREF	$V_{FBREG(DIFF)}$	Difference $V_{FBREG(TH)} – V_{FBREF}$	-14	0	14	mV
FB Pin VREG – VMIN Difference	$V_{FBREG(MIN)}$		6	19	32	mV
FB Pin VMAX – VMIN Difference	$V_{FB(MAX)MIN}$		25	39	52	mV
FB Pin MINBOOST Threshold	$V_{FBBSTN(TH)}$		3.54	3.60	3.65	V
FB Pin MINBOOST VFBREF	$V_{FBBSTN(DIFF)}$	Difference $V_{FBBSTN(TN)} – V_{FBREF}$	-160	-148	-136	mV
FB Pin MAXBOOST Threshold	$V_{FBBSTP(TH)}$		3.75	3.8	3.85	V
FB Pin MAXBOOST VFBREF	$V_{FBBSTP(DIFF)}$	Difference $V_{FBBSTP(TN)} – V_{FBREF}$	42	55	68	mV
FB CMP Trans Conductance Normal Gain	$G_{FB(CMP)(NORM)}$	T_J = 25 °C $V_{FB} > V_{FBBSTN(TH)}$ and $V_{FB} < V_{FBBSTP(TH)}$	85	95	105	µA/µV
FB CMP Trans Conductance Boost Gain	$G_{FB(CMP)(BST)}$	T_J = 25 °C $V_{FB} < V_{FBBSTN(TH)}$ or $V_{FB} > V_{FBBSTP(TH)}$	325	365	405	µA/µV
Trans Impedance 100 °C / 25 °C Ratio	$G_{FB(CMP)(RATIO)}$	See Note D		93		%
FB Pole Frequency	$FB_{(BW)}$	See Note A	187	316	654	kHz
FB Pin Bleed Current	$I_{FB(DN)}$	T_J = 25 °C, See Note A		100		nA

Parameter	Symbol	Conditions BPS = 12 V T_J = 0 °C to 100 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary-Side of Safety Isolation Barrier (cont.)						
PS Pin						
PS Pin Selection0 Resistor	$R_{PS(SEL0)}$	Required Resistor 1% E96 Series		75		kΩ
PS Pin Selection1 Resistor	$R_{PS(SEL1)}$	Required Resistor 1% E96 Series		75		kΩ
PS Pin Selection2 Resistor	$R_{PS(SEL2)}$	Required Resistor 1% E96 Series		75		kΩ
PS Pin Selection3 Resistor	$R_{PS(SEL3)}$	Required Resistor 1% E96 Series		169		kΩ
PS Pin Selection4 Resistor	$R_{PS(SEL4)}$	Required Resistor 1% E96 Series		169		kΩ
PS Pin Selection5 Resistor	$R_{PS(SEL5)}$	Required Resistor 1% E96 Series		255		kΩ
PS Pin Selection6 Resistor	$R_{PS(SEL6)}$	Required Resistor 1% E96 Series		340		kΩ
PS Pin Selection7 Resistor	$R_{PS(SEL7)}$	Required Resistor 1% E96 Series		499		kΩ
G1 and G2 Pins						
G1, G2 Clamp Voltage (Freq 0,1)	$V_{G1(CLMP)}$ $V_{G2(CLMP)}$	BPS = 15 V	10.3	11.7	13.5	V
G1, G2 Clamp Voltage (Freq 2,3)	$V_{G1(CLMP)}$ $V_{G2(CLMP)}$	BPS = 15 V	5.0	6.0	7.0	V
G1, G2 BP Voltage Drop	$V_{G1(CLMP)(DROP)}$ $V_{G2(CLMP)(DROP)}$	BPS = 15 V See Note A	0.65	1.1	1.5	V
G1, G2 Source Current	$I_{G1(SOURCE)}$ $I_{G2(SOURCE)}$	BPS = 15 V, VG1 = VG2 = 0 V	0.65	1.1	1.5	A
G1, G2 Sink Current	$I_{G1(SINK)}$ $I_{G2(SINK)}$	BPS = 15 V, VG1 = VG2 = VG1(CLMP)	1.6	2	2.2	A

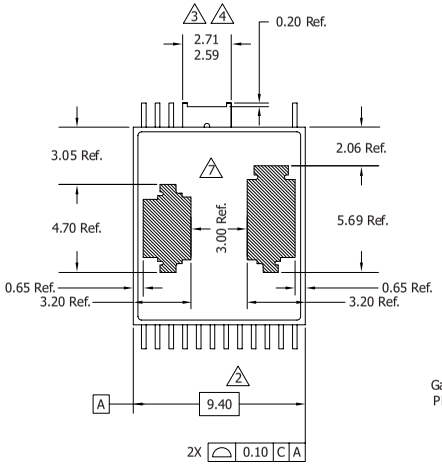
Parameter	Symbol	Conditions BPS = 12 V T_J = 0 °C to 100 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary-Side of Safety Isolation Barrier (cont.)						
D1 and D2 Pin						
D1, D2 Breakdown Voltage	BV_{D1D2}		150			V
D1, D2 External Resistor	$R_{D1D2(EXT)}$	Recommended external R between SR FET Drain and D1, D2 pin	200		1500	Ω
D1, D2 Inverse Current	$I_{D1D2(INV)}$	Allowed current out of D1, D2 when below GND	-5			mA
D1, D2 SR On Threshold	$V_{D1D2ON(TH)}$	See Note E	-275	-250	-210	mV
D1, D2 SR Off Threshold	$V_{D1D2OFF(TH)}$	See Note E	3	8.5	12.5	mV
D1, D2 SR Off Threshold Matching	$\Delta V_{D1D2OFF}$		-2.6	0	2.6	mV
D1, D2 Ouput Bias Current – Off	$I_{D1D2OFF}$	Bias Current Out of D1, D2 at $V_{D1D2OFF(TH)}$	-17	-13	-9	µA
Secondary Control Over-Temperature						
Secondary Control Over-Temperature Stop	$SC_{(OT)(STOP)}$	See Note A	123	130	137	°C
Secondary Control Over-Temperature Start	$SC_{(OT)(START)}$	See Note A		75		°C
Primary-Side of Safety Isolation Barrier						
5VL Pin						
5VL Power-Up Threshold	$V_{5VL(UV+)}$	C5VL = 1 µF / 10 V Ceramic	3	3.5	4	V
5VL Power-Up Hysteresis	$V_{5VL(HYST)}$	C5VL = 1 µF / 10 V Ceramic		1.5		V
FL Pin						
FL - Logic 1 Output Voltage	$V_{FL(1)}$	I_{FL} = 10 mA, 5VL = 5 V	4.55	4.7	4.929	V
FL - Logic 0 Output Voltage	$V_{FL(0)}$	I_{FL} = +10 mA	0.17	0.25	0.42	V

NOTES:
A. Not tested parameter. Guaranteed by design.
B. In typical LLC application circuit.
C. Normally limited by internal circuitry.
D. Not tested parameter. Based on device characterization.
E. Production test limits. Observed operational threshold for SR MOSFET drain (D1, D2), also depends on chosen D1, D2 resistors $R_{D1D2(EXT)}$ values.

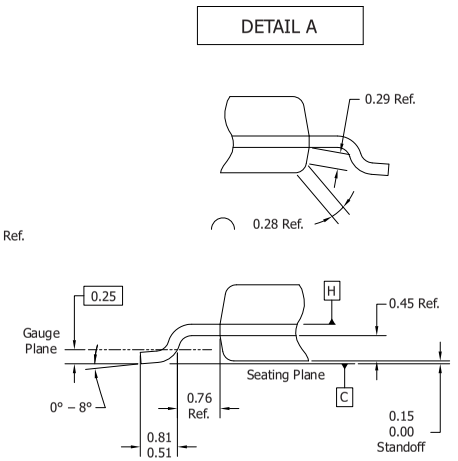
InSOP-24C

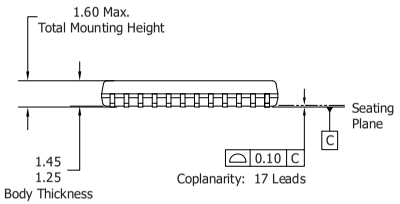


TOP VIEW

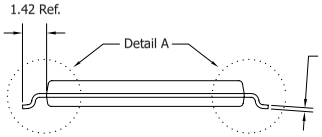


BOTTOM VIEW

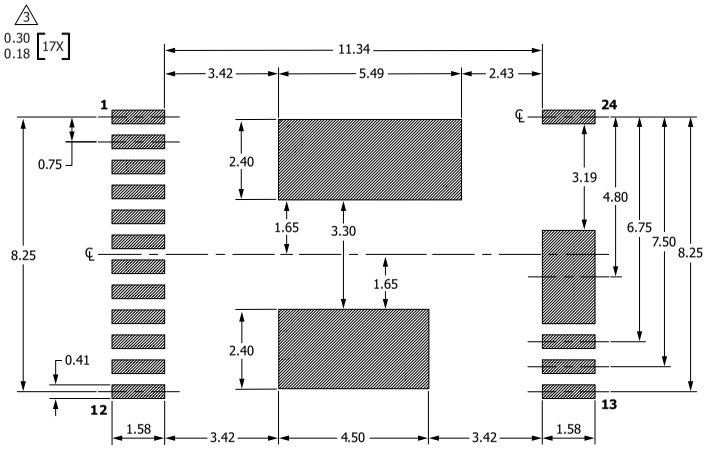




SIDE VIEW



END VIEW



Note: The PCB footprint shown is the minimum recommended layout for basic thermal, mechanical and electrical interconnect, including package-to-PCB creepage. Modifications are expected, based on application-specific requirements, to add copper areas for improved thermal performance or reduce for increased on-PCB creepage.

PCB PAD LAYOUT

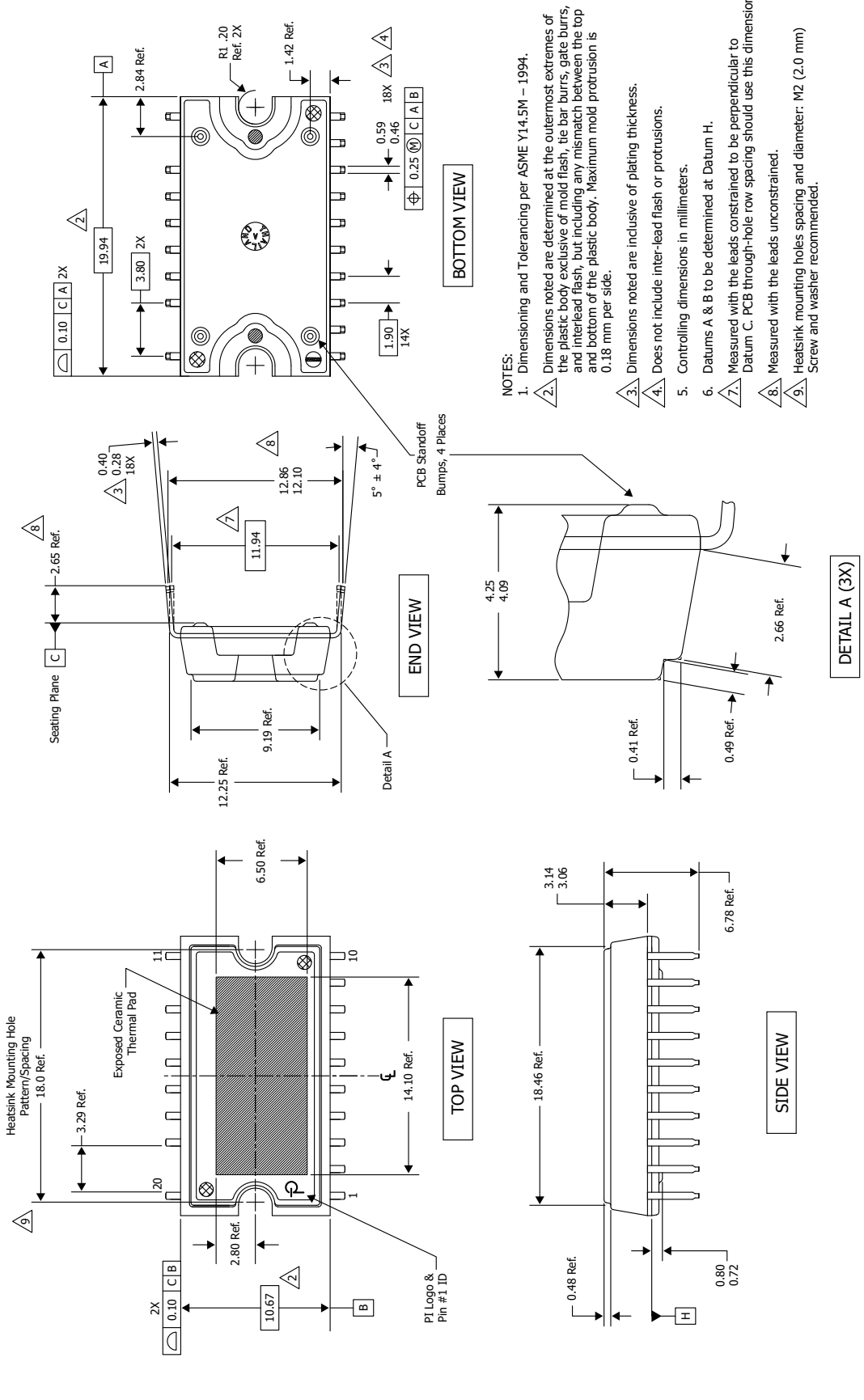
Notes:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 mm per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. Exposed pad size and location dimensions are for reference only.

POD_inSOP-24C_B_031417

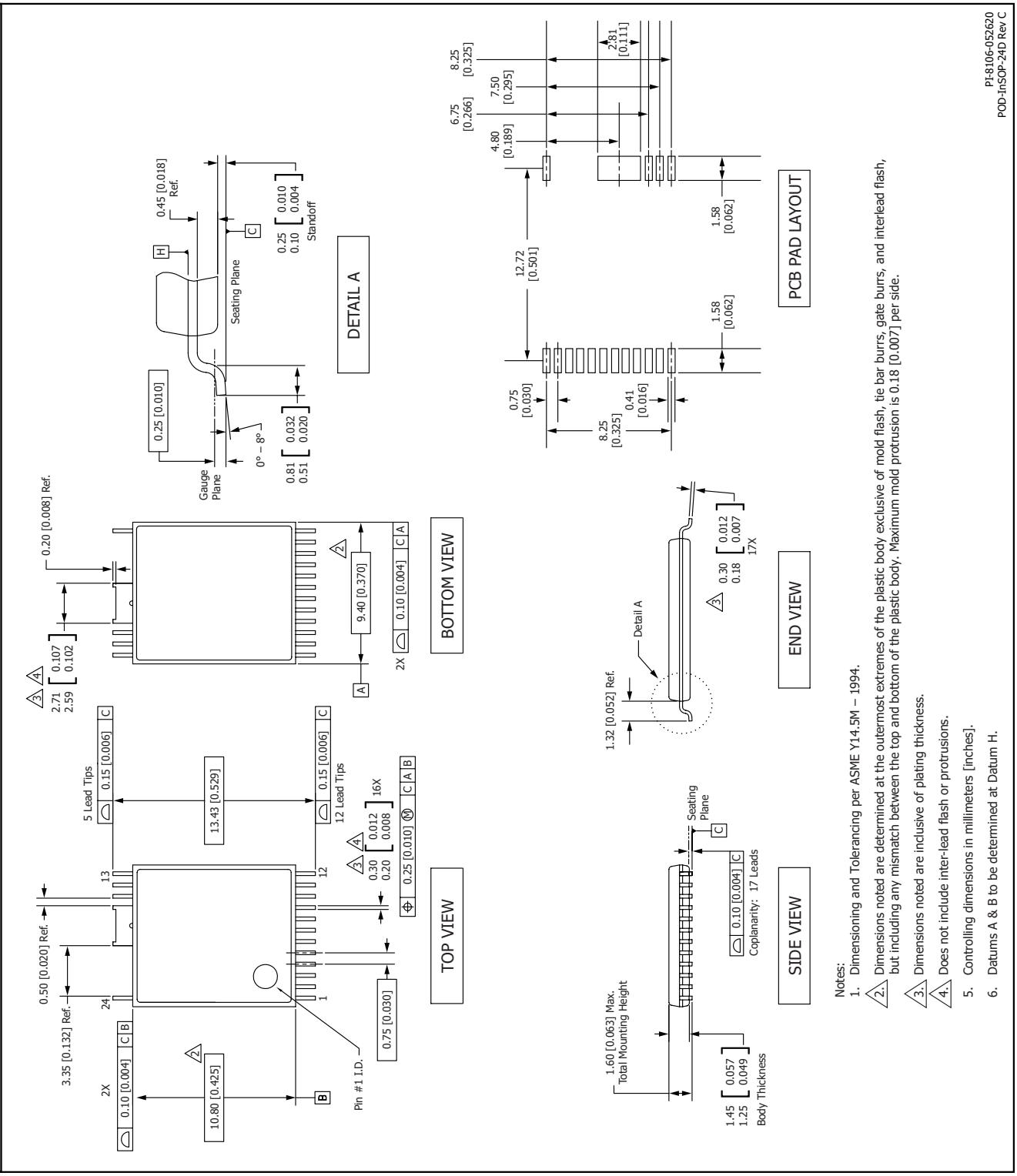
PI-8294-102423

POWeDIP-20B



PI-8892d-061223
POD-POWeDIP-20B Rev D
POD-POWeDIP-20B_D_061223

InSOP-24D



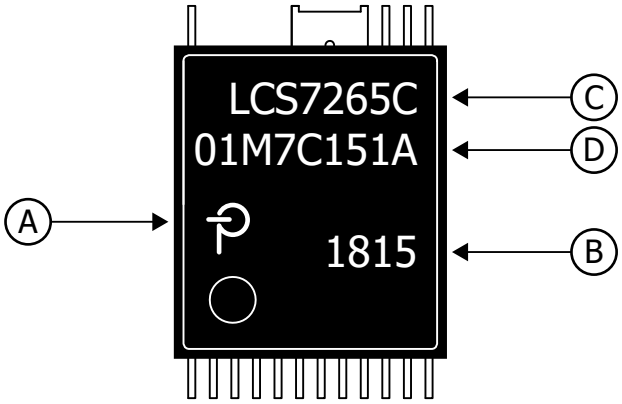
P1-8106-052620
POD-InSOP-24D Rev C

Notes:

1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters [inches].
6. Datums A & B to be determined at Datum H.

PACKAGE MARKING

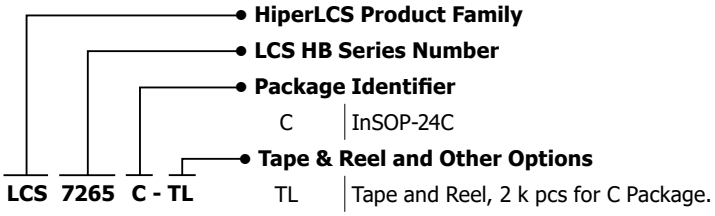
InSOP-24C



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

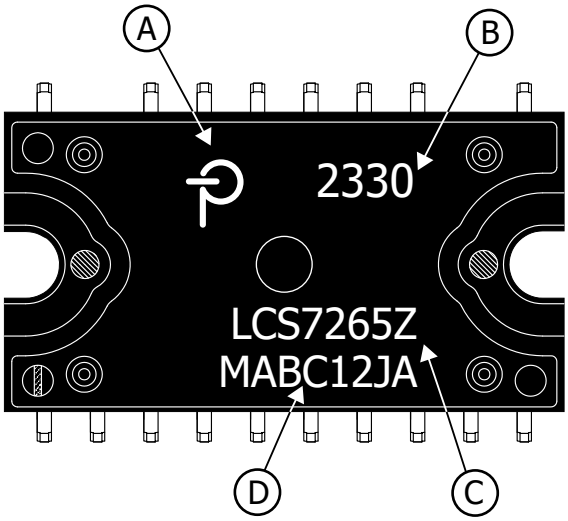
PI-9310-021121

Part Ordering Information



PACKAGE MARKING

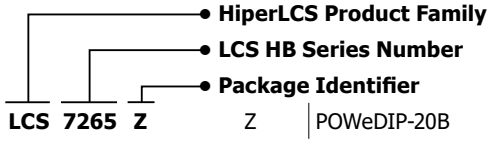
POWeDIP-20B



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Number

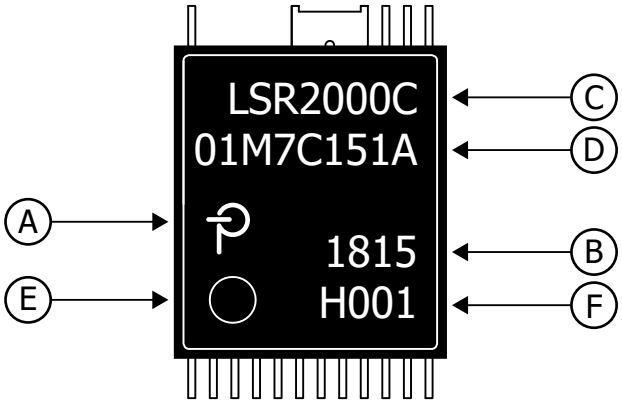
PI-9718-102423

Part Ordering Information



PACKAGE MARKING

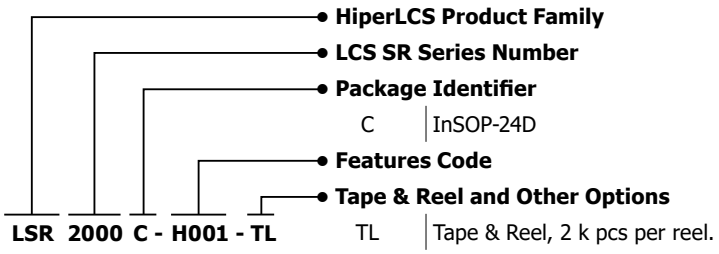
InSOP-24D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Pin 1 Indicator
F. Features Code

PI-9311-021621

Part Ordering Information



Feature Code	Frequency Range	Nominal Frequency	Burst Mode
H001	0	90 kHz	See Table 6
H002	1	120 kHz	See Table 6
H003	2	180 kHz	See Table 6
H004	3	240 kHz	See Table 6
H005	3	240 kHz	<2%

MSL Table

Part Number	MSL Rating
LCS7260C	3
LCS7262C	3
LCS7265C	3
LSR2000C	3

Part Ordering Information

Part Number	Option	Quantity
LCS7260C	Reel	2000
LCS7262C	Reel	2000
LCS7265C	Reel	2000
LCS7265Z	Tube	25
LCS7268Z	Tube	25
LCS7269Z	Tube	25
LSR2000C-H001	Reel	2000
LSR2000C-H002	Reel	2000
LSR2000C-H003	Reel	2000
LSR2000C-H004	Reel	2000
LSR2000C-H005	Reel	2000

Revision	Notes	Date
B	Production release.	03/21
C	Updates.	03/22
D	Updates including adding error codes.	11/22
E	Added H005 codes.	07/23
F	Production release of POWeDIP.	01/25

For the latest updates, visit our website: www.power.com

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

Life Support Policy

POWER INTEGRATIONS PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Worldwide: +1-65-635-64480
Americas: +1-408-414-9621
e-mail: usasales@power.com

China (Shanghai)
Rm 2410, Charity Plaza, No. 88
North Caoxi Road
Shanghai, PRC 200030
Phone: +86-21-6354-6323
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2, Keji Nan
8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
e-mail: chinasales@power.com

Germany
(AC-DC/LED/Motor Control Sales)
Einsteinring 24
85609 Dornach/Aschheim
Germany
Tel: +49-89-5527-39100
e-mail: eurosales@power.com

Germany (Gate Driver Sales)
HellwegForum 3
59469 Ense
Germany
Tel: +49-2938-64-39990
e-mail: igbt-driver.sales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI) Italy
Phone: +39-024-550-8701
e-mail: eurosales@power.com

Japan
Yusen Shin-Yokohama 1-chome Bldg.
1-7-9, Shin-Yokohama, Kohoku-ku
Yokohama-shi,
Kanagawa 222-0033 Japan
Phone: +81-45-471-1021
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
e-mail: taiwansales@power.com

UK
Building 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge
CB4 1YG
Phone: +44 (0) 7823-557484
e-mail: eurosales@power.com