Design Example Report

Title	**720 W 60 V 12 A Power Factor Corrected LLC PSU with CV and CC Modes and Uses HiperLCS™2-HB LCS7268Z, HiperLCS™2-SR LSR2000C-H005 and HiperPFS™-3 PFS7539H**
Specification	180 VAC – 280 VAC Input; 60 V, 12 A Output
Application	2-wheeler EVs and Tool Chargers
Author	Applications Engineering Department
Document Number	DER-984
Date	February 27, 2025
Revision	A

Summary and Features

- Integrated PFC and LLC stages, self biased in startup for low component count
- Precise control of both SR and HB to optimize efficiency
- High frequency (up to 360 kHz) LLC for small transformer size
- Boost PFC input stage, PF >0.99
- Accurate constant Battery current (CC) regulation, ±5%
- Accurate constant Battery voltage (CV) regulation, ±1%
- 94% full load efficiency at 230 VAC
- External CC/CV control option
- Wide output battery voltage range: 26 VDC to 60 VDC
- Wide output battery current range: 0 A to 12 A

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer to provide the AC input to the prototype board.
Since there is no separate bias converter in this design, ~400 VDC is present on bulk capacitor C40 and C49 immediately after the supply is powered down. For safety, this capacitor must be discharged with an appropriate resistor (10 k / 2 W is adequate), or the supply must be allowed to stand ~10 minutes before handling.

1 Introduction

This engineering report describes a Constant Voltage (CV) and Constant Current (CC) 2-wheeler EV and power tool charger using a Power Factor Corrected (PFC) AC-DC converter and an isolated LLC converter. It contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, design spreadsheet and performance data.

CC and CV control are provided by a daughter card that provides external bias to the Feedback pin of the Synchronous rectification controller (LSR2000). The report examines the operation of the power converter using a HiperPFS-3 PFC IC and the HiperLCS-2 LLC + SR chipset. The daughter board provides a facsimile of an OEM charger.

The highline-only HiperPFS-3 (PFS7539H) IC is a CCM boost PFC controller and switcher IC that provides unity PF across input voltage range of 180 to 280 VAC. The feedback resistors on the FB pin (Pin 7) of the PFS7539H are selected to deliver a regulated 400 VDC output.

The HiperLCS2-HB LCS7268Z resonant half-bridge switcher IC uses the POWeDIP high power package.

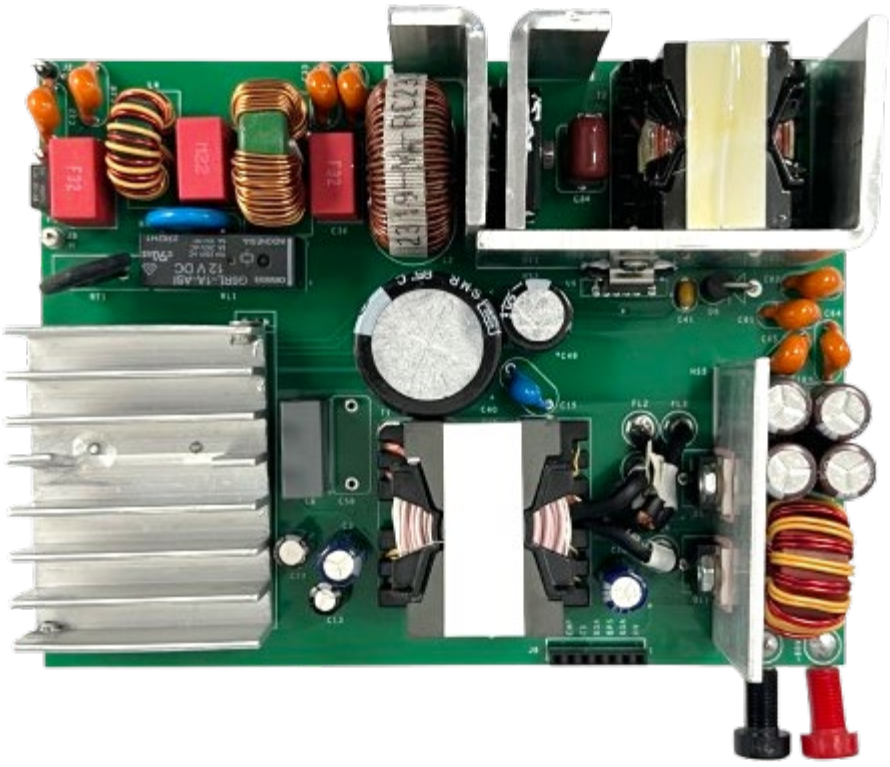


Figure 1 – DER-984 Populated Power Converter Board, Top View

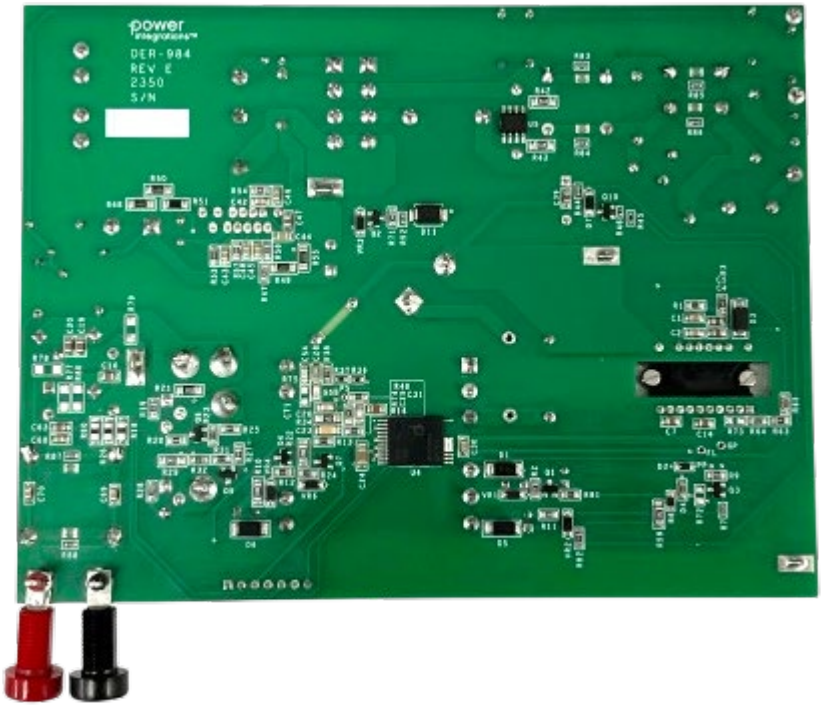


Figure 2 – DER-984 Populated Power Converter Board, Bottom View

Figures 1 and 2 show the main circuit board containing the HiperPFS-3 and HiperLCS-2 chipset devices. A vertical PQ3535 transformer is mounted on the top side of the main board. The secondary IC LSR2000C is located on the bottom side of the main board, behind the transformer. Two rectifier bridges are used in parallel, for better thermal performance. The board has heatsinks mounted on it to cool the parallel input bridge rectifiers, the PFS7339H IC, the LCS7268Z IC and the secondary-side synchronous rectifier MOSFETs.

The daughter card is a small detachable PCB, containing the control circuit to provide the bias signal to the main circuit board. The mode selection of CV or CC is made using a combination of Single-pole Double Throw (SPDT) and Double-pole Double Throw (DPDT) switches. The reference operating point for CV or CC, is set using variable resistors. Voltage/current feedback is obtained from the main circuit board and the error is processed via the analog PI controller. The output from the PI controller is provided to the Feedback pin (pin 7) of U2 (HiperLCS secondary IC LSR2000C). Figures 3 and 4 show the assembled daughter card, and switch positions for CC and CV mode.

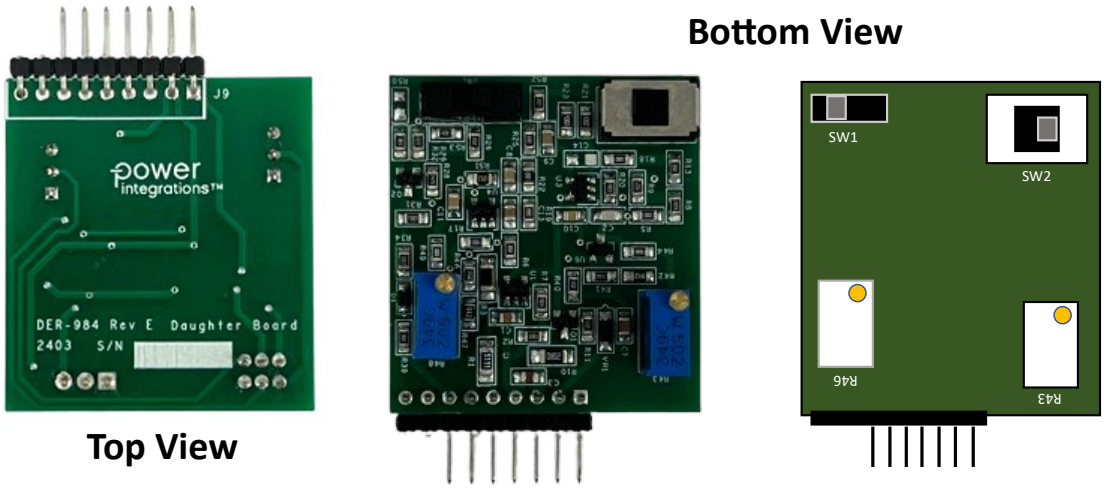


Figure 3 – Populated Daughter card with the switch positions for CC Mode of the converter.

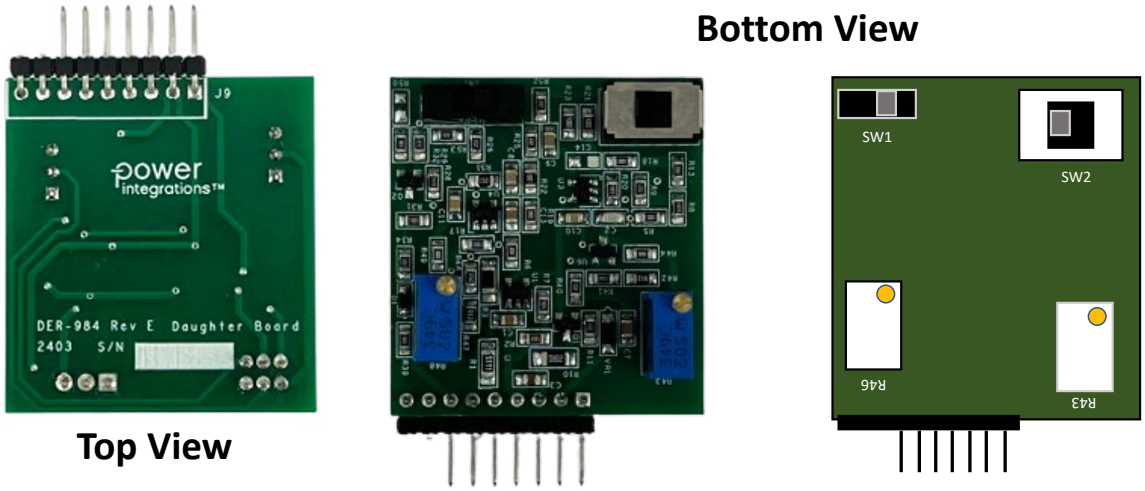


Figure 4 – Populated Daughter card with the switch positions for CV Mode of the converter.

2 Power Supply Specification

The table below represents the typical acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$\mathbf{V_{IN}}$	180	230	280	VAC	Single phase input
Frequency	$\mathbf{f_{LINE}}$	47	50/60	64	Hz	
Power Factor	**PF**	0.9				Full Load, 230 VAC.
Main Converter Output						
Output Voltage	$\mathbf{V_{LG}}$	30	60		V	(720 W) Full Load.
Output Current	$\mathbf{I_{LG}}$		12		A	
Total Output Power						
Continuous Output Power	$\mathbf{P_{OUT}}$		720		W	
Power Supply Efficiency						
			92.9			Measured at 180 VAC, Full Load.
Full Load 60 V / 12 A.	η_{Main}		94.1		%	Measured at 230 VAC, Full Load.
			94.5			Measured at 280 VAC, Full load.
No Load Input Power						Measured at 280 VAC.
Total System No-Load Consumption for 60 V output	$PIN_{No\text{-}Load}$		712		mW	Includes loading provided by CV/CC Daughter card
Ambient Temperature	$\mathbf{T_{AMB}}$	0		40	°C	See Thermal Section for Conditions.

3 Schematic

The schematic for the main board and daughter card are shown in Figures 5, 6, 7 and 8:

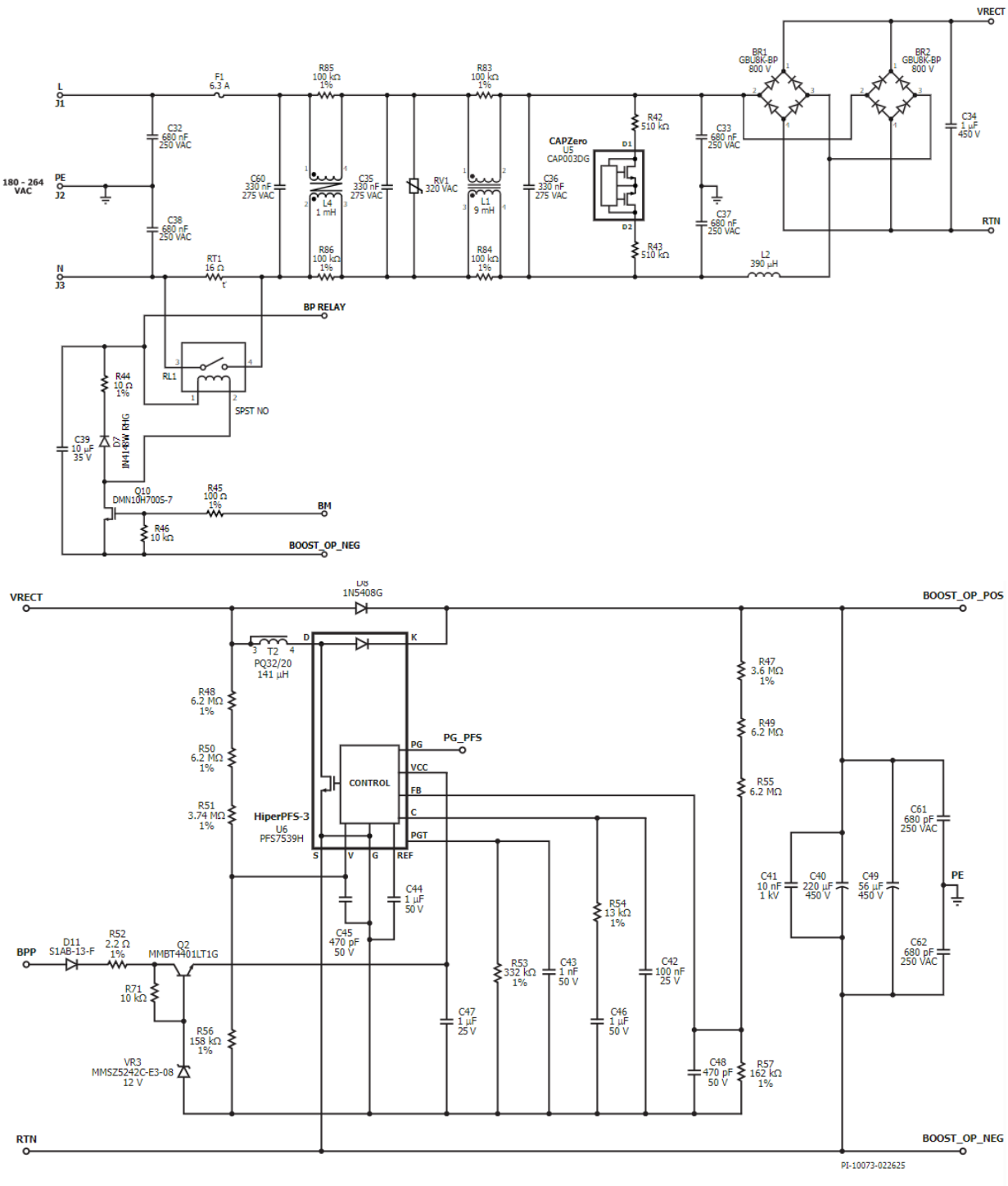


Figure 5 – Input Filter, Bridge Rectifier, and PFC stage

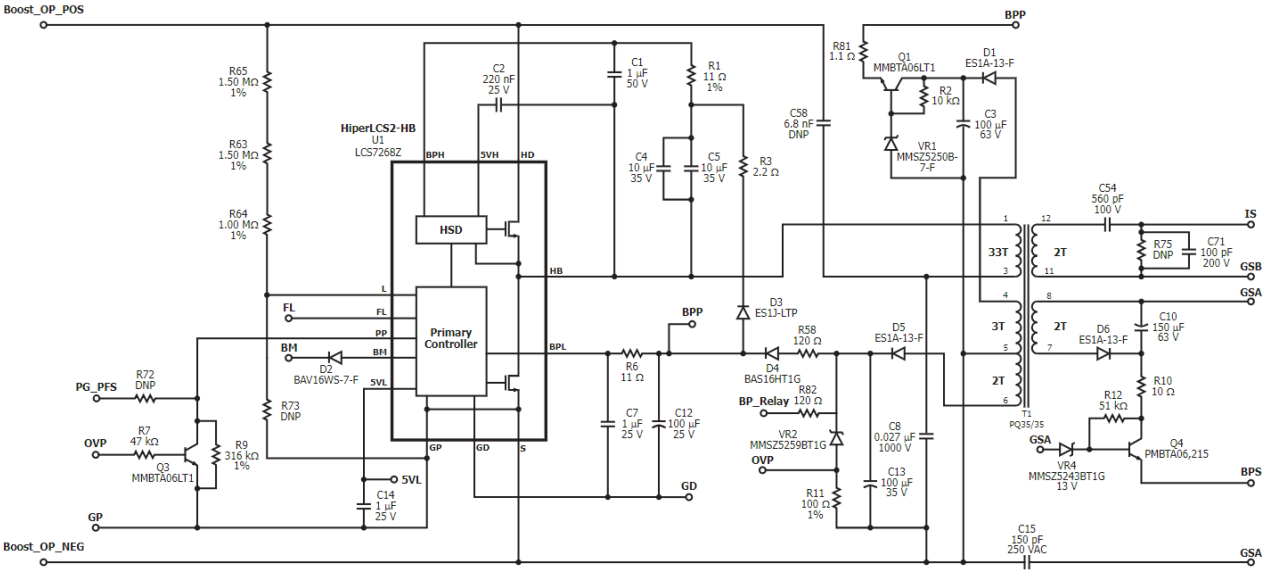


Figure 6 – LLC Stage (Primary Side)

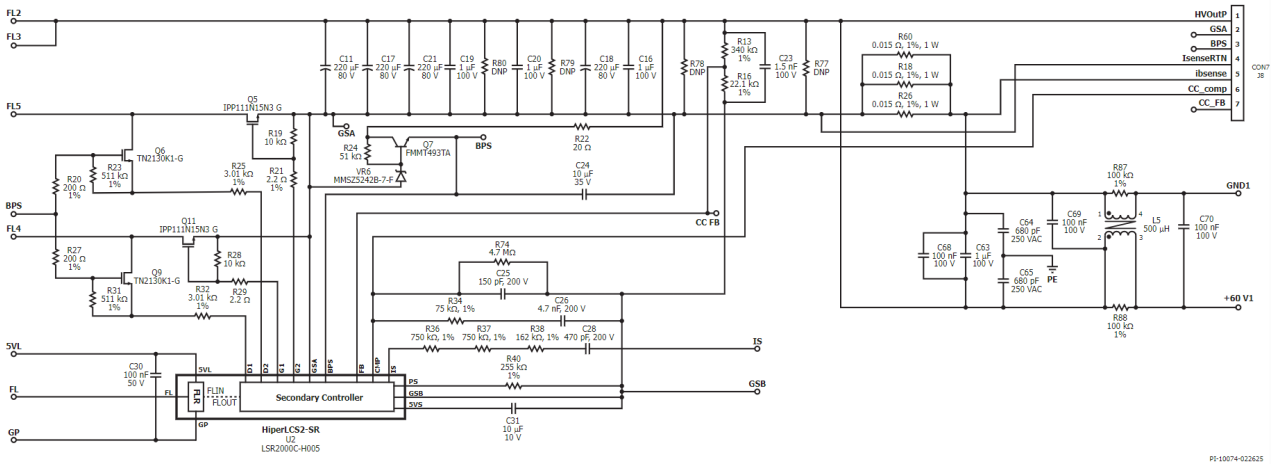


Figure 7 – LLC Stage (Secondary Side)

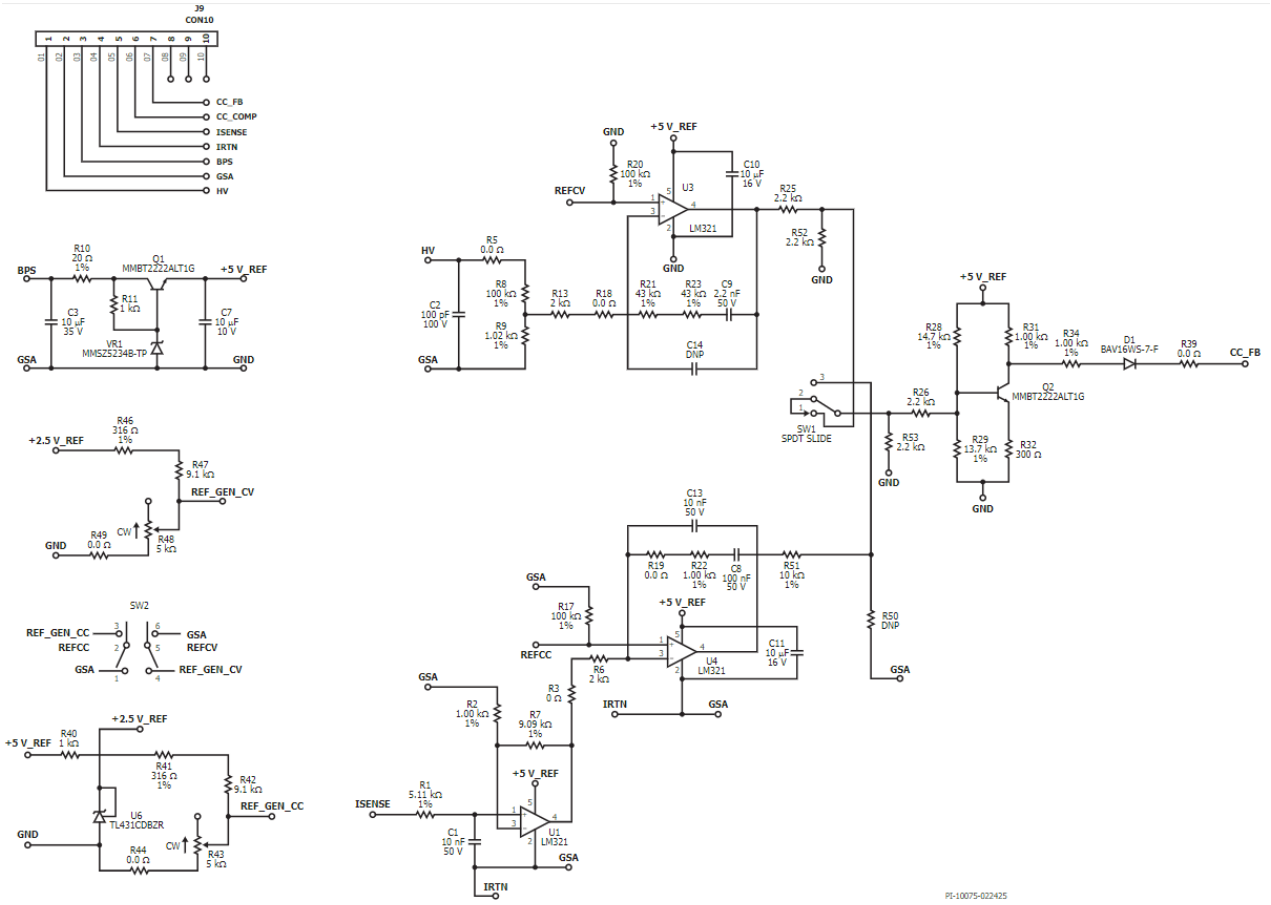


Figure 8 – CV/CC control daughter board

4 Circuit Description

4.1 EMI Filtering / Rectifier Stage

Figure 5 shows the schematic of the EMI and rectifier stage. Fuse F1 protects in case of a primary overcurrent fault/failure. A 16 Ω thermistor RT1 is used to limit inrush current during start-up. Varistor RV1 protects against differential mode line surge. Inductors L1 and L4 along with C32 and C38 are used to control common mode noise, while C35, C36, C60, and L2 are reduce differential mode noise. Resistors R42 and R43 are connected to the integrated X-capacitor discharge IC U5 and quickly reduce the voltage across C35, C36, and C60 to safe levels when the PSU is disconnected from the AC mains. AC input is rectified through bridge diodes BR1 and BR2. Relay RL1 is used to bypass thermistor RT1 after initial start-up. Its operation is controlled by the BM pin on HiperLCS2-HB (U1). When significant load is drawn from the main output, the BM pin will transition from low to high and turn-on Q10. This allows current to flow through the coil of RL1 which causes the shorting out RT1 to maximize efficiency. During very light loads or the no load condition, BM will transition from high to low, de-energizing RL1 to reduce power consumption.

4.2 Main PFC Stage

Figure 5 also shows the PFC stage centered around the HiperPFS-3 controller (U6). T2 is the PFC choke. D8 is a bypass diode used to pre-charge bulk capacitors (C40 & C49) and an inrush current path for when AC is first applied. A resistor divider comprised of R47, R49, R55, and R57 provide output voltage feedback to U6. Capacitor C48 decouples FB pin of U6. Components R54, C42, and C46 are for loop compensation, while resistors R48, R50, R51, and R56 provide input voltage information to U6. Capacitor C44 is used to program U6 to support either Full power or Efficiency modes via the REF pin. Resistor R53 which via the PGT pin sets the bulk voltage level at which the PG pin will enter a high impedance state to signal the DC-DC stage to turn off when the bulk voltage is low. However, for this design, L-pin of HiperLCS2-HB is used for start-up instead of PG pin signal.

4.3 LLC Converter

Figure 6 shows the primary power section of the LLC converter using the HiperLCS2-HB switcher IC. Figure 7 shows the secondary section of the LLC converter using HiperLCS2-SR, a secondary master controller with secondary-primary communication that includes integrated safety rated isolation, and a synchronous rectification driver stage.

4.4 LLC Primary

The high-voltage input bus is filtered by capacitors C40 and C49. Line sense (L-pin) detects input bus voltage via resistors (R63, R64, and R65). The HiperLCS2-HB IC, U1, will initiate

soft-start when L-pin rises above UV+ threshold. Output overvoltage is sensed from the primary bias-winding (pins 5 and pin 6) of transformer T1, via Zener diode VR2 and resistor R11 and coupled to the PP pin via resistor R7 and transistor Q3. If an output overvoltage occurs, Zener VR2 conducts and current will be pulled from the PP pin to ground via transistor Q3 and switching is interrupted. In normal operation, resistor R9 sets the PP pin primary frequency range and determines fault-response. Diode D2 couples the BM pin to an external in-rush relay drive circuit to switch out the soft-start circuit in normal operation. Note: BM transitions to a low state when in light load burst mode.

Capacitors C14 and C7 decouple the 5VL and BPL pins referencing them to GP and GD pins respectively. The primary return power-ground, RTN, is connected to the S-pin (SOURCE), primary-bias winding and bias capacitor. The RTN ground is Kelvin connected to the node formed by the negative-pins of bulk-capacitors C40 and C49. It is important to keep the small signal ground (GP), separate from system power-ground (RTN). The RTN power-ground offers a low-impedance path for system noise, allowing secondary-coupled noise currents to be safely delivered to the RTN/bulk-capacitor ground without disturbing the small-signal ground (GP pin).

Diode D5 rectifies primary bias winding voltage. Capacitor C13 provides energy storage and capacitor C7 provides local high-frequency decoupling for the BPL-pin. During start-up, before switching commences, the BPL pin charges capacitors C7 and C12 via resistor R6. The resistor limits output current from the BPL pin. Capacitor C12 provides sufficient energy storage to sustain startup prior to the primary bias winding becoming energized which only occurs once switching begins. C12 also provides boot-strap energy to the HiperLCS2-HB high-side bias via diode D3 and resistor R3. Capacitor C12 must be large enough to provide the necessary bias energy during startup. As a guide, the capacitance of C12 should be approximately 5x the sum of the capacitance of high-side bias capacitor C4 and C5.

Resistor R6 limits output current draw from the BPL by the PFC stage. Diode D4 is a blocking diode to prevent the charge current supplied by the BPL pin from being diverted to capacitor C13. During normal operation the bias current flows from the bias winding to capacitor C13. The BPL-pin has an internal shunt regulator to limit the BPL pin voltage. Resistor R58 limits the BPL shunt-current when BPL shunt-voltage-clamping is active, limiting BPL power dissipation.

For best no-load performance, the bias should be designed to deliver a minimum of 15 V at the BPL pin. The BPL shunt will engage if the bias voltage at the BPL pin exceeds 21 V. The bias winding voltage may vary up to 25% when the output load changes from zero to full load. Careful attention should be paid to choosing the appropriate steady state bias-winding voltage. If voltage is above BPL clamp threshold, it will cause additional power dissipation in the BPL circuitry and can induce thermal shutdown of the HiperLCS2-HB IC.

During the on-period of the low-side power MOSFET, the high-side bootstrap is charged via diode D3 and resistor R3 feeding capacitors C4 and C5. For the first few switching cycles at startup, capacitors are uncharged C4 and C5 and resistor R3 is required to limit current. Resistor R1 and capacitor C1 provide additional low-frequency filtering for the BPH pin. The high-side 5VH pin is decoupled via capacitor C2. Note that all high-side decoupling is tied to the HB pin.

The resonant tank transformer T1 is the sum of inductance L_R (transformer-integrated resonant inductor) and magnetizing inductance, L_M, which appear in series between the HB pin and the node formed by the junction of capacitors C13 and C58.

Y-capacitor C15 provides decoupling between primary and secondary grounds to reduce common mode noise.

4.5 LLC Secondary

The HiperLCS2-SR (U2) IC has primary side pins that are safety-isolated from the secondary side. Pin 5VL on the primary side of the HiperLCS2-SR is connected to the 5V reference provided by the 5VL pin on the HiperLCS2-HB IC. This connection provides power for the primary-side of the HiperLCS2-SR IC. The GP pin on the HiperLCS2-SR IC couples to the primary small signal ground pin of the HiperLCS2-HB IC. Capacitor C30 provides local decoupling to the 5VL and GP pins of U2. The FL pin provides a control signal generated by the master controller on the secondary-side of the HiperLCS2-SR IC which is passed across the isolation barrier to the primary-side via the integrated FluxLink magneto inductive communication link. This control signal is delivered to the HiperLCS2-HB IC.

Transformer output pins T1 FL2/FL3 provide the positive output voltage, which is rectified by SR MOSFETs Q11 and Q5, and filtered by capacitors C11, C16, C17, C18, C19, C20, C21, and C23. These capacitors have low combined ESR, which is the predominant factor in determining output ripple. Their combined capacitance should be chosen to provide the desired off-time in burst-mode. The capacitors are connected to the secondary-side power ground (GND).

Transformer output pins T1 FL4/FL5 provide the return path for synchronous rectifier MOSFETs Q11 and Q5 respectively. The secondary power path is from T1 FL2/FL3 through capacitors C11, C16, C17, C18, C19, C20, C21, and C23. To balance the two secondary power-phases, it is important to ensure that the secondary power path lengths of Q11 and Q5 are equal.

Capacitor C24 decouples the BPS pin, connecting it to the secondary SR-drive ground (GSA pin). Capacitor C31 decouples the 5VS pin connecting it to the secondary small signal ground (GSB pin).

Diode D6 and capacitor C10, rectify and filter the output from the secondary bias winding of T1 appearing on pin 7 (with respect to output power ground GND). Components Q4, R12 and VR4 act as voltage regulator to provide a regulated 12.5 V to the BPS pin. 12.5 V was chosen to ensure that during nominal output voltage, the secondary bias winding will provide current to BPS pin. Components Q7, R24, R22 and VR6 take the energy from the output voltage and support the BPS pin during output voltage operation. Zener diode VR6 is chosen with a typical voltage of 12 V to ensure the circuit only operates when there is insufficient energy from the transformer bias winding. It is also acts as fast start-up circuit to provide initial bias to the BPS pin (while there is not enough voltage developed across the bias winding) to wake-up U2 and prevent output overshoot during start-up.

The small signal secondary ground GSB is used for feedback and compensation and provides the ground for IS-pin signals. Output voltage is sensed via resistors R13 and R16 with local capacitor decoupling via C23 to GSB (small-signal secondary ground) which attenuates any high-frequency noise. The voltage feedback resistor-divider network is scaled to provide 3.75 V at the FB pin of the secondary IC when the DC output voltage is 61 V. The FB pin is also biased by the analog controller on the daughter board. The current sensing resistors R60, R18, and R26 develop a voltage drop that is proportional to the output DC current. This voltage is used by the analog controller when providing current control. Compensation is provided between CMP and GSB pins, via R34, C25 and C26 which provide a pole (R13, C26) and zero (R34, C26) and a high frequency pole (R34, C25). Resistor R74 is connected across C25 to bleed a small amount of current to ensure VFB(REF) is always slightly lower than VFBREG(TH), this prevents switching frequency locking into Fmax. The transformer IS winding T1 output that appears on pin 12 (the return is provided by T1 pin 11 which is grounded to GSB secondary small-signal ground) provides information that together with capacitor C54 that sets the burst threshold for low load. This signal is coupled via C28 and resistors R36, R37, and R38 to the IS pin of U2. C54 and C71 acts as capacitor divider network to reduce the current going into the IS pin.

Drive for the Q11 and Q5 synchronous MOSFETs is driven by the output pins G1 and G2 pins via resistors R29 and R21 respectively. The drive resistors are optional but may be required to reduce high-frequency ringing. In the event of an FMEA open-connection between G1/G2 and Q11/Q5 gate, local pull-down resistors R28 and R19 ensure that Q11 and Q5 remain off.

There is a maximum pin voltage of 150 V for D1 and D2 pins. Q9 and Q6 protect these pins from possible overvoltage. Pins D1 and D2 sense the drain voltages on the synchronous rectifiers Q11 and Q5 via resistors R32 and R25 and FETs Q9 and Q6, respectively. The resistors limit negative current (WRT GND) into both pins. These resistor values can be increased to adjust the SR turn-off threshold. Increasing the resistor value will cause synchronous rectification to end at a higher current. Q9 and Q6 conduct when there is zero drain voltage on Q11 and Q5. Note: D1 and D2 signal paths go through resistors R32 and R25, drain-source of Q9 and Q6 and through the SR-MOSFETs (Q11, Q5)

respectively after which both are returned to GSA. The total path length for both D1 and D2 signals should be equal, to ensure optimal SR operation.

The PS pin resistor R50 is used to program the burst threshold and CV/CC modes.

4.6 CV/CC Control

The daughter board receives energy from the BPS via connector J9 (pin 3). A +5 V reference voltage is used by the analog circuitry on the daughter card. The reference voltage is generated by R10, Q1 and VR1. The Gate clamping Zener VR1 has a typical voltage of 6.2 V.

The daughter board has two variable resistances R43 and R48. R40 and voltage regulator U6 are used to generate a +2.5 V. From this 2.5 V signal, the reference for the current control circuit is generated using the resistive divider network of R41, R42 and R43. Potentiometer R43 is adjusted to provide a voltage of ~600 mV, when the power supply output current is 12 A. The voltage across R43 acts as the reference to the current control circuit. The resistive divider R46, R47 and R48 are used to generate a reference voltage for the voltage control circuit. The potentiometer R48 is adjusted to generate ~600 mV when the power supply output voltage is 60 V. A Double Pole Double Throw (DPDT) switch (SW2) is used to pass only one reference to the analog control circuit. When the CV mode is selected, the voltage across R48 is provided as a reference to the voltage controller. The "ground" signal is provided as a reference to the current controller. This arrangement prevents input from the current feedback in CV mode. When the CC mode is selected, the voltage across R43 is provided as a reference to the current controller.

Current control is realized using the Op-Amp U4, plus resistors R6, R19, R22, C8 and C13. The capacitor C13 improves dynamic response, the gain of the controller being set by the resistors. The output voltage of the controller varies between 5 V and zero. The resistors R51, R50 and R53 adjust the influence of the current controller on the output inverter stage.

The voltage controller is realized using the Op-Amp U3, resistors R13, R21, R23, C9 and C14. Capacitor C14 improves dynamic response with gain being set by the resistors. The output voltage of the controller varies between 5 V and zero, and drives the base of the transistor Q2 via resistor R26.

The Single Pole Double Throw (SPDT) switch (SW1) is used to pass only one controller output to the inverter stage. The transistor-based inverter is realized using the resistors R31, R32, R28, R29, R26 and NPN transistor Q2. The bias operating point is set by R28 and R29. R34 is used to adjust voltage gain of the inverter. Diode D1 ensures unidirectional flow of current into the FB pin of the secondary control IC U2.

5 PCB Layout

Figure 9 shows the main and daughter Printed Circuit Boards (PCBs) used for the power supply.

PCB specifications for the main and daughter boards:

- Layer count: 2 layers
- Solder mask: Green
- Silkscreen: White
- Finish: LF HASL
- Board thickness: 1.6 mm
- Copper thickness: 2 oz (2.8 mils)
- Material: FR4

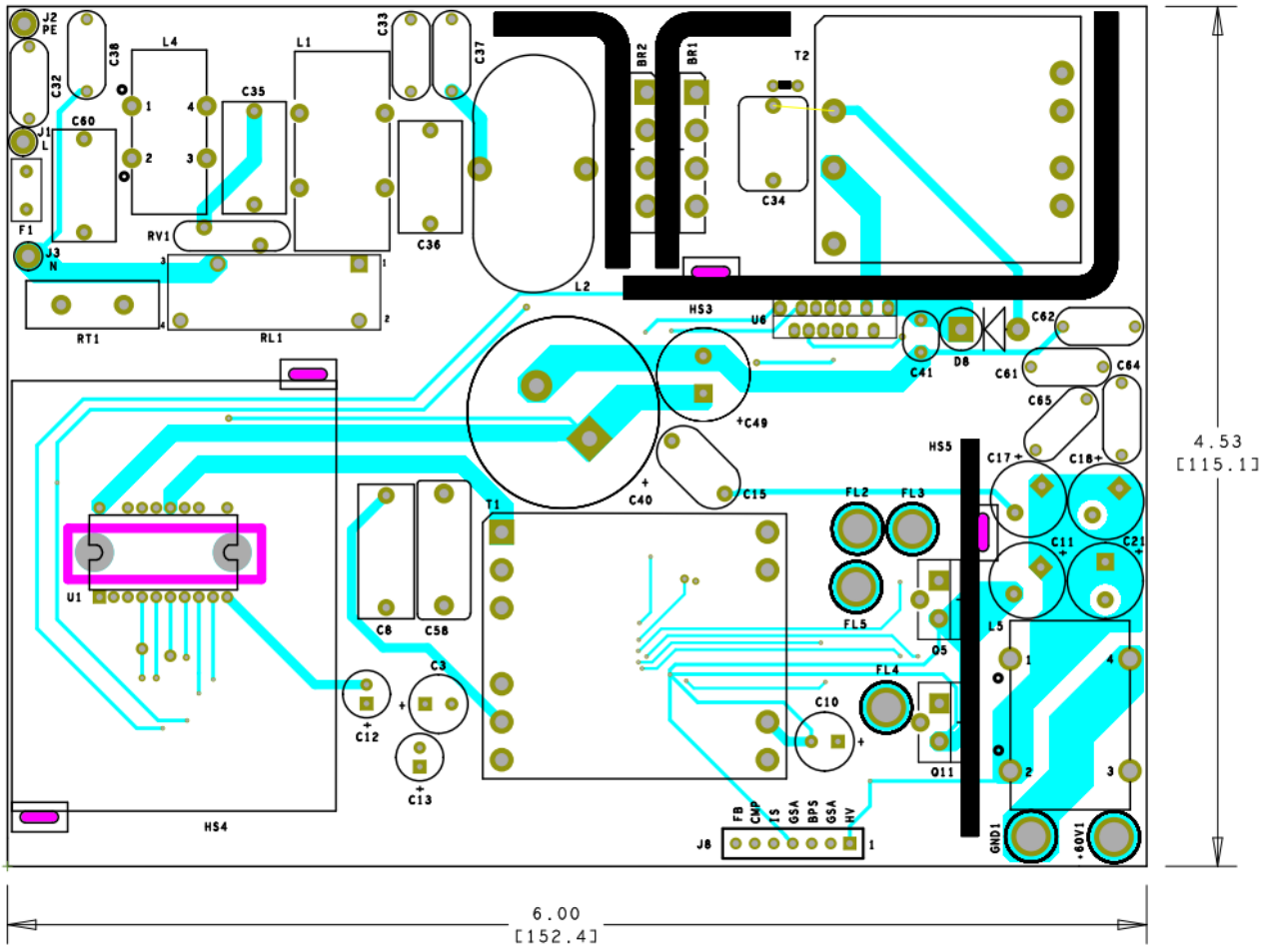


Figure 9 – Main Board, Top Side PCB.

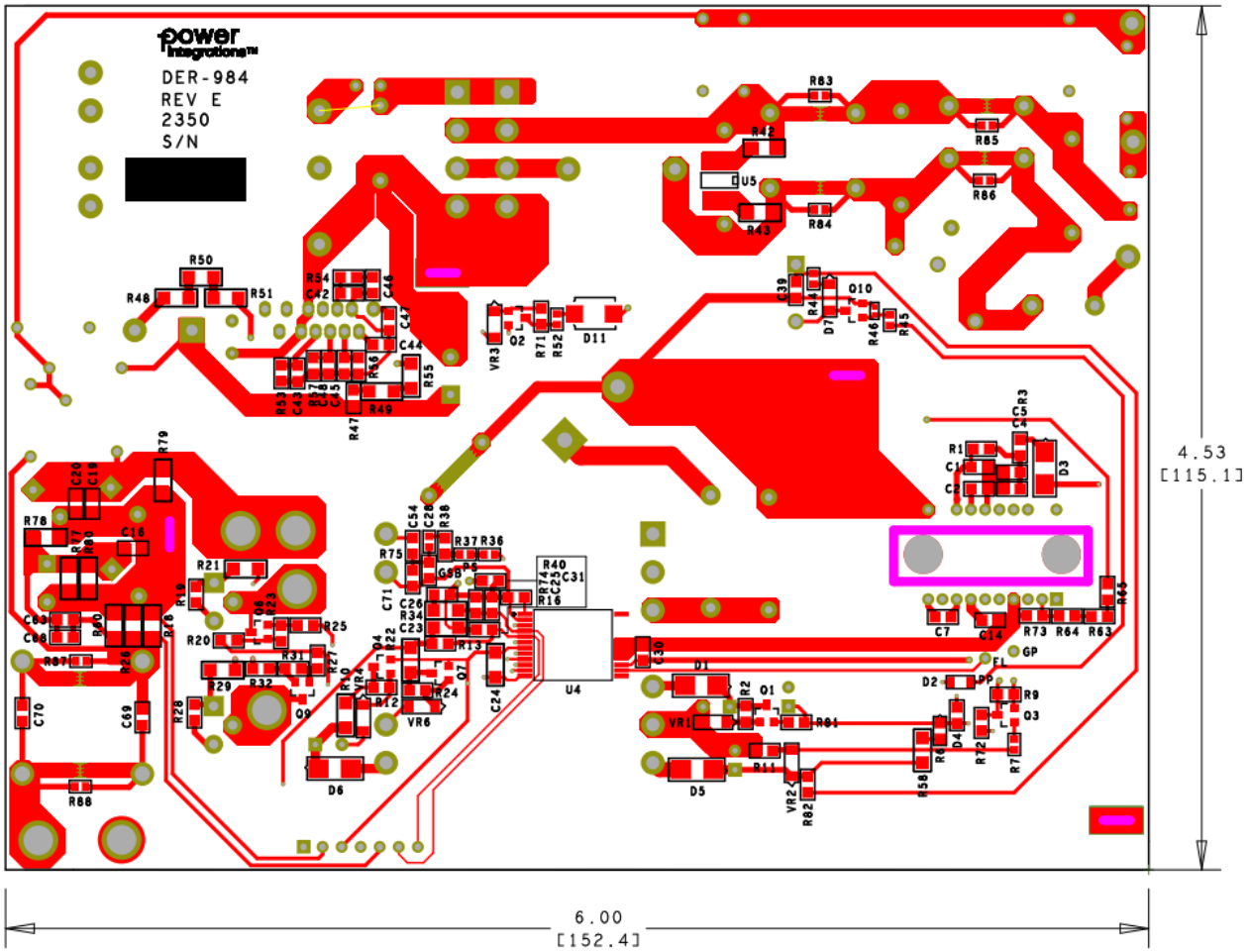


Figure 10 – Main Board, Bottom Side PCB.

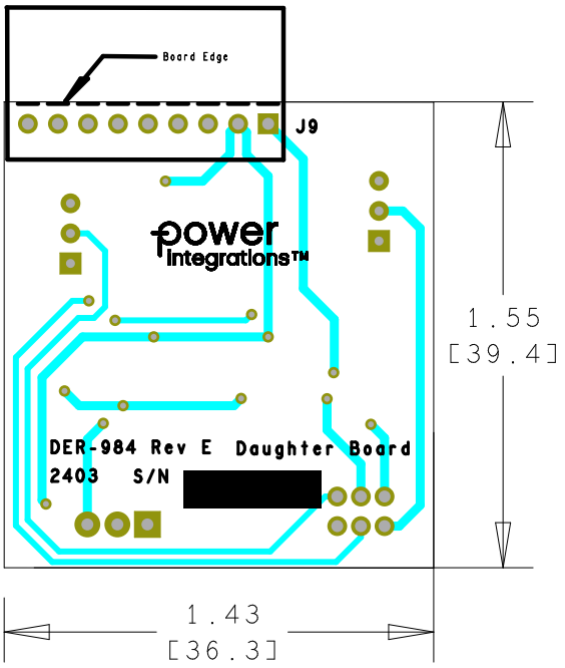


Figure 11 – Daughter Board, Top Side PCB.

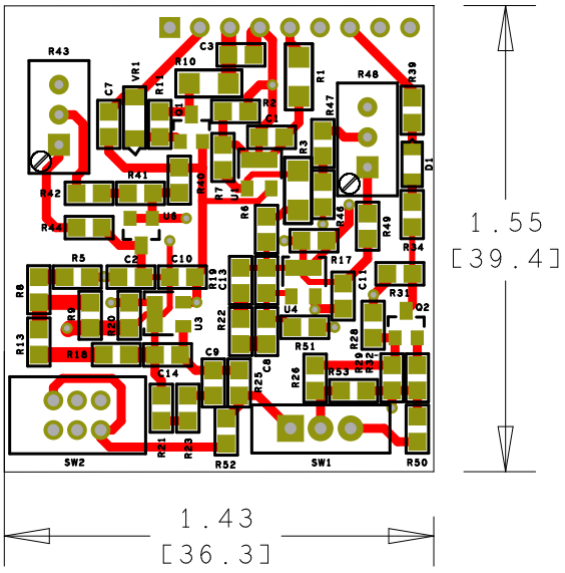


Figure 12 – Daughter Board, Bottom Side PCB.

6 Bill of Materials

6.1 Main Board Electrical Parts

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	2	BR1 BR2	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial Co.
2	2	C1 C46	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX Corporation
3	1	C2	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
4	1	C3	100 µF, 63, Electrolytic, Low ESR, 270 mOhm, (8 x 15)	ELXZ630ELL101MH15D	Nippon Chemi-Con
5	3	C4 C5 C39	10 µF ±10% 35 V Ceramic Capacitor X5R 0805 (2012 Metric)	C2012X5R1V106K125AC	TDK Corporation
6	2	C7 C14	1 µF, ±10%, 25 V, Ceramic, X7R, 0805 (2012 Metric)	GCM21BR71E105KA56L	Murata Electronics North America
7	1	C8	0.027 µF, ±5%, Film Capacitor, 600 VAC 1000 VDC (1 kV), Polypropylene (PP), Metallized Radial	R76QI227050H4J	KEMET
8	1	C10	150 µF, 63, Electrolytic, Low ESR, 210 mOhm, (8 x 20)	ELXZ630ELL151MH20D	Nippon Chemi-Con
9	4	C11 C17 C18 C21	220 µF, 80 V, 20%, Aluminum, Radial, Can, 10000 Hrs @ 105 °C, (10 x 26.5, 5 mm LS)	EKZN800ELL221MJ25S UCY2D391MHD9	United Chemi-Con
10	1	C12	100 µF, 25 V, Electrolytic, Very Low ESR, 130 mOhm, (6.3 x 11)	EKZE250ELL101MF11D	Nippon Chemi-Con
11	1	C13	100 µF, 35 V, Electrolytic, Gen Purpose, (6.3 x 12.2)	ECA-1VHG101	Panasonic
12	1	C15	150 pF, 250 VAC, Film, X1Y1	CD70-B2GA151KYNS	TDK
13	4	C16 C19 C20 C63	1 µF, 100 V, Ceramic, X7S, 0805	C2012X7S2A105K125AB	TDK Corp
14	1	C23	1.5 nF, 100 V, Ceramic, X7R, 1206	12061C152KAT2A	AVX Corp
15	1	C24	10 µF, ±10%, 35 V, Ceramic, X7R, 1206 (3216 Metric)	GMJ316BB7106KLHT	Taiyo Yuden
16	1	C25	150 pF, 5%, 200 V, Ceramic, COG, NP0, -55 °C ~ 125 °C, 0805 (2012 Metric)	08052A151JAT2A	AVX Corp
17	1	C26	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX Corp
18	1	C28	470 pF, 200 V, Ceramic, X7R, 0603	06032C471KAT2A	AVX
19	1	C30	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
20	1	C31	10 µF, ±10%, 10V, Ceramic Capacitor, Soft Termination, X7R, 0805 (2012 Metric)	C2012X7R1A106K125AE	TDK Corp
21	8	C32 C33 C37 C38 C61 C62 C64 C65	680 pF, Ceramic, Y1	440LT68-R	Vishay
22	1	C34	CAP, FILM, 1.0 µF, 10%, 450 VDC, RADIAL	ECW-FD2W105Q1	Panasonic
23	3	C35 C36 C60	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.0 mm x 8.50 mm	890324024003CS	Wurth Electronics Inc.
24	1	C40	220 µF, 450 V, Electrolytic, SMR SNAP (25.4 x 30)	ESMR451VSN221MQ30S	United Chemi-con
25	1	C41	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX Corp
26	1	C42	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX Corp
27	1	C43	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX Corp
28	1	C44	1 µF, ±10%, 50 V, Ceramic, X7R, 0805 (2012 Metric)	CL21B105KBFNNNE	Samsung Electro-Mechanics
29	2	C45 C48	470 pF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB471	Yageo
30	1	C47	1 µF, 25 V, Ceramic, X5R, 0805	C2012X5R1E105K	TDK
31	1	C49	56 µF, 450 V, Electrolytic, (12.5 x 30)	450LXW56MEFR12.5X30	Rubycon

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
32	1	C54	680 pF 200 V X7R MULTI-LAYER CERAMIC +/- 10 %	C0805C681K2RACAUTO	Kemet
33	1	C58*	6.8 nF, 1600 V, Film	B32652A1682J	Epcos Ind
34	3	C68-C70	100 nF 100 V 10 % X7R 0805	C0805C104K1RACTU	Kemet
35	1	C71	100 pF, ±10%, 200 V, Ceramic, C0G, NP0, 0805 (2012 Metric)	C0805C101K2GACAUTO	KEMET
36	3	D1 D5 D6	50 V, 1 A, General Purpose, DO-214AC	ES1A-13-F	Diode Inc.
37	1	D2	75 V, 0.15 A, Switching, SOD-323	BAV16WS-7-F	Diode Inc.
38	1	D3	600 V, 1 A, Super Fast, 35 ns, DO-214AC, SMA	ES1J-LTP	Micro Commercial Co.
39	1	D4	75 V, 200 mA, Rectifier, SOD323	BAS16HT1G	ON Semiconductor
40	1	D7	DIODE, GEN PURP, 100 V, 150 MA, SOD123, SOD-123F	1N4148W RHG	Taiwan Semiconductor Corporation
41	1	D8	1000 V, 3 A, Rectifier, DO-201AD	1N5408G	ON Semiconductor
42	1	D11	50 V, 1 A, Standard Recovery, GPP, SMB	S1AB-13-F	Diode Inc.
43	1	F1	FUSE BRD MNT 6.3 A 350 VAC 72 VDC	0697H6300-02	Belfuse
44	4	HS3-HS5 HS40	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	
45	1	L1	9 mH, 5 A, Common Mode Choke	T22148-902S P.I. Custom	Fontaine Technologies
46	1	L2	390 µH, 5 A, INDUCTOR TORD HI AMP	2319-V-RC	JW Miller
47	1	L4	1 mH, +/- 10%, Toroidal Common Mode Choke, custom, Wound on Toroid Core: PI# 32-00343-00	32-00448-00	Power Integrations
48	1	L5	500 µH, +/- 10%, Toroidal Common Mode Choke, custom, Wound on Toroid Core: PI# 32-00379-00	32-00449-00	Power Integrations
49	2	Q1 Q3	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1	Infineon Tech
50	1	Q2	NPN, Small Signal BJT, GP, 40 V, 600 mA, 250 MHz, 300mW, SOT-23, SOT-23-3 (TO-236)	MMBT4401LT3G	On Semiconductor
51	1	Q4	Bipolar (BJT) Transistor, NPN, 80 V, 500 mA, 100 MHz, 250 mW, Surface Mount TO-236AB, TO-236-3, SC-59, SOT-23-3, SOT-23	PMBTA06,215	Nexperia USA Inc.
52	2	Q5 Q11	150 V 83 A MOSFET N-CH TO220-3	IPP111N15N3 G	Infineon Technologies
53	2	Q6 Q9	MOSFET, N-Channel, 300 V, 85 mA (Tj), 360 mW (Tc), Surface Mount TO-236AB (SOT23)	TN2130K1-G	Microchip Technology
54	1	Q7	NPN, 100 V, 1000 Ma, SOT23-3	FMMT493TA	Diodes Inc
55	1	Q10	MOSFET, N-Channel 100 V 170 mA (Ta) 360 mW (Ta) Surface Mount PG-SOT23, TO-236-3, SC-59, SOT-23-3	BSS169H6327XTSA1	Infineon Technologies
56	1	R1	RES, 11 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF11R0V	Panasonic
57	4	R2 R19 R28 R71	RES, 10 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
58	1	R3	RES, 2.2 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R2V	Panasonic
59	1	R6	RES, 11 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ110V	Panasonic
60	1	R7	RES, 47 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
61	1	R9	RES, 316 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3163V	Panasonic
62	1	R10	RES, 10 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J100V	Panasonic
63	1	R11	RES, 100 Ohms ±1% 0.125 W, 1/8 W Chip Resistor, 0805 (2012 Metric), Thick Film	RMCF0805FT100R	Stackpole Electronics Inc

64	2	R12 R24	RES, 51 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ513V	Panasonic
65	1	R13	RES, 340 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3403V	Panasonic
66	1	R16	RES, 22.1 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2212V	Panasonic

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
67	3	R18 R26 R60	0.015 Ohm, ±1%, ±75 ppm/ °C, 1 W, 1206 (3216 Metric), Current Sense, -55 °C ~ 155 °C	ERJ-8CWFR015V	Panasonic Electronic Components America, Inc.
68	2	R20 R27	RES, 200 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2000V	Panasonic
69	1	R21	RES, 2.2 R, 1%, 1/4 W, Thick Film, 1206	RC1206FR-072R2L	Yago
70	1	R22	RES, 20 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J200V	Panasonic
71	2	R23 R31	RES, 511 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5113V	Panasonic
72	2	R25 R32	RES, 3.01 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3011V	Panasonic
73	1	R29	RES, 2.2 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J2R2V	Panasonic
74	1	R34	RES, 75 kOhms, ±1%, 0.25 W, 1/4 W, Chip Resistor 1206 (3216 Metric), Automotive AEC-Q200, Thick Film	CRCW120675K0FKTA	Vishay Dale
75	2	R36 R37	RES, 750 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF7503V	Panasonic
76	2	R38 R57	RES, 162 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1623V	Panasonic
77	1	R40	RES, 255 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2553V	Panasonic
78	2	R42 R43	RES, 510 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J514V	Panasonic
79	1	R44	RES, 10 Ohms, ±1%, 0.1 W, 1/10 W, Chip Resistor 0603 (1608 Metric), Moisture Resistant, Thick Film	RC0603FR-0710RL	Yageo
80	1	R45	RES, 100 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
81	1	R46	RES, 10 k, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ103X	Panasonic
82	1	R47	RES, 3.6 M, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ365V	Panasonic
83	4	R48-R50 R55	RES, 6.2 M, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
84	1	R51	RES, 3.74 M, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay Dale
85	1	R52	RES, 2.2 R, 1%, 1/16 W, Thick Film, 0603	ERJ-3RQF2R2V	Panasonic
86	1	R53	RES, 332 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3323V	Panasonic
87	1	R54	RES, 13.0 k, 1%, 1/8 W, Thick Film, 0805	RC0805FR-0713KL	Yageo
88	1	R56	RES, 158 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1583V	Panasonic
89	1	R58	RES, 120 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J121V	Panasonic
90	2	R63 R65	RES, 1.5 M, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1504V	Panasonic
91	1	R64	RES, 1.0 M, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1004V	Panasonic
92	1	R72*	RES, 18.2 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1822V	Panasonic
93	1	R73*	RES, 0 R, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole Electronics Inc
94	1	R74	RES, 4.7 M, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ475V	Panasonic
95	1	R75*	RES, 11.8 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1182V	Panasonic
96	4	R77-R80*	RES, 24.9 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2492V	Panasonic
97	1	R81	RES, 1.1 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ1R1V	Panasonic
98	1	R82	RES, 120 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ121V	Panasonic

99	6	R83-R88	RES, 100 kOhms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	RC0603FR-07100KL	Yageo
100	1	RL1	RELAY GEN PURPOSE SPST 8 A 12 V	G6RL-1A-ASI-DC12	OMRON
101	1	RT1	NTC Thermistor, 16 Ohms, 4 A	CL-70	Thermometrics
102	1	RV1	470 VAC, 4.5 KA, 14 mm, RADIAL	MOV-14D471K	Bourns
103	1	T1	Bobbin, PQ35/35, Vertical, 12 pins	BQ35/35-1112CPFR	TDK
104	1	T2	Bobbin, PQ32/20, Vertical, 12 pins	YC-PQ3220	Ying Chin
Item	**Qty.**	**Reference Designator**	**Description**	**Manufacturer Part Number**	**Manufacturer**
105	1	U1	HiperLCS2-HB, LCS7268Z, POWeDIP-20B	LCS7268Z	Power Integrations
106	1	U4	HiperLCS2-SR, LSR2000C-H005, InSOP-24D	LSR2000C-H005	Power Integrations
107	1	U5	CAPZero, CAP003DG,SO-8C	CAP003DG	Power Integrations
108	1	U6	HiperPFS-3, PFS7397H, eSIP-16C	PFS7539H	Power Integrations
109	1	VR1	DIODE ZENER 20 V 500 MW SOD123	MMSZ5250B-7-F	Diodes, Inc
110	1	VR2	DIODE ZENER 39 V 500 MW SOD123	MMSZ5259BT1G	ON Semi
111	1	VR3	Zener Diode, 12 V, ±2%, 500 mW, Surface Mount, SOD-123	MMSZ5242C-E3-08	Vishay General Semiconductor - Diodes Division
112	1	VR4	13 V, 5%, 500 mW, SOD-123	MMSZ5243BT1G	ON Semiconductor
113	1	VR6	DIODE ZENER 12 V 500 MW SOD123	MMSZ5242B-7-F	Diodes, Inc

* Do Not Populate (DNP), refer to schematic notes if need to populate

6.2 Main Board Mechanical Parts

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	1	HS41	SHTM, HEATSINK, DER-984, Al extrusion AAVID G2230, Custom		Custom
2	1	HS42	SHTM, HEATSINK, DER-984, AL, 3003, .090" Rev A		Custom
3	1	HS43	SHTM, HEATSINK, Bridge, Right Side, AL, 3003, 0.090", Custom. Created for Michael Madson for DER-984	61-00334-00	Custom
4	1	HS44	SHTM, HEATSINK, Bridge, Left Side, AL, 3003, 0.090", Custom. Created for Michael Madson for DER-984	61-00335-00	Custom
5	1	HS45	SHTM, HEATSINK, PFS17539H, DRW, DER-984, AL, 3003, 0.090", Custom. Created for Michael Madson for DER-984	61-00336-00	Custom
6	3	J1-J3	PCB Terminal Hole, 18 AWG	N/A	N/A
7	1	J8	7 Position (1 x 7) Female header, 0.1 pitch, 00.126" (3.20 mm), Vertical, Au	PPPC071LFBN-RC	Sullins Connector Solutions

6.3 Daughter Board Electrical Parts

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	2	C1 C13	10 nF, 50 V, Ceramic, X7R, 0805	C0805X103K5RAC7210	Kemet
2	1	C2	100 pF 100 V 10% X7R 0805	08051C101JAT2A	AVX Corp
3	1	C3	10 μF ±10% 35 V Ceramic Capacitor X5R 0805 (2012 Metric)	C2012X5R1V106K125AC	TDK Corporation
4	1	C7	10 μF, ±10%, 10 V, Ceramic Capacitor, Soft Termination, X7R, 0805 (2012 Metric)	C2012X7R1A106K125AE	TDK Corp

5	1	C8	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
6	1	C9	2.2 nF, 50 V, Ceramic, X7R, 0805	08055C222KAT2A	AVX Corp
7	2	C10 C11	10 µF, 16 V, Ceramic, X5R, 0805	GRM21BR61C106KE15L	Murata
8	1	C14*	470 nF, ±10%, 50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Samsung Electro-Mechanics
9	1	D1	75 V, 0.15 A, Switching, SOD-323	BAV16WS-7-F	Diode Inc.
10	2	Q1 Q2	NPN, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT2222ALT1G	On Semiconductor
11	1	R1	RES, 5.11 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF5111V	Panasonic
Item	**Qty.**	**Reference Designator**	**Description**	**Manufacturer Part Number**	**Manufacturer**
12	4	R2 R22 R31 R34	RES, 1.00 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1001V	Panasonic
13	1	R3	RES, 0 R, Jumper, 0.25 W, 1/4 W, Thick Film, -55 °C ~ 155 °C, 1206 (3216 Metric),	CRCW12060000Z0EA	Panasonic
14	6	R5 R18 R19 R39 R44 R49	RES, 0 R, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole Electronics Inc
15	2	R6 R13	RES, 2 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ202V	Panasonic
16	1	R7	RES, 9.09 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9091V	Panasonic
17	3	R8 R17 R20	RES, 100 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1003V	Panasonic
18	1	R9	RES, 1.02 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1021V	Panasonic
19	1	R10	RES, 20 R, 1%, 1/2 W, Thin Film, 1206	RNCP1206FTD20R0	Stackpole Electronics
20	2	R11 R40	RES, 1 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
21	2	R21 R23	RES, SMD, 43 K, 1%, 1/8 W, 0805, ±100 ppm/ °C, -55 °C ~ 155 °C	RC0805FR-0743KL	Yageo
22	5	R25 R26 R50* R52 R53	RES, 2.2 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ222V	Panasonic
23	1	R28	RES, 14.7 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1472V	Panasonic
24	1	R29	RES, 13.7 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1372V	Panasonic
25	1	R32	RES, 300 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ301V	Panasonic
26	2	R41 R46	RES, 316 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3160V	Panasonic
27	2	R42 R47	RES, 9.1 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ912V	Panasonic
28	2	R43 R48	POT, 5K, 0.5 W, TH	PV36W502C01B00	Murata Electronics
29	1	R51	RES, 10.0 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
30	1	SW1	SWITCH SLIDE SPDT 30V.2A PC MNT	EG1218	E-Switch
31	1	SW2	Slide Switch, DPDT, Through Hole	EG2209	E-Switch
32	3	U1 U3 U4	OP AMP SINGLE LOW PWR SOT23-5	LM321MF	Texas Instruments
33	1	U6	IC, Shunt Regulator Adj., 2.495 V, 2.2%, 100 mA, 0 °C ~ 70 °C (TA), SOT23-3, TO-236-3, SC-59, SOT-23-3	TL431CDBZR	Texas Instruments
34	1	VR1	Zener Diode, 6.2 V, 500 mW, ±5%, Surface Mount, SOD-123	MMSZ5234B-TP	Micro Commercial Co

* Do Not Populate (DNP), refer to schematic notes if need to populate

6.4 Daughter Board Mechanical Parts

Item	**Qty.**	**Reference Designator**	**Description**	**Manufacturer Part Number**	**Manufacturer**
1	1	J9	CONN HEADER 10POS .100 R/A TIN, Unshrouded, Breakaway Connector 0.100" (2.54 mm), Through Hole, Right Angle, Tin	0022288100	Molex

7 Magnetics

7.1 PFC Choke (T2) Specification

7.1.1 Electrical Diagram

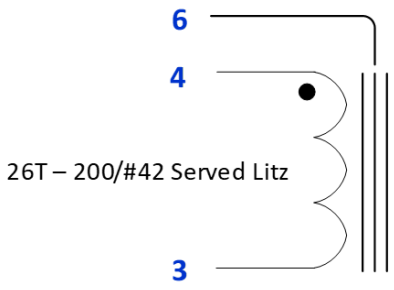


Figure 13 – PFC Choke Electrical Diagram.

7.1.2 Electrical Specifications

Inductance	Pins 3-4 measured at 100 kHz, 0.4 RMS.	140 μH ±5%

7.1.3 Material List

Item	Description
[1]	Core: TDK PC95, PQ32/20Z-12.
[2]	Bobbin: PQ32/20, Vertical, 12 Pins.
[3]	Litz wire: 200/#42, Single Coated Solderable, Served.
[4]	Tape, Polyester Film: 3M 1350-F1 or Equivalent, 9 mm Wide.
[5]	Tape, Polyester Film: 3M 1350-F1 or Equivalent, 10 mm Wide.
[6]	#42 Bus wire
[7]	Varnish: Dolph BC-359, or Equivalent.

7.1.4 Inductor Build Diagram

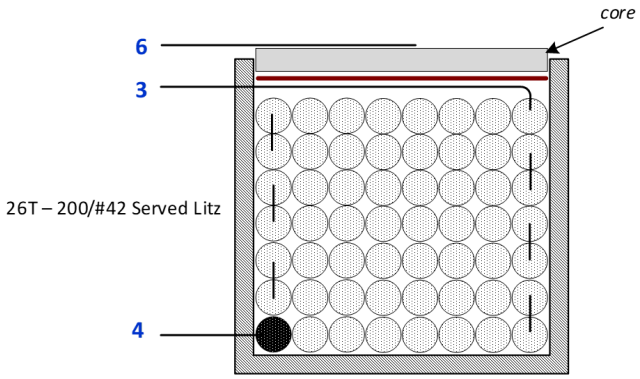


Figure 14 – PFC Inductor Build Diagram.

7.1.5 Inductor Illustrations

Bobbin Pin-out reference:

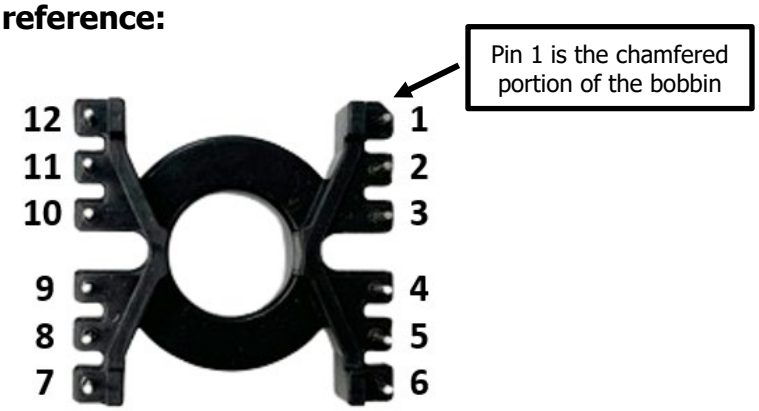
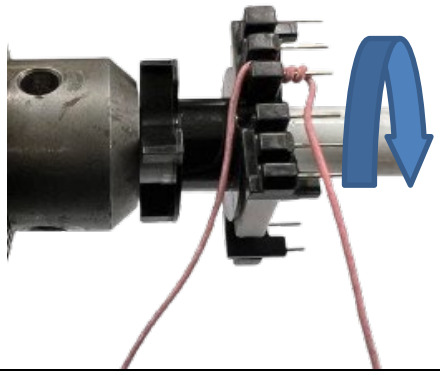
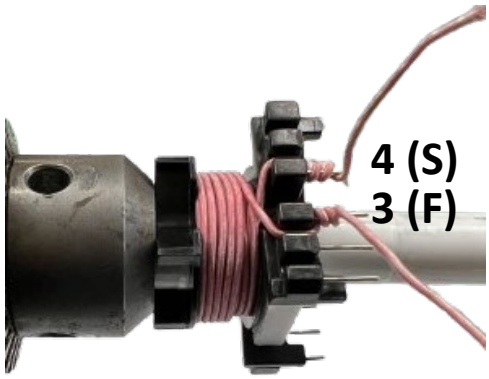
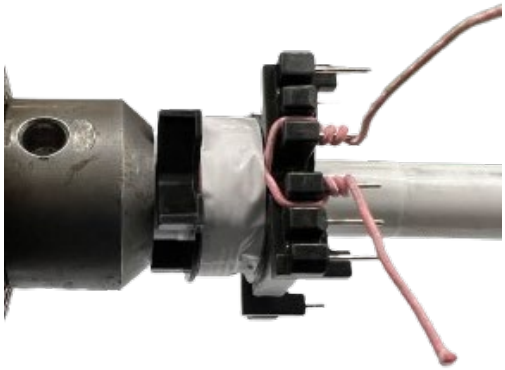
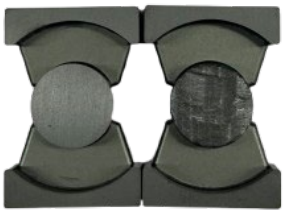
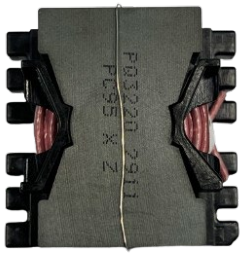
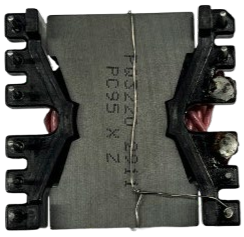


Figure 15 – PFC Choke Bobbin Pin-out (bottom view).

WD1		Place the bobbin on the mandrel with the pin side to the right. Rotate the bobbin in a clockwise direction i.e. top side moving away from the operator.
		Start at pin 4, wire 26T of item [3] forming 3 layers with tight tension to fill the bobbin width in a neat flat wind. Terminate winding at pin 3.

Insulation layer		Add 1T of tape, item [4].
Assembly	 	Solder windings 3 and 4 to their respective pins. Grind core to achieve 140 μH inductance.
Shield grounding	  6 (S & F)	Start at pin 6, wind 1T of item [6] across the middle core and terminate at pin 6 as well.

FINISH		Add 2 to 3 layers of item [5] along the outside surface of the core. Remove pins 1, 2, 5, 7, and 12. Dip in varnish, item [7] and cure in oven as required.

7.2 Common Mode Choke (L4) Specification

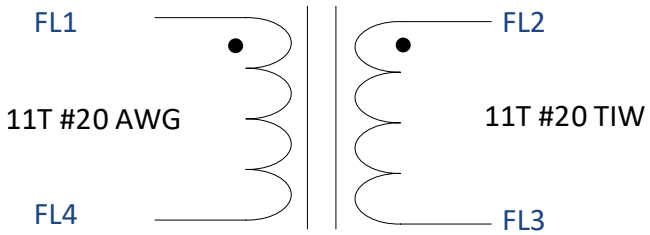


Figure 16 – Inductor Electrical Diagram

7.2.1 Electrical Specifications

Inductance	FL1-4 or FL2-3, measured at 100 kHz, 0.4 V_{RMS}	1 mH +10%

7.2.2 Material List

Item	Description	
[1]	Ferrite Core Toroid: ENCOM T16/10/7C	**PI P/N 32-00343-00**
[2]	Magnet Wire: #20 AWG	
[3]	Triple Insulated Wire: #20 AWG, Furukawa TEX-E or Equivalent.	

7.2.3 Construction Details

1. Bifilar wind 11 turns of items [2] and [3] together as shown in the figure below.

Figure 17 – Finished Inductor

7.3 Output Common Mode Choke (L5) Specification

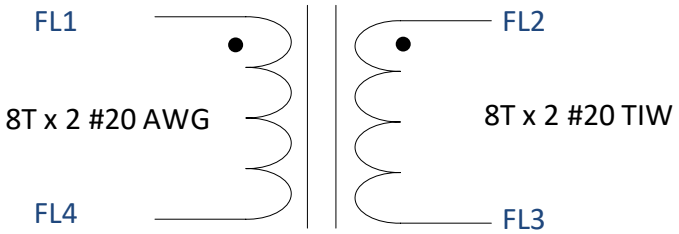


Figure 18 – Inductor Electrical Diagram

7.3.1 Electrical Specifications

Inductance	FL1-4 or FL2-3, measured at 100 kHz, 0.4 V_{RMS}	500 µH +10%

7.3.2 Material List

Item	Description
[1]	Ferrite Core Toroid: VITROPERM 500 F -VAC/19 x 15 x 10 **PI P/N 32-00379-00**
[2]	Magnet Wire: #20 AWG
[3]	Triple Insulated Wire: #20 AWG, Furukawa TEX-E or Equivalent.

7.3.3 Construction Details

1. Bifilar wind 8 turns of 2 strands each of items [2] and [3] as shown in the figure below.

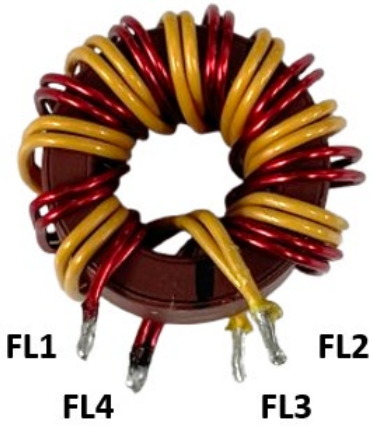


Figure 19 – Finished Inductor

7.4 LLC Transformer (T1) Specification

7.4.1 Electrical Diagram

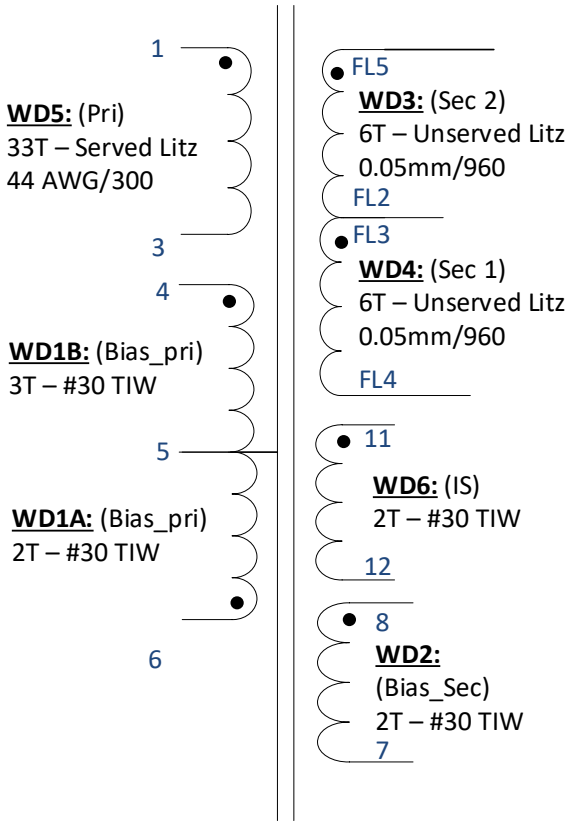


Figure 20 – LLC Transformer Electrical Diagram.

7.4.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1,2, 4, 5, 6 to FL5-FL3, FL2-FL4, pins 7, 8, 11, 12.	3000 VAC
Primary Inductance (Lpri)	Pins 1-2, all other windings open, measured at 100 kHz, 1 V_{RMS}	240 µH ±5%
Primary Leakage1 (LlkpALL)	Pins 1-2, short ALL other pins except IS-winding, measured at 100 kHz, 1 V_{RMS}	76 µH ±5%

7.4.3 Material List

Item	Description
[1]	Core: PQ35/35, PC95 magnetic material or equivalent
[2]	Bobbin: PQ3535 -Vertical, 12pins (6/6)
[3]	Litz wire: #44AWG/300_Served Litz.
[4]	Litz wire: 0.05 mm/960_Unserved Litz.
[5]	Triple Insulated Wire: #30AWG
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 9 mm wide.

[7]	Tape: 3M 1298 Polyester Film, 1 mil thick, 15 mm wide.
[8]	Tape: 3M 1298 Polyester Film, 1 mil thick, 34 mm wide.
[9]	Separator Tape: 1.5 mm wide.
[10]	Teflon Tube
[11]	#33 Bus Wire
[12]	Varnish: Dolph BC-359, or equivalent.

7.4.4 Transformer Build Diagram

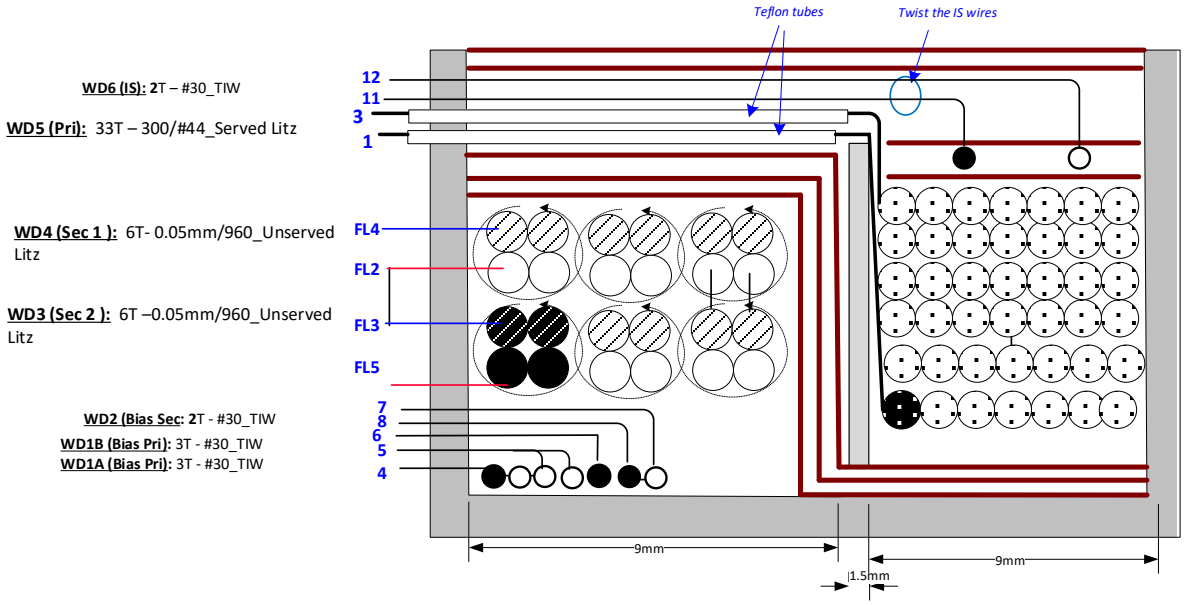
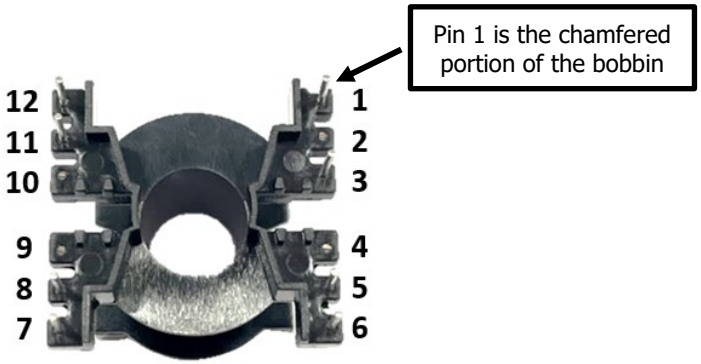
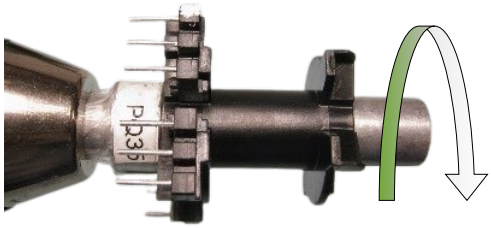
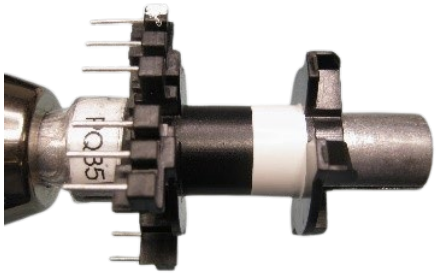
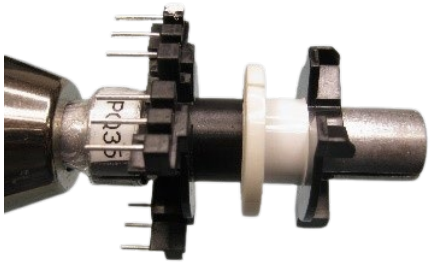
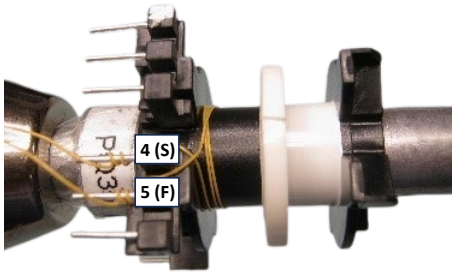


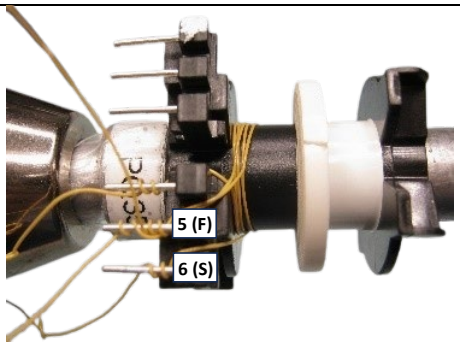
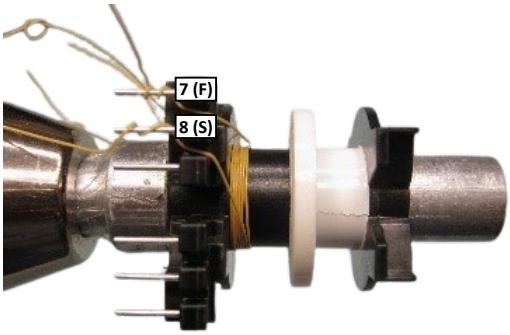
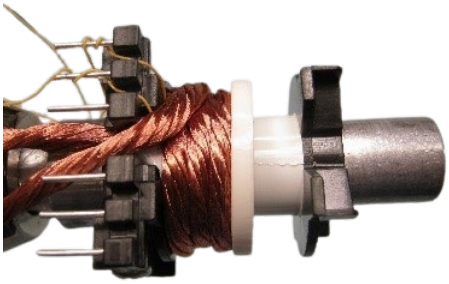
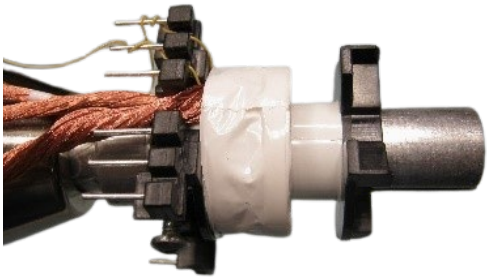
Figure 21 – LLC Transformer Build Diagram.

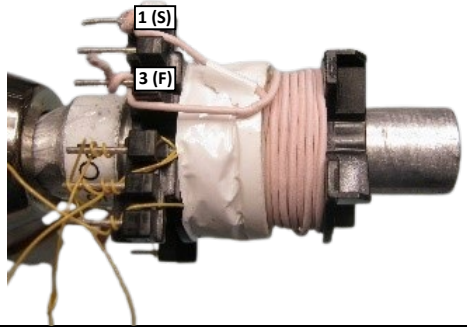
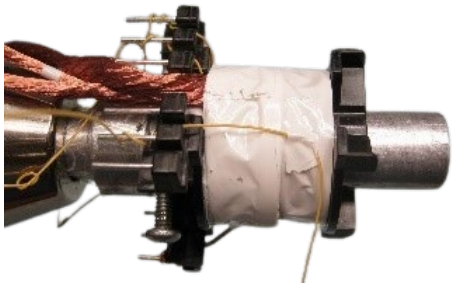
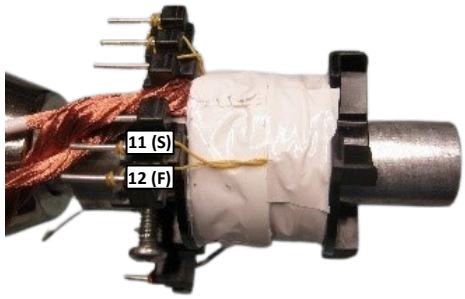
7.4.5 Winding Preparation

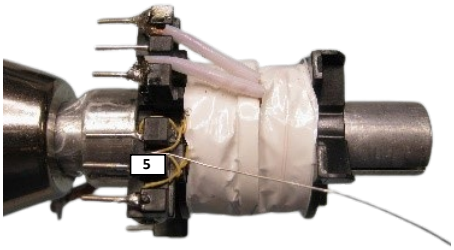
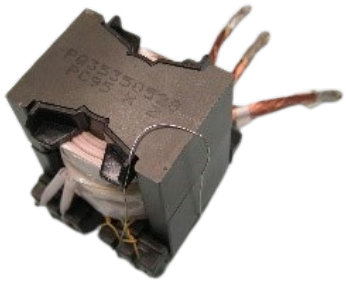
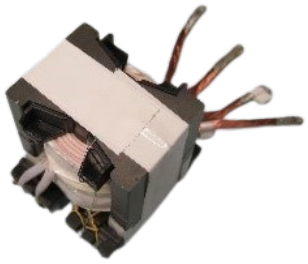
BOBBIN	
WD2 (Bias sec winding)	**The wires to the pins 7 and 8 shall be twisted together, before terminating in the pins**
WD3 & WD4 Secondary	Prepare Item [4] 0.05 mm/ 960 at around 24 in. long. Split strands into two groups, each for WD3(Sec2) and WD4(Sec1). ➢ Put labels on FL2, FL3, FL4 and FL5. **The winding should remain twisted together. (Twisted together for balanced leakage inductance between WD3 and WD4).**  
WD6 (IS winding)	**The wires to the pins 11 and 12 shall be twisted together, before terminating in the pins**

7.4.6 Transformer construction

Bobbin position and separator	  	Position the bobbin on the mandrel such that the primary side of the bobbin is on the left side. Winding direction of the bobbin is clockwise. To make and locate the divider for this transformer, place 1 layer of tape Item [6] on the right side of the bobbin and place separator tape Item [9] with height almost same as edge of bobbin.
WD1A, WD1B (Bias Primary)		For WD1B, wind 3T of wire Item [5] on the left chamber starting at pin 4 and terminate at pin 5.

		For WD1A, wind 2T of wire Item [5] on the left chamber starting at pin 6 and terminate at pin 5.
WD2 **(Bias Secondary)**		On the left chamber, wind 2T of wire Item [5] starting at pin 8 and terminate at pin 7.
WD3 & WD4 **(Sec 2 & Sec 1)**	 	Wind 6T of prepared Secondary wire Item [4] on the left chamber, enter and exit wires in the secondary slot. Secure the secondary winding with 1 layer of tape Item [7].

	 	Remove tape Item [6] and separator tape Item [9] and wrap 2 layers of tape Item [7] making the secondary wires fully covered especially in the area where the separation tape was removed. Overlap the tape where it creeps to the right chamber. Re-attach separator tape Item [9] in its previous location.
WD5 (Primary)		Wind 33T of wire Item [3] starting at pin 1 and terminate at pin 3.
WD6 (IS)	 	Add 1 layer of tape Item [8] on top of the Primary winding. Wind 2T of wire Item [5] starting at pin 11 and terminate at pin 12. Add another layer of tape Item [8] to secure this winding.

Finish	   	Twist all wires for all windings. Insert Teflon tube Item [10] for the Primary winding ends before soldering to their respective pins. Solder bus wire Item [11] to pin 5 and lean along the cores before securing the transformer with tape. Use two layers of tape Item [7] to wrap the inner sides of the bottom core. Grind the other core to achieve 240 μH primary inductance. Insert core with tapes at the bottom, gapped core on the top of transformer, and secure with tape. Dip the transformer in varnish item [12].

8 PFC Design Spreadsheet

In this design, the input AC voltage varies from 180 to 280 VAC. The output DC bus voltage from the PFC stage is specified as 400 V. The DC bus capacitors are chosen as 270 μF, to match a typical customer requirement.

1	Hiper_PFS-3_Boost_080516; Rev.1.0; Copyright Power Integrations 2016	INPUT	INFO	OUTPUT	UNITS	Continuous Mode Boost Converter Design Spreadsheet
2	Enter Application Variables					Design Title
3	Input Voltage Range	High Line		High Line		Input voltage range
4	VACMIN	180		180	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other voltages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX	280		280	VAC	Maximum AC input voltage
6	VBROWNIN			173	VAC	Expected Typical Brown-in Voltage per IC specifications; Line impedance not accounted.
7	VBROWNOUT			162	VAC	Expected Typical Brown-out voltage per IC specifications; Line impedance not accounted.
8	VO	400	Warning	400	VDC	Load voltage is too high and will result in high VDS stress
9	PO	760		760	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	n	0.96		0.96		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX	30		30	VDC	Maximum Output voltage ripple
15	tHOLDUP	10		10	ms	Holdup time
16	VHOLDUP_MIN			310	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	Yes		Yes		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
19						
20	KP and INDUCTANCE					
21	KP_TARGET	0.685		0.685		Target ripple to peak inductor current ratio at the peak of VACMIN. Affects inductance value
22	LPFC_TARGET (0 bias)			140	μH	PFC inductance required to hit KP_TARGET at peak of VACMIN and full load
23	LPFC_DESIRED (0 bias)			140	μH	LPFC value used for calculations. Leave blank to use LPFC_TARGET. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation. Calculated inductance

						with rounded (integral) turns for powder core.
24	KP_ACTUAL			0.657		Actual KP calculated from LPFC_ACTUAL
25	LPFC_PEAK			140	µH	Inductance at VACMIN, 90°. For Ferrite, same as LPFC_DESIRED (0 bias)
26						
27	Basic current parameters					
28	IAC_RMS			4.40	A	AC input RMS current at VACMIN and Full Power load
29	IO_DC			1.90	A	Output average current/Average diode current
30						
31						
32	PFS Parameters					
33	PFS Part Number	Auto		PFS7539H		If examining brownout operation, over-ride autopick with desired device size
34	Operating Mode	Full Power		Full Power		Mode of operation of PFS. For Full Power mode enter "Full Power" otherwise enter "EFFICIENCY" to indicate efficiency mode
35	IOCP min			10.0	A	Minimum Current limit
36	IOCP typ			10.5	A	Typical current limit
37	IOCP max			11.0	A	Maximum current limit
38	IP			9.06	A	MOSFET peak current
39	IRMS			3.17	A	PFS MOSFET RMS current
40	RDSON			0.40	Ohms	Typical RDSon at 100 'C
41	FS_PK			102	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
42	FS_AVG			96	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
43	PCOND_LOSS_PFS			4.0	W	Estimated PFS conduction losses
44	PSW_LOSS_PFS			5.2	W	Estimated PFS switching losses
45	PFS_TOTAL			9.2	W	Total Estimated PFS losses
46	TJ Max			100	deg C	Maximum steady-state junction temperature
47	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
48	HEATSINK Theta-CA		Info	1.99	°C/W	Big heatsink; Consider changing Rth or TJ
49						
50						
51	INDUCTOR DESIGN					
52	Basic Inductor Parameters					
53	LPFC (0 Bias)			140	µH	Value of PFC inductor at zero current. This is the value measured with LCR meter. For powder, it will be different than LPFC.
54	LP_TOL			10.0	%	Tolerance of PFC Inductor Value (ferrite only)
55	IL_RMS			4.55	A	Inductor RMS current (calculated at VACMIN and Full Power Load)

56	Material and Dimensions					
57	Core Type	Ferrite		Ferrite		Enter "Sendust", "Pow Iron" or "Ferrite"
58	Core Material	Auto		PC44/PC95		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
59	Core Geometry	Auto		PQ		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
60	Core	PQ32/20		PQ32/20		Core part number
61	Ae			170.00	mm^2	Core cross sectional area
62	Le			55.50	mm	Core mean path length
63	AL			6530.00	nH/t^2	Core AL value
64	Ve			9.44	cm^3	Core volume
65	HT (EE/PQ) / ID (toroid)			5.12	mm	Core height/Height of window; ID if toroid
66	MLT			67.1	mm	Mean length per turn
67	BW			8.98	mm	Bobbin width
68	LG			0.82	mm	Gap length (Ferrite cores only)
69	Flux and MMF calculations					
70	BP_TARGET (ferrite only)			3900	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
71	B_OCP (or BP)			3833	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
72	B_MAX			2996	Gauss	peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance
73						
74	µ_TARGET (powder only)			N/A	%	%µ at peak current vs. zero current, at VACMIN, Full Power Load, divided by permeability at 0 current (powder only)
75	µ_MAX (powder only)			N/A	%	%µ vs. zero current, at VACMIN Full Power LOAD (powder only)
76	µ_OCP (powder only)			N/A	%	%µ vs. zero current, at IOCP_typ (powder only)
77	I_TEST			10.5	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			3658	Gauss	Flux density at I_TEST and maximum tolerance inductance
79	µ_TEST (powder only)			N/A	%	relative permeability at I_TEST and typical inductance (powder only)
80	Wire					
81	TURNS			26		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
82	ILRMS			4.55	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	42	Info	42	AWG	!!! Info. Selected wire gauge is too thick and may caused increased losses due to skin effect. Consider

						using multiple strands of thinner wires or Litz wire
85	Filar	200		200		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.064	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			1.26	mm	Will be different than OD if Litz
88	DCR			0.06	ohm	Choke DC Resistance
89	P AC Resistance Ratio			1.38		Ratio of total Cu loss including HF ACR loss vs. assuming only DCR (uses Dowell equations)
90	J			7.19	A/mm^2	Estimated current density of wires. It is recommended that 6 < J < 8
91	FIT			89%	%	Percentage fill of winding window for EE/PQ core. Full window approx. 90%
92	Layers			3.3		Estimated layers in winding
93	Loss calculations					
94	BAC-p-p			2053	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
95	LPFC_CORE_LOSS			2.48	W	Estimated Inductor core Loss
96	LPFC_COPPER_LOSS			1.81	W	Estimated Inductor copper losses
97	LPFC_TOTAL_LOSS			4.28	W	Total estimated Inductor Losses
98						
99						
100	Built-in PFC Diode					
101	PFC Diode Part Number			INTERNAL2		PFC Diode Part Number
102	Type			SPECIAL		PFD Diode Type
103	Manufacturer			PI		Diode Manufacturer
104	VRRM			530	V	Diode rated reverse voltage
105	IF			6	A	Diode rated forward current
106	Qrr					high temperature
107	VF			1.44	V	Diode rated forward voltage drop
108	PCOND_DIODE			2.74	W	Estimated Diode conduction losses
109	PSW_DIODE			0.59	W	Estimated Diode switching losses
110	P_DIODE			3.32	W	Total estimated Diode losses
111	TJ Max			100	deg C	Maximum steady-state operating temperature
112	Rth-JS				degC/W	
113	HEATSINK Theta-CA			1.99	degC/W	
114						
115						
116	Output Capacitor					
117	Output Capacitor	270		270	μF	Minimum value of Output capacitance
118	VO_RIPPLE_EXPECTED			23.3	V	Expected ripple voltage on Output with selected Output capacitor
119	T_HOLDUP_EXPECTED			11.4	ms	Expected holdup time with selected Output capacitor
120	ESR_LF			0.68	ohms	Low Frequency Capacitor ESR
121	ESR_HF			0.27	ohms	High Frequency Capacitor ESR
122	IC_RMS_LF			1.30	A	Low Frequency Capacitor RMS current

123	IC_RMS_HF			1.79	A	High Frequency Capacitor RMS current
124	CO_LF_LOSS			1.13	W	Estimated Low Frequency ESR loss in Output capacitor
125	CO_HF_LOSS			0.86	W	Estimated High frequency ESR loss in Output capacitor
126	Total CO LOSS			2.00	W	Total estimated losses in Output Capacitor
127						
128						
129	Input Bridge (BR1) and Fuse (F1)					
130	I^2t Rating			21.17	A^2*s	Minimum I^2t rating for fuse
131	Fuse Current rating			5.99	A	Minimum Current rating of fuse
132	VF			0.90	V	Input bridge Diode forward Diode drop
133	IAVG			3.73	A	Input average current at 70 VAC.
134	PIV_INPUT BRIDGE			396	V	Peak inverse voltage of input bridge
135	PCOND_LOSS_BRIDGE			7.13	W	Estimated Bridge Diode conduction loss
136	CIN			1.0	µF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
137	RT			9.90	ohms	Input Thermistor value
138	D_Precharge			1N5407		Recommended precharge Diode
139						
140						
141	PFS3 small signal components					
142	C_REF			1.0	µF	REF pin capacitor value
143	RV1			4.0	MOhms	Line sense resistor 1
144	RV2			6.0	MOhms	Line sense resistor 2
145	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
146	RV4			155.5	kOhms	Description pending, could be modified based on feedback chain R1-R4
147	C_V			0.514	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
148	C_VCC			1.0	µF	Supply decoupling capacitor
149	C_C			100	nF	Feedback C pin decoupling capacitor
150	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
151	PGT set resistor			320.5	kohm	Power good threshold setting resistor
152						
153						
154	Feedback Components					
155	R1			4.0	Mohms	Feedback network, first high voltage divider resistor
156	R2			6.0	Mohms	Feedback network, second high voltage divider resistor
157	R3			6.0	Mohms	Feedback network, third high voltage divider resistor
158	R4			155.5	kohms	Feedback network, lower divider resistor

159	C1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
160	R5			15.0	kohms	Feedback network: zero setting resistor
161	C2			1000	nF	Feedback component- noise suppression capacitor
162						
163						
164	Loss Budget (Estimated at VACMIN)					
165	PFS Losses			9.20	W	Total estimated losses in PFS
166	Boost diode Losses			3.32	W	Total estimated losses in Output Diode
167	Input Bridge losses			7.13	W	Total estimated losses in input bridge module
168	Inductor losses			4.28	W	Total estimated losses in PFC choke
169	Output Capacitor Loss			2.00	W	Total estimated losses in Output capacitor
170	EMI choke copper loss			0.50	W	Total estimated losses in EMI choke copper
171	Total losses			25.93	W	Overall loss estimate
172	Efficiency			0.97		Estimated efficiency at VACMIN, full load.
173						
174						
175	CAPZero component selection recommendation					
176	CAPZero Device			CAP005DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
177	Total Series Resistance (R1+R2)			0.48	k-ohms	Maximum Total Series resistor value to discharge X-Capacitors
178						
179						
180	EMI filter components recommendation					
181	CIN_RECOMMENDED			1000	nF	Metallized polyester film capacitor after bridge, ratio with Po
182	CX2			680	nF	X capacitor after differential mode choke and before bridge, ratio with Po
183	LDM_calc			151	µH	estimated minimum differential inductance to avoid <10kHz resonance in input current
184	CX1			680	nF	X capacitor before common mode choke, ratio with Po
185	LCM			10	mH	typical common mode choke value
186	LCM_leakage			30	µH	estimated leakage inductance of CM choke, typical from 30~60uH
187	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
188	LDM_Actual			121	µH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
189	DCR_LCM	0.10		0.10	Ohms	total DCR of CM choke for estimating copper loss
190	DCR_LDM	0.10		0.10	Ohms	total DCR of DM choke(or CM #2) for estimating copper loss

191						
192	Note: CX2 can be placed between CM chock and DM choke depending on EMI design requirement.					
193						

Note: The warning on 400 V output was verified on the bench that it has adequate margin on VDS stress from the datasheet limits. The choice of Litz wire was verified on bench and gives sufficient efficiency and thermal measurement.

9 LLC Design Spreadsheet

In this design, the LLC is designed to operate with resonance at 600 V. This ensures that the converter is in deep DCM (below resonance) under full load. As the converter operates with variable current and voltage, the converter is specifically designed to operate across a wide frequency range. During testing, the converter was loaded to 12.5 A @ 60 V.

1	**ACDC_HiperLCS2_090324; Rev.2.0; Copyright Power Integrations 2024**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**HiperLCS-2 Design Spreadsheet**
2	General					
3	Description			>		LCS7268Z-900W-60V-15A-SynchRF-33T-6T-169uH-75uH-27nF-94kHz
4	Input Parameters					
5	VIN MIN	350		350	V	Brownout Threshold Voltage
6	VIN RES	600		600	V	Input Voltage at Resonance - lower Vres to lower Npri
7	VIN NOM	400		400	V	Nominal Input Voltage - default CRM Vres=Vnom (or DCM Vres>Vnom, CCM Vres<Vnom)
8	VIN MAX	450		450	V	Maximum Input Voltage - decrease Vmax to lower Fmax
9	PFC	YES		YES		Input Option
10	**Output Parameters**					
11	Vout1	60.00		60.00	V	Main Output Voltage
12	Iout1 PK	15.0		15.0	A	Peak Main Output Current - default = 200% of Iout1Cont - used to select device size - increasing (IOUT1 PK) peak power will lower (LRES)
13	Pout1 PK			900.0	W	Main Output Peak Power
14	Iout1 CONT	12.0		12.0	A	Continuous Main Output Current - default 50% of Ppeak - used to select

						device size - losses calculated at this power level
15	Pout1 CONT			720.0	W	Continues Main Output Power
16	External CC	YES		YES		Use external CC operation
17	Vout1 Min (CC)	26.0		26.0	V	Minimum Output Voltage when operating in CC - lower VoutMin lowers Lm and also lowers efficiency
18	VCC			0.125	V	Output current sense resistor voltage when operating at CC-threhsold
19	RCC			9.00	mΩ	Output current sense resistor value
20	RCC Rated Power			3.04	W	Output current sense resistor rated power
21	**Estimated Parameters, Design Choices and Selections**					
22	FS Range	3		3		Frequency Range
23	FS Vnom (Target)	111.0		111.0	kHz	Switching Frequency at VinNom
24	Output Rectifier	SynchRF		SynchRF		Output Rectifier
25	Ron_SR1			5.0	mΩ	Sync. Rectifier ON Resitance
26	VF_SR1				V	Output Diode Average Voltage Drop
27	**Design Results**					
28	DESIGN RESULT			Design Passed		Current Design Status
29	**Device Variables**					
30	DEVNAME	LCS7268Z		LCS7268Z		PI Device Name
31	QOSS			294	nC	Equivalent Combined Half-bridge charge (Qoss) at 480V
32	RDSON			0.260	Ω	RDSON of selected device
33	Fault Responce	NON_LATCHING		NON_LATCHING		..
34	**Tank Circuit Components & Operation Frequency Range**					
35	Integrated Magnetics	YES		YES		Integrated Transformer Requirements
36	LP Nominal			243.34	uH	Nominal Primary Inductance
37	Lm			168.8	uH	Magnetizing inductance of transformer - modified by Kz, Device size and frequency
38	Lres			74.5	uH	Series resonant or primary leakage inductance - modified by Pmax

39	Cres	27.00		27.00	nF	Series resonant capacitor.
40	f_calc@Vbrownout			86.9	kHz	Frequency at PoutCont at Vbrownout, full load - adjust VinBrownout
41	f_calc@resonance			112.2	kHz	Frequency at PoutCont at Vres (defined by Lres and Cres) - adjust Vres)
42	f_calc@Vnom			93.8	kHz	Frequency at PoutCont at Vnom - adjust FS Vnom Target or Vnom
43	f_calc@Vinmax			232.3	kHz	Expected frequency at maximum input voltage and full load; Heavily influenced by n_eq and primary turns
44	VINGmaxInversion			346.9	V	Minimum Input Voltage for negative Gain at 100% load. Below this voltage the Gain becomes positive (unstable loop)
45	**Core Dimensions/TRF Mechanical Parameters**					
46	AE			190.00	mm^2	Transformer Core Cross-sectional area
47	VE			0.0	cm^3	Transformer Core Volume
48	MLT			69.74	mm	Middle Length of a Turn
49	AW			152.00	mm^2	Core Window area
50	BW			20.80	mm	Bobbin Winding Width
51	Bobbin Chambers			2		Bobbin Chambers
52	ChambDist	1.50		1.50	mm	Width of bobbin with no windings - empty space between primary/secondary generates leakage inductance
53	Bobbin Height			7.80	mm	Height of the bobbin, maximum Stack height
54	Prim. Bobbin Chamber Width			10.98	mm	Part of the bobbin allocated for primary
55	Sec. Bobbin Chamber Width			8.32	mm	Part of the bobbin allocated for secondary
56	K-PD			0.35		Penetration Depth multiplier (for Single Strand LITZ calulation)
57	**Transformer Generic Parameters**					
58	CR_TYPE	PQ35		PQ35		Transformer Core Type
59	FR_TYPE			3C95		Magnetic material used

60	BACmax Actual			234.96	mT	Estmated Flux Density at Vnom - increase Ns to reduce Bmax
64	kSecChamb			0.40		Percentage of Bobbin Chamber Width used for Secondary Windings - Adjust to change Used Percentage of Primary/Secondary Windows
65	**Transformer Primary Parameters**					
66	Npri			33		Calculated Primary Winding Total Number of Turns
67	Iprim RMS			3.60	A	Transformer Primary Winding RMS Current at PoutCont and VinNom
79	**Main Output Parameters**					
80	NSec	6		6		Secondary Number of Turns
81	ISRMS			22.94	A	Transformer Secondary Winding RMS Current
93	**Circuit Losses**					
97	CO ESR Loss			0.38	W	Output Capacitor ESR Loss at VinNom and PoutCont
98	PLOSS Switch			1.69	W	Single Primary Switch Conduction Loss at VinNom and PoutCont
99	PLOSS Output Rectifier			0.44	W	Single Output Rectifier Conduction Loss at VinNom and PoutCont
100	PLOSS RCC			2.03	W	Current sense resisitor power loss at VinNom and PoutCont
102	PLOSS Circuit Total			6.67	W	Circuit Total Loss at VinNom and PoutCont
103	**Circuit Components**					
104	RZ1			150	kΩ	Control Zero (boost high-frequency gain)
105	CP2			100	pF	Control Pole2 (roll-off high-frequency gain)
106	Cp1			2.2	nF	Control Pole1 (roll-off low-frequency gain)
107	Resr CO			1.00	mOhms	ESR of the output capacitor
108	COmin			647	uF	Min CO to satisfy burst conditions
109	RD1			500	Ω	RD1 Resistor value
110	RD2			500	Ω	RD2 Resistor value
111	CBPL			1	uF	CBPL Capacitor Value /25V

112	CBPH			1	uF	CBPH Capacitor Value /25V
113	C5VL			1	uF	C5VL Capacitor Value /10V
114	C5VH			220	nF	C5VH Capacitor Value /10V
115	C5VFL			100	nF	C5VLFL Capacitor Value /10V
116	C5VS			10	uF	C5VS Capacitor Value /10V
117	CBPS			10	uF	CBPS Capacitor Value /35V
118	RL_Up			open	kΩ	L-pin Input Voltage (Vin) Sense Resistor
119	RL_Down			shorted	Ω	L-pin to Ground Resistor
120	RPP			316	kΩ	RPP Resistor /1% E96 series
121	RPS			75	kΩ	RPS Resistor /1% E96 series
122	**Bias, IS Circuit & Feedback Components**					
123	NPB			2		Primary Bias Turns
124	NSB			2		Secondary Bias Turns
125	NVIS			2		Secondary (Is) Sense Turns
126	RIS			1702	kΩ	Rrs Resistor Value
127	CIS			470	pF	IS sense winding coupling capacitor
128	RFBH			360.6	kΩ	Calulated value of top feedback resistor. use series closest resistor 1% E96
129	RFBL			24.0	kΩ	Calulated value of low feedback resistor. use series closest resistor 1% E96
130	**Currents and Winding loss elements**					
131	Iprim RMS			3.60	A	Transformer Primary Winding RMS Current at PoutCont at VinNom
132	ISRMS			22.94	A	Transformer Secondary Winding RMS Current at PoutCont at VinNom
133	Irms_SR			9.42	A	Secondary Rectifier RMS Current at PoutCont at VinNom
134	Irms_CO1			19.55	A	Output Capacitor RMS Current at PoutCont at VinNom
139	**Advanced Settings**					
140	Kz	0.9		0.9		coefficient of surplus ZVS energy @ Vnom - raise Kz to lower Vin(GmaxInv) - Kz should be >= 1.0 to ensure ZVS operation

141	Tdd1_Vinnom			250	ns	Half-bridge slew at 100% load @ Vnom - raise Tdd1 to lower ZVS currents
142	Coupling			0.89		Transformer Coupling
143	Cpri			40.00	pF	Stray Capacitance at transformer primary
144	PP or Lpin	PP		PP		HB Startup current selection
145	R_L_UP_ACT				kΩ	Actual Value of L-pin Input Voltage (Vin) Sense Resistor
146	VLUV-				V	..
147	VLUV+				V	..
148	VLOV-				V	..
149	VLOV+				V	..
150	External Resonant Inductor (Ext.Lres) Calculations					
172	Errors, Warnings, Information					
173	Information			0		Number of variables required bench functionality check. Check the variables with "Info" in the third column .
174	Design Warnings			0		Number of variables whose values exceed electrical/datasheet specifications. Check the variables with "Err" in the third column .
175	Design Errors			0		The list of design variables which result in an infeasible design.

10 Heat Sink of the Synchronous MOSFET

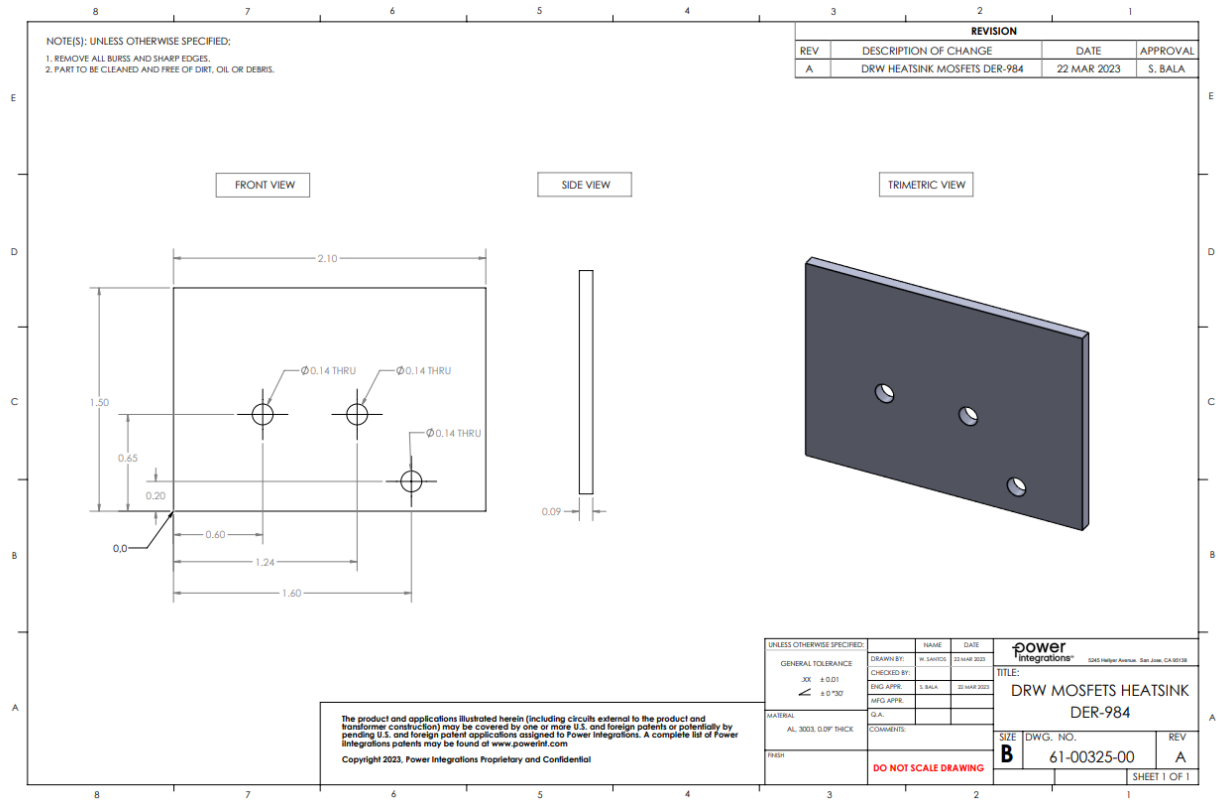


Figure 22 – Synchronous MOSFET Heat Sink

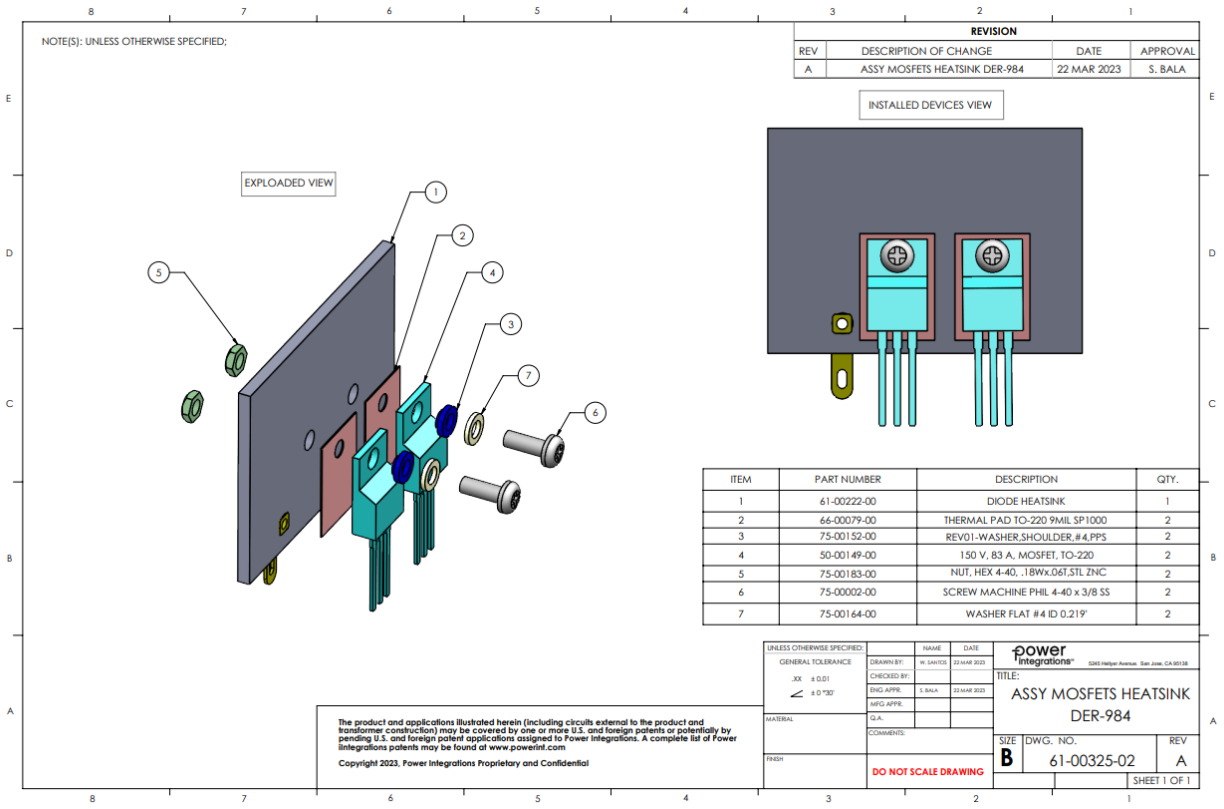


Figure 23 – Synchronous MOSFET Heat Sink Assembly

11 Heat sink of the PFS7539H

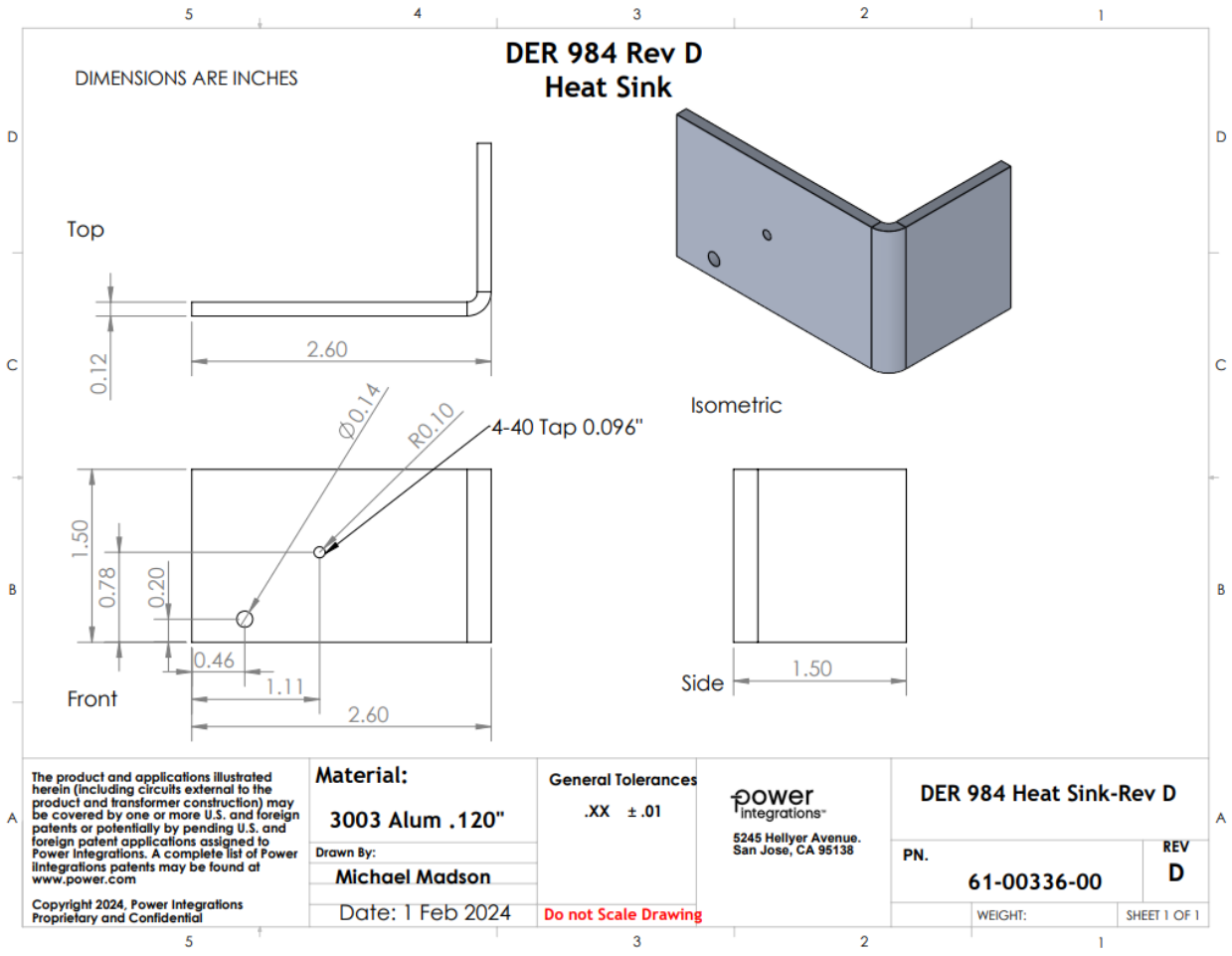
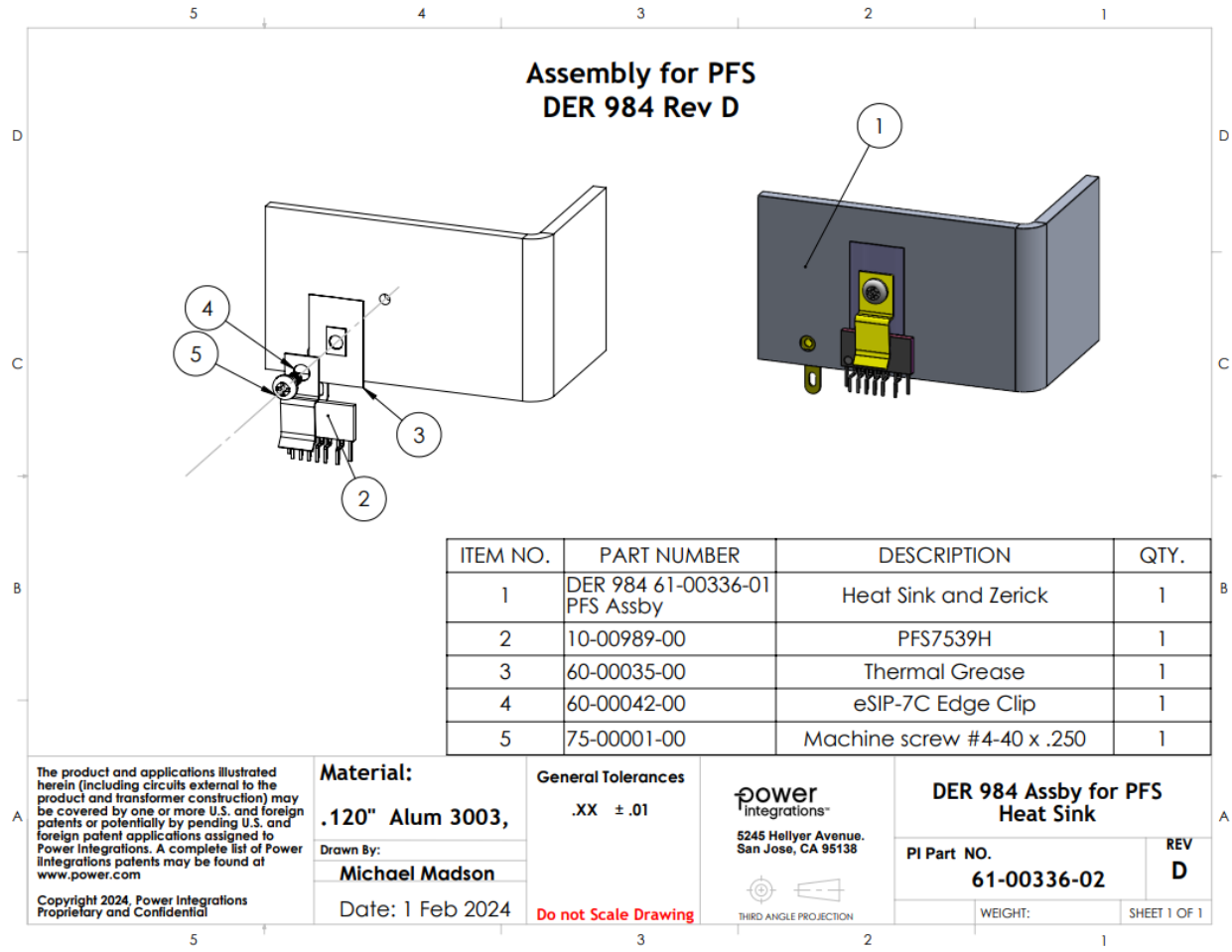


Figure 24 – PFC Heat Sink



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	DER 984 61-00336-01 PFS Assby	Heat Sink and Zerick	1
2	10-00989-00	PFS7539H	1
3	60-00035-00	Thermal Grease	1
4	60-00042-00	eSIP-7C Edge Clip	1
5	75-00001-00	Machine screw #4-40 x .250	1

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com

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Material: .120" Alum 3003,

Drawn By: Michael Madson

Date: 1 Feb 2024

General Tolerances .XX ± .01

Do not Scale Drawing

power integrations

5245 Hellyer Avenue. San Jose, CA 95138

THIRD ANGLE PROJECTION

DER 984 Assby for PFS Heat Sink

PI Part NO. 61-00336-02

REV D

WEIGHT:

SHEET 1 OF 1

Figure 25 – PFC Heat Sink Assembly

12 Heat sink of the Bridge Rectifier

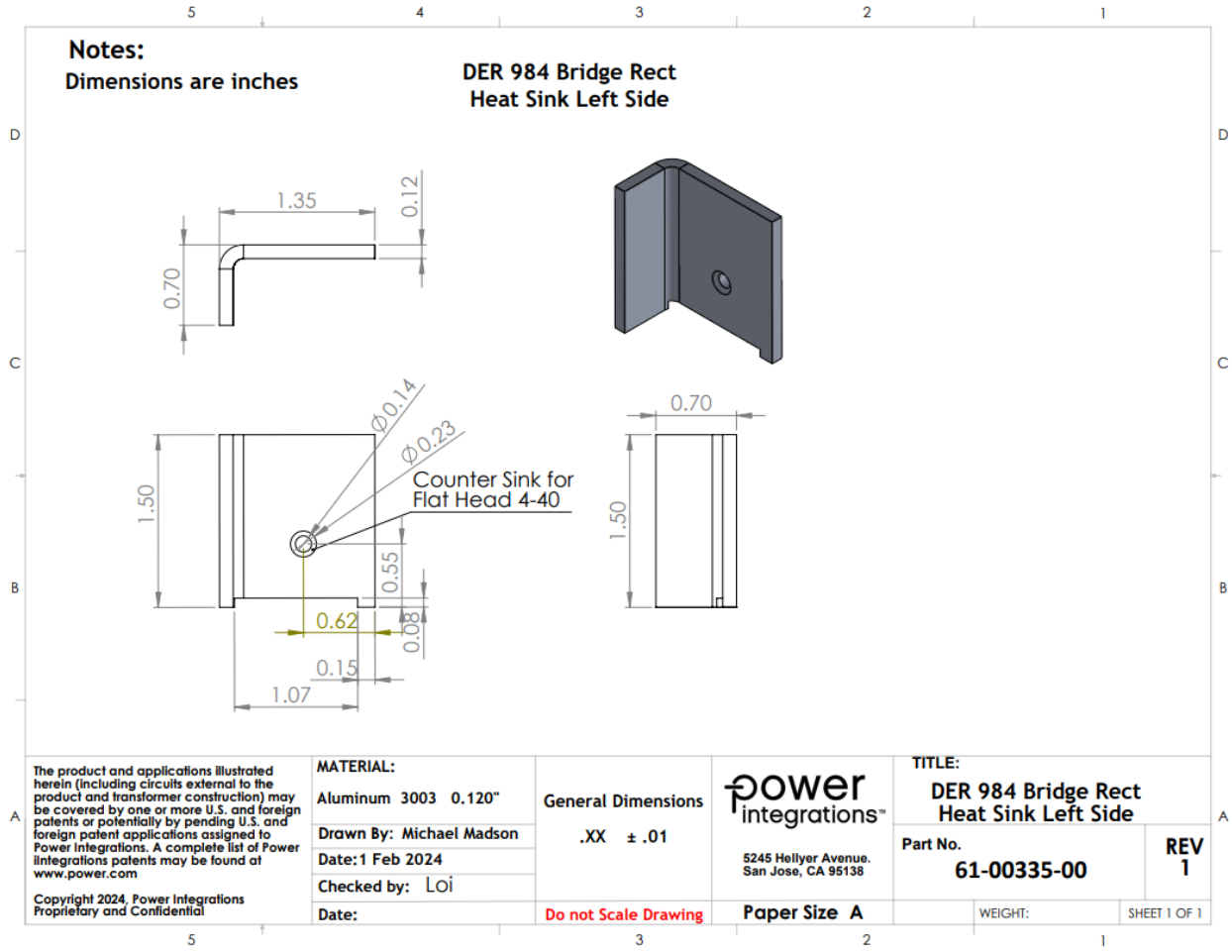


Figure 26 – Bridge Rectifier Left Side

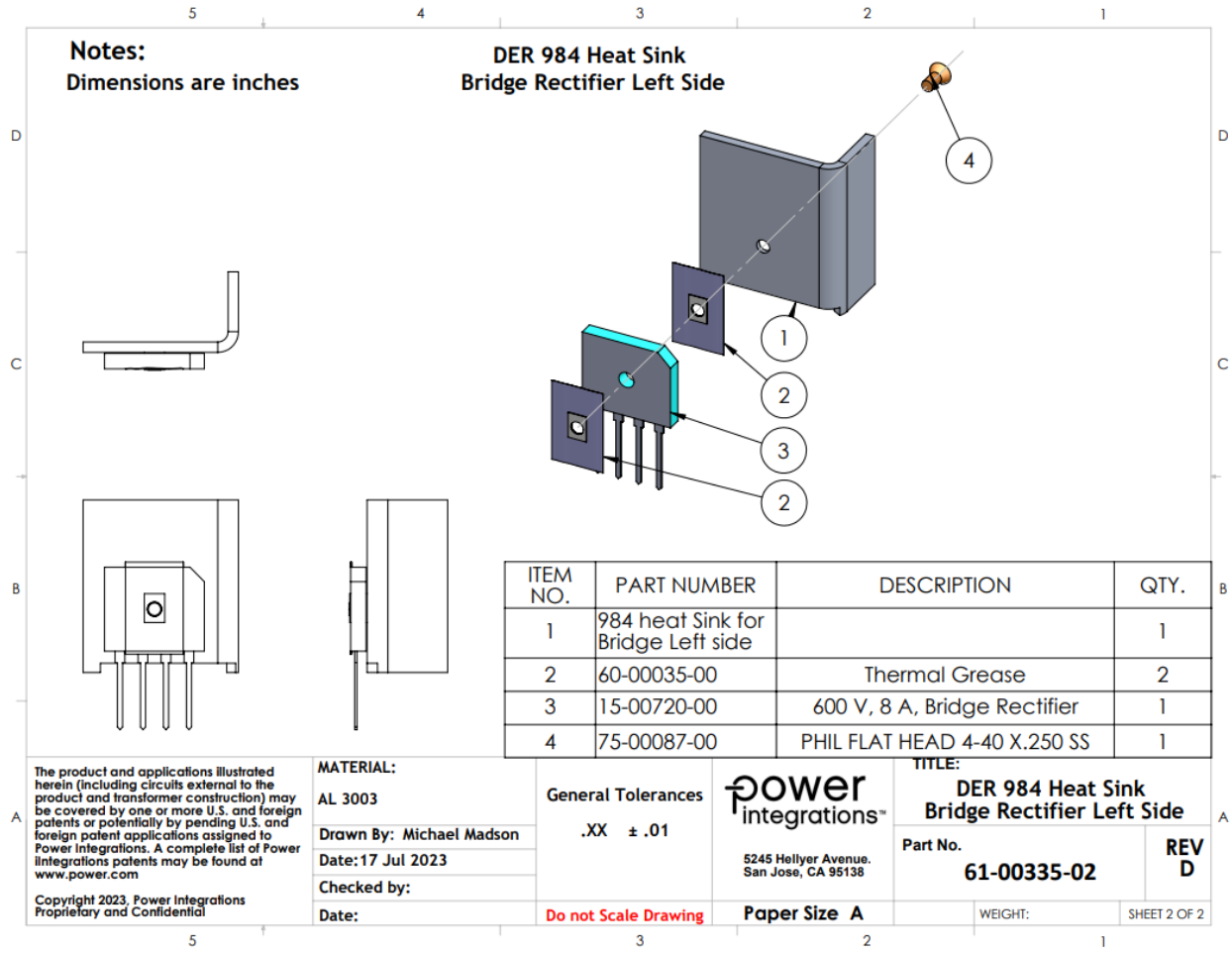


Figure 27 – Bridge Rectifier Left Side Assembly

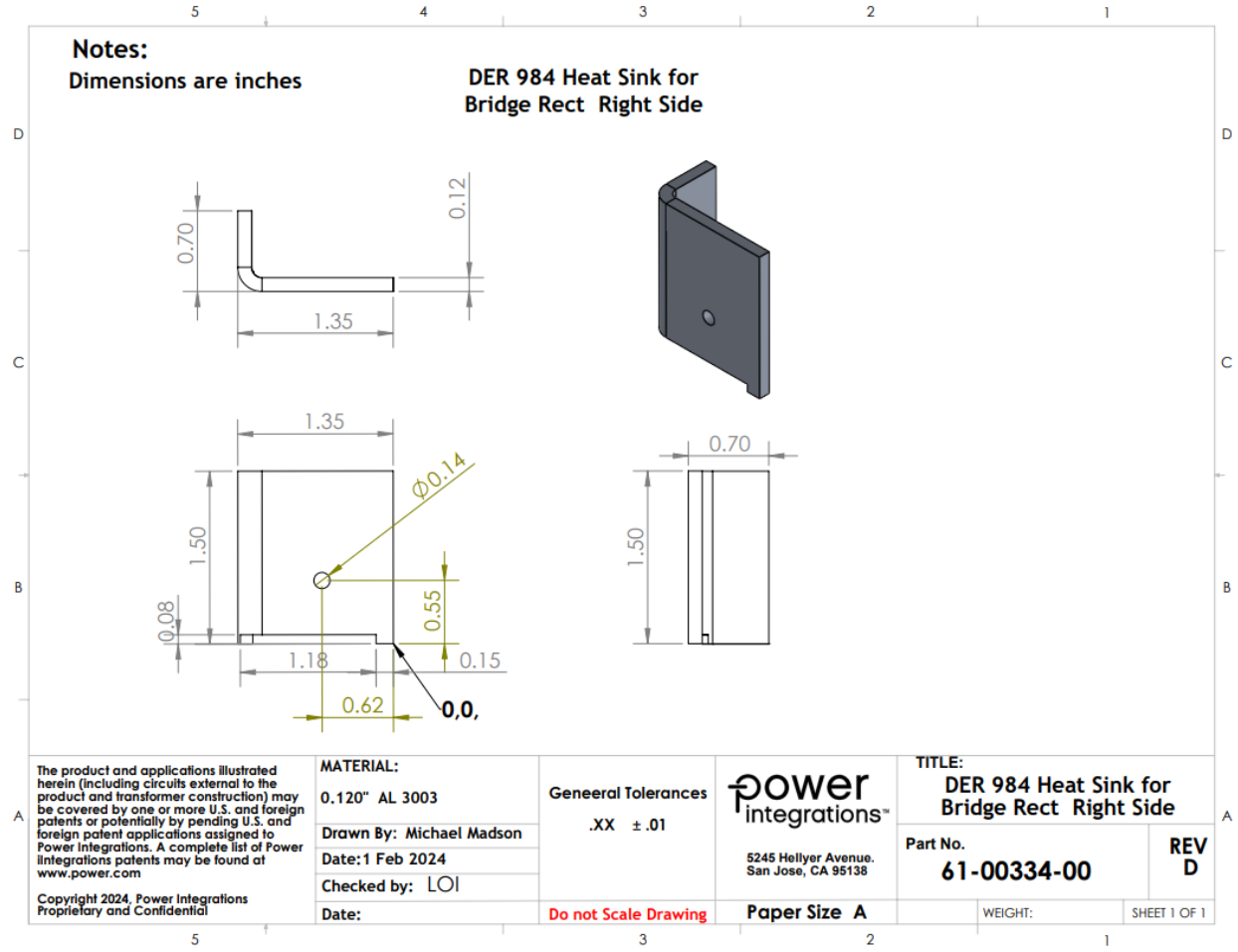


Figure 28 – Bridge Rectifier Right Side

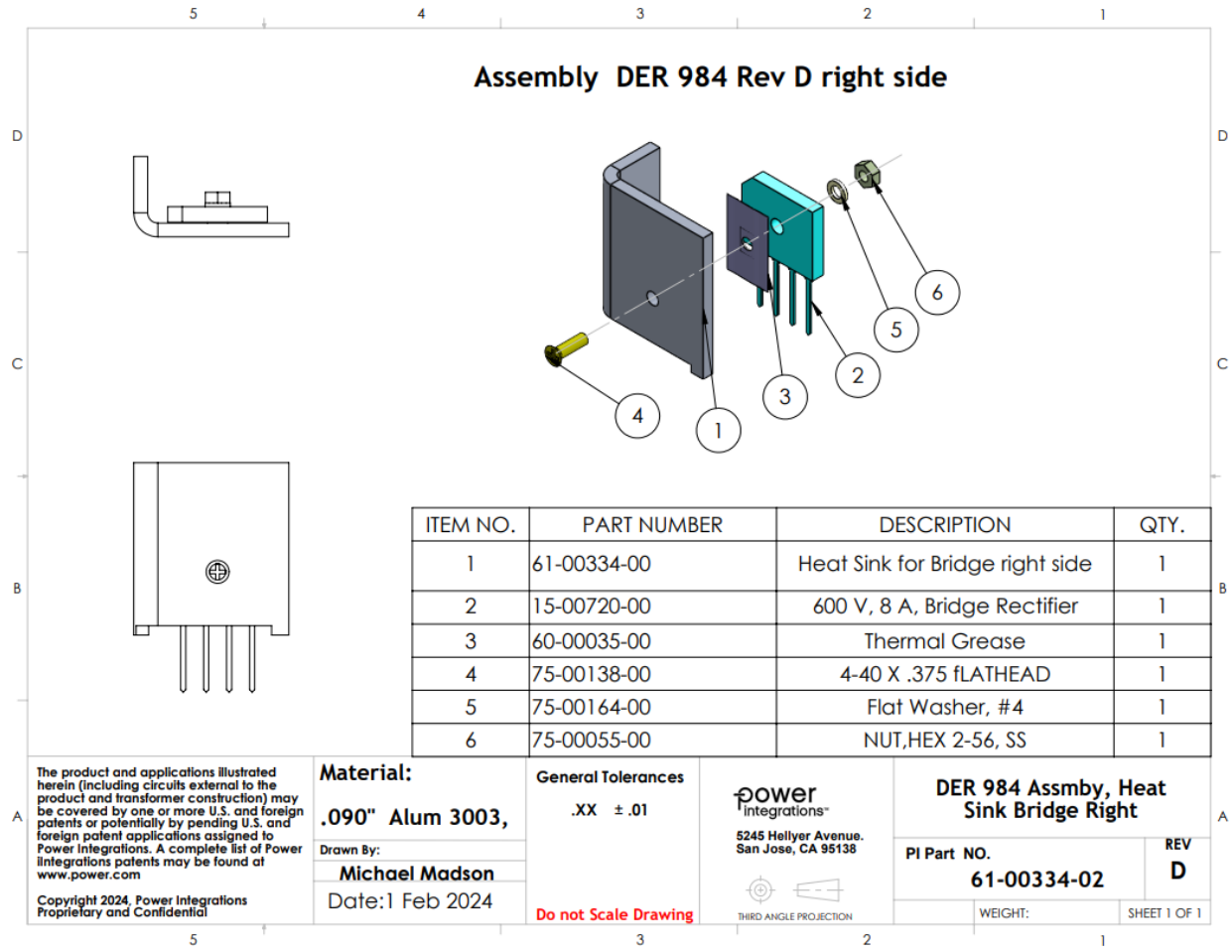


Figure 29 – Bridge Rectifier Right Side Assembly

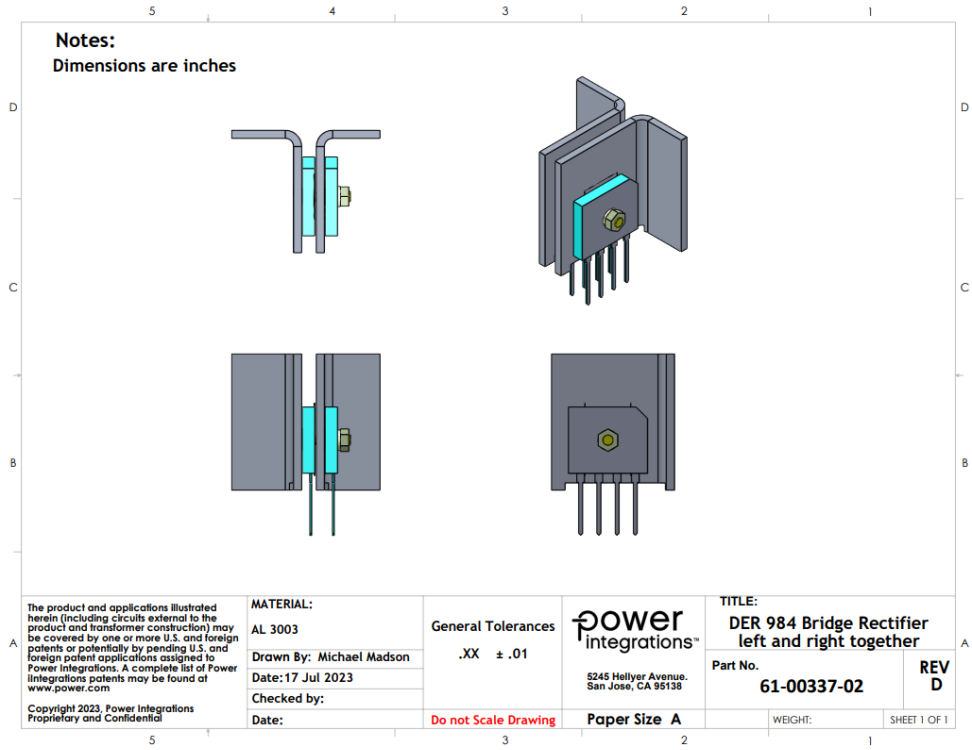


Figure 30 – Assembled View of Both Rectifier Bridges

13 Heat sink of the LLC Primary IC

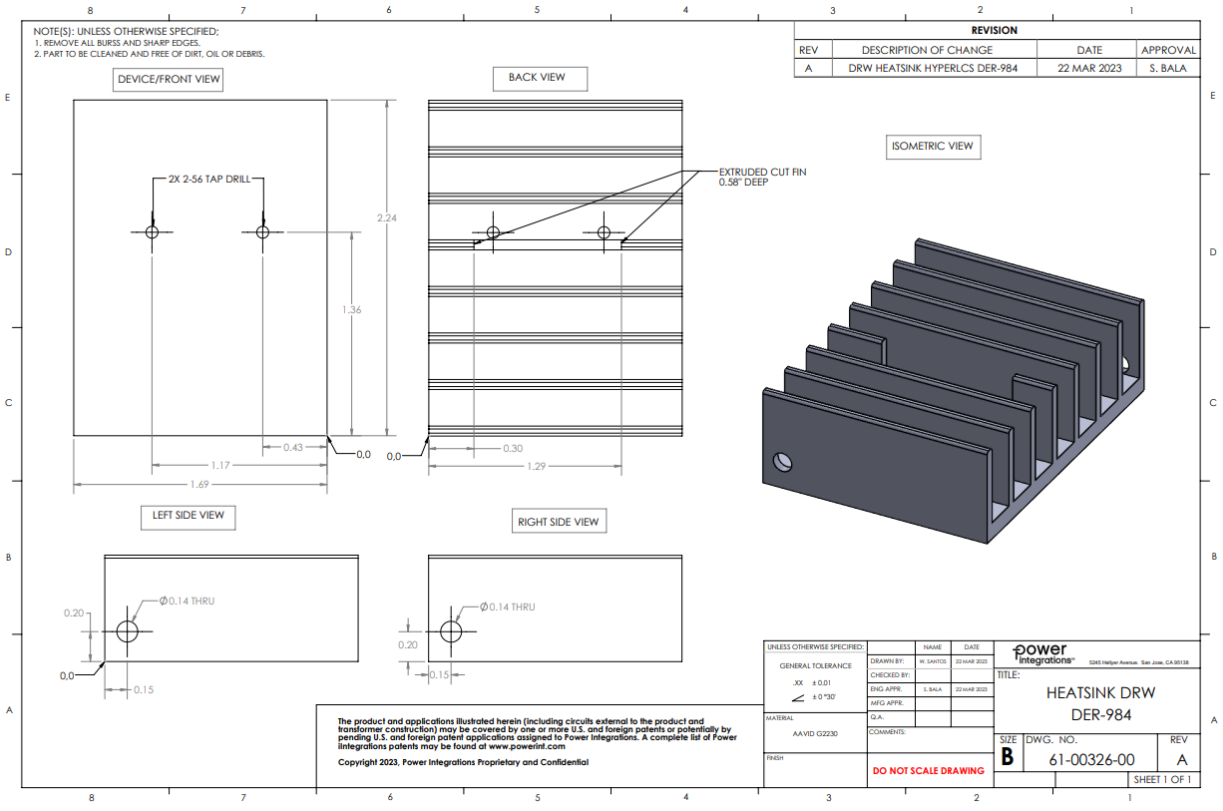


Figure 31 – LLC Primary IC Heat Sink

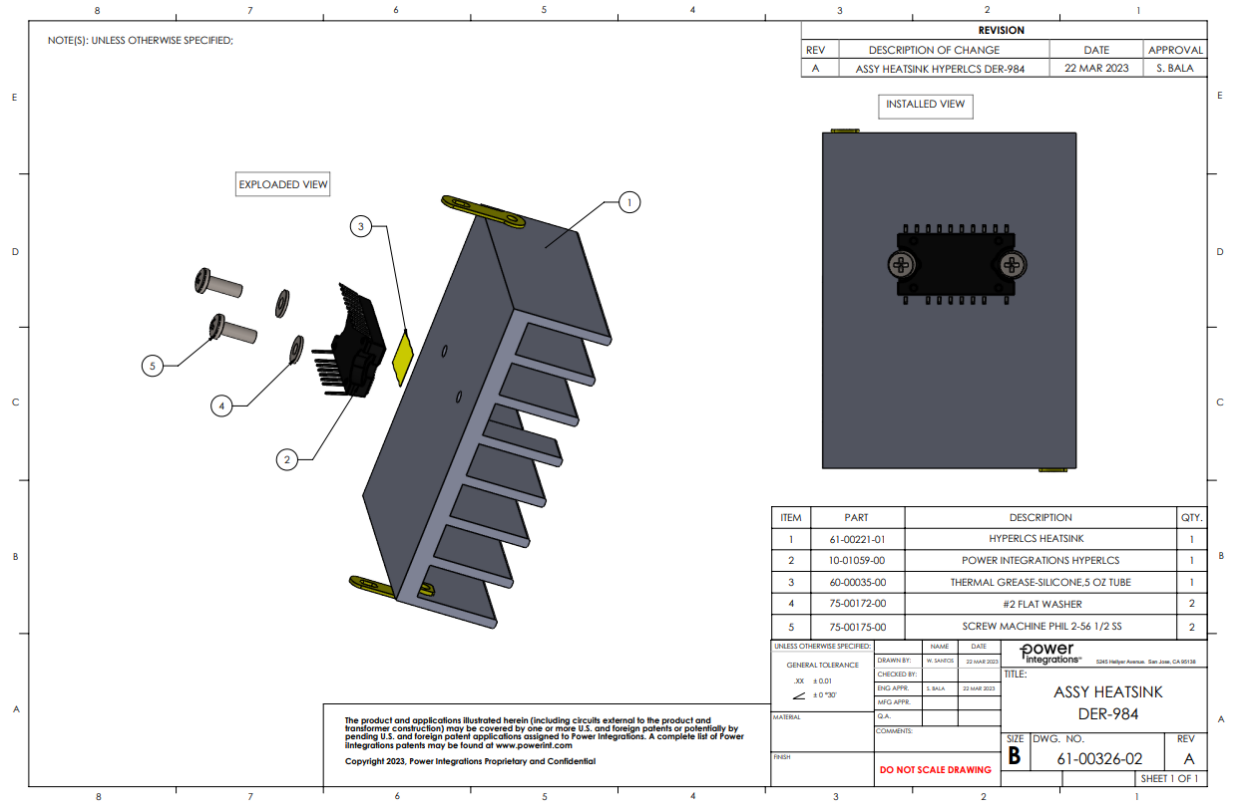


Figure 32 – LLC Primary IC Heat Sink Assembly

14 Performance Data

This section provides the description of various performance test conducted, to demonstrate the performance of the converter for charger application. All performance data was measured at room temperature unless otherwise specified.

14.1 Constant Voltage (CV) and Constant Current (CC) Mode

The daughter card was attached to the Main board. The mode of operation (CC or CV) was selected using SPDT and DPDT switches. Under CV mode, the reference voltage was set using the variable resistor R48. Under CC mode, the reference current was set using the variable resistor R43. The performance under CV and CC mode was shown in the Figure 33.

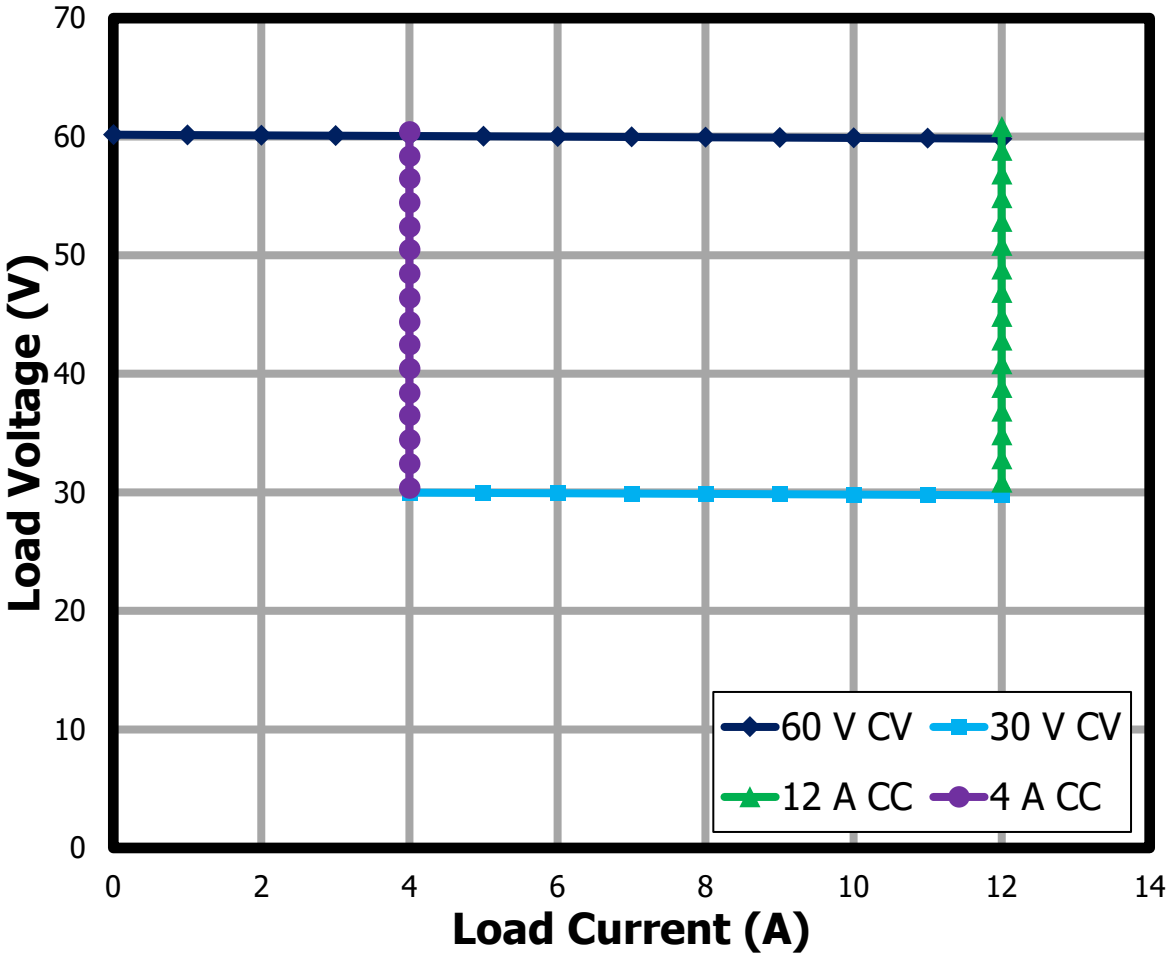


Figure 33 – CV/CC mode of operation with 230 VAC input

14.2 End to end Efficiency

Figure 34 shows power supply efficiency with respect to output power for different input line voltages.

For CV mode output, the daughter card switch positions were set accordingly (refer to Fig. 4) and the reference voltage set to 60 V using variable resistor R48. A variable AC source was used to supply a sine wave input and a DC electronic load set to CC mode was used as load on the output.

For CC mode output, the daughter card switch positions were set accordingly (refer to Fig. 3) and the reference current set to 12 A using variable resistor R43. A variable AC source was used to supply a sine wave input and a DC electronic load set to CV mode was used as load on the output.

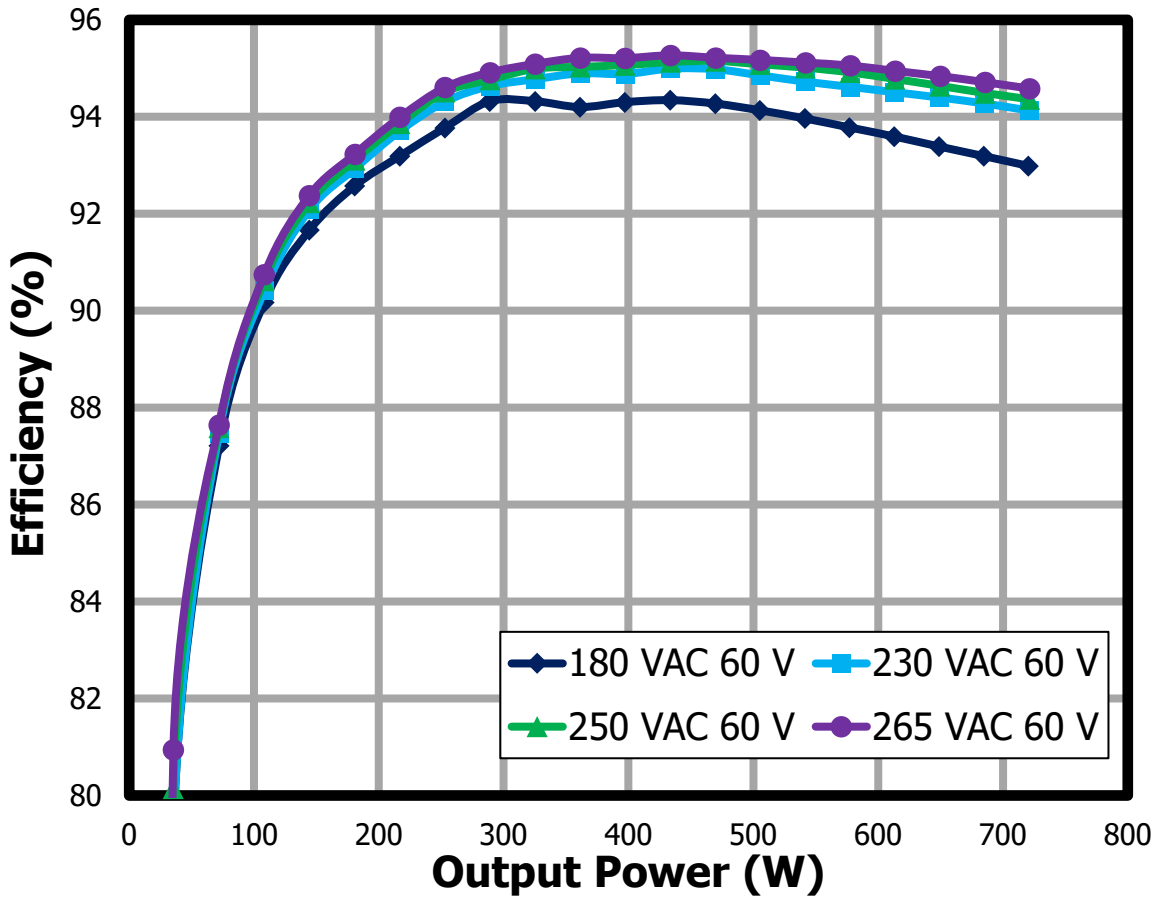


Figure 34 – Total Efficiency vs. Load, 60 V Output CV Mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
179	4.33	0.997	775	60.1	12.0	720	93.0
179	4.11	0.997	735	60.1	11.4	685	93.2
179	3.89	0.997	695	60.1	10.8	649	93.4
179	3.66	0.996	655	60.2	10.2	613	93.6
179	3.44	0.996	615	60.2	9.59	577	93.8
180	3.23	0.995	576	60.2	8.99	541	94.0
180	3.01	0.994	537	60.3	8.38	505	94.1
180	2.79	0.993	498	60.3	7.79	470	94.3
180	2.58	0.992	459	60.3	7.19	433	94.3
180	2.37	0.991	421	60.3	6.58	397	94.3
180	2.16	0.990	383	60.4	5.98	361	94.2
180	1.94	0.990	345	60.4	5.39	325	94.3
180	1.72	0.990	306	60.4	4.78	289	94.3
180	1.52	0.989	270	60.4	4.19	253	93.8
180	1.31	0.987	233	60.5	3.59	217	93.2
180	1.10	0.987	195	60.5	2.99	181	92.6
180	0.89	0.985	158	60.5	2.39	144	91.7
180	0.69	0.972	120	60.5	1.79	108	90.2
180	0.49	0.936	82.6	60.5	1.19	72.0	87.2
180	0.30	0.819	44.8	60.6	0.59	35.5	79.1

Table 1 – Efficiency at 180 VAC, 60 V CV mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
230	3.36	0.994	766	60.2	12.0	721	94.1
230	3.19	0.994	727	60.2	11.4	685	94.3
230	3.02	0.993	688	60.2	10.8	649	94.4
230	2.85	0.993	649	60.2	10.2	613	94.5
230	2.68	0.992	610	60.2	9.59	577	94.6
230	2.51	0.992	572	60.3	8.99	542	94.7
230	2.34	0.992	533	60.3	8.38	505	94.9
230	2.17	0.992	495	60.3	7.79	470	95.0
230	2.01	0.991	456	60.3	7.19	434	95.0
230	1.84	0.992	419	60.4	6.58	397	94.9
230	1.67	0.992	381	60.4	5.98	361	94.9
230	1.51	0.991	343	60.4	5.39	325	94.8
230	1.34	0.991	305	60.4	4.78	289	94.6
230	1.18	0.990	268	60.4	4.19	253	94.3
230	1.02	0.990	231	60.5	3.59	217	93.7
230	0.86	0.986	195	60.5	2.99	181	92.9
230	0.70	0.974	157	60.5	2.39	144	92.1
230	0.55	0.949	120	60.5	1.79	108	90.4
230	0.40	0.896	82.3	60.5	1.19	72.0	87.5
230	0.26	0.749	44.8	60.6	0.59	35.5	79.1

Table 2 – Efficiency at 230 VAC, 60 V CV mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
250	3.10	0.989	764	60.2	12.0	721	94.4
250	2.94	0.989	725	60.2	11.4	685	94.5
250	2.78	0.989	686	60.2	10.8	650	94.6
250	2.62	0.989	647	60.2	10.2	613	94.8
250	2.47	0.989	609	60.3	9.59	578	94.9
250	2.31	0.989	570	60.3	8.99	542	95.0
250	2.16	0.988	532	60.3	8.38	506	95.1
250	2.00	0.987	494	60.3	7.79	470	95.2
250	1.85	0.986	456	60.4	7.19	434	95.1
250	1.69	0.991	418	60.4	6.58	397	95.1
250	1.54	0.990	380	60.4	5.98	361	95.0
250	1.39	0.989	343	60.4	5.39	325	95.0
250	1.24	0.989	305	60.4	4.78	289	94.8
250	1.09	0.987	268	60.5	4.19	253	94.5
250	0.94	0.982	231	60.5	3.59	217	93.9
250	0.80	0.972	194	60.5	2.99	181	93.1
250	0.66	0.954	157	60.5	2.39	144	92.2
250	0.52	0.924	119	60.5	1.79	108	90.6
250	0.38	0.865	82.2	60.6	1.19	72.0	87.6
250	0.27	0.649	44.2	60.6	0.59	35.5	80.1

Table 3 – Efficiency at 250 VAC, 60 V CV mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
265	2.97	0.972	763	60.2	12.0	721	94.6
265	2.82	0.972	724	60.2	11.4	686	94.7
265	2.67	0.971	685	60.2	10.8	650	94.8
265	2.52	0.971	646	60.3	10.2	614	94.9
265	2.37	0.970	608	60.3	9.58	578	95.1
265	2.22	0.970	570	60.3	8.99	542	95.1
265	2.07	0.969	531	60.3	8.38	506	95.2
265	1.92	0.973	494	60.3	7.79	470	95.2
265	1.77	0.972	455	60.4	7.19	434	95.3
265	1.62	0.971	417	60.4	6.58	397	95.2
265	1.48	0.970	380	60.4	5.98	361	95.2
265	1.34	0.967	342	60.4	5.39	325	95.1
265	1.20	0.961	305	60.4	4.78	289	94.9
265	1.06	0.951	267	60.5	4.18	253	94.6
265	0.93	0.939	231	60.5	3.59	217	94.0
265	0.79	0.924	194	60.5	2.99	181	93.2
265	0.65	0.905	156	60.5	2.39	144	92.4
265	0.51	0.876	119	60.5	1.79	108	90.8
265	0.38	0.816	82.2	60.6	1.19	72.0	87.6
265	0.29	0.566	43.8	60.6	0.59	35.5	80.9

Table 4 – Efficiency at 265 VAC, 60 V CV mode

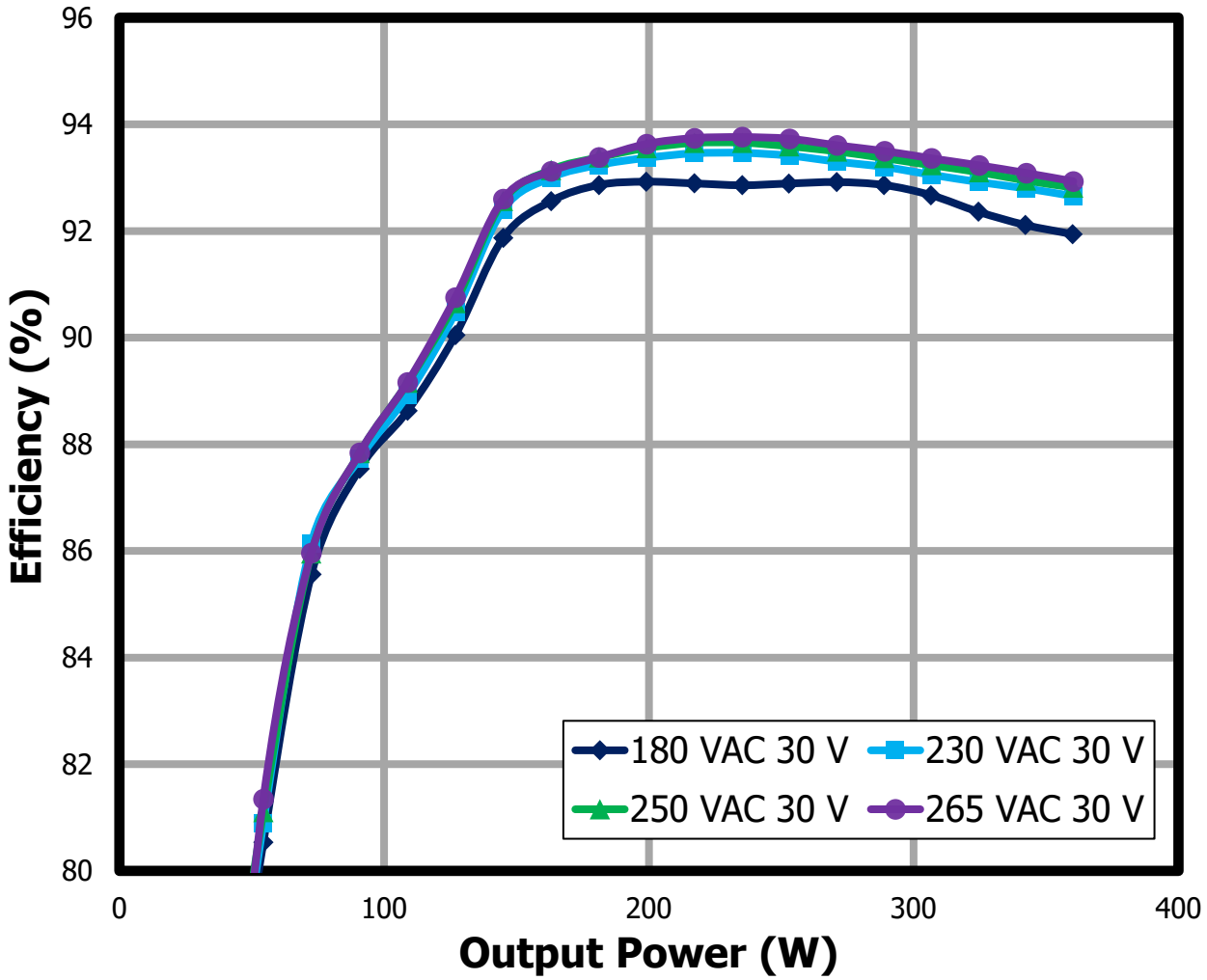


Figure 35 – Total Efficiency vs. Load, 30 V Output CV Mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
180	2.20	0.990	392	30.0	12.0	360	91.9
180	2.09	0.990	371	30.0	11.4	342	92.1
180	1.98	0.990	351	30.1	10.8	324	92.4
180	1.86	0.990	331	30.1	10.2	307	92.7
180	1.75	0.990	311	30.1	9.59	289	92.9
180	1.64	0.990	292	30.1	8.99	271	92.9
180	1.53	0.989	272	30.2	8.39	253	92.9
180	1.43	0.988	253	30.2	7.79	235	92.9
180	1.32	0.986	234	30.2	7.19	217	92.9
180	1.21	0.986	214	30.2	6.58	199	92.9
180	1.10	0.987	195	30.2	5.99	181	92.9
180	0.99	0.987	176	30.3	5.39	163	92.6
180	0.89	0.985	158	30.3	4.79	145	91.9
180	0.80	0.981	141	30.3	4.19	127	90.0
180	0.70	0.973	123	30.3	3.59	109	88.6
180	0.60	0.960	104	30.3	2.99	90.8	87.5
180	0.50	0.938	84.8	30.4	2.39	72.5	85.6
180	0.41	0.906	67.5	30.4	1.79	54.4	80.5
180	0.32	0.839	48.8	30.4	1.19	36.2	74.2
180	0.23	0.685	28.8	30.4	0.59	17.9	62.0

Table 5 – Efficiency at 180 VAC, 30 V CV mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
230	1.71	0.992	389	30.0	12.0	360	92.7
230	1.62	0.991	369	30.1	11.4	342	92.8
230	1.53	0.991	349	30.1	10.8	325	92.9
230	1.45	0.991	330	30.1	10.2	307	93.1
230	1.36	0.991	310	30.1	9.59	289	93.2
230	1.28	0.990	291	30.2	8.99	271	93.3
230	1.19	0.990	271	30.2	8.39	253	93.4
230	1.11	0.990	252	30.2	7.79	235	93.5
230	1.02	0.989	232	30.2	7.19	217	93.5
230	0.94	0.988	213	30.2	6.58	199	93.4
230	0.86	0.986	194	30.3	5.99	181	93.2
230	0.78	0.980	175	30.3	5.39	163	93.0
230	0.70	0.973	157	30.3	4.79	145	92.4
230	0.63	0.964	140	30.3	4.19	127	90.5
230	0.56	0.951	122	30.3	3.59	109	88.9
230	0.48	0.931	103	30.3	2.99	90.8	87.7
230	0.41	0.898	84.2	30.4	2.39	72.5	86.1
230	0.34	0.856	67.2	30.4	1.79	54.4	80.9
230	0.28	0.768	48.8	30.4	1.19	36.2	74.2
230	0.23	0.529	27.7	30.4	0.59	17.9	64.5

Table 6 – Efficiency at 230 VAC, 30 V CV mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
250	1.57	0.990	388	30.0	12.0	360	92.8
250	1.49	0.990	368	30.1	11.4	342	92.9
250	1.41	0.990	349	30.1	10.8	325	93.1
250	1.33	0.989	329	30.1	10.2	307	93.2
250	1.25	0.989	309	30.1	9.59	289	93.4
250	1.17	0.988	290	30.1	8.99	271	93.5
250	1.10	0.987	270	30.2	8.39	253	93.6
250	1.02	0.985	251	30.2	7.79	235	93.7
250	0.94	0.982	232	30.2	7.19	217	93.7
250	0.87	0.978	213	30.2	6.58	199	93.6
250	0.80	0.971	194	30.2	5.99	181	93.4
250	0.73	0.963	175	30.3	5.39	163	93.1
250	0.66	0.953	157	30.3	4.79	145	92.6
250	0.59	0.942	140	30.3	4.19	127	90.7
250	0.53	0.926	122	30.3	3.59	109	89.2
250	0.46	0.903	103	30.3	2.99	90.8	87.8
250	0.39	0.869	84.3	30.4	2.39	72.5	86.0
250	0.33	0.820	67.0	30.4	1.79	54.4	81.1
250	0.26	0.734	48.5	30.4	1.19	36.2	74.7
250	0.23	0.479	27.1	30.4	0.59	17.9	65.9

Table 7 – Efficiency at 250 VAC, 30 V CV mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
265	1.51	0.971	388	30.1	12.0	360	92.9
265	1.43	0.970	368	30.1	11.4	343	93.1
265	1.36	0.968	348	30.1	10.8	325	93.2
265	1.29	0.965	329	30.1	10.2	307	93.4
265	1.21	0.962	309	30.1	9.59	289	93.5
265	1.14	0.957	290	30.2	8.99	271	93.6
265	1.07	0.952	270	30.2	8.39	253	93.7
265	1.00	0.945	251	30.2	7.79	235	93.8
265	0.93	0.939	232	30.2	7.19	217	93.7
265	0.86	0.932	213	30.2	6.58	199	93.6
265	0.79	0.924	194	30.3	5.99	181	93.4
265	0.72	0.915	175	30.3	5.39	163	93.1
265	0.65	0.904	157	30.3	4.79	145	92.6
265	0.59	0.893	140	30.3	4.19	127	90.8
265	0.52	0.878	122	30.3	3.59	109	89.2
265	0.46	0.855	103	30.3	2.99	90.8	87.8
265	0.39	0.819	84.3	30.4	2.39	72.5	86.0
265	0.32	0.777	66.8	30.4	1.79	54.4	81.3
265	0.31	0.602	49.7	30.4	1.19	36.2	72.9
265	0.23	0.419	25.5	30.4	0.59	17.9	70.0

Table 8 – Efficiency at 265 VAC, 30 V CV mode

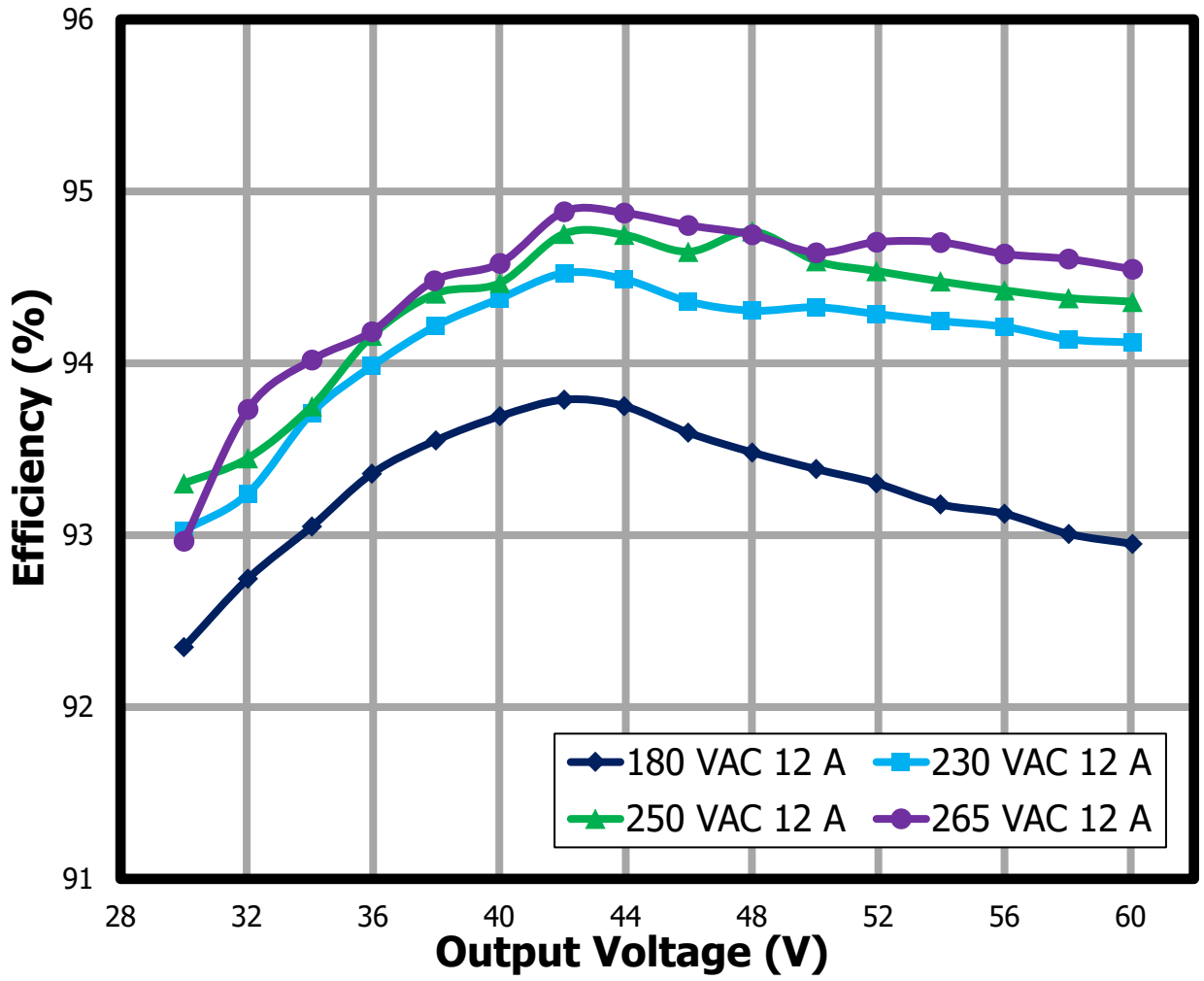


Figure 36 – Efficiency at 12 A CC Mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
179	4.35	777	0.997	60.1	12.0	722	92.9
179	4.19	749	0.997	58.0	12.0	697	93.0
179	4.04	722	0.997	56.0	12.0	672	93.1
179	3.89	695	0.996	54.0	12.0	647	93.2
179	3.74	668	0.996	51.9	12.0	623	93.3
179	3.60	643	0.996	50.0	12.0	601	93.4
179	3.46	618	0.996	48.0	12.0	577	93.5
179	3.31	592	0.995	46.0	12.0	554	93.6
179	3.16	565	0.995	44.0	12.0	529	93.8
180	3.03	540	0.994	42.1	12.1	507	93.8
180	2.89	516	0.994	40.0	12.1	483	93.7
180	2.75	491	0.993	38.0	12.1	459	93.6
180	2.62	466	0.993	36.0	12.1	435	93.4
180	2.49	443	0.992	34.1	12.1	412	93.1
180	2.35	418	0.992	32.0	12.1	388	92.7
180	2.22	394	0.987	30.0	12.1	364	92.3

Table 9 – Efficiency at 180 VAC, 12 A CC mode

Input Voltage (V_{AC})	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
229	3.37	768	0.994	60.1	12.0	723	94.1
230	3.25	742	0.994	58.0	12.0	698	94.1
230	3.13	715	0.994	56.0	12.0	673	94.2
230	3.02	688	0.993	54.0	12.0	649	94.2
230	2.91	663	0.993	51.9	12.0	625	94.3
230	2.80	639	0.993	50.0	12.0	602	94.3
230	2.69	613	0.993	48.0	12.0	578	94.3
230	2.58	588	0.992	46.0	12.1	555	94.4
230	2.46	561	0.992	44.0	12.1	530	94.5
230	2.36	537	0.992	42.1	12.1	508	94.5
230	2.25	513	0.992	40.0	12.1	484	94.4
230	2.14	488	0.992	38.0	12.1	460	94.2
230	2.04	464	0.991	36.0	12.1	436	94.0
230	1.94	441	0.990	34.1	12.1	413	93.7
230	1.83	417	0.992	32.0	12.1	389	93.2
230	1.72	391	0.992	30.0	12.1	364	93.0

Table 10 – Efficiency at 230 VAC, 12 A CC mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
249	3.11	768	0.990	60.1	12.1	724	94.4
250	3.00	741	0.989	58.0	12.1	699	94.4
250	2.89	714	0.989	56.0	12.0	674	94.4
250	2.78	687	0.989	54.0	12.0	649	94.5
250	2.68	661	0.989	51.9	12.0	625	94.5
250	2.58	637	0.989	50.0	12.0	603	94.6
250	2.48	612	0.989	48.0	12.1	580	94.8
250	2.38	586	0.989	46.0	12.1	555	94.6
250	2.27	560	0.989	44.0	12.1	530	94.7
250	2.18	538	0.988	42.1	12.1	509	94.8
250	2.07	513	0.992	40.0	12.1	485	94.5
250	1.97	488	0.991	38.0	12.1	461	94.4
250	1.87	463	0.991	36.0	12.1	436	94.2
250	1.78	441	0.991	34.1	12.1	413	93.8
250	1.68	416	0.991	32.0	12.1	389	93.4
250	1.58	390	0.990	30.0	12.1	364	93.3

Table 11 – Efficiency at 250 VAC, 12 A CC mode

Input Voltage (VAC)	Input Current (A)	PF	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
265	2.99	768	0.971	60.1	12.1	726	94.5
265	2.88	741	0.971	58.0	12.1	701	94.6
265	2.78	713	0.971	56.0	12.1	675	94.6
265	2.66	687	0.974	54.0	12.0	650	94.7
265	2.56	661	0.974	51.9	12.0	626	94.7
265	2.47	637	0.974	50.0	12.1	603	94.6
265	2.37	611	0.974	48.0	12.1	579	94.7
265	2.28	586	0.973	46.0	12.1	556	94.8
265	2.17	559	0.973	44.0	12.1	531	94.9
265	2.08	536	0.973	42.1	12.1	508	94.9
265	1.99	513	0.973	40.0	12.1	485	94.6
265	1.90	489	0.973	37.9	12.2	462	94.5
265	1.80	464	0.973	36.0	12.1	437	94.2
265	1.71	440	0.972	34.1	12.1	414	94.0
265	1.61	415	0.972	32.0	12.1	389	93.7
265	1.53	392	0.970	30.0	12.2	365	93.0

Table 12 – Efficiency at 265 VAC, 12 A CC mode

14.3 No-Load Input Power

The total no-load input power of both PFC and LLC including the daughter card was measured at room temperature with an integration time of 10 minutes. The output was completely disconnected from the load and the input power meter was the only probe connected. At 60 V CV mode, the converter was operating at Full Frequency (FF) mode during No Load condition. FF causes increased switching loss in the LLC primary and secondary devices. The converter was purposely designed to operate with FF down to very light loads, due to the output current ripple requirement of the charger. The daughter board was operating for all no-load tests.

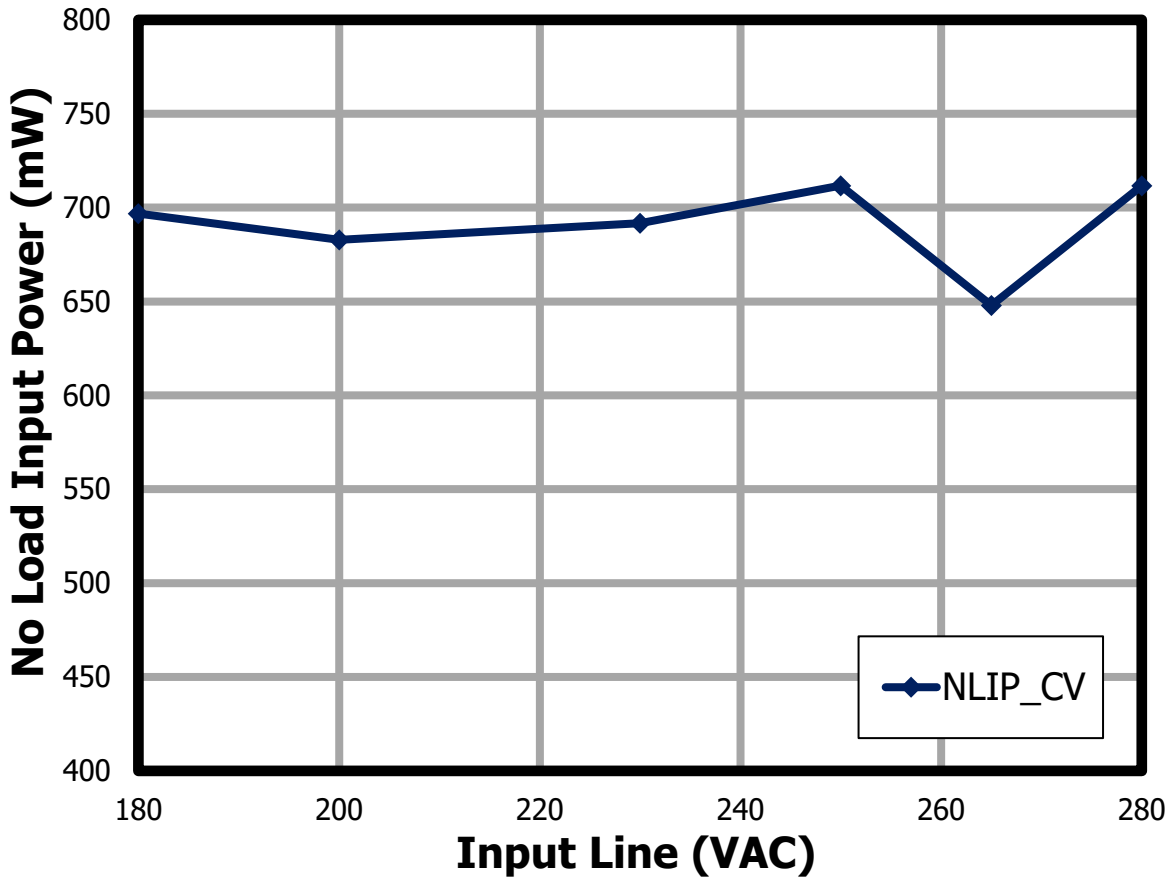


Figure 37 – No-Load Input Power

Input Line (VAC)	No Load Input Power (mW)
180	697
200	683
230	692
250	712
265	648
280	712

Table 13 – No-Load Input Power

14.4 Power Factor

Power Factor was measured at different line voltages with varying loads using a power meter. The converter operated in CV mode with the reference voltage set to 60 V. A variable AC source was used to supply a Sine wave input and a DC electronic load set to CC mode was used as load on the output.

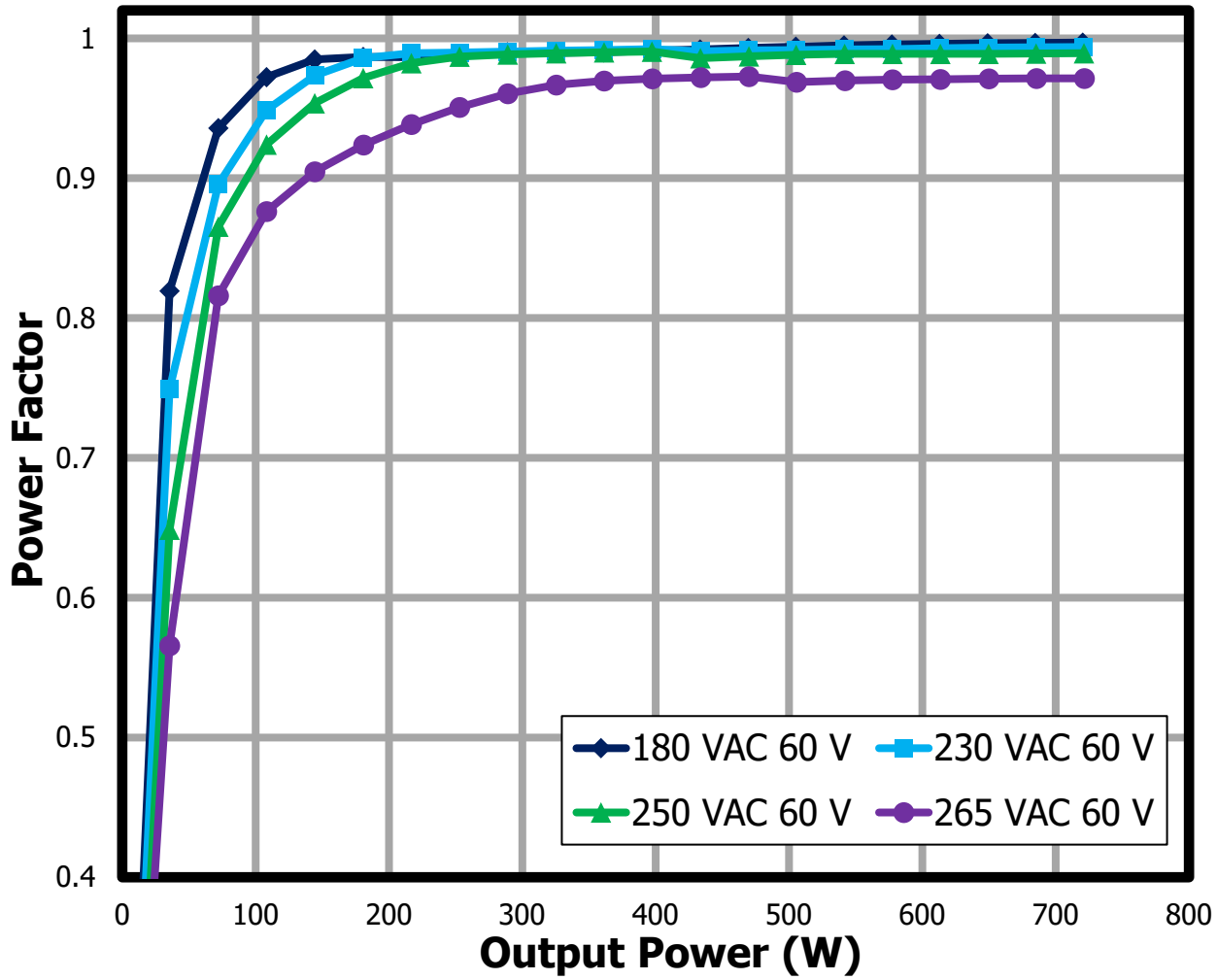


Figure 38 – Power Factor at 60V CV Mode

Load (W)	Power Factor (PF)			
	180 VAC	230 VAC	250 VAC	265 VAC
72 W (10% Load)	0.936	0.896	0.865	0.816
144 W (20% Load)	0.985	0.974	0.954	0.905
360 W (50% Load)	0.990	0.992	0.990	0.970
720 W (100% Load)	0.997	0.994	0.989	0.972

Table 14 – Power Factor across load at 60 V CV Mode

14.5 Total Harmonic Distortion

Total harmonic distortion (THD) in the AC Current was measured at different line voltages with varying loads using a power meter. The converter operated in CV Mode with the reference voltage as 60 V. A variable AC source was used to supply a sine wave input and a DC electronic load set to CC mode was used as load on the output.

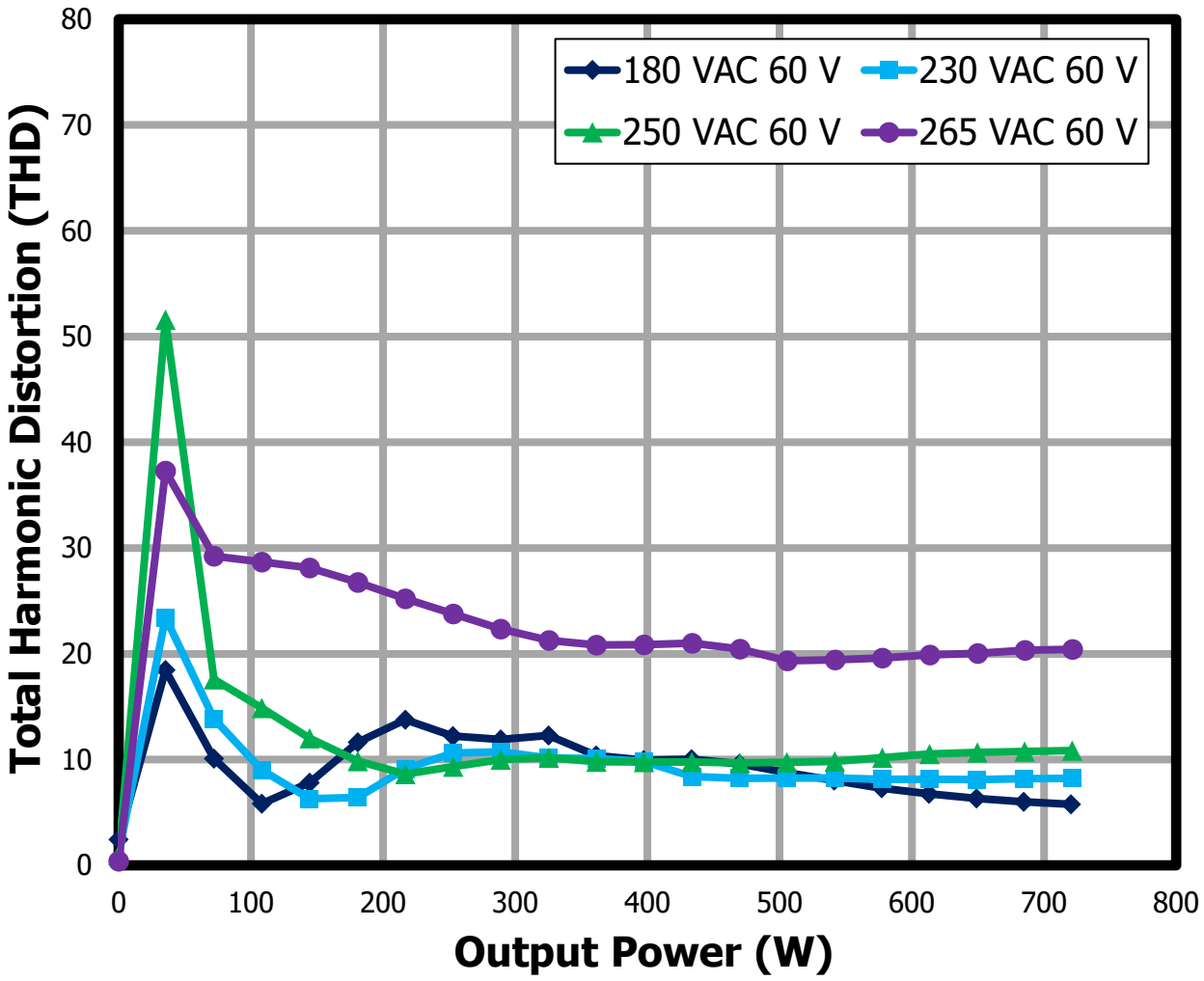


Figure 39 – Total Harmonic Distortion at 60 V CV Mode

14.6 Line Regulation

Line regulation was measured with an AC source connected to the input. The electronic load is set in CC mode to draw a constant current output from the power supply. The converter was controlled to be in CV Mode, with the reference set as 60 V. The load was varied with the electronic load and input AC voltage was varied with the AC source.

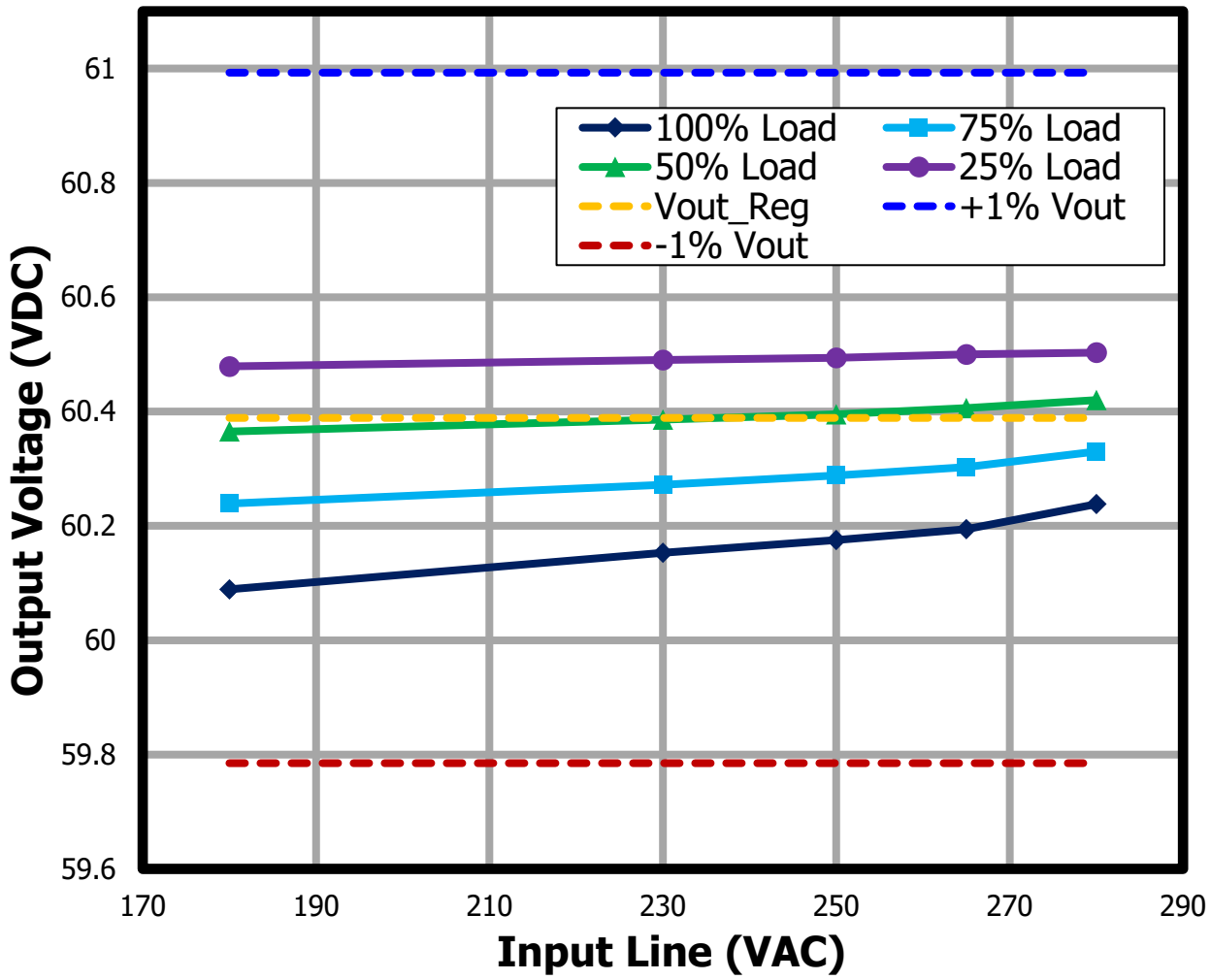


Figure 40 – Line Regulation at 60 V CV Mode

Input Voltage (VAC)	VOUT (V)			
	25% LOAD	50% LOAD	75% LOAD	FULL LOAD
180	60.5	60.4	60.2	60.1
230	60.5	60.4	60.3	60.2
250	60.5	60.4	60.3	60.2
265	60.5	60.4	60.3	60.2
280	60.5	60.4	60.3	60.2

Table 15 – Line Regulation across load at 60 V CV Mode

14.7 Load Regulation

Load regulation was measured by decreasing the load from full load down to zero using an DC electronic load. The test was repeated at different line voltages.

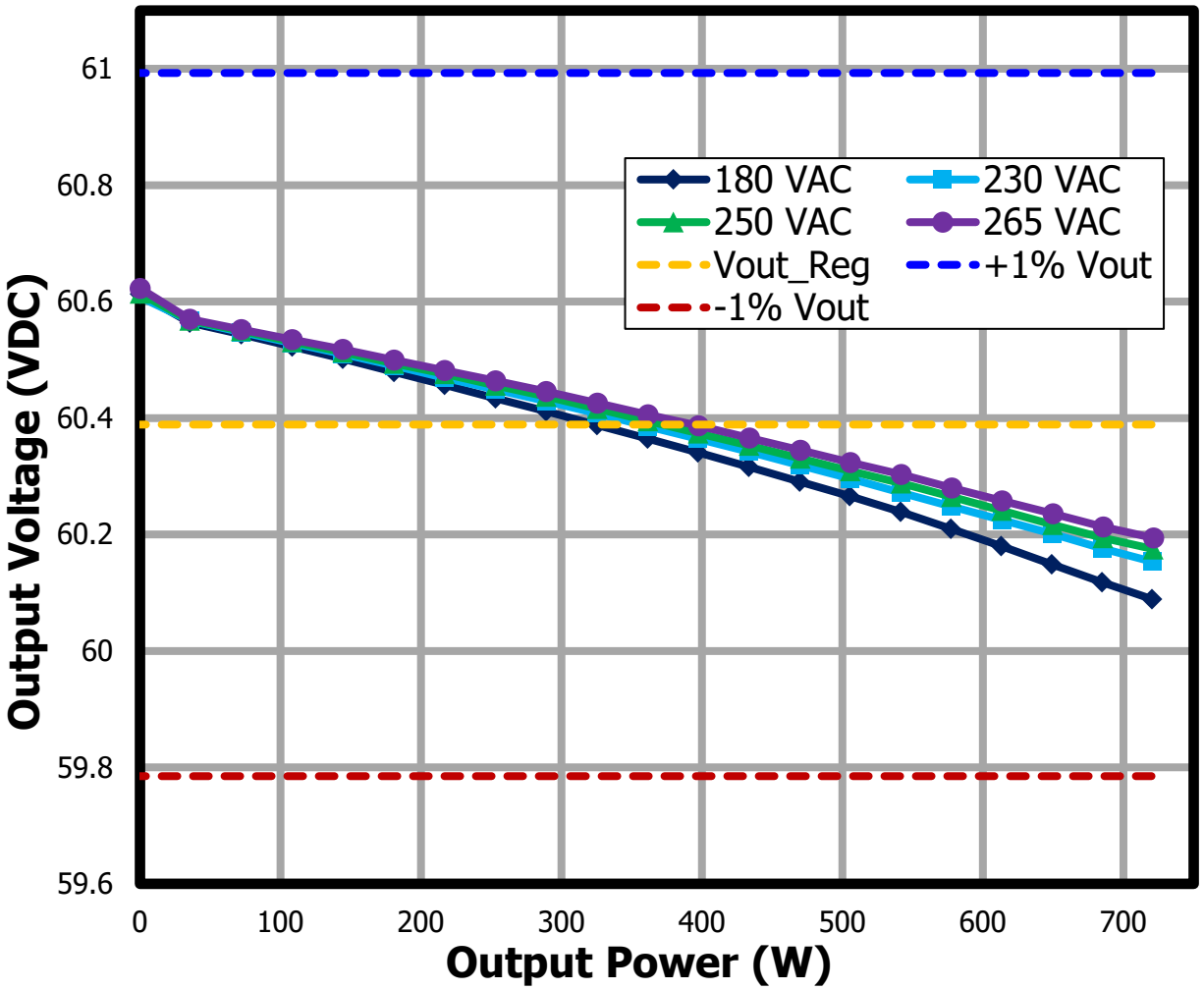


Figure 41 – Load Regulation at 60 V CV Mode

Input Voltage (VAC)	P_{OUT} (W)	V_{OUT} (V)
180	720	60.1
180	685	60.1
180	649	60.1
180	613	60.2
180	577	60.2
180	541	60.2
180	505	60.3
180	470	60.3
180	433	60.3
180	397	60.3
180	361	60.4
180	325	60.4
180	289	60.4
180	253	60.4
180	217	60.5
180	181	60.5
180	144	60.5
180	108	60.5
180	72.0	60.5
180	35.5	60.6

Input Voltage (VAC)	P_{OUT} (W)	V_{OUT} (V)
230	721	60.2
230	685	60.2
230	649	60.2
230	613	60.2
230	577	60.2
230	542	60.3
230	505	60.3
230	470	60.3
230	434	60.3
230	397	60.4
230	361	60.4
265	325	60.4
265	289	60.4
265	253	60.4
265	217	60.5
265	181	60.5
265	144	60.5
265	108	60.5
265	72.0	60.5
265	35.5	60.6

Table 16 – Load Regulation at 180 VAC and 230 VAC (60 V CV Mode)

Input Voltage (VAC)	P_{OUT} (W)	V_{OUT} (V)
250	721	60.2
250	685	60.2
250	650	60.2
250	613	60.2
250	578	60.3
250	542	60.3
250	506	60.3
250	470	60.3
250	434	60.4
250	397	60.4
250	361	60.4
250	325	60.4
250	289	60.4
250	253	60.5
250	217	60.5
250	181	60.5
250	144	60.5
250	108	60.5
250	72.0	60.6
250	35.5	60.6

Input Voltage (VAC)	P_{OUT} (W)	V_{OUT} (V)
265	721	60.2
265	686	60.2
265	650	60.2
265	614	60.3
265	578	60.3
265	542	60.3
265	506	60.3
265	470	60.3
265	434	60.4
265	397	60.4
265	361	60.4
265	325	60.4
265	289	60.4
265	253	60.5
265	217	60.5
265	181	60.5
265	144	60.5
265	108	60.5
265	72.0	60.6
265	35.5	60.6

Table 17 – Load Regulation at 250 VAC and 265 VAC (60 V CV Mode)

15 Waveforms

The figures below show the expected waveforms for different input voltage and output loading conditions set for the UUT.

15.1 Input AC Current, 100% Load – 60 V / 12 A

Input current was measured at varying line voltages with an electronic load set to CC mode at full load, 12 A.

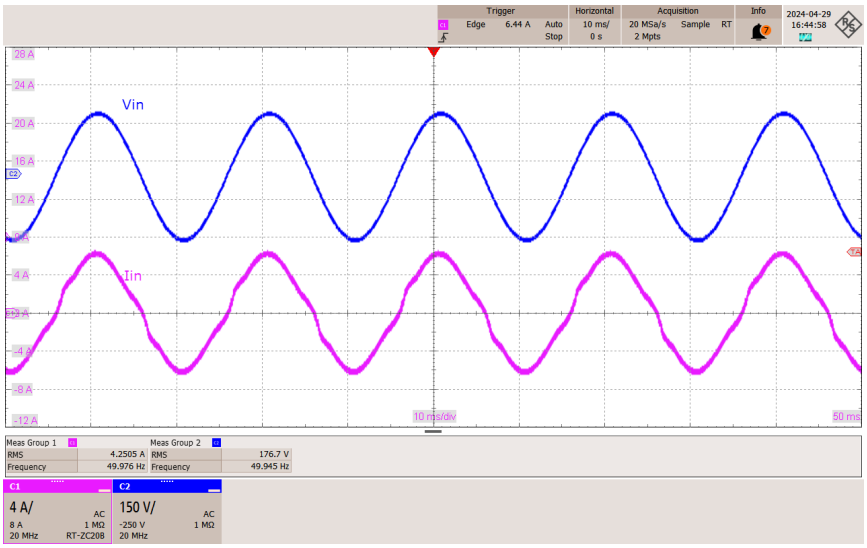


Figure 42 – Input Current, 180 VAC.
50 Hz, 10 ms/div.
CH1: I_{IN}, 4 A/div.
CH2: V_{IN}, 150 V/div.

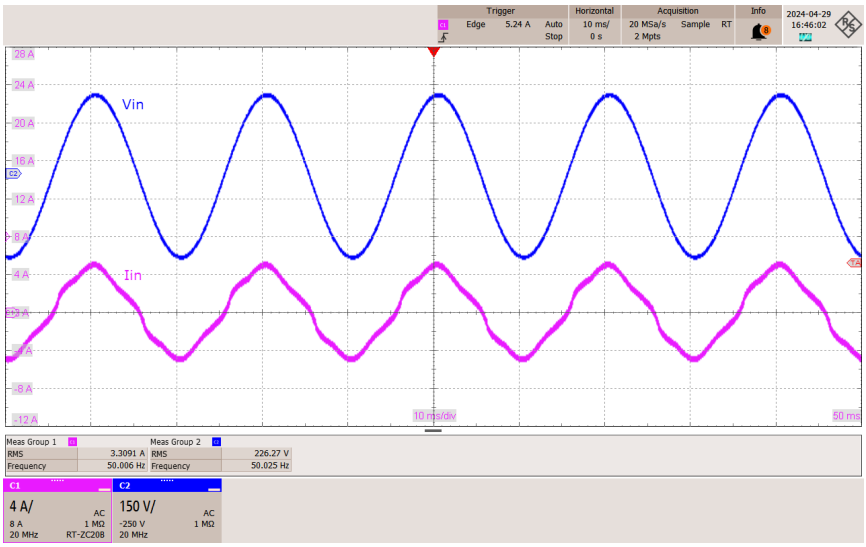


Figure 43 – Input Current, 230 VAC.
50 Hz, 10 ms/div.
CH1: I_{IN}, 4 A/div.
CH2: V_{IN}, 150 V/div.

15.2 PFC Voltage and Current, 100% Load

The figures below show the CCM operation of HiperPFS-3 with 230 VAC input.

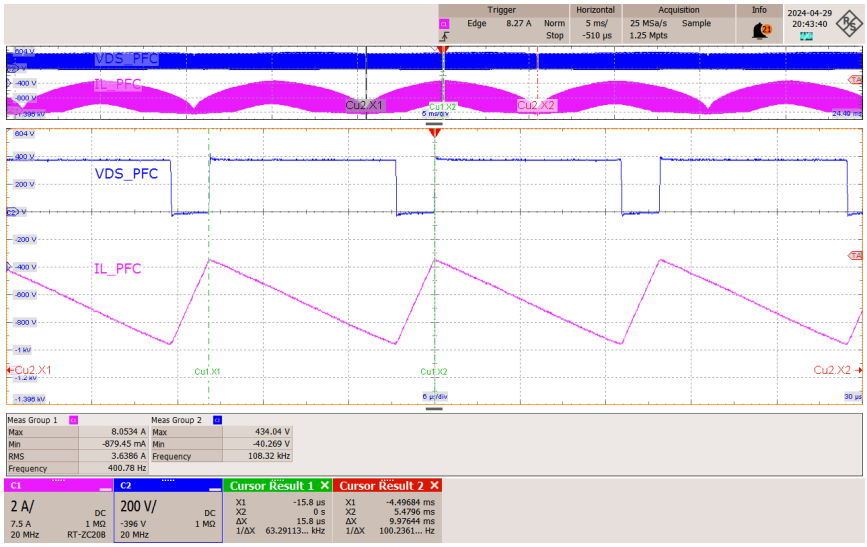


Figure 44 – VDS and Choke Current, 230 VAC.
Time Division: 5 ms/div.
Zoom Time Division: 6 μs/div.
CH1: IL_PFC, 2 A/div.
CH2: VDS_PFC, 200 V/div.

15.3 Start Up Waveforms

Input was supplied from an AC source and the output was connected to an electronic load set to full load. The load was disconnected for the no-load test. Figures 45 and 46 show the waveforms for V_{BULK}, VAC and V_{OUT} during start-up at both full load and no-load.

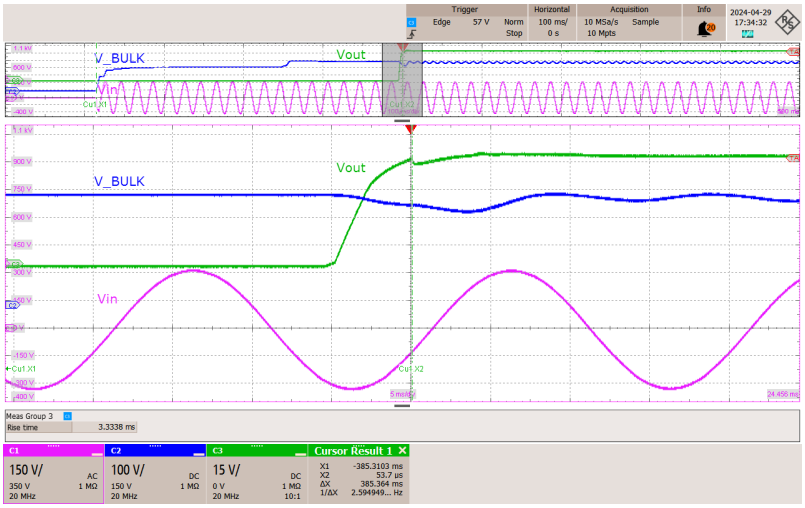


Figure 45 – Unit Start-up, 230 VAC, Full Load.
Regulation Time: 385.36 ms.
V_{OUT} Rise Time: 3.3338 ms.
Zoom Time Division: 5 ms/div.
CH1: V_{IN}, 150 V/div.
CH2: V_{BULK}, 100 V/div.
CH3: V_{OUT}, 15 V/div.

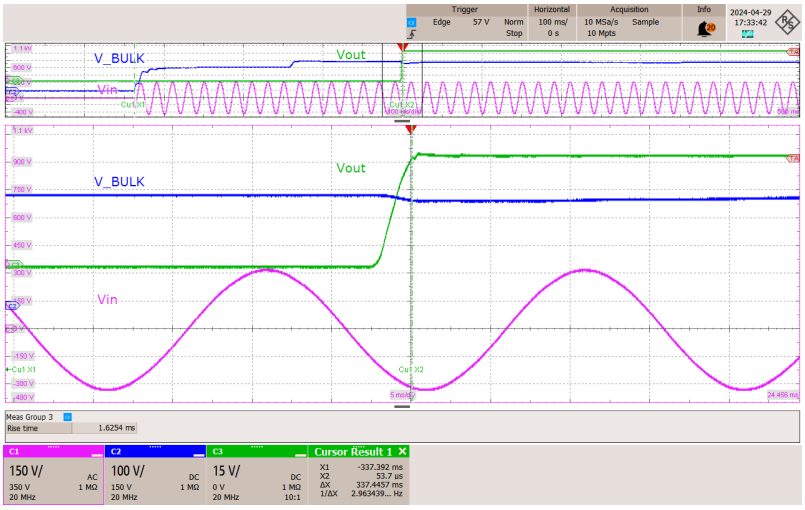


Figure 46 – Unit Start-up, 230 VAC, No Load.
Regulation Time: 337.45 ms.
V_{OUT} Rise Time: 1.6254 ms.
Zoom Time Division: 5 ms/div.
CH1: V_{IN}, 150 V/div.
CH2: V_{BULK}, 100 V/div.
CH3: V_{OUT}, 15 V/div.

15.4 LLC Primary Voltage and Current

Voltage and current of both LLC half-bridge and secondary output section with output loaded using an electronic load set to CC mode and varied at different loading conditions are shown in Figures 47-52.

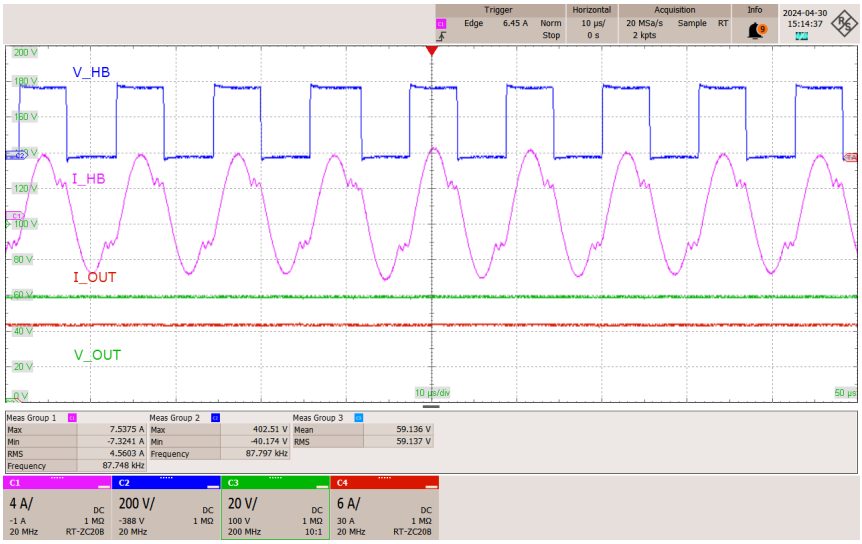


Figure 47 – LLC Stage Primary Voltage and Current, 60 V 12 A.
Time Division: 10 μs/div.
CH1: HB Current, 4 A/div.
CH2: HB Voltage, 200 V/div.
CH3: Output Voltage, 20 V/div.
CH4: Output Current, 6 A/div.

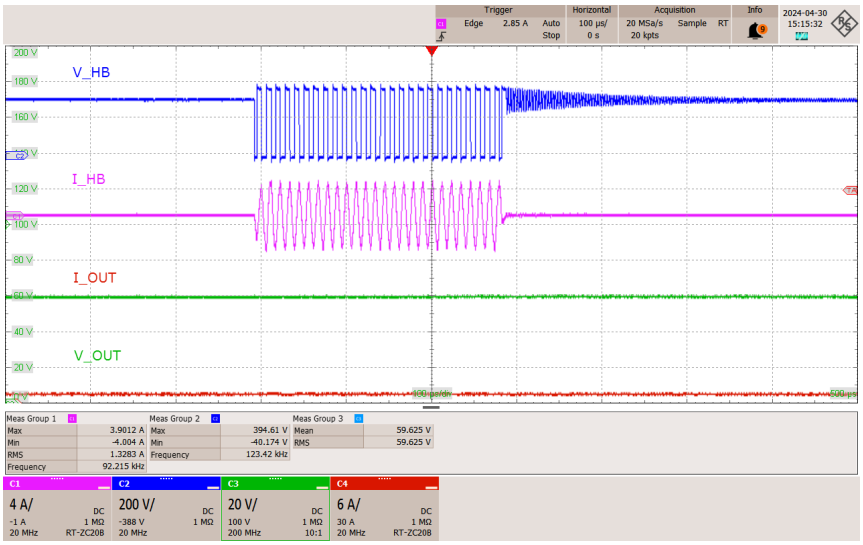


Figure 48 – LLC Stage Primary Voltage and Current, 60 V 0.2 A.
Time Division: 100 μs/div.
CH1: HB Current, 4 A/div.
CH2: HB Voltage, 200 V/div.
CH3: Output Voltage, 20 V/div.
CH4: Output Current, 6 A/div.

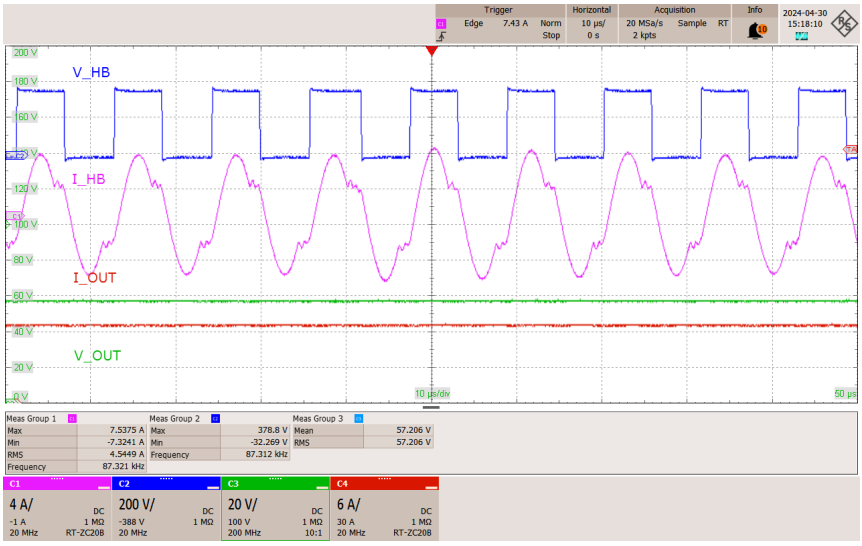


Figure 49 – LLC Stage Primary Voltage and Current, 58 V 12 A.
Time Division: 10 μs/div.
CH1: HB Current, 4 A/div.
CH2: HB Voltage, 200 V/div.
CH3: Output Voltage, 20 V/div.
CH4: Output Current, 6 A/div.

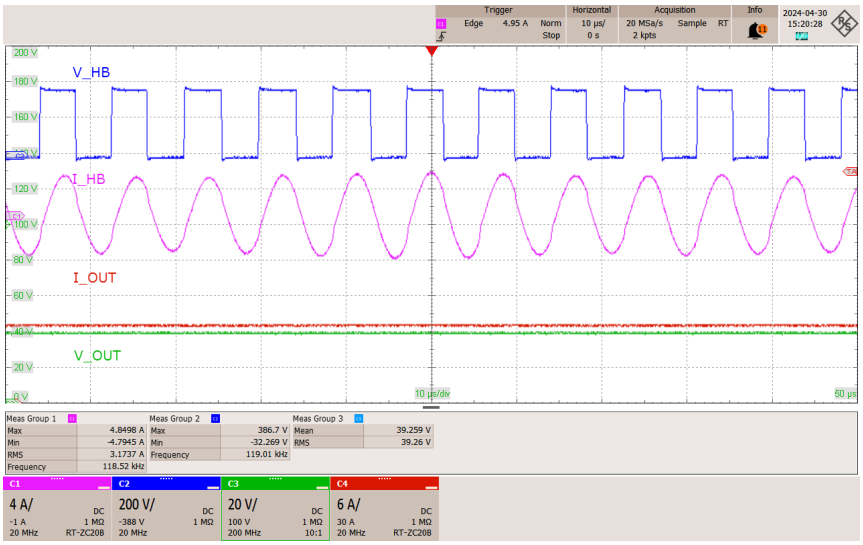


Figure 50 – LLC Stage Primary Voltage and Current, 40 V 12 A.
Time Division: 10 μs/div.
CH1: HB Current, 4 A/div.
CH2: HB Voltage, 200 V/div.
CH3: Output Voltage, 20 V/div.
CH4: Output Current, 6 A/div.

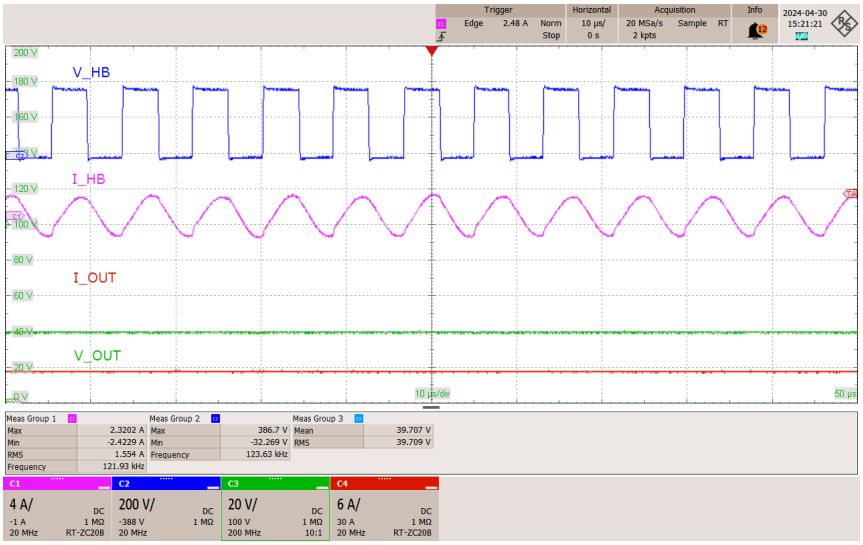


Figure 51 – LLC Stage Primary Voltage and Current, 40 V 4 A.
Time Division: 10 μs/div.
CH1: HB Current, 4 A/div.
CH2: HB Voltage, 200 V/div.
CH3: Output Voltage, 20 V/div.
CH4: Output Current, 6 A/div.

Figure 52 – LLC Stage Primary Voltage and Current, 30 V 4 A.
Time Division: 10 µs/div.
CH1: HB Current, 4 A/div.
CH2: HB Voltage, 200 V/div.
CH3: Output Voltage, 20 V/div.
CH4: Output Current, 6 A/div.

15.5 SR Waveforms

The voltage across the secondary synchronous rectifier MOSFET under continuous and discontinuous mode of operation were recorded at 60 V/ 12 A and 30 V/ 4 A and are shown in Figures 53 and 54 respectively.

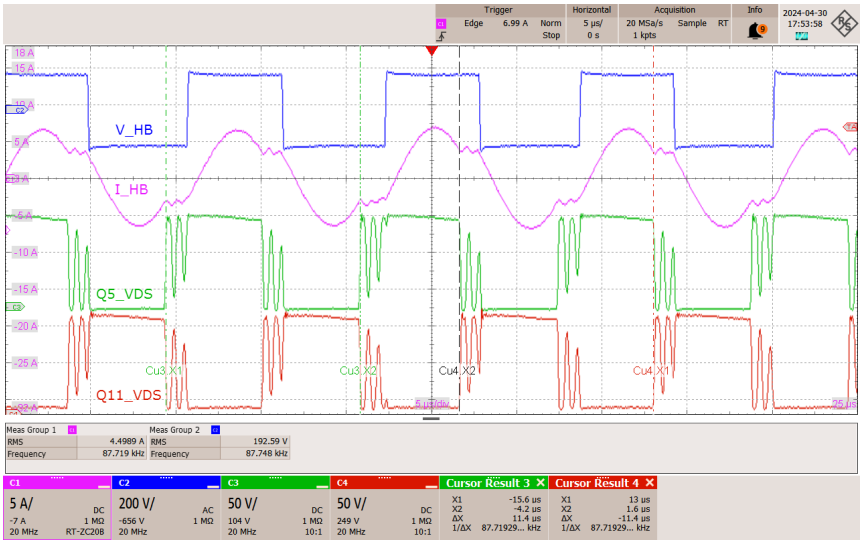


Figure 53 – Output Rectifier Peak Reverse Voltage at 60 V, 12 A.
Time Division: 5 μs/div.
CH1: HB Current, 5 A/div.
CH2: HB Voltage, 200 V/div.
CH3: Q_5 V_{DS}, 50 V/div.
CH4: Q_{11} V_{DS}, 50 V/div.

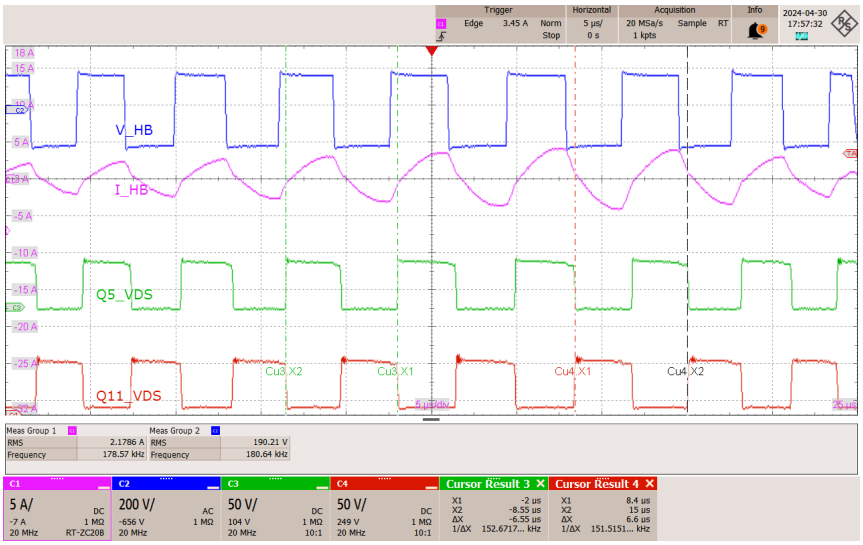


Figure 54 – Output Rectifier Peak Reverse Voltage at 30 V, 4 A.
Time Division: 5 μs/div.
CH1: HB Current, 5 A/div.
CH2: HB Voltage, 200 V/div.
CH3: Q_5 V_{DS}, 50 V/div.
CH4: Q_{11} V_{DS}, 50 V/div.

15.6 Dynamic Loading

Figure 55 and 56 show the response of the LLC converter during a dynamic loading at 60 V output in CV mode.

Electronic Load setting was as follows:
Duty Cycle = 50%, Frequency = 100 Hz, Slew Rate = 800 mA/μs.

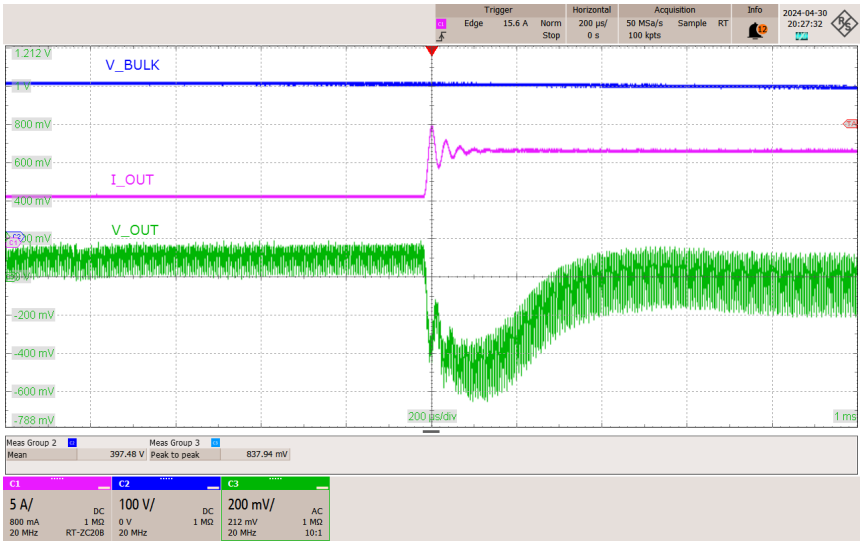


Figure 55 – Dynamic Loading, 230 VAC, 50-100% Load.
Time Division: 200 μs/div.
1.40% Output Regulation Change.
CH1: I_{OUT}, 5 A/div.
CH2: V_{BULK}, 100 V/div.
CH3: V_{OUT}, 200 mV/div.

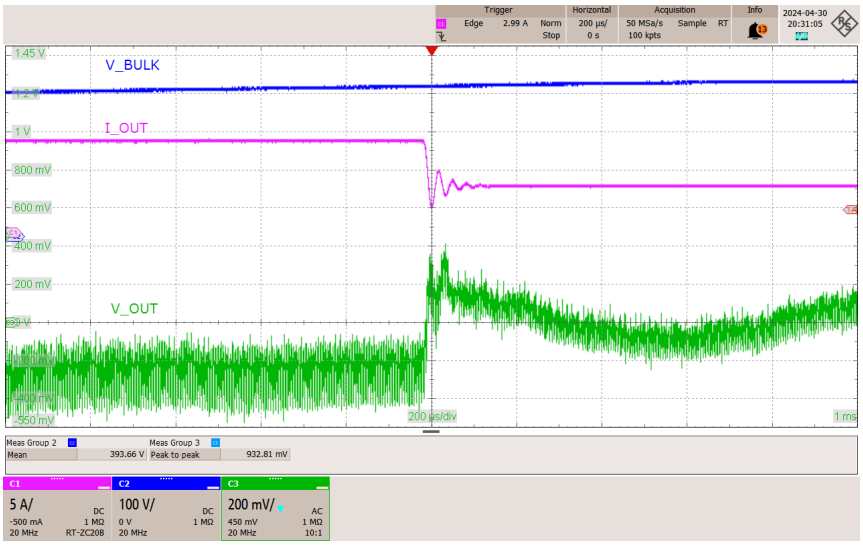


Figure 56 – Dynamic Loading. 230 VAC, 100-50% Load
Time Division: 200 µs/div.
1.55% Output Regulation Change.
CH1: I_{OUT}, 5 A/div.
CH2: V_{BULK}, 100 V/div.
CH3: V_{OUT}, 200 mV/div.

16 Temperature Profiles

The board was placed in horizontal position and 1 foot away from a fan (non-enclosed set-up) with electronic load set at constant current mode with full load current of 12 A. UUT was soaked for 1 hour before measurement was made.

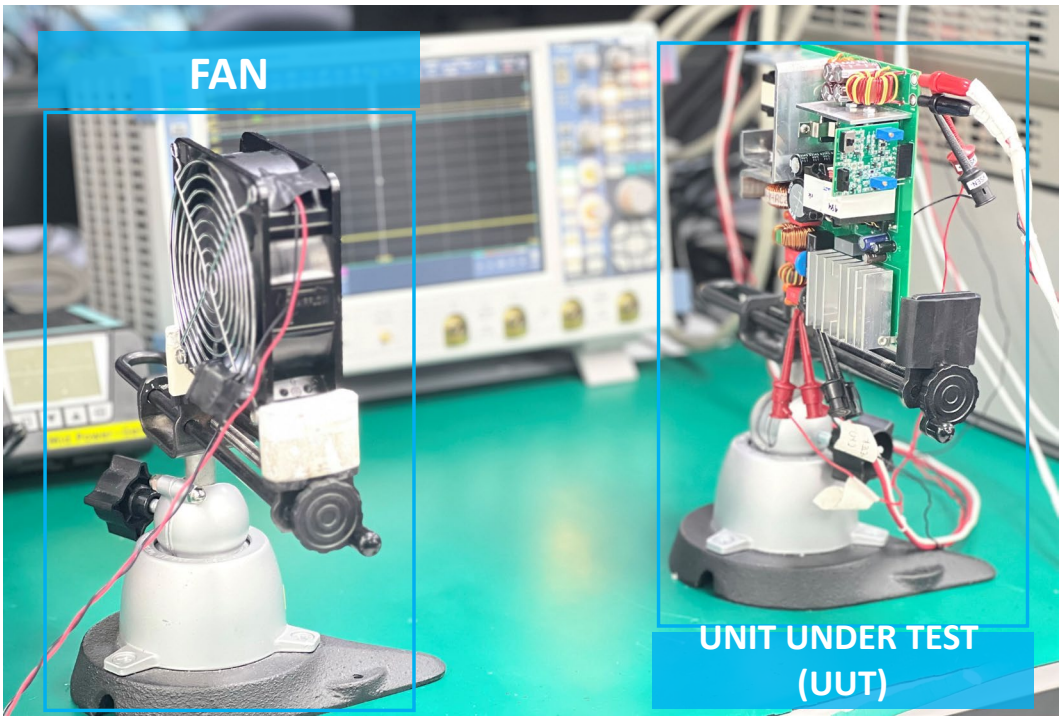
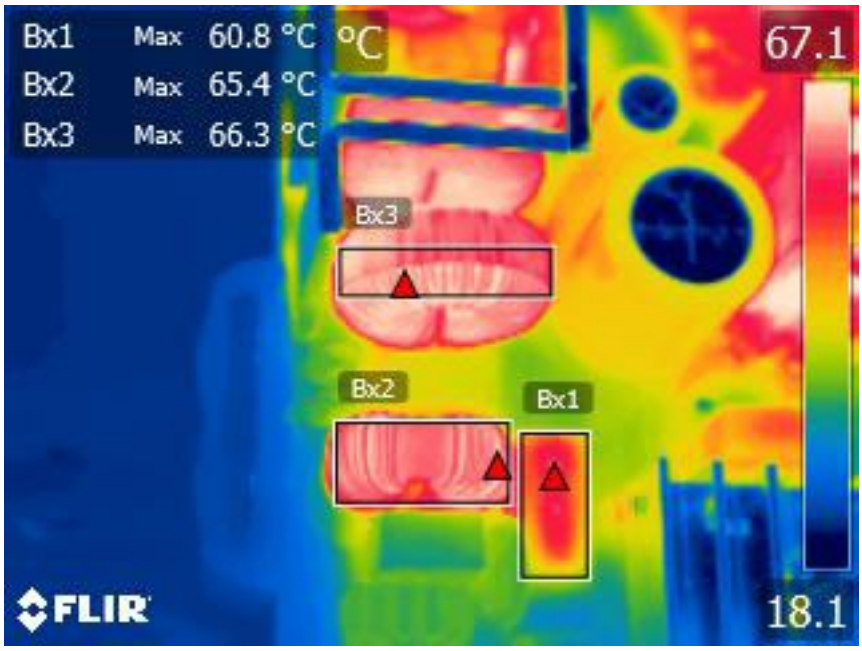


Figure 57 – Thermals Test Set-up

Fan Specifications:

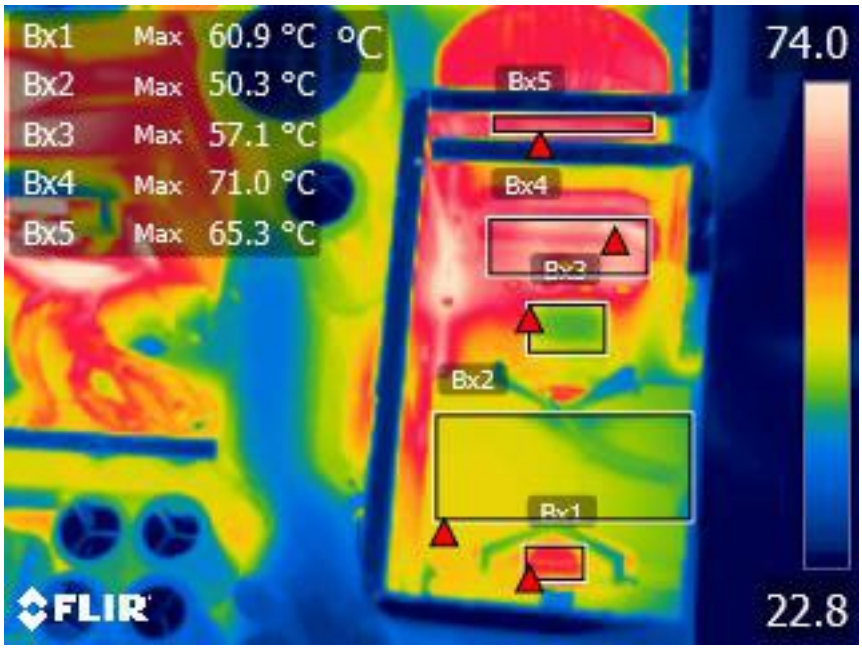
- Fan Type: Axial Fan
- Voltage Rating: 220 – 240 V
- Frequency: 50/60 Hz
- Power Current: 0.125/0.11 A
- Air Speed: 2900 RPM
- Direction of Air Flow: Horizontal

16.1 180 VAC, 50 Hz, 720 W Output



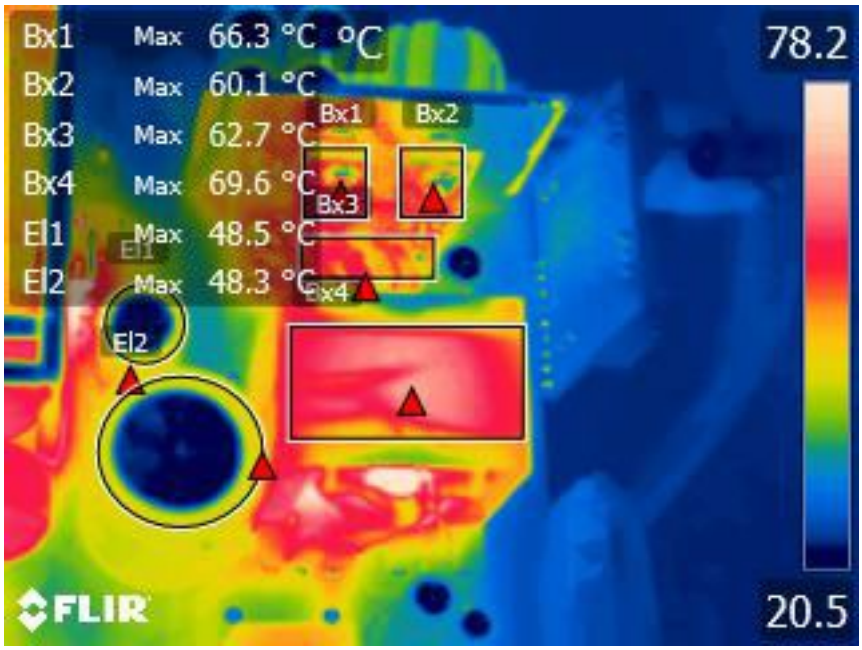
Legend	Ref. des.	Description	Temperature (˚C)
BX1	RT1	THERMISTOR	60.8
BX2	L4	CMC	65.4
BX3	L1	DIFF CHK	66.3
		AMBIENT	24

Figure 58 – EMI Side, 100% Load, 180 VAC.



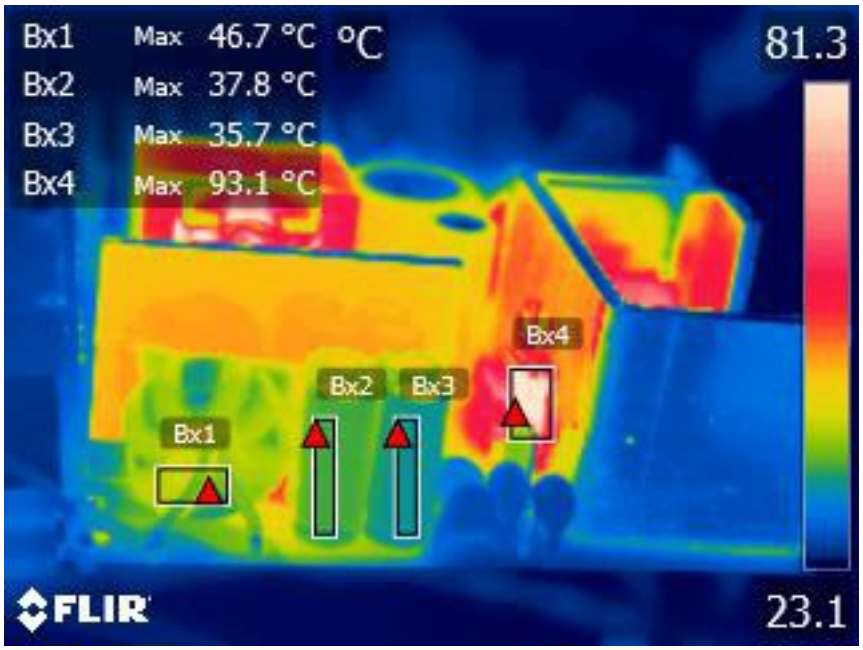
Legend	Ref. des.	Description	Temperature (˚C)
BX1	T2	PFC CHK WIRE	60.9
BX2	T2	PFC CHK CORE	50.3
BX3	C34	XCAP	57.1
BX4	BR1	BRIDGE DIODE 1	71.0
BX5	BR2	BRIDGE DIODE 2	65.3
		AMBIENT	24

Figure 59 – Bridge Rectifier and PFC Side, 100% Load, 180 VAC.



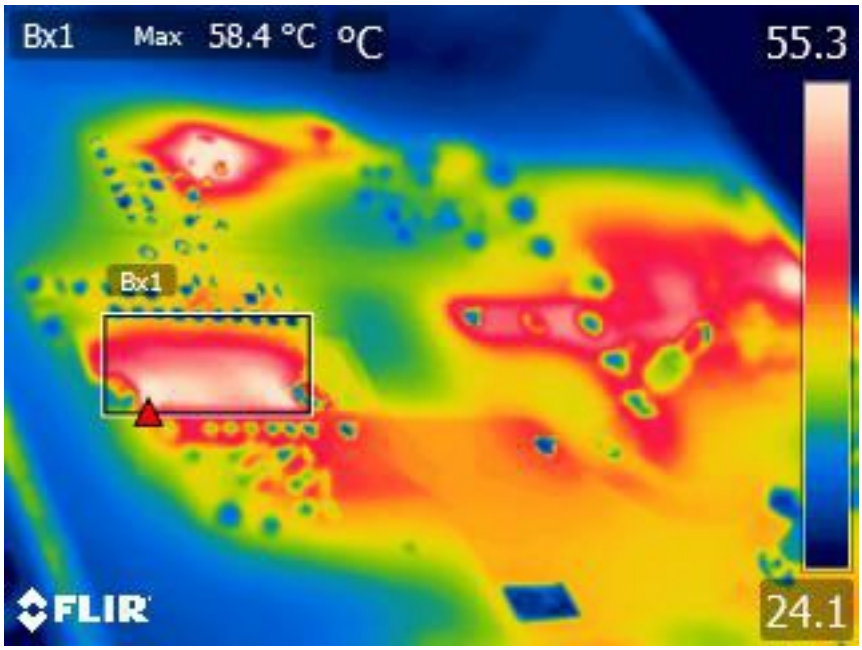
Legend	Ref. des.	Description	Temperature (˚C)
BX1	Q5	SR2	66.3
BX2	Q11	SR1	60.1
BX3	T1	LLC TRF WDG	62.7
BX4	T1	LLC TRF CORE	69.6
El1	C49	BULK CAP 2	48.5
El2	C40	BULK CAP 1	48.3
		AMBIENT	24

Figure 60 – LLC Primary and Secondary Side, 100% Load, 180 VAC.



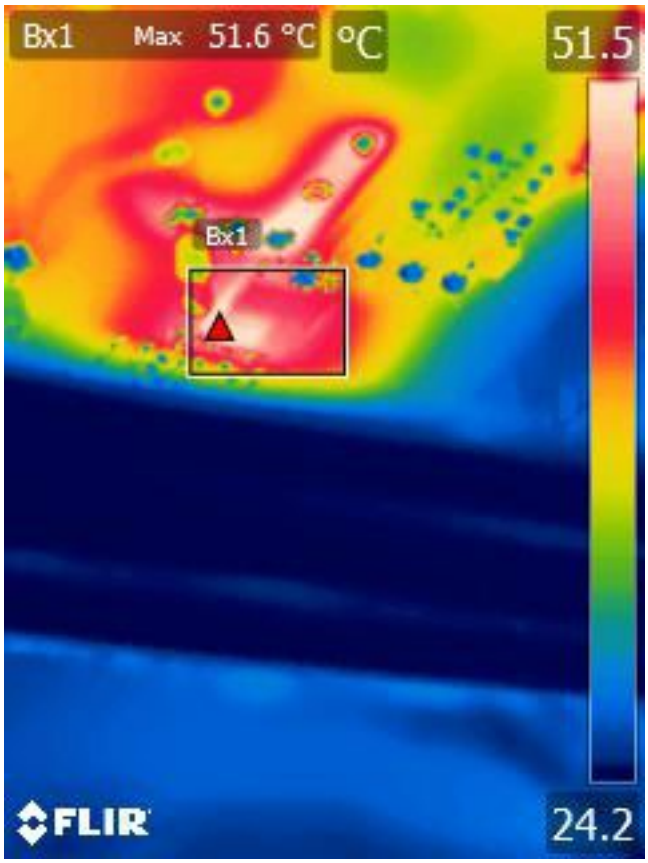
Legend	Ref. des.	Description	Temperature (˚C)
BX1	L5	OUTPUT CMC	46.7
BX2	C21	OUTPUT ECAP 4	37.8
BX3	C18	OUTPUT ECAP 3	35.7
BX4	U6	HIPERPFS-3	93.1
		AMBIENT	24

Figure 61 – PFS and Secondary Side, 100% Load, 180 VAC.



Legend	Ref. des.	Description	Temperature (˚C)
BX1	U1	HIPERLCS-2 HB	58.4
		AMBIENT	24

Figure 62 – Bottom Side Thermal Picture, 100% Load, 180 VAC.



Legend	Ref. des.	Description	Temperature (˚C)
BX1	U4	HIPERLCS-2 SR	51.5
		AMBIENT	24

Figure 63 – Bottom Side Thermal Picture, 100% Load, 180 VAC.

17 Revision History

Date	Author	Revision	Description and Changes	Reviewed
27-Feb-25	AAM	A	Initial Release	Apps & Mktg

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