Design Example Report

Title	**720 W DC-DC LLC Resonant Half-bridge Converter with Synchronous Rectification Using HiperLCS™2-HB LCS7268Z and HiperLCS2-SR LSR2000C**
Specification	400 VDC Input; 48 VDC Output
Application	High Efficiency Isolated DC-DC Conversion
Author	Applications Engineering Department
Document Number	DER-978
Date	January 15, 2025
Revision	A

Summary and Features

- Integrated LLC and SR-driver stages reduce component count
- Master controller allows precise control of synchronous rectification to maximize efficiency
- High efficiency across line and load
  - >97% full load conversion efficiency across line
  - 98% efficient at 50% load and nominal line
  - 95% efficient at 10% load across line
- No Load input power <71 mW
- High frequency (up to 250 kHz) LLC ensures small transformer size.
- Secondary-side sensing and feedback control provides fast transient response
- Integrated synchronous rectification driver

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PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at https://www.power.com/company/intellectual-property-licensing/.

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Important Notes:
Although this board is designed to meet safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer and a suitable rectification stage to provide the DC input to the prototype board.
Since there is no separate bias converter in this design, ~380-400 VDC is present on bulk capacitor C1 immediately after the supply is powered down. For safety, this capacitor must be discharged with an appropriate resistor (10 kΩ, 2 W resistor is recommended), or the supply must be allowed to stand for at least 10 minutes before handling.

1 Introduction

This report describes a DC-DC 720 W, 48 V, 15 A power supply. The circuit is designed to operate from a fixed DC input that ranges from 380 VDC to 420 VDC.

The circuit is a resonant half-bridge (LLC) that employs the HiperLCS-2 chipset – a half bridge primary device and a secondary master controller with an integrated SR driver and barrier crossing technology (FluxLink™). In addition, the ICs provide comprehensive protection features.

Figure 1 – DER-978, Top View.

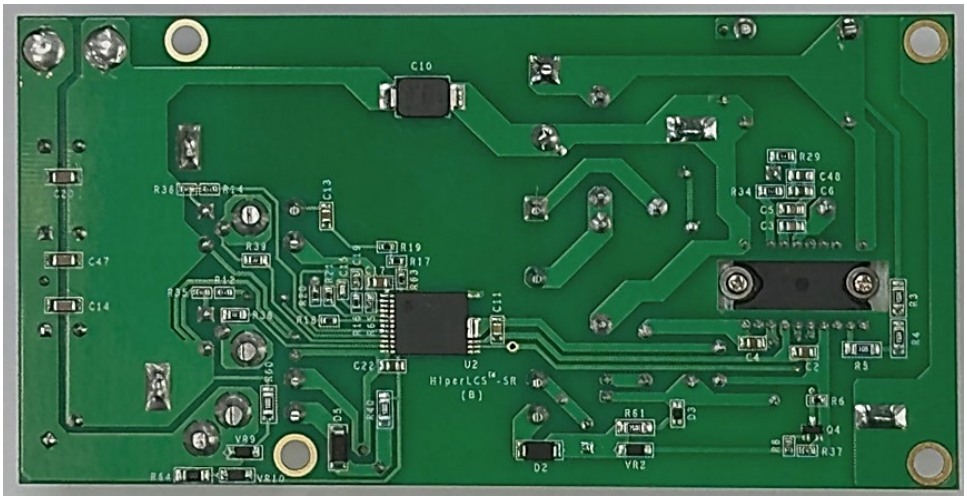


Figure 2 – DER-978, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min.	Typ.	Max.	Units	Comments
Input						
Voltage	V_{IN}	380	400	420	VDC	DC-Input
No Load Input Power	$P_{IN(NL)}$		70		mW	measured at 400 VDC
Main Converter Output						
Output Voltage	V_{OUT}		48		V	±1% Output regulation
Output P-P Ripple Voltage	V_{RIPPLE}			650	mV_{PK-PK}	Within 1% of output at full load
Output Current	I_{OUT}		15		A	Full load
Total Output Power						
Continuous Output Power	P_{OUT}		720		W	Full load
Efficiency						
100% Load	η_{Main}		97.4		%	Measured at 400 VDC input.
50% Load			98.0			
20% Load			97.0			
Ambient Temperature	T_{AMB}	0		40	°C	See thermal design section of report for operating conditions.

3 Schematic

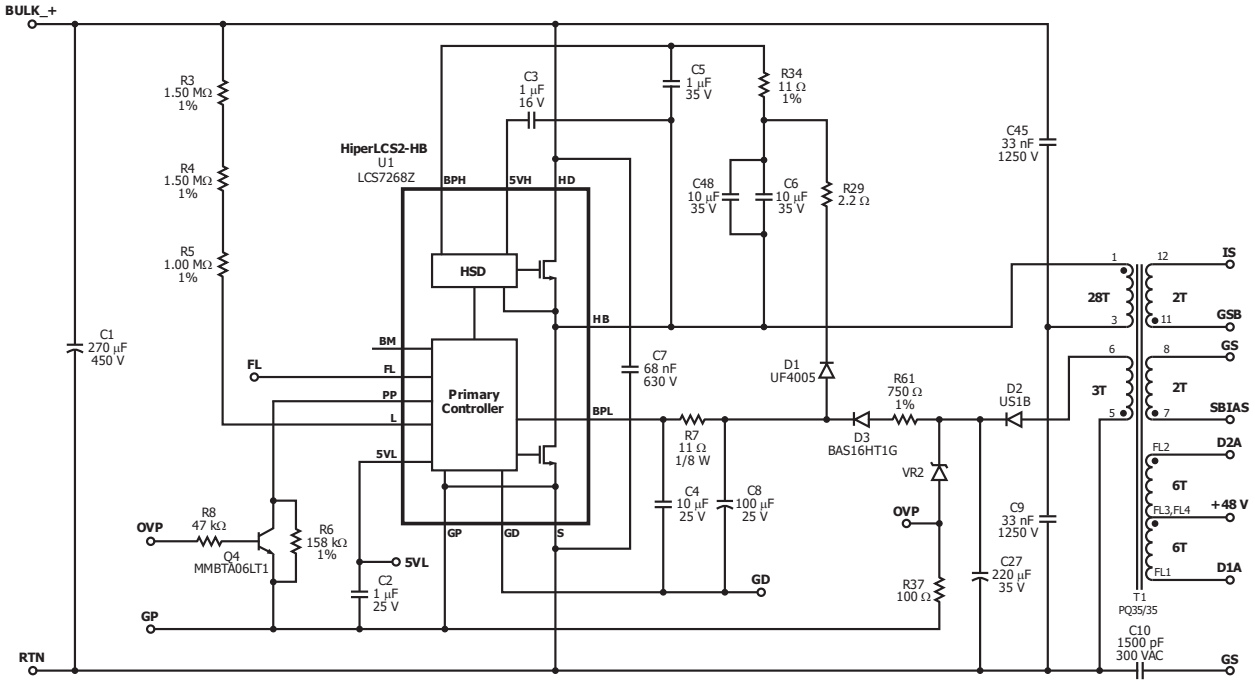


Figure 3 – Schematic of LLC Stage (Primary Side)

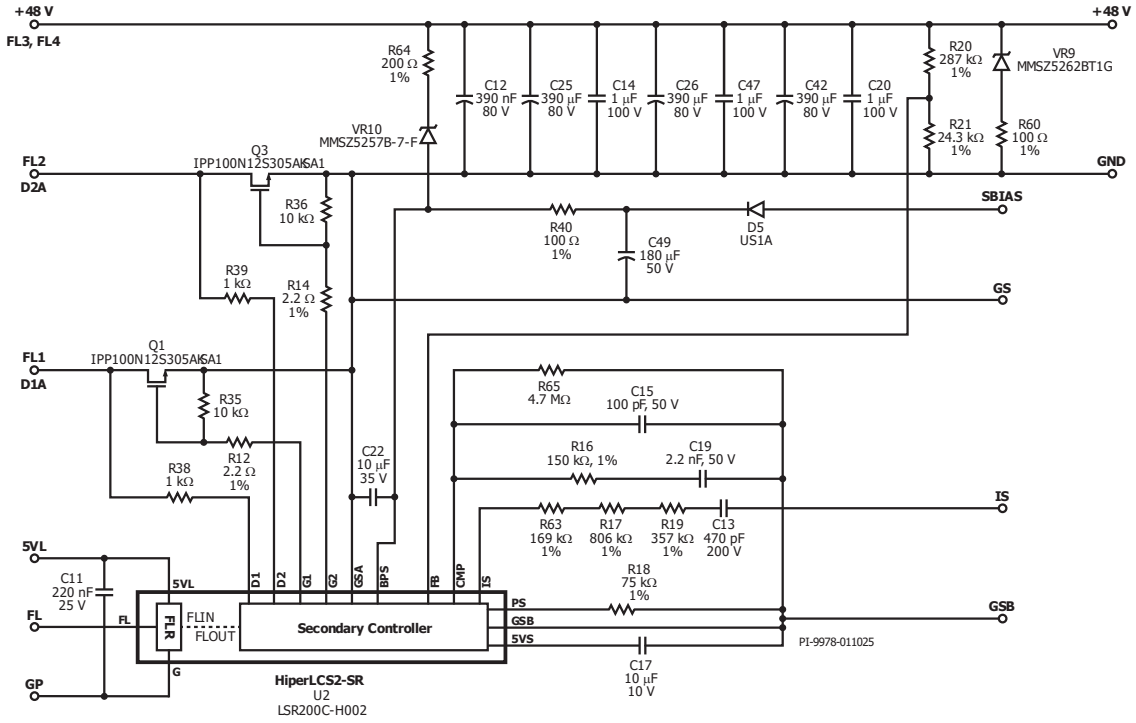


Figure 4 – Schematic of LLC Stage (Secondary Side)

4 Circuit Description

4.1 LLC Converter

The design consists of an LLC converter using the HiperLCS2-HB IC, a primary half-bridge with integrated MOSFETs, and the HiperLCS2-SR IC, a secondary master controller with secondary-primary communication that includes integrated safety rated isolation, and a synchronous rectification driver stage.

4.2 LLC Primary

The high-voltage input bus is filtered through capacitor C1. Line sense (L-pin) detects the input bus voltage via resistors R3, R4 and R5. The HiperLCS2-HB IC, U1, will initiate soft-start when the L-pin goes above UV+ threshold. Output overvoltage is sensed from the primary bias-winding (pin 5 and pin 6) of transformer T1, via Zener diode VR2 and resistor R37 and coupled to the PP pin via resistor R8 and transistor Q4. When an output over-voltage occurs, Zener VR2 conducts and current will be pulled from the PP pin to ground via transistor Q4 which interrupts switching. In normal operation, Resistor R6 sets the primary frequency range via the PP pin.

Capacitors C2 and C4 decouple the 5VL and BPL pins referencing them to GP and GD respectively. The primary return power-ground, RTN, is connected to the S-pin (SOURCE), primary-bias winding and bias capacitor. It is very important to keep the small signal ground (GP), separate from the system power-ground (RTN). The RTN power-ground offers a low-impedance path for system noise, allowing secondary-coupled noise currents to be safely delivered to the RTN/bulk-capacitor ground without disturbing the small-signal ground (GP pin).

Diode D2 rectifies the primary bias winding voltage. Capacitor C27 provides decoupling to the RTN ground. Capacitor C4 provides local high-frequency decoupling for the BPL-pin. During start-up, before switching commences, the BPL pin charges capacitors C4 and C8, via resistor R7. The resistor limits output current from the BPL pin. Capacitor C8 provides energy storage to sustain start-up prior to the primary bias winding becoming energized which only occurs once switching begins. Capacitor C8 provides boot-strap energy to the HiperLCS2-HB high-side bias via diode D1 and resistor R29. Capacitor C8 should be large enough to provide the necessary bias during startup. As a guide, the capacitance of C8 should be more than 5x the sum of the capacitance of high-side bias capacitors C6 and C48.

Prior to bias winding activation during start-up, diode D3 acts as a blocking diode to prevent the charge current supplied by the BPL pin from being diverted to charge capacitor C27. During normal operation the bias current flows from the bias winding to capacitor C27. The BPL-pin has an internal shunt regulator to limit the BPL voltage. Resistor R61 limits

the BPL shunt-current when BPL shunt-voltage-clamping is active, limiting BPL power dissipation.

Careful attention should be paid to the steady state bias-winding voltage. If voltage is above the BPL clamp threshold, it will cause additional power dissipation in the BPL circuitry which may induce thermal shutdown of the HiperLCS-2 IC. It is important to recognize that the bias winding voltage may vary by up to 25% when the output load changes from zero to full load. For best no-load performance, the bias should be designed to deliver a minimum of 15 V. The BPL shunt will engage if the bias voltage at the BPL pin exceeds 21 V.

During the on-period of the low-side power MOSFET, the high-side bootstrap is charged via diode D1 and resistor R29 feeding capacitors C6 and C48. For the first few switching cycles at startup, capacitor C6 and C48 typically carry no charge and resistor R29 is required to limit current. Resistor R34 and capacitor C5 provide additional low-frequency filtering to the BPH pin. The high-side 5VH pin is decoupled via capacitor C3. Note that all high-side decoupling is tied to the HB pin.

The resonant tank inductance is the sum of inductance L_R (transformer-integrated resonant inductor) and magnetizing inductance, L_M, which appear in series between the HB pin and the node formed by the junction of capacitors C9 and C45.

Y-capacitor C10 provides decoupling between primary and secondary grounds to reduce common mode noise on the secondary controller induced by primary-side switching noise.

4.3 LLC Secondary

The HiperLCS2-SR (U2) IC has primary side pins that are safety-isolated from the secondary side. Pin 5VL on the primary side of the HiperLCS2-SR is connected to the 5V reference provided by the 5VL pin on the HiperLCS2-HB IC. This connection provides power for the primary-side of the HiperLCS2-SR IC. The GP pin on the HiperLCS2-SR IC couples to the primary small signal ground pin of the HiperLCS2-HB IC. Capacitor C11 provides local decoupling to the 5VL and GP pins of U2. The FL pin provides a control signal generated by the master controller on the secondary-side of the HiperLCS2-SR IC which is passed across the isolation barrier to the primary-side via the integrated FluxLink magneto inductive communication link. This control signal is delivered to the HiperLCS2-HB IC.

Transformer T1 output pins FL3/FL4 provide the positive output voltage, which is rectified by SR MOSFETs Q3 and Q4, and filtered by capacitors C12, C14, C20, C25, C26, C42 and C47. These capacitors have low combined ESR, which is the predominant factor in determining output ripple. Their combined capacitance should be chosen to provide the desired off-time in burst-mode. The capacitors are connected to the secondary-side power ground (GND).

Transformer output pins T1 FL1/FL2 provide the return path for synchronous rectifier MOSFETs Q1 and Q3 respectively. The secondary power path is from T1 FL3/FL4 through capacitors C12, C14, C20, C25, C26, C42 and C47. To optimize matching of the two secondary power-phases, it is important to ensure that the secondary power path lengths of Q1 and Q3 are equal.
Capacitor C22 decouples the BPS pin, connecting it to the secondary SR-drive ground (GSA pin). Capacitor C17 decouples the 5VS pin connecting it to the secondary small signal ground (GSB pin).

Transformer T1 pin 7 feeds a diode D5 and capacitor C49 to rectify and filter the secondary bias voltage. The bias return is connected to T1 pin 8 and the secondary power ground (GND rail). The Zener diode VR9 and resistor R60 provide a small pre-load to ensure the output maintains regulation during no-load operation. Resistor R64 limits the current through VR10 and provides a limit to the bias voltage on the BPS pin.

Output voltage is sensed via feedback resistors R20 and R21 which are referenced to GSB, the secondary small signal ground.

The small signal secondary ground (GSB pin) is used as a reference for feedback and compensation and provides the ground for IS-pin signals. The GSA pin is used to return SR-gate-drive signals. Loop compensation is positioned between the CMP and GSB pins - provide a 2 poles (formed by C19 plus R16, and C15) and a zero (C15, R16). The transformer IS winding T1 presented on pins 12 and 11 is grounded to the GSB pin and provides high frequency small-signal information which is capacitor coupled via C13 and resistors R17, R19 and R63 to the IS pin.

Pin D1 and D2 sense the drain voltages on the synchronous rectifiers Q1 and Q3 via resistors R38 and R39 respectively. The resistors limit the negative sensing current (WRT GND) into both pins. The resistor values are used to control the SR MOSFET turn-off thresholds. Increasing the resistor value will cause the SR MOSFET to turn off at higher SR current.

Drive for the Q1 and Q3 synchronous MOSFETs is driven by the output of pins G1 and G2 via resistors R12 and R14. The drive resistors are optional and limit high-frequency MOSFET driver ringing. In the event of an FMEA open-connection fault condition between G1/G2 and Q1/Q3 gate, local pull-down resistors R35 and R36 ensure that Q1 and Q3 remain off.

The PS pin resistor R18 is used to select burst threshold.

5 PCB Layout

The reference design employs the single layer PCB shown below. The board dimensions are 137.4 x 70.0 mm.

5.1 PCB Specifications

- Layer Count: 1 layer
- Solder Mask: Green
- Silkscreen: White
- Finish: ENIG
- Board Thickness: 1.6 mm
- Copper Thickness: 2 oz (2.8 mils)
- Material: FR4

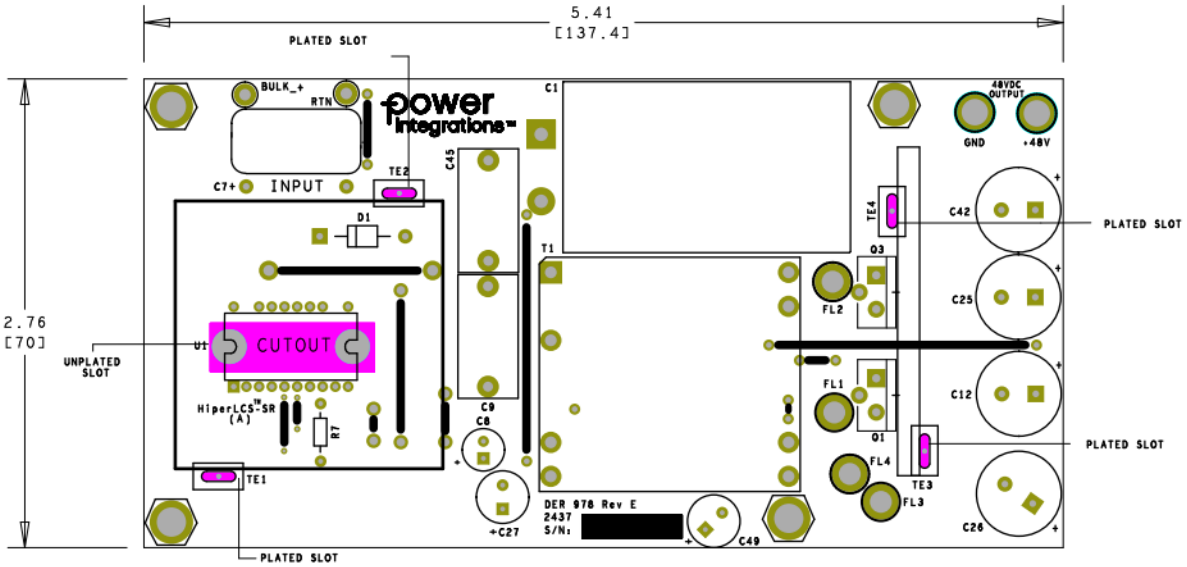


Figure 5 – Printed Circuit Layout, Top Side.

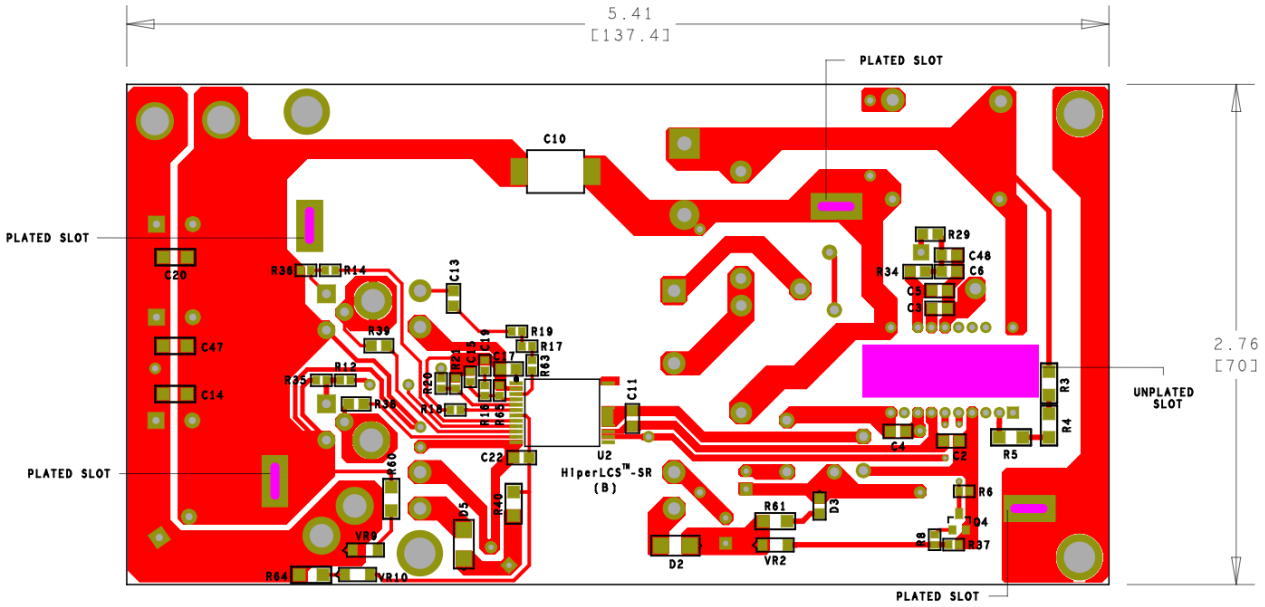


Figure 6 – Printed Circuit Layout, Bottom Side.

5.2 PCB Assembly Instructions

The reference design uses a single layer PCB design. Shown below is the bare printed circuit board (PCB) top side with the identified jumper locations. There are 10 jumper connections using AWG 24 wire.

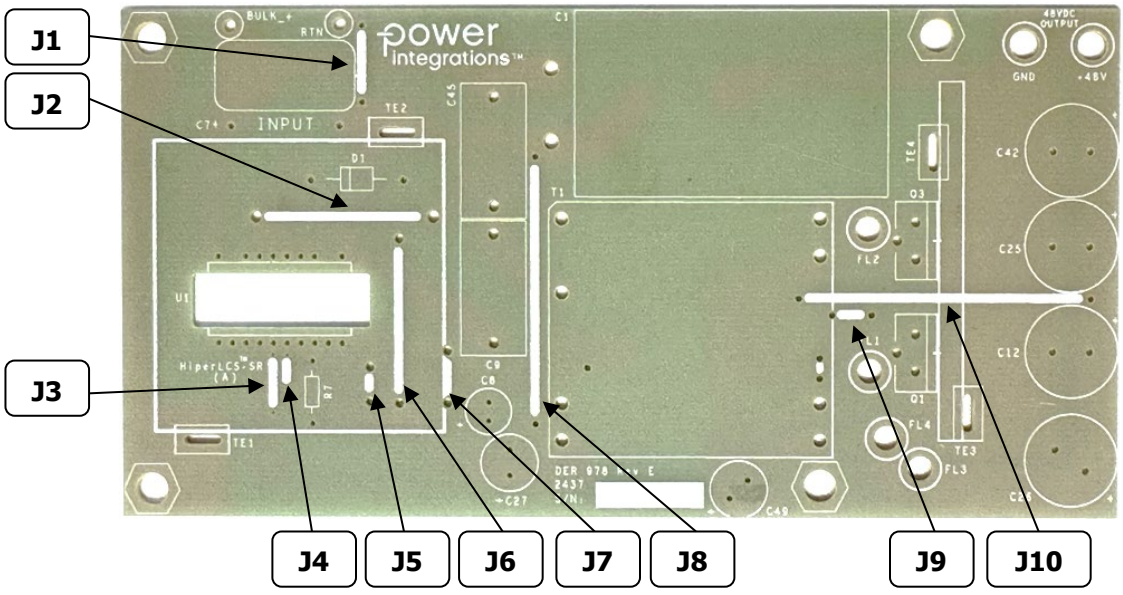


Figure 7 – PCB with Jumper Designations

Table 1 Jumper Cables

Ref Des	Total Jumper Wire Length (mm)
J1	17
J2	31
J3	14
J4	10
J5	11
J6	29
J7	14
J8	43
J9	11
J10	46

6 Bill of Materials

6.1 Electrical Parts

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	1	C1	270 µF, 450 V, Electrolytic, (25.4 x 40)	ESMQ451VSN271MQ40S	United Chemi-con
2	1	C2	1 µF, ±10%, 25 V, Ceramic, X7R, 0805 (2012 Metric)	GCM21BR71E105KA56L	Murata Electronics North America
3	1	C3	CAP, CER, 1 µF, 16 V, X7R, 0805	GRM21BR71C105KA01K	Murata Electronics North America
4	1	C4	10 µF ±10% 25 V Ceramic Capacitor X7S 0805 (2012 Metric)	C2012X7S1E106K125AC	TDK Corporation
5	1	C5	1 µF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX Corporation
6	3	C6, C22, C48	10 µF ±10% 35 V Ceramic Capacitor X5R 0805 (2012 Metric)	C2012X5R1V106K125AC	TDK Corporation
7	1	C7	68 nF, 630 V, Film	ECQ-E6683KF	Panasonic
8	1	C8	100 µF, 25 V, Electrolytic, Very Low ESR, 130 mOhm, (6.3 x 11)	EKZE250ELL101MF11D	Nippon Chemi-Con
9	2	C9, C45	0.033 µF, Film Capacitor, 500 VAC 1250 VDC (1.25 kV), Polypropylene (PP), Metallized Radial	B32652A7333J000	EPCOS - TDK Electronics
10	1	C10	1500 pF, ±20%, 300 VAC, X1, Y1, Ceramic Capacitor E, Nonstandard SMD	DK1E3EA152M86RBH01	Murata Electronics
11	1	C11	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
12	4	C12, C25, C26, C42	390 µF, 80 V, Electrolytic, Low ESR, (12.5 x 26.5)	EKZN800ELL391MK25S	United Chemi-Con
13	1	C13	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
14	3	C14, C20, C47	1 µF, 100 V, Ceramic, X7R, 1206	C3216X7R2A105K	TDK Corp
15	1	C15	100 pF 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
16	1	C17	10 µF, ±10%, 10 V, Ceramic Capacitor, Soft Termination, X7R, 0805 (2012 Metric)	C2012X7R1A106K125AE	TDK Corp
17	1	C19	2.2 nF 50 V, Ceramic, X7R, 0603	C0603C222K5RACTU	Yageo
18	1	C27	220 µF, 35 V, Electrolytic, Very Low ESR, 56 mOhm, (8 x 15)	EKZE350ELL221MH15D	Nippon Chemi-Con
19	1	C49	180 µF, 50 V, Electrolytic, Very Low ESR, 46 mOhm, (8 x 20)	EKZE500ELL181MH20D	Nippon Chemi-Con
20	1	D1	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
21	1	D2	DIODE ULTRA FAST, 1 A, 100 V, SMA	US1B-13-F	Diodes, Inc
22	1	D3	75 V, 200 mA, Rectifier, SOD323	BAS16HT1G	ON Semiconductor
23	1	D5	DIODE ULTRA FAST GPP 50 V, 1 A, SMA	US1A-13-F	Diodes, Inc
24	2	Q1, Q3	MOSFET, N-Channel, 120 V, 100 A (Tc), 300 W (Tc), Through Hole PG-TO220-3-1, TO-220,TO-220AB,TO-220-3	IPP100N12S305AKSA1	Infineon Technologies
25	1	Q4	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1	Infineon Tech
26	2	R3, R4	RES, 1.50 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
27	1	R5	RES, 1.00 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1004V	Panasonic
28	1	R6	RES, 158 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1583V	Panasonic
29	1	R7	RES, 11 R, 5%, 1/8 W, Carbon Film	299-11-RC	Xicon
30	1	R8	RES, 47 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
31	2	R12, R14	RES, 2.2 R, 1%, 1/16 W, Thick Film, 0603	ERJ-3RQF2R2V	Panasonic
32	1	R16	RES, 150 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1503V	Panasonic
33	1	R17	RES, 806 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF8063V	Panasonic
34	1	R18	RES, 75.0 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF7502V	Panasonic
35	1	R19	RES, 357 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3573V	Panasonic
36	1	R20	RES, 287 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2873V	Panasonic
37	1	R21	RES, 24.3 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2432V	Panasonic
38	1	R29	RES, 2.2 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R2V	Panasonic
39	1	R34	RES, 11 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF11R0V	Panasonic
40	2	R35, R36	RES, 10 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
41	1	R37	RES, 100 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
42	2	R38, R39	RES, 1 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
43	2	R40, R60	RES, 100 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1000V	Panasonic
44	1	R61	RES, 750 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7500V	Panasonic
45	1	R63	RES, 169 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1693V	Panasonic
46	1	R64	RES, 200 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2000V	Panasonic
47	1	R65	RES, 4.7 M, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ475V	Panasonic
48	1	T1	Bobbin, PQ35/35, Vertical, 12 pins	B65882B0012T001	TDK
49	1	U1	HiperLCS2-HB, LCS7268Z, POWeDIP-20B	LCS7268Z	Power Integrations
50	1	U2	HiperLCS2-SR, LSR2000C-H002, InSOP-24D	LSR2000C-H002	Power Integrations
51	1	VR2	DIODE ZENER 39 V 500 MW SOD123	MMSZ5259BT1G	Onsemi
52	1	VR9	DIODE ZENER 51 V 500 MW SOD123	MMSZ5262BT1G	Onsemi
53	1	VR10	DIODE ZENER 33 V 500 MW SOD123	MMSZ5257B-7-F	Diodes, Inc

6.2 Mechanical Parts

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	1	HS1	SHTM, HEATSINK, DER978_SR_MOSFET, DRW, AL, 3003, Extrusion, Custom.	61-00359-00	Custom
2	1	HS2	SHTM, HEATSINK, Heatsinks\DER-978_PCD, DRW, AL, 3003, Extrusion, Custom.	61-00341-00	Custom
3	4	STDOFF1, 2, 3, 4	Standoff Hex,6-32, .375L, F/F, NYL, 94V-0	8441B	Keystone Elect
4	4	TE1, TE2, TE3, TE4	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	Zierick

7 Magnetics

7.1 LLC Transformer

7.1.1 Electrical Diagram

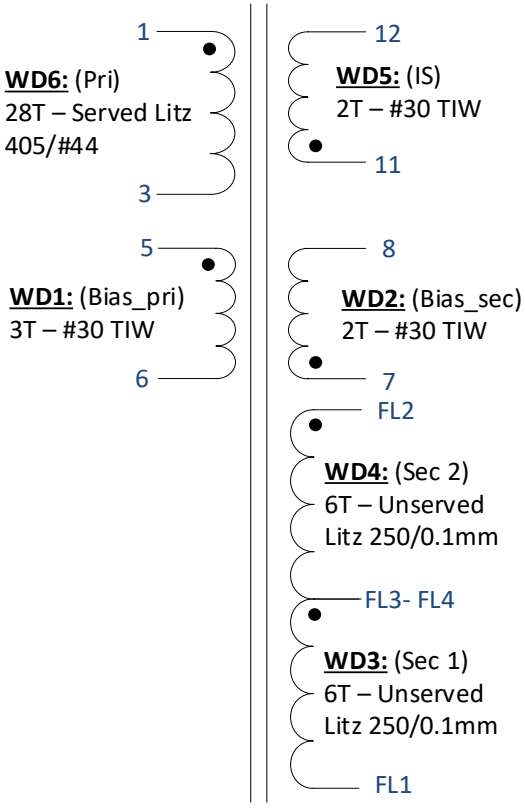


Figure 8 – LLC Transformer Electrical Diagram

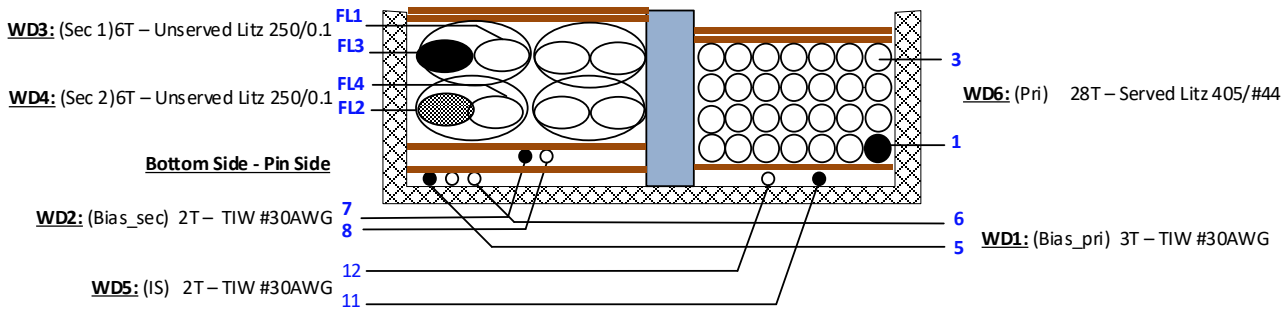
7.1.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1,3,5,6 to FL1-FL3, FL2-FL4, pins 7,8,11,12.	3000 VAC
Primary Inductance (Lpri)	Pins 1-3, all other windings open, measured at 100 kHz, 1 Vrms	350 µH ±5%
Primary Leakage1 (LlkpALL)	Pins 1-3, short **ALL** other pins except IS-winding pins 11-12, measured at 100 kHz, 1 Vrms	60 µH ±5%
Primary Leakage2 (LkpIS)	Measured at Pins 1-3 (100 kHz, 1 Vrms), Short **ONLY** IS-winding Pins 11-12.	45 µH
Primary Leakage3 (LkpSEC1)	Measured at Pins 1-3 (100 kHz, 1 Vrms), Short **ONLY** FL2, FL3, FL4	63 µH
Primary Leakage4 (LkpSEC2)	Measured at Pins 1-3 (100 kHz, 1 Vrms), Short **ONLY** FL1, FL3, FL4	63 µH
Resonant Frequency (Fres)	Measured Frequency	2 MHz

7.1.3 Material List

Item	Description
[1]	Core: PQ3535 – PC95 (TDK) or equivalent
[2]	Bobbin with Cover: PQ3535-V, 12pins (6/6)
[3]	Litz wire: 405/#44 AWG_Served Litz. Alternate Part (Litz wire: 270/#42 AWG_Served Litz)
[4]	Litz wire: 0.100/250_Unserved Litz. Alternate Parts (Litz wire: 0.100/125 twist together; 0.100/500 split in half)
[5]	Triple Insulated Wire: #30AWG
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 9 mm wide.
[7]	Tape: 3M 1298 Polyester Film, 1 mil thick, 10 mm wide.
[8]	Tape: 3M 1298 Polyester Film, 1 mil thick, 11 mm wide.
[9]	Separator Tape: 3 mm wide.

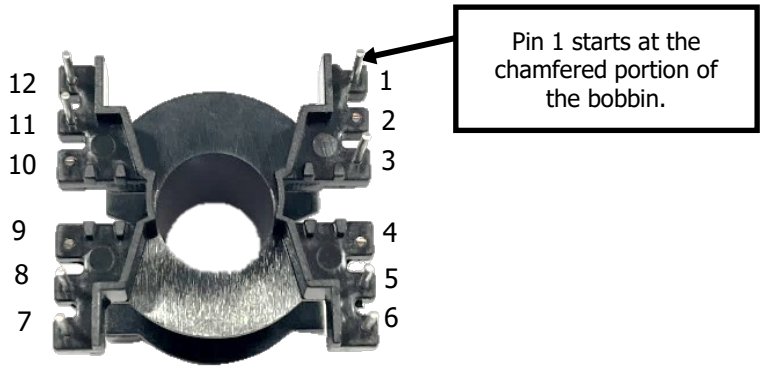
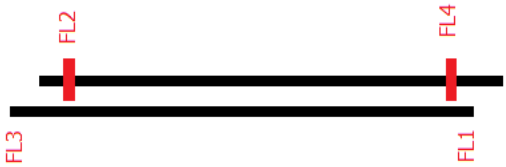
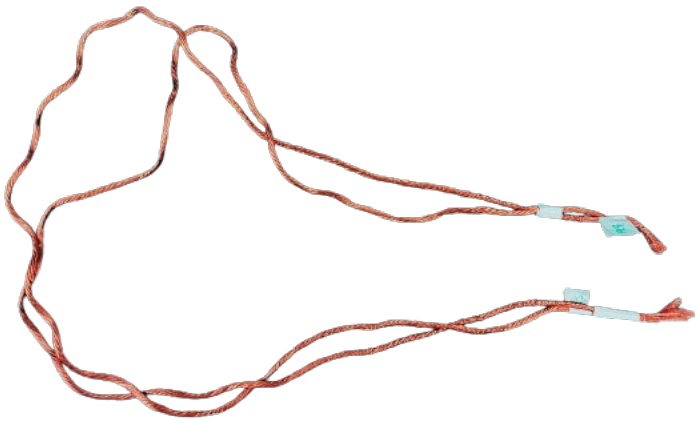
7.1.4 LLC Transformer Build Diagram

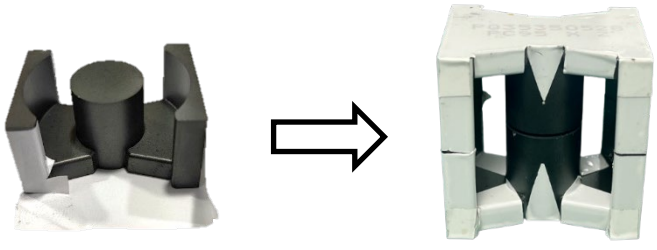


Notes: 1. Wire leads 11&12(WD5) should be twisted together before crossing the isolation barrier.
2. Wire leads 1&3(WD6) should be twisted together before crossing the isolation barrier.

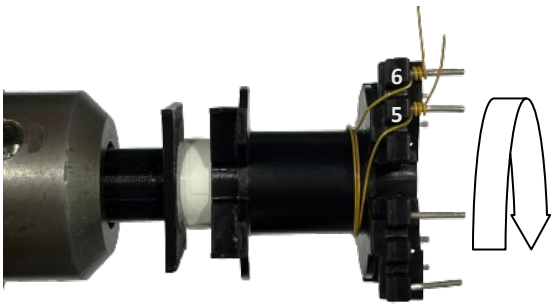
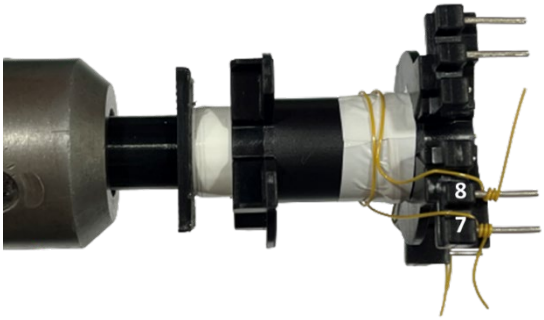
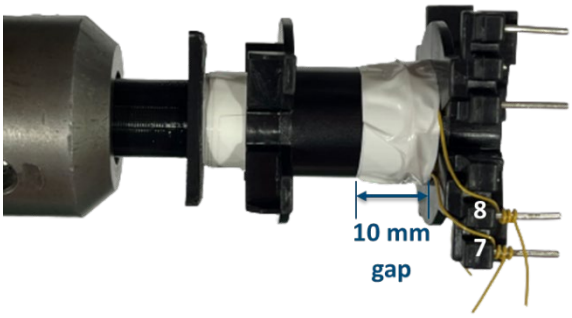
Figure 9 – LLC Transformer Build Diagram

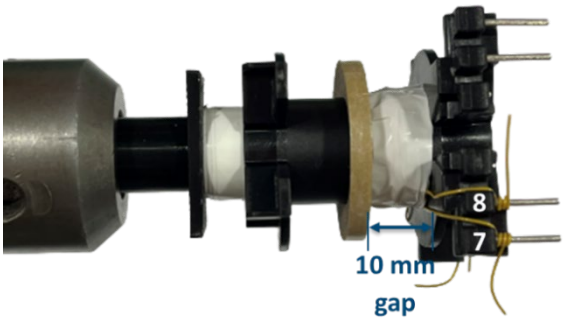
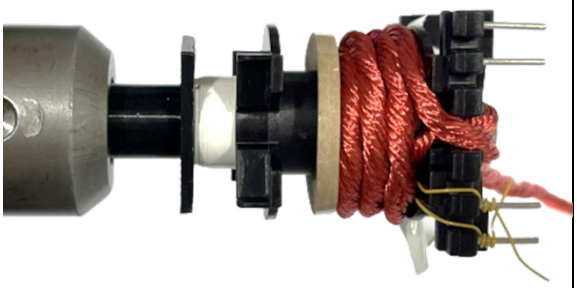
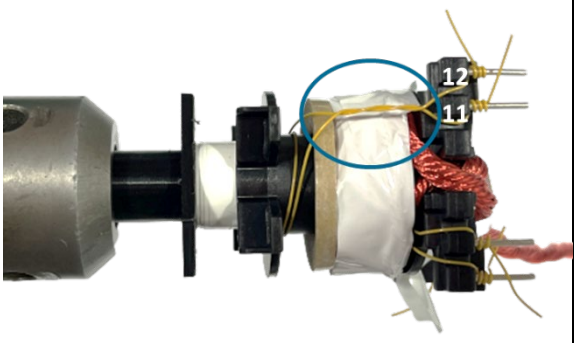
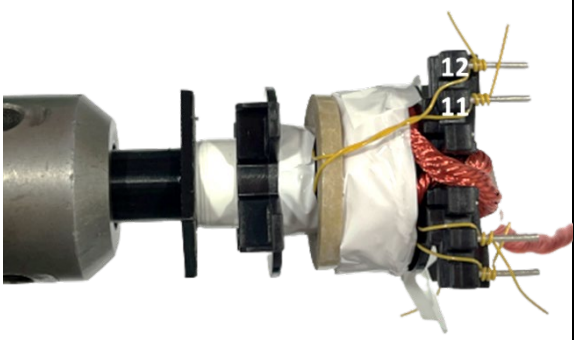
7.1.5 Winding Preparation

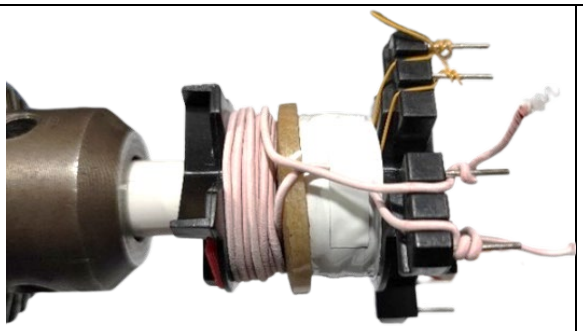
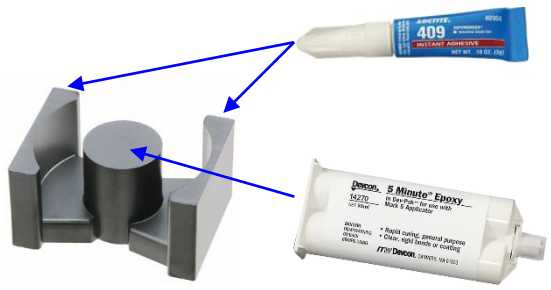
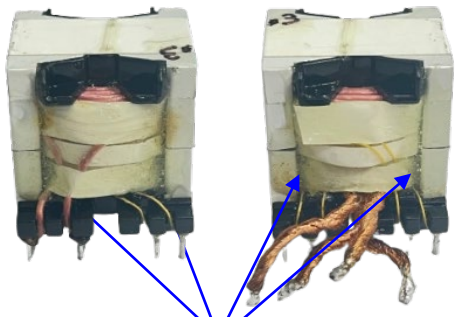
BOBBIN	Remove bobbin pins #s 2,4, 9 and 10, they will not be used to terminate any wires on the transformer. See figure below for the transformer pin-out reference. 
WD3 & WD4 Secondary	Prepare Item [4] 0.100/250 at around 24 in. long for WD3(Sec1) and WD4(Sec2). Label the two separate wires as seen on the diagram.  

	Tape together FL2 and FL3 ends then insert FL2 and FL3 pairing on the winding machine as shown. Turn the winding machine for 150-160 turns (quantifies the wire twisting). * It is important that wires are tightly coupled for optimum operation. When using the alternate wires, make sure to do this and ensure that combined wires (0.100/125) are also tightly twisted.  Final twisting is as shown. The two wires should be finely twisted together for balanced secondary winding inductance and better thermal performance. 
CORE	Tape the outer area of the core ensuring that all the outer surface is covered. 

7.1.6 Transformer Illustrations

Winding Number	Illustration	Instructions
WD1 **Primary Bias Winding**		Bobbin is turned clockwise. Wind the 3T primary bias winding starting with Pin 5 and end the winding at Pin 6.
WD1 **Primary Bias Winding** **Taping**		Add 1 layer of tape (10 mm) above Primary Bias Winding.
WD2 **Secondary Bias Winding**		Wind the 2T secondary bias winding starting with Pin 7 and ending at Pin 8.
WD2 **Secondary Bias Winding** **Taping**		Add one layer of 10 mm tape above Secondary Bias Winding. This tape may be used as a guide on how to place the gap between primary and secondary.

Primary and Secondary gapping tape		Use 3 mm electrical tape (cut the tape as stacked) and use the end of the 10 mm tape as a guide of placing the gap properly.
WD3 and WD4 Secondary Winding		Complete the 6T of the Secondary Winding of FL2-FL4 and FL3-FL1 and terminate at the bottom of the bobbin. Add two layers of 11 mm tape to secure the winding.
WD5 IS Winding		Wind 2T of IS Winding starting at Pin 11 and terminate it at Pin 12. Twist the ends together before completely terminating.
WD5 IS Winding Taping		Add a single layer of 9 mm tape on top of the IS winding. It should be tightly covered.

WD6 **Primary Winding**		Place the primary winding wires on Pin 1 and temporarily tape the wire onto the secondary side. Start winding the 28 T Primary Winding and terminate at pin 3.
WD6 **Primary Winding** **Taping**		Twist this primary wire before terminating it to Pins 1 and 3. Tape the primary wires with two layers of 9 mm tape.
Improvement for **Audible noise**	  	Grind the core and make sure to get the correct inductances from the transformer. Add epoxy to the center of the core, just enough to fill the gap. Then put a drop of glue on the side legs of the core. After, wrap one layer of tape along the outside surface of the core to secure the core. *Make sure that wires are not damaged/ grazed when inserting the core. Dip the transformer in varnish. Add epoxy (Devcon, 5minute Epoxy, Mfg Part No: 14270) along the sides of the varnished transformer and allow to dry.

8 LLC Transformer Design Spreadsheet

1	**ACDC_HiperLCS2_ POWeDIP_110923; Rev.1.11; Copyright Power Integrations 2023**	**INPUT**	**INFO**	**OUTPUT**	**UNITS**	**HiperLCS-2 Design Spreadsheet**
2	General					
3	Description			>		LCS7268Z-960W-48V-20A-SynchRF-28T-6T-288uH-60uH-66nF-77kHz
4	**Input Parameters**					
5	V_{IN} MIN	300		300	V	Brownout Threshold Voltage
6	V_{IN} RES	400		400	V	Input Voltage at Resonance - lower Vres to lower Npri
7	V_{IN} NOM	400		400	V	Nominal Input Voltage - default CRM Vres=Vnom (or DCM Vres>Vnom, CCM Vres<Vnom)
8	V_{IN} MAX	430		430	V	Maximum Input Voltage - decrease Vmax to lower Fmax
9	PFC	NO		NO		Input Option
10	**Output Parameters**					
11	Vout1	48.00		48.00	V	Main Output Voltage
12	Iout1 PK	20.0		20.0	A	Peak Main Output Current - default = 200% of Iout1Cont - used to select device size - increasing (IOUT1 PK) peak power will lower (LRES)
13	Pout1 PK			960.0	W	Main Output Peak Power
14	Iout1 CONT	15.0		15.0	A	Continuous Main Output Current - default 50% of Ppeak - used to select device size - losses calculated at this power level
15	Pout1 CONT			720.0	W	Continues Main Output Power
16	External CC	NO		NO		Use external CC operation
17	Vout1 Min (CC)				V	Minimum Output Voltage when operating in CC - lower VoutMin lowers Lm and also lowers efficiency
18	VCC				V	Output current sense resistor voltage when operating at CC-threshold
19	RCC				mOhm	Output current sense resistor value

20	RCC Rated Power				W	Output current sense resistor rated power
21	**Estimated Parameters, Design Choices and Selections**					
22	FS Range	1		1		Frequency Range
23	FS Vnom (Target)	80.0		80.0	kHz	Switching Frequency at VinNom
24	Output Rectifier	SynchRF		SynchRF		Output Rectifier
25	Ron_SR1			5.0	mOhms	Sync. Rectifier ON Resitance
26	VF_SR1				V	Output Diode Average Voltage Drop
27	**Design Results**					
28	DESIGN RESULT			Design Passed		Current Design Status
29	**Device Variables**					
30	DEVNAME	LCS7268Z		LCS7268Z		PI Device Name
31	COSS			263	pF	Equivalent Coss of selected device
32	RDSON			0.260	Ohms	RDSON of selected device
33	Fault Response	NON_LATCHING		NON_LATCHING		..
34	**Tank Circuit Components & Operation Frequency Range**					
35	Integrated Magnetics	YES		YES		Integrated Transformer Requirements
36	LP Nominal			348.24	μH	Nominal Primary Inductance
37	Lm			288.3	μH	Magnetizing inductance of transformer - modified by Kz, Device size and frequency
38	Lres			59.9	μH	Series resonant or primary leakage inductance - modified by Pmax
39	Cres	66.00		66.00	nF	Series resonant capacitor.
40	f_calc@Vbrownout			52.6	kHz	Frequency at PoutCont at Vbrownout, full load - adjust VinBrownout
41	f_calc@resonance			80.0	kHz	Frequency at PoutCont at Vres (defined by Lres and Cres) - adjust Vres)
42	f_calc@Vnom			76.5	kHz	Frequency at PoutCont at Vnom - adjust FS Vnom Target or Vnom

43	f_calc@Vinmax			86.7	kHz	Expected frequency at maximum input voltage and full load; Heavily influenced by n_eq and primary turns
44	VINGmaxInversion			276.2	V	Minimum Input Voltage for negative Gain at 100% load. Below this voltage the Gain becomes positive (unstable loop)
45	**Core Dimensions/TRF Mechanical Parameters**					
46	AE			171.00	mm^2	Transformer Core Cross-sectional area
47	VE			13.6	cm^3	Transformer Core Volume
48	MLT			75.00	mm	Middle Length of a Turn
49	AW			253.30	mm^2	Core Window area
50	BW			22.50	mm	Bobbin Winding Width
51	Bobbin Chambers			2		Bobbin Chambers
52	ChambDist	3.00		3.00	mm	Width of bobbin with no windings - empty space between primary/secondary generates leakage inductance
53	Bobbin Height			7.50	mm	Height of the bobbin, maximum Stack height
54	Prim. Bobbin Chamber Width			8.25	mm	Part of the bobbin allocated for primary
55	Sec. Bobbin Chamber Width			11.25	mm	Part of the bobbin allocated for secondary
56	K-PD			0.35		Penetration Depth multiplier (for Single Strand LITZ calculation)
57	**Transformer Generic Parameters**					
58	CR_TYPE	PQ35/35		PQ35/35		Transformer Core Type
59	FR_TYPE	PC95		PC95		Magnetic material used
60	BACmax Actual			292.91	mT	Estimated Flux Density at Vnom - increase Ns to reduce Bmax
61	Use Litz Primary	YES		YES		Primary Windings Bundled (served) Yes/No
62	Use Litz Secondary	YES		YES		Secondary Windings Bundled (served) Yes/No
63	Fixed Litz Bundles	NO		NO		Use preferred Litz Wire Bundles (yes) - or use customer bundle (no)

64	kSecChamb			0.40		Percentage of Bobbin Chamber Width used for Secondary Windings - Adjust to change Used Percentage of Primary/Secondary Windows
65	**Transformer Primary Parameters**					
66	Npri			28		Calculated Primary Winding Total Number of Turns
67	Iprim RMS			4.07	A	Transformer Primary Winding RMS Current at PoutCont and VinNom
68	Prim. Wire Type			LITZ		Primary Wire Type
69	Primary Litz Wire Type	SERVED		SERVED		Litz Insulation type, SERVED bundled with sleave, UNSERVED loose wires
70	Target Prim. Current density			6.0	A/mm^2	Primary current density target - reduce target to increase copper
71	Prim. Single Strand Wire Gauge	44		44	AWG	Single Strand Gauge (LITZ) / AWG (ECW)
72	Prim. Single Strand Diameter			0.05	mm	Primary Single Strand Copper Diameter
73	Number of Prim. Strands	405		405		Prim. Number of Strands (LITZ) / Fillars (ECW)
74	Actual Prim. Current Density			5.07	A/mm^2	Actual Primary Current Density
75	Actual Prim. Copper Diameter			1.01	mm	Primary Equivalent Total Copper Diameter
76	Actual Prim. External Diameter			1.29	mm	Primary Wire External Diameter (bundle size - copper plus insulation plus fill)
77	Layers Primary			4.67		Not Rounded Primary number of layers
78	Primary Window Usage			86.28	%	Used Percentage of Available Primary Winding Window - Maximum copper gives 100%
79	**Main Output Parameters**					
80	NSec	6		6		Secondary Number of Turns
81	ISRMS			18.40	A	Transformer Secondary Winding RMS Current
82	Sec. Wire Type			LITZ		Main Output Wire Type

83	Secondary LIZ Wire type	UNSERVED		UNSERVED		Litz Insulation type, SERVED bundled with sleave, UNSERVED loose wires
84	Target Sec. Current density			8.0	A/mm^2	Secondary current density target - reduce target to increase copper
85	Sec. Single Strand Wire Gauge	38		38	AWG	Single Strand Gauge (LITZ) / AWG (ECW)
86	Sec. Single Strand Diameter			0.10	mm	Secondary Single Strand Copper Diameter
87	Number of Sec. Strands	250		250		Sec. Number of Strands (LITZ) / Fillars (ECW)
88	Actual Sec. Curr Density			9.19	A/mm^2	Sec. Actual Current Density
89	Actual Sec. Copper Diameter			1.60	mm	Secondary Equivalent Total Copper Diameter
90	Actual Sec. External Diameter			2.04	mm	Secondary Wire External Diameter (bundle size - copper plus insulation plus fill)
91	Layers Secondary			2.40		Not Rounded Secondary number of layers
92	Secondary Window Usage			81.76	%	Used Percentage of Available Secondary Winding Window - Maximum copper gives 100%
93	**Losses at Integrated Magnetics**					
94	CoreLoss			1.03	W	Core Losses at VinNom
95	Pr.WindLoss			1.07	W	Primary Winding Losses at VinNom and PoutCont
96	Sec.WindLoss			1.81	W	Secondary Winding Losses at VinNom and PoutCont
97	CO ESR Loss			0.11	W	Output Capacitor ESR Loss at VinNom and PoutCont
98	PLOSS Switch			2.15	W	Single Primary Switch Conduction Loss at VinNom and PoutCont
99	PLOSS Output Rectifier			0.69	W	Single Output Rectifier Conduction Loss at VinNom and PoutCont
100	PLOSS RCC			0.00	W	Current sense resistor power loss at VinNom and PoutCont
101	PLOSS Total			9.72	W	Total Loss at VinNom and PoutCont
102	**Circuit Components**					
103	RZ1			150	kOhm	Control Zero (boost high-frequency gain)

104	CP2			100	pF	Control Pole2 (roll-off high-frequency gain)
105	Cp1			2.2	nF	Control Pole1 (roll-off low-frequency gain)
106	Resr CO			1.00	mOhms	ESR of the output capacitor
107	COmin			1079	µF	Min CO to satisfy burst conditions
108	RD1			500	Ohm	RD1 Resistor value
109	RD2			500	Ohm	RD2 Resistor value
110	CBPL			1	µF	CBPL Capacitor Value /25 V
111	CBPH			1	µF	CBPH Capacitor Value /25 V
112	C5VL			1	µF	C5VL Capacitor Value /10 V
113	C5VH			220	nF	C5VH Capacitor Value /10 V
114	C5VFL			100	nF	C5VLFL Capacitor Value /10 V
115	C5VS			10	µF	C5VS Capacitor Value /10 V
116	CBPS			10	µF	CBPS Capacitor Value /35 V
117	RL			0	kOhms	L-pin Input Voltage (Vin) Sense Resistor
118	RPP			158	kOhms	RPP Resistor /1% E96 series
119	RPS			75	kOhms	RPS Resistor /1% E96 series
120	**Bias, IS Circuit & Feedback Components**					
121	NS1			3		Primary Bias Turns
122	NSB			2		Secondary Bias Turns
123	NVIS			2		Secondary (Is) Sense Turns
124	RIS			1338	kOhms	Rrs Resistor Value
125	CIS			470	pF	IS sense winding coupling capacitor
126	RFBH			283.7	kOhm	Calculated value of top feedback resistor. use series closest resistor 1% E96
127	RFBL			24.0	kOhm	Calculated value of low feedback resistor. use series closest resistor 1% E96
128	**Currents and Winding loss elements**					
129	Iprim RMS			4.07	A	Transformer Primary Winding RMS Current at PoutCont at VinNom
130	ISRMS			18.40	A	Transformer Secondary Winding RMS Current at PoutCont at VinNom
131	Irms_SR			11.78	A	Secondary Rectifier RMS Current at PoutCont at VinNom

132	Irms_CO1			10.65	A	Output Capacitor RMS Current at PoutCont at VinNom
133	RdcPrim			0.06	Ohms	Primary Winding DC Resistance
134	RacPrim			0.06	Ohms	Primary Winding AC Resistance
135	RdcSec			5.024	mOhms	Secondary Winding DC Resistance
136	RacSec			5.348	mOhms	Secondary Winding AC Resistance
137	**Advanced Settings**					
138	Kz	1.3		1.3		coefficient of surplus ZVS energy @ Vnom - raise Kz to lower Vin (GmaxInv) - Kz should be >= 1.0 to ensure ZVS operation
139	Tdd1_Vinnom			250	ns	Half-bridge slew at 100% load @ Vnom - raise Tdd1 to lower ZVS currents
140	Coupling			0.89		Transformer Coupling
141	Cpri			40.00	pF	Stray Capacitance at transformer primary
142	**External Resonant Inductor (Ext.Lres) Calculations**					
143	PP or Lpin	PP		PP		HB Startup current selection
144	Ext.Lres Core	Auto		N/A		External Resonant Inductor Core
145	Ext.Lres Ferrite					External Resonant Inductor magnetic material
146	Lres			59.9	μH	Series resonant or primary leakage inductance - modified by Pmax
147	Ext.Lres Ae				mm^2	External Resonant Inductor Core Cross-sectional area
148	Ext.Lres Turns					External Resonant Inductor Turns
149	Ipk(@startup)				A	Device level IOVL value
150	BACmax(Lres) @Vbo				mT	External Resonant Inductor Estimated Flux Density at Vbo
151	BACmax(Lres) @Startup				mT	External Resonant Inductor Estimated Flux Density at Vbo
152	Ext.Lres Wire Type					External Resonant Inductor Wire Type

153	Ext.Lres LIz Wire Type					Litz Insulation type, SERVED bundled with sleave, UNSERVED loose wires
154	Target Ext.Lres Current density				A/mm^2	External Resonant Inductor current density target - reduce target to increase copper
155	Ext.Lres Single Strand Wire Gauge				AWG	Single Strand Gauge (LITZ) / AWG (ECW)
156	Ext.Lres Single Strand Diameter				mm	External Resonant Inductor Single Strand Copper Diameter
157	Number of Ext.Lres Strands					External Resonant Inductor Number of Strands (LITZ) / Fillars (ECW)
158	Actual Ext.Lres Current Density				A/mm^2	Actual External Resonant Inductor Current Density
159	Actual Ext.Lres Copper Diameter				mm	External Resonant Inductor Equivalent Total Copper Diameter
160	Actual Ext.Lres External Diameter				mm	External Resonant Inductor Wire External Diameter (bundle size - copper plus insulation plus fill)
161	Ext.Lres Layers					Not Rounded External Resonant Inductor number of layers
162	Ext.Lres Window Usage (height)				%	Used Percentage of Available External Resonant Inductor Winding Window - Maximum copper gives 100%
163	Ext.Lres CoreLOSS				W	Core Loss at VBO
164	Ext.Lres CopperLOSS Total				W	Total Copper Loss at nominal

9 Heatsinks

Two heatsinks are used for the design. One is for the primary side HiperLCS2-HB IC and the other is for the synchronous rectifier MOSFETs on the output.

9.1 Primary Device Heatsink

The HiperLCS2-HB IC on the primary side uses an aluminum heatsink with fins.

Note: When tightening the fixing screws for the primary IC, a torque screwdriver should be used, set to 1 pound-inch.

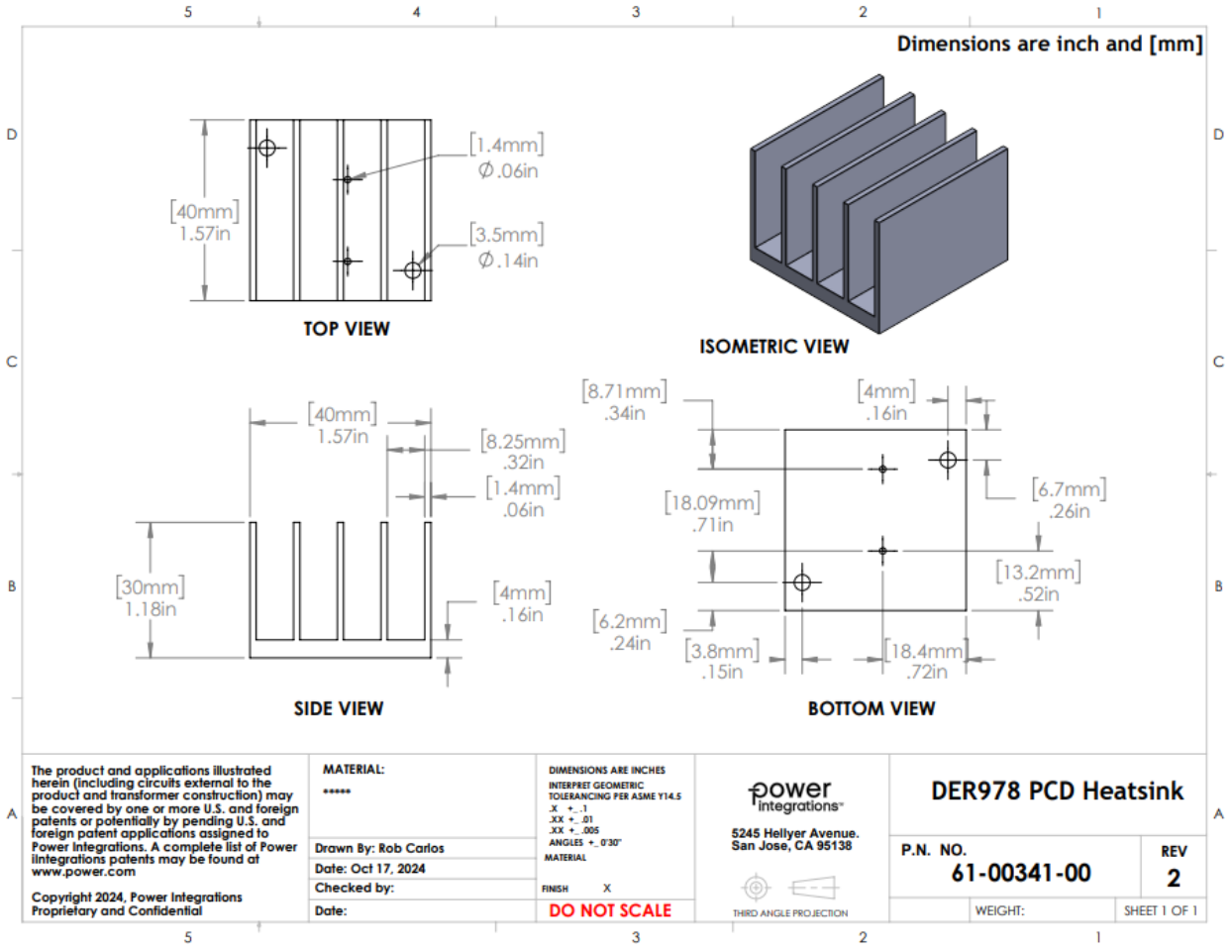
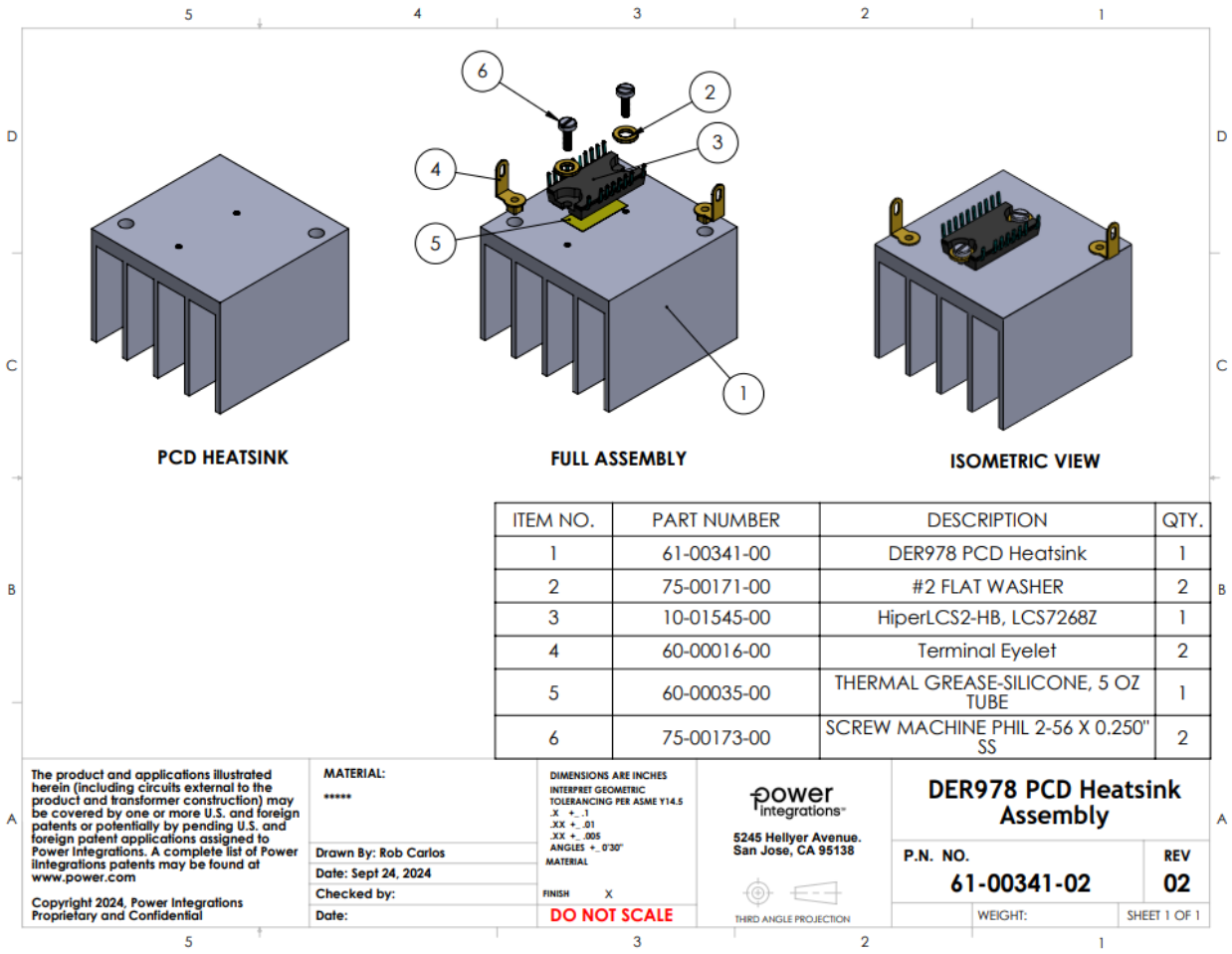


Figure 10 – Primary Device Heatsink Drawing.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00341-00	DER978 PCD Heatsink	1
2	75-00171-00	#2 FLAT WASHER	2
3	10-01545-00	HiperLCS2-HB, LCS7268Z	1
4	60-00016-00	Terminal Eyelet	2
5	60-00035-00	THERMAL GREASE-SILICONE, 5 OZ TUBE	1
6	75-00173-00	SCREW MACHINE PHIL 2-56 X 0.250" SS	2

MATERIAL: *****

Drawn By: Rob Carlos
Date: Sept 24, 2024
Checked by:
Date:

DIMENSIONS ARE INCHES
INTERPRET GEOMETRIC TOLERANCING PER ASME Y14.5
.X +_.1
.XX +_.01
.XX +_.005
ANGLES +_ 0'30"
MATERIAL
FINISH X
DO NOT SCALE

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138
THIRD ANGLE PROJECTION

DER978 PCD Heatsink Assembly

P.N. NO. 61-00341-02
REV 02
WEIGHT:
SHEET 1 OF 1

Figure 11 – Primary Device Heatsink Assembly Drawing.

9.2 Synchronous Rectifier Heatsink

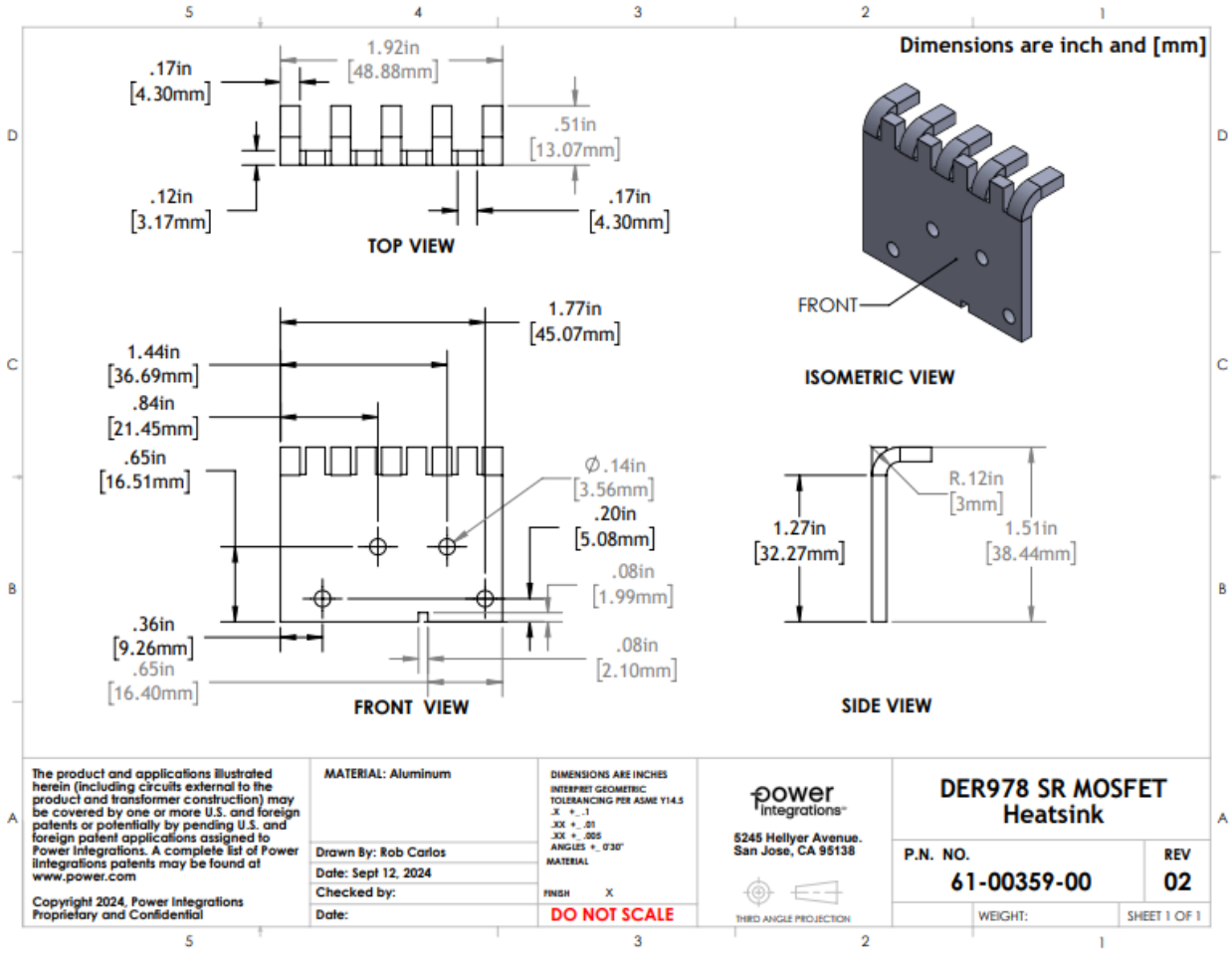
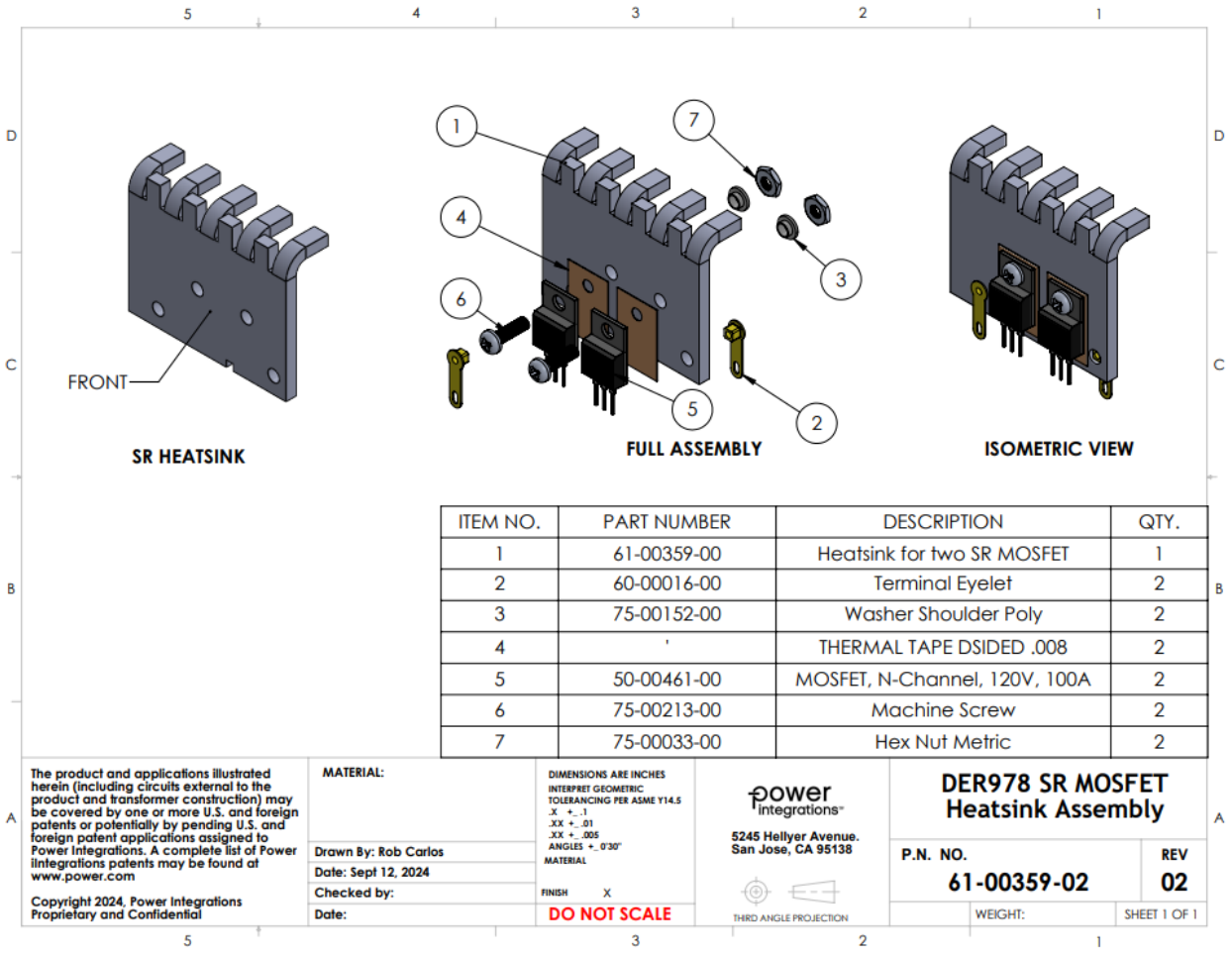


Figure 12 – SR MOSFET Heatsink Drawing.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00359-00	Heatsink for two SR MOSFET	1
2	60-00016-00	Terminal Eyelet	2
3	75-00152-00	Washer Shoulder Poly	2
4	'	THERMAL TAPE DSIDED .008	2
5	50-00461-00	MOSFET, N-Channel, 120V, 100A	2
6	75-00213-00	Machine Screw	2
7	75-00033-00	Hex Nut Metric	2

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com

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MATERIAL:

Drawn By: Rob Carlos
Date: Sept 12, 2024
Checked by:
Date:

DIMENSIONS ARE INCHES
INTERPRET GEOMETRIC TOLERANCING PER ASME Y14.5
.X +_.1
.XX +_.01
.XX +_.005
ANGLES +_0°30'
MATERIAL
FINISH X
DO NOT SCALE

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138
THIRD ANGLE PROJECTION

DER978 SR MOSFET Heatsink Assembly
P.N. NO. 61-00359-02
REV 02
WEIGHT:
SHEET 1 OF 1

Figure 13 – SR MOSFET Heatsink Assembly Drawing.

10 Performance Data

In this section, the power supply's performance under different line and load conditions is described. Tests include DC-DC efficiency, no-load input power, line and load regulation, operating waveforms, and thermal measurements. The set-up and test conditions are described for each section.

10.1 Efficiency

DC-DC efficiency of the unit with respect to output power is shown in Figure 14. The efficiency was tested for three different line conditions. A high-power DC source was used to supply the DC input and a DC electronic load set to CCH mode was used for output.

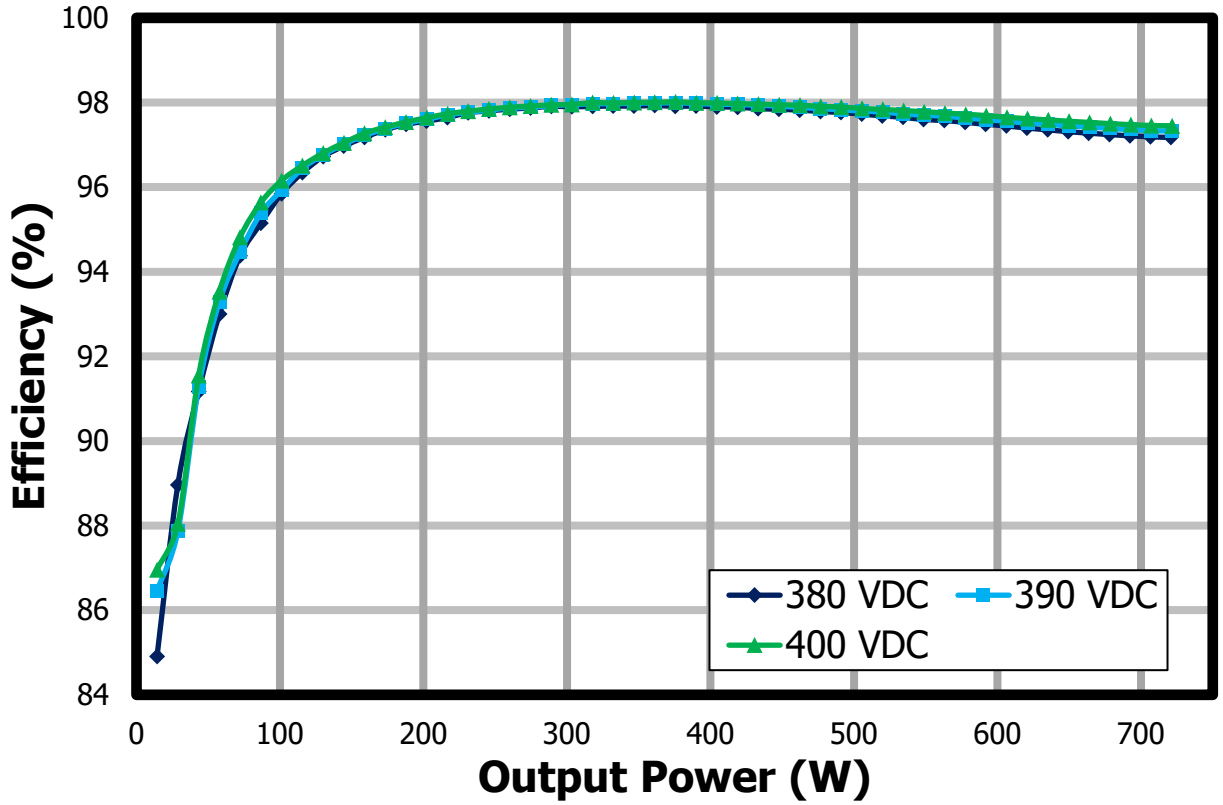


Figure 14 – Total Efficiency vs. Load, Output Power.

Table 2 Efficiency Data

Input	Load (%)	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
380 VDC	100	380	1.95	742	48.1	15.0	721	97.2
	98.0	380	1.91	727	48.1	14.7	707	97.2
	96.0	380	1.88	712	48.1	14.4	692	97.2
	94.0	380	1.84	697	48.1	14.1	678	97.2
	92.0	380	1.80	682	48.1	13.8	664	97.3
	90.0	380	1.76	667	48.1	13.5	649	97.3
	88.0	380	1.72	652	48.1	13.2	635	97.4
	86.0	380	1.68	637	48.1	12.9	621	97.4
	84.0	380	1.64	622	48.1	12.6	606	97.4
	82.0	380	1.60	607	48.1	12.3	592	97.5
	80.0	380	1.56	592	48.1	12.0	577	97.5
	78.0	380	1.52	577	48.1	11.7	563	97.6
	76.0	380	1.48	562	48.1	11.4	549	97.6
	74.0	380	1.44	547	48.2	11.1	534	97.6
	72.0	380	1.40	532	48.2	10.8	520	97.7
	70.0	380	1.36	517	48.2	10.5	505	97.7
	68.0	380	1.32	502	48.2	10.2	491	97.8
	66.0	380	1.28	487	48.2	9.90	477	97.8
	64.0	380	1.24	472	48.2	9.60	462	97.8
	62.0	380	1.20	458	48.2	9.30	448	97.8
	60.0	380	1.17	443	48.2	9.00	433	97.9
	58.0	380	1.13	428	48.2	8.70	419	97.9
	56.0	380	1.09	413	48.2	8.40	404	97.9
	54.0	380	1.05	398	48.2	8.10	390	97.9
	52.0	380	1.01	384	48.2	7.80	375	97.9
	50.0	380	0.971	369	48.2	7.50	361	97.9
	48.0	380	0.932	354	48.2	7.20	347	97.9
	46.0	380	0.893	339	48.2	6.90	332	97.9
	44.0	380	0.854	325	48.2	6.60	318	97.9
	42.0	380	0.816	310	48.2	6.30	303	97.9
	40.0	380	0.777	295	48.2	6.00	289	97.9
	38.0	380	0.738	280	48.2	5.70	274	97.9
	36.0	380	0.700	266	48.2	5.40	260	97.8
	34.0	380	0.661	251	48.2	5.10	246	97.8
	32.0	380	0.623	236	48.2	4.80	231	97.8
	30.0	380	0.584	222	48.2	4.50	217	97.6
	28.0	380	0.546	207	48.2	4.20	202	97.6
	26.0	380	0.507	193	48.2	3.90	188	97.5
	24.0	380	0.469	178	48.2	3.60	173	97.4
	22.0	380	0.430	163	48.2	3.30	159	97.2
	20.0	380	0.392	149	48.2	3.00	144	97.0
	18.0	380	0.354	134	48.2	2.70	130	96.7
	16.0	380	0.316	120	48.2	2.40	116	96.3
	14.0	380	0.278	105	48.2	2.10	101	95.8
	12.0	380	0.240	91.1	48.2	1.80	86.7	95.1
	10.0	380	0.201	76.5	48.2	1.50	72.2	94.4
	8.00	380	0.163	62.1	48.2	1.20	57.8	93.0
	6.00	380	0.125	47.5	48.2	0.899	43.3	91.2
	4.00	380	0.085	32.4	48.1	0.599	28.8	89.0
	2.00	380	0.044	16.8	47.9	0.298	14.3	84.9

Input	Load (%)	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
390 VDC	100	390	1.90	741	48.1	15.0	722	97.3
	98.0	390	1.86	727	48.1	14.7	707	97.3
	96.0	390	1.83	712	48.1	14.4	693	97.4
	94.0	390	1.79	697	48.1	14.1	679	97.4
	92.0	390	1.75	682	48.1	13.8	664	97.4
	90.0	390	1.71	667	48.2	13.5	650	97.4
	88.0	390	1.67	652	48.2	13.2	635	97.5
	86.0	390	1.63	637	48.2	12.9	621	97.5
	84.0	390	1.59	622	48.2	12.6	607	97.6
	82.0	390	1.56	607	48.2	12.3	592	97.6
	80.0	390	1.52	592	48.2	12.0	578	97.6
	78.0	390	1.48	577	48.2	11.7	563	97.7
	76.0	390	1.44	562	48.2	11.4	549	97.7
	74.0	390	1.40	547	48.2	11.1	534	97.7
	72.0	390	1.36	532	48.2	10.8	520	97.8
	70.0	390	1.33	517	48.2	10.5	506	97.8
	68.0	390	1.29	502	48.2	10.2	491	97.8
	66.0	390	1.25	487	48.2	9.90	477	97.9
	64.0	390	1.21	472	48.2	9.60	462	97.9
	62.0	390	1.17	457	48.2	9.30	448	97.9
	60.0	390	1.14	443	48.2	9.00	433	97.9
	58.0	390	1.10	428	48.2	8.70	419	98.0
	56.0	390	1.06	413	48.2	8.40	405	98.0
	54.0	390	1.02	398	48.2	8.10	390	98.0
	52.0	390	0.983	383	48.2	7.80	376	98.0
	50.0	390	0.945	369	48.2	7.50	361	98.0
	48.0	390	0.908	354	48.2	7.20	347	98.0
	46.0	390	0.870	339	48.2	6.90	332	98.0
	44.0	390	0.832	324	48.2	6.60	318	98.0
	42.0	390	0.794	310	48.2	6.30	303	97.9
	40.0	390	0.757	295	48.2	6.00	289	97.9
	38.0	390	0.719	280	48.2	5.70	275	97.9
	36.0	390	0.682	266	48.2	5.40	260	97.9
	34.0	390	0.644	251	48.2	5.10	246	97.8
	32.0	390	0.606	236	48.2	4.80	231	97.8
	30.0	390	0.569	222	48.2	4.50	217	97.7
	28.0	390	0.531	207	48.2	4.20	202	97.6
	26.0	390	0.494	193	48.2	3.90	188	97.5
	24.0	390	0.457	178	48.2	3.60	173	97.4
	22.0	390	0.419	163	48.2	3.30	159	97.2
	20.0	390	0.382	149	48.2	3.00	144	97.0
	18.0	390	0.345	134	48.2	2.70	130	96.8
	16.0	390	0.307	120	48.2	2.40	116	96.4
	14.0	390	0.270	105	48.2	2.10	101	95.9
	12.0	390	0.233	90.9	48.2	1.80	86.7	95.4
	10.0	390	0.196	76.5	48.2	1.50	72.2	94.5
	8.00	390	0.159	61.9	48.2	1.20	57.8	93.3
	6.00	390	0.122	47.4	48.2	0.899	43.3	91.3
	4.00	390	0.084	32.8	48.2	0.599	28.8	87.9
	2.00	390	0.042	16.5	47.9	0.298	14.3	86.5

Input	Load (%)	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
400 VDC	100	400	1.85	741	48.1	15.0	722	97.4
	98.0	400	1.82	726	48.1	14.7	707	97.5
	96.0	400	1.78	711	48.1	14.4	693	97.5
	94.0	400	1.74	696	48.1	14.1	679	97.5
	92.0	400	1.70	681	48.2	13.8	664	97.5
	90.0	400	1.67	666	48.2	13.5	650	97.6
	88.0	400	1.63	651	48.2	13.2	635	97.6
	86.0	400	1.59	636	48.2	12.9	621	97.6
	84.0	400	1.55	621	48.2	12.6	607	97.7
	82.0	400	1.52	606	48.2	12.3	592	97.7
	80.0	400	1.48	591	48.2	12.0	578	97.7
	78.0	400	1.44	576	48.2	11.7	563	97.8
	76.0	400	1.40	561	48.2	11.4	549	97.8
	74.0	400	1.37	546	48.2	11.1	535	97.8
	72.0	400	1.33	532	48.2	10.8	520	97.8
	70.0	400	1.29	517	48.2	10.5	506	97.9
	68.0	400	1.25	502	48.2	10.2	491	97.9
	66.0	400	1.22	487	48.2	9.90	477	97.9
	64.0	400	1.18	472	48.2	9.60	462	97.9
	62.0	400	1.14	457	48.2	9.30	448	97.9
	60.0	400	1.11	442	48.2	9.00	433	98.0
	58.0	400	1.07	428	48.2	8.70	419	98.0
	56.0	400	1.03	413	48.2	8.40	405	98.0
	54.0	400	1.00	398	48.2	8.10	390	98.0
	52.0	400	0.958	383	48.2	7.80	376	98.0
	50.0	400	0.922	369	48.2	7.50	361	98.0
	48.0	400	0.885	354	48.2	7.20	347	98.0
	46.0	400	0.848	339	48.2	6.90	332	98.0
	44.0	400	0.811	324	48.2	6.60	318	98.0
	42.0	400	0.775	310	48.2	6.30	303	98.0
	40.0	400	0.738	295	48.2	6.00	289	97.9
	38.0	400	0.701	280	48.2	5.70	275	97.9
	36.0	400	0.664	266	48.2	5.40	260	97.9
	34.0	400	0.628	251	48.2	5.10	246	97.8
	32.0	400	0.591	236	48.2	4.80	231	97.8
	30.0	400	0.555	222	48.2	4.50	217	97.7
	28.0	400	0.518	207	48.2	4.20	202	97.6
	26.0	400	0.482	193	48.2	3.90	188	97.5
	24.0	400	0.445	178	48.2	3.60	173	97.4
	22.0	400	0.409	163	48.2	3.30	159	97.3
	20.0	400	0.372	149	48.2	3.00	144	97.0
	18.0	400	0.336	134	48.2	2.70	130	96.8
	16.0	400	0.299	120	48.2	2.40	116	96.5
	14.0	400	0.263	105	48.2	2.10	101	96.2
	12.0	400	0.227	90.6	48.2	1.80	86.7	95.6
	10.0	400	0.190	76.2	48.2	1.50	72.2	94.8
	8.00	400	0.154	61.8	48.2	1.20	57.8	93.5
	6.00	400	0.118	47.3	48.2	0.899	43.3	91.5
	4.00	400	0.082	32.8	48.2	0.599	28.9	88.0
	2.00	400	0.041	16.4	47.9	0.298	14.3	87.0

10.2 No-Load Input Power

No-load input power was measured with only the DC source connected to the input. The unit under test (UUT) was turned on and allowed to stabilize for 5 minutes then measured with an integration time of 15 minutes.

Note: To more accurately determine the no-load input power, no output connections were attached to the UUT.

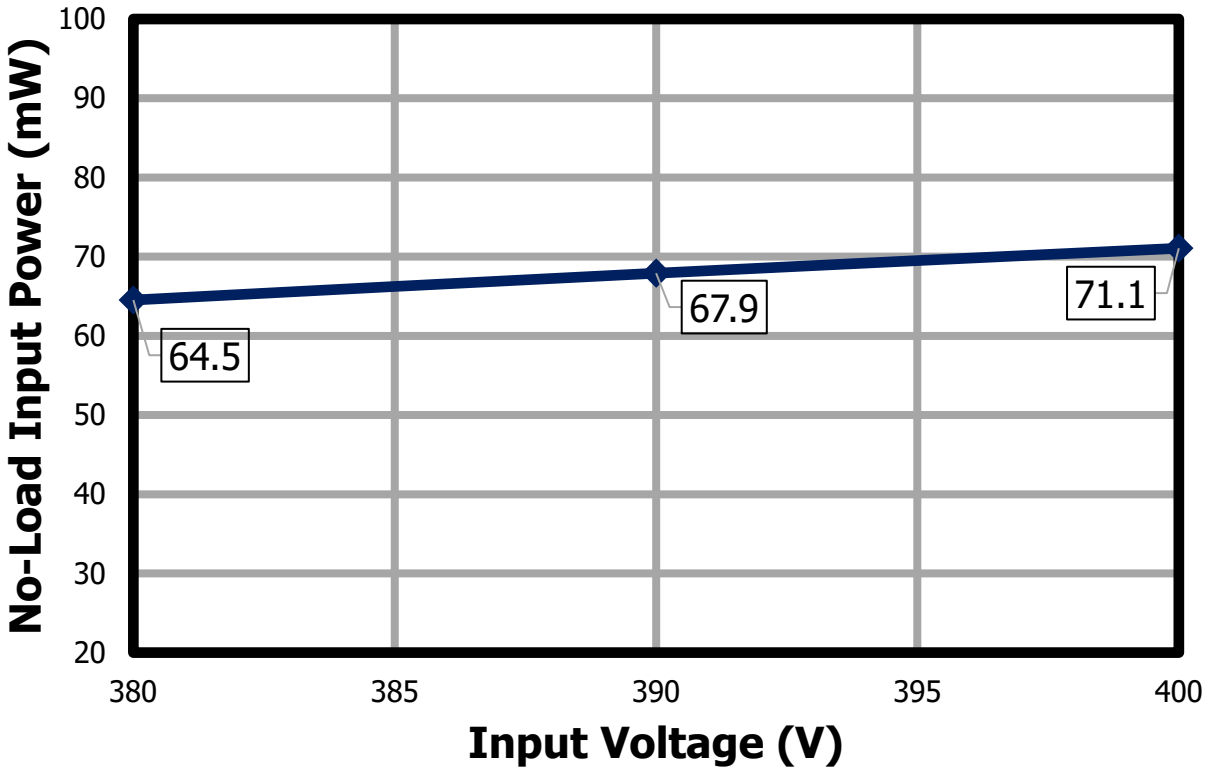


Figure 15 – No-Load Input Power vs. Input Voltage.

Table 3 No Load Input Power

V_{IN} (V)	P_{no_load} (mW)
380	64.5
390	67.9
400	71.1

10.3 Line Regulation

Line regulation describes the relationship between the DC input voltages and the output voltage. The output regulation was monitored from 380 VDC to 400 VDC at full load, half load, and no-load conditions.

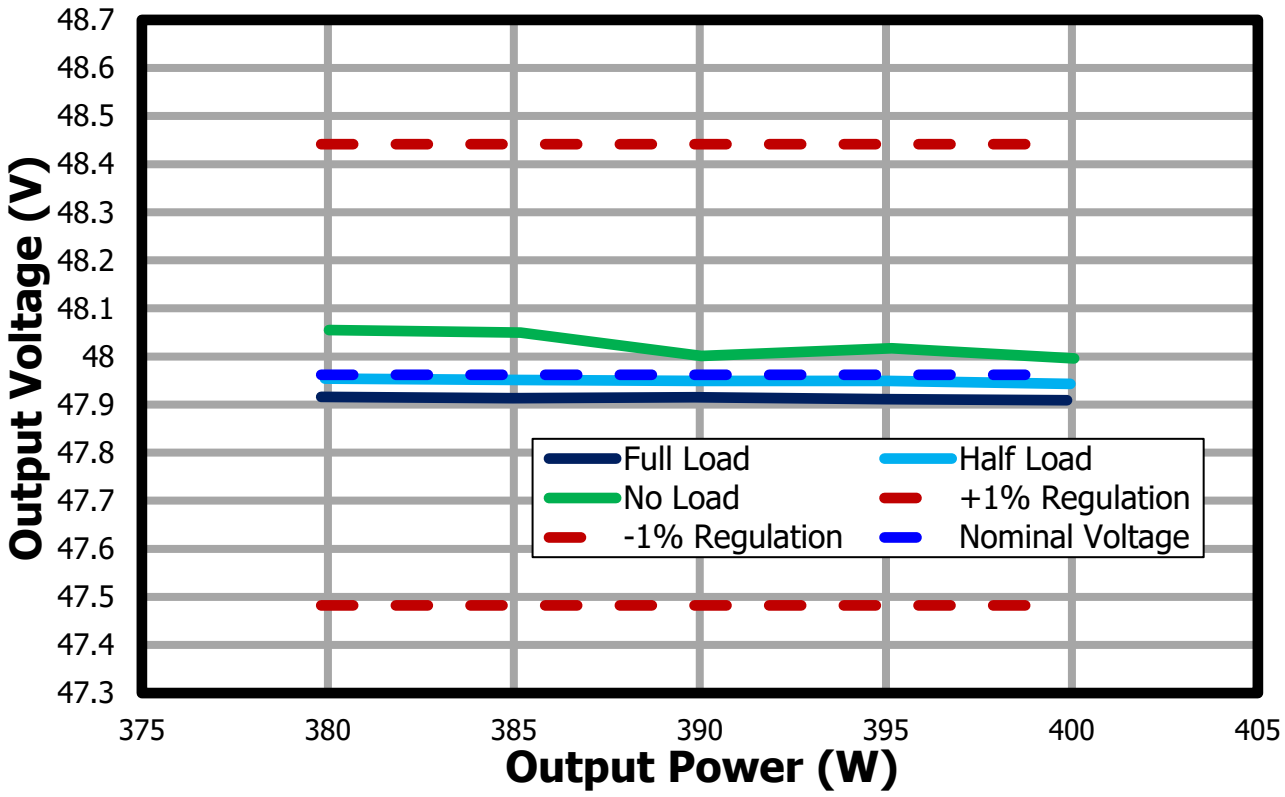


Figure 16 – Line Regulation.

Table 4 Line Regulation

V_{IN} (V)	V_{OUT} NL(V)	V_{OUT} HL(V)	V_{OUT} FL(V)
380	48.1	48.0	47.9
385	48.1	48.0	47.9
390	48.0	47.9	47.9
395	48.0	47.9	47.9
400	48.0	47.9	47.9

10.4 Load Regulation

The graph describes output power against output voltage. Output voltage was measured between 0-100% for three different DC line voltages.

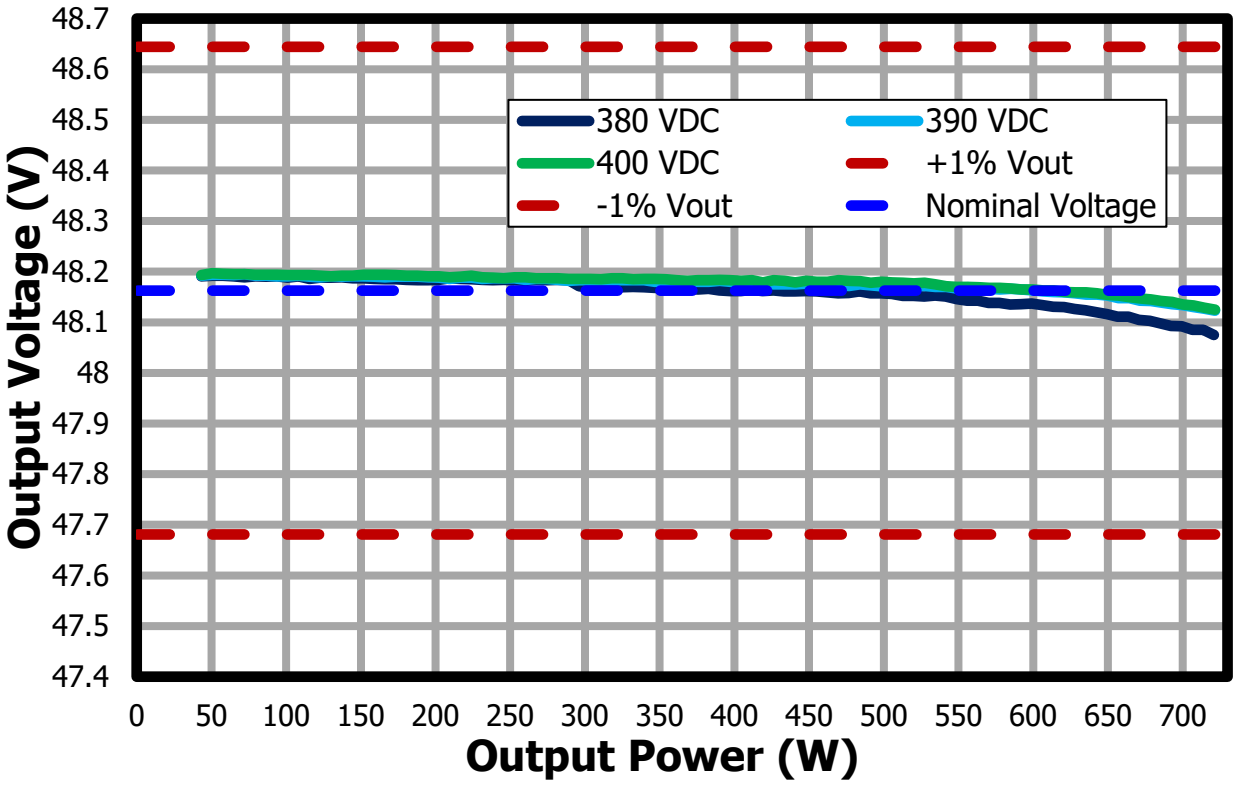


Figure 17 – Load Regulation.

Table 5 Load Regulation

P_{OUT} (W)	V_{IN}		
	380 V	**390 V**	**400 V**
721	48.1	48.1	48.1
649	48.1	48.2	48.2
577	48.1	48.2	48.2
505	48.2	48.2	48.2
433	48.2	48.2	48.2
361	48.2	48.2	48.2
289	48.2	48.2	48.2
217	48.2	48.2	48.2
144	48.2	48.2	48.2
72.2	48.2	48.2	48.2

11 Waveforms

Waveforms were recorded for different DC input voltage and output loading conditions set for the UUT.

11.1 LLC Primary Voltage and Current

The figures below show the primary voltage and current waveforms with the UUT operating from 400 VDC. The load used was an electronic load set at CCH mode. Waveforms were recorded at full load, half load, and no load.

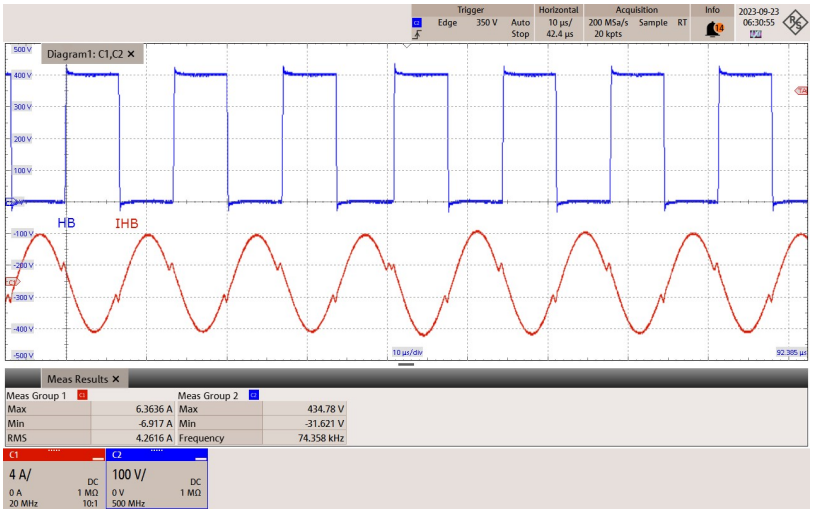


Figure 18 – LLC Stage Primary Voltage and Current, 100% Load.
Time Division: 10 μs / div.
Frequency: 74.4 kHz
HB Current (RMS): 4.26 A
CH1: HB Current, 4 A / div.
CH2: HB Voltage, 100 V / div.

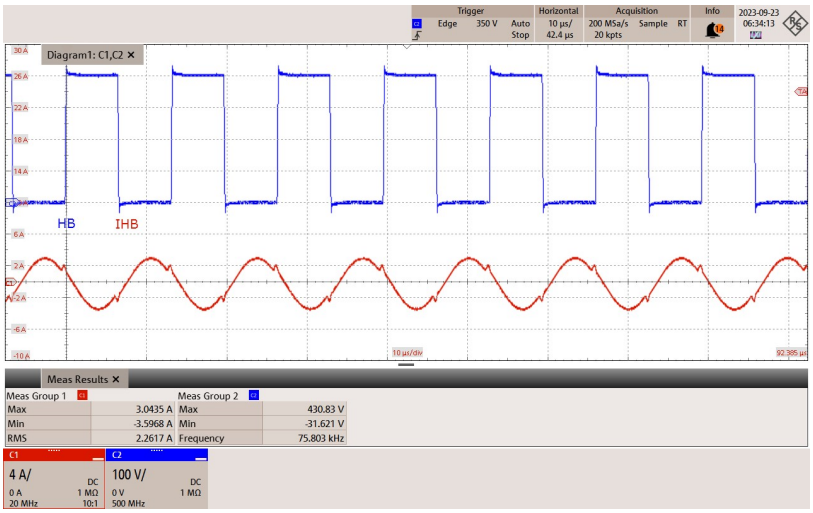


Figure 19 – LLC Stage Primary Voltage and Current, 50% Load.
Time Division: 10 µs / div.
Frequency: 75.8 kHz
HB Current (RMS): 2.26 A
CH1: HB Current, 4 A / div.
CH2: HB Voltage, 100 V / div.

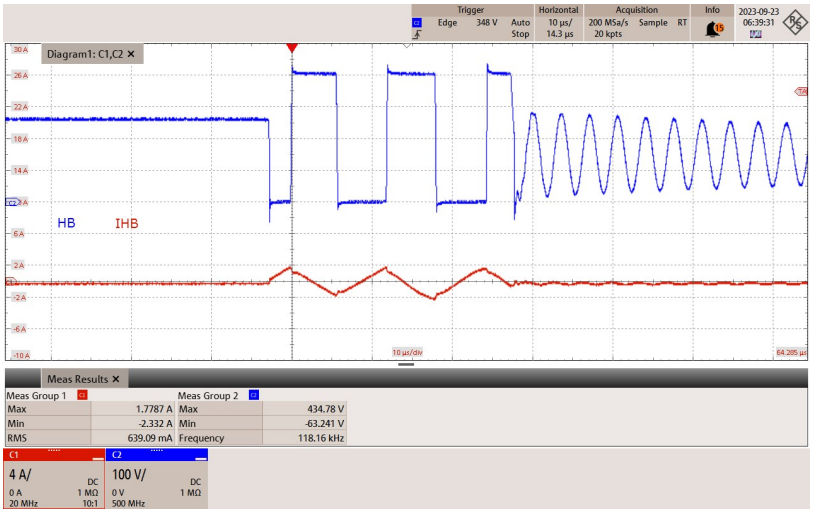


Figure 20 – LLC Stage Primary Voltage and Current, No-Load.
Time Division: 10 µs / div.
CH1: HB Current, 4 A / div.
CH2: HB Voltage, 100 V / div.

11.2 SR Waveforms

11.2.1 Drain-Source Voltage

Drain-source voltage waveforms across the synchronous rectifiers Q1 and Q3 were measured with input voltage of 400 VDC, at full load.

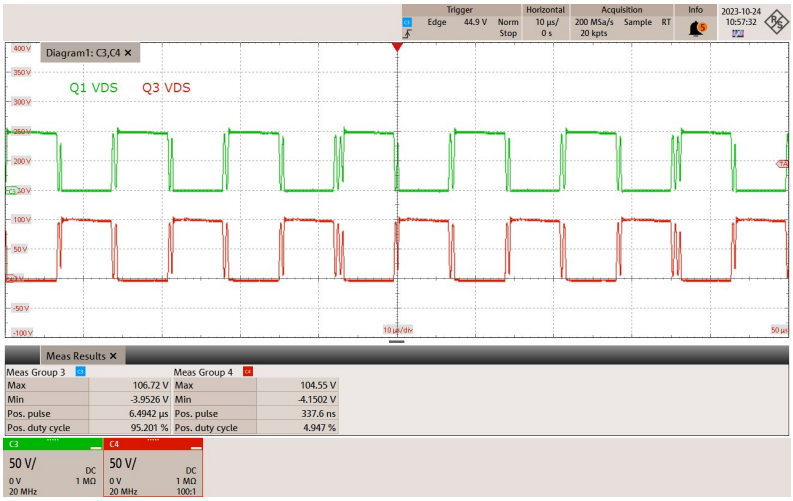


Figure 21 – Output Rectifier Peak Reverse Voltage. 400 VDC, Full Load.
Time Division: 10 µs / div.
CH3: Q_1 V_{DS}, 50 V / div.
CH4: Q_3 V_{DS}, 50 V / div.

11.2.2 Gate-Source Voltage

SR Gate drive was measured from the gate to source pins of the SR MOSFETs Q1 and Q3.

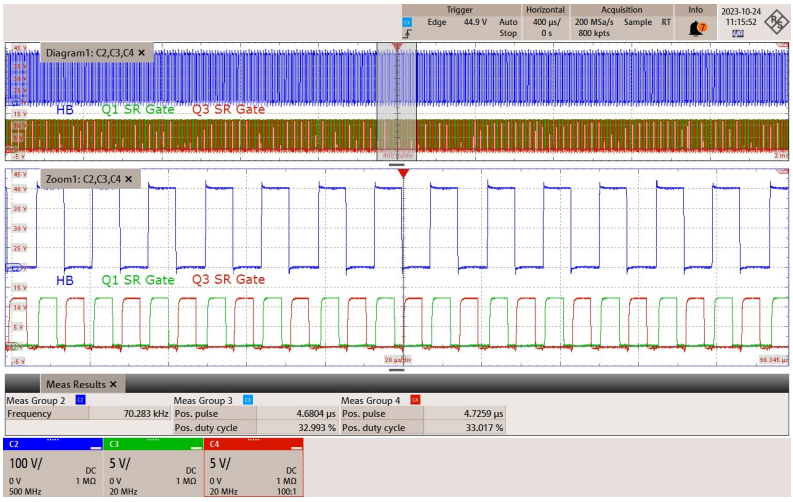


Figure 22 – Synchronous Rectifier Gate Drive. 400 VDC, Full Load.
Time Division: 400 µs / div.
Zoom Time Division: 20 µs / div.
CH2: HB, 100 V / div.
CH3: Q_1 V_{GS}, 5 V / div.
Ch4: Q_3 V_{GS}, 5 V / div.

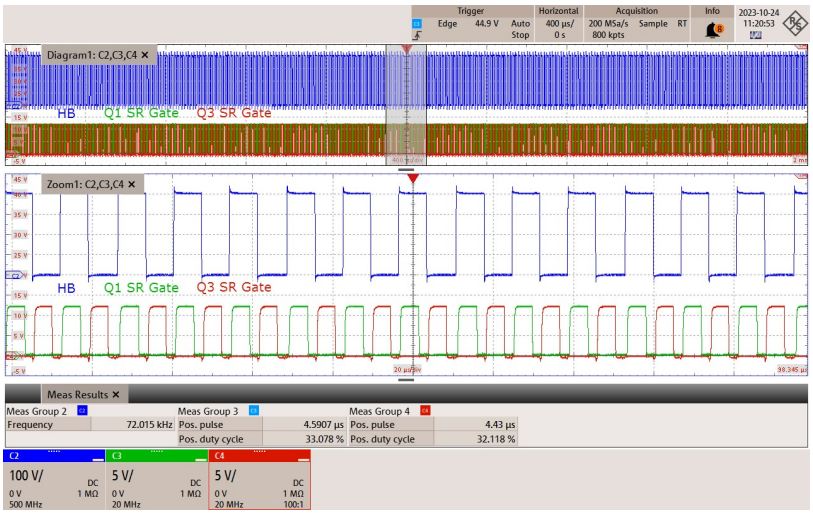


Figure 23 – Synchronous Rectifier Gate Drive. 400 VDC, Half Load.
Time Division: 400 µs / div.
Zoom Time Division: 20 µs / div.
CH2: HB, 100 V / div.
CH3: Q_1 V_{GS}, 5 V / div.
Ch4: Q_3 V_{GS}, 5 V / div.

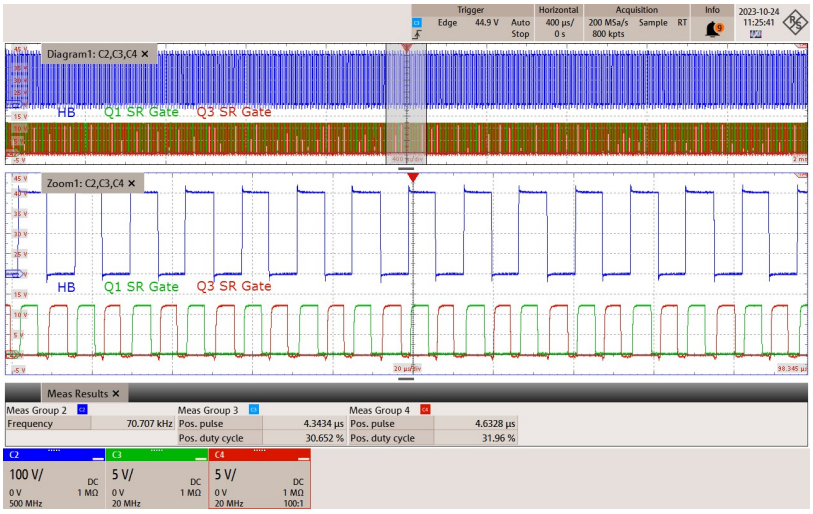


Figure 24 – Synchronous Rectifier Gate Drive. 400 VDC, 20% Load.
Time Division: 400 µs / div.
Zoom Time Division: 20 µs / div.
CH2: HB, 100 V / div.
CH3: Q_1 V_{GS}, 5 V / div.
Ch4: Q_3 V_{GS}, 5 V / div

11.3 Start Up Waveforms

Startup waveforms were captured with a DC input voltage adjusted between 380 VDC and 400 VDC. Loads were set to no load and full load for each input voltages.

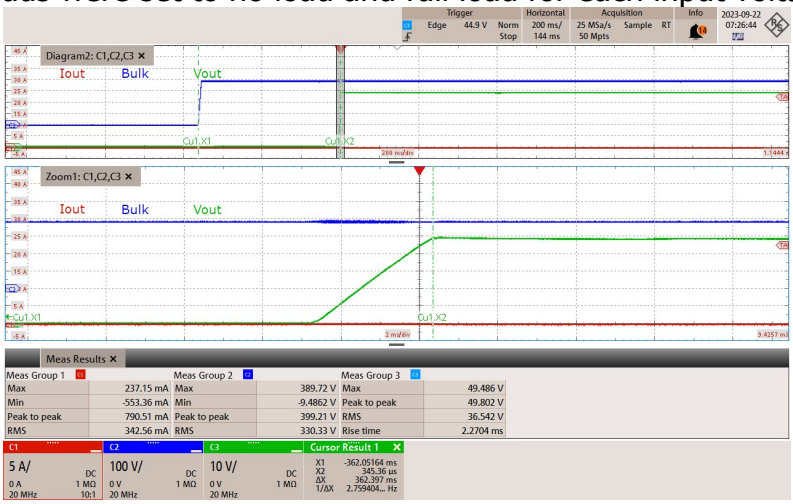


Figure 25 – Output Voltage at Start Up. 380 VDC, No Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 362 ms.
V_{OUT} Rise Time: 2.27 ms.
CH1: I_{OUT}, 5 A / div.
CH2: V_{BULK}, 100 V / div.
Ch3: V_{OUT}, 10 V / div.

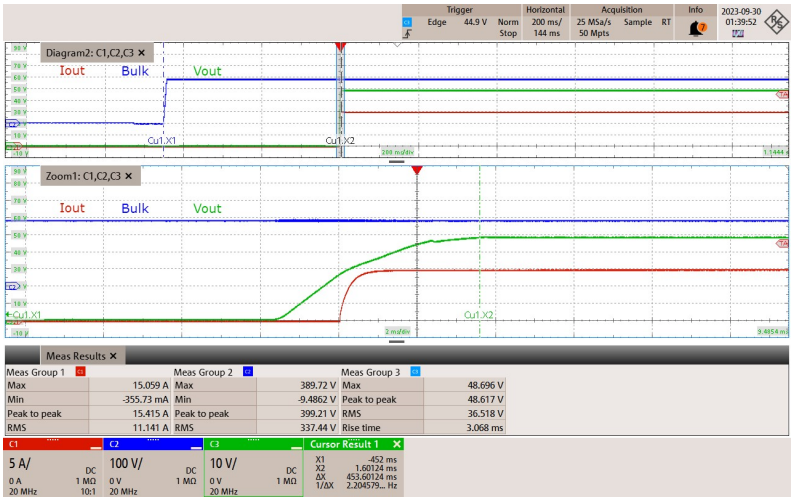


Figure 26 – Output Voltage at Start Up. 380 VDC, Full Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 454 ms.
V_{OUT} Rise Time: 3.07 ms.
CH1: I_{OUT}, 5 A / div.
CH2: V_{BULK}, 100 V / div.
Ch3: V_{OUT}, 10 V / div.

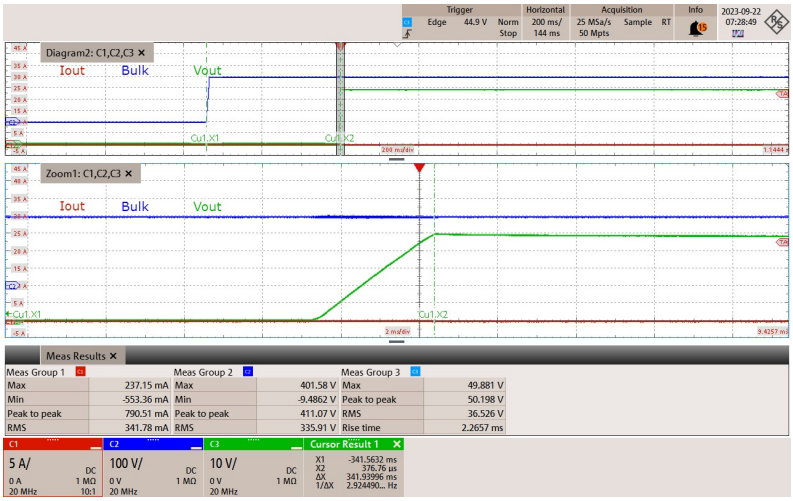


Figure 27 – Output Voltage at Start Up. 390 VDC, No Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 342 ms.
V_{OUT} Rise Time: 2.27 ms.
CH1: I_{OUT}, 5 A / div.
CH2: V_{BULK}, 100 V / div.
Ch3: V_{OUT}, 10 V / div.

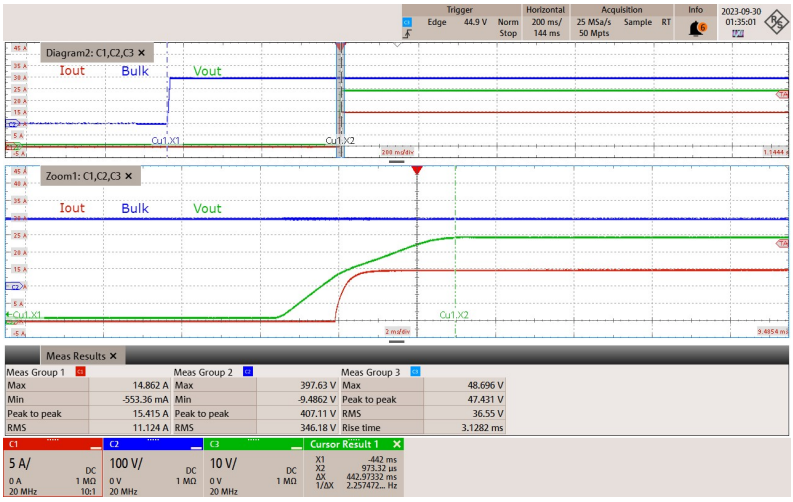


Figure 28 – Output Voltage at Start Up. 390 VDC, Full Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 443 ms.
V_{OUT} Rise Time: 3.13 ms.
CH1: I_{OUT}, 5 A / div.
CH2: V_{BULK}, 100 V / div.
Ch3: V_{OUT}, 10 V / div

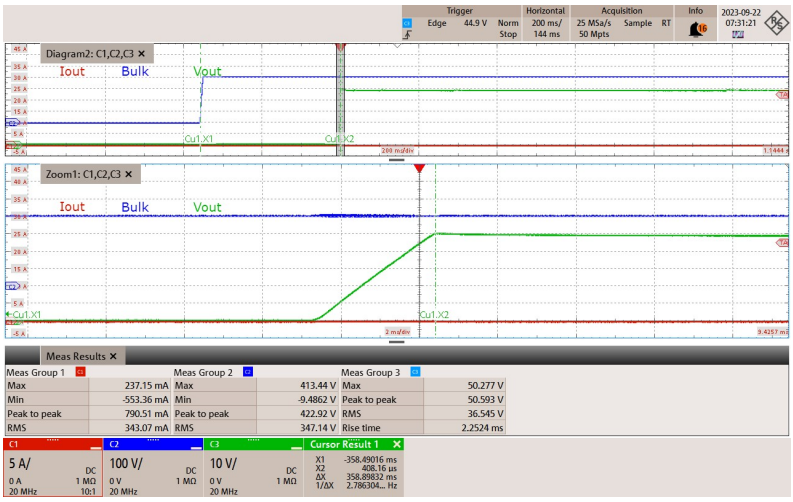


Figure 29 – Output Voltage at Start Up. 400 VDC, No Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 359 ms.
V_{OUT} Rise Time: 2.25 ms.
CH1: I_{OUT}, 5 A / div.
CH2: V_{BULK}, 100 V / div.
Ch3: V_{OUT}, 10 V / div

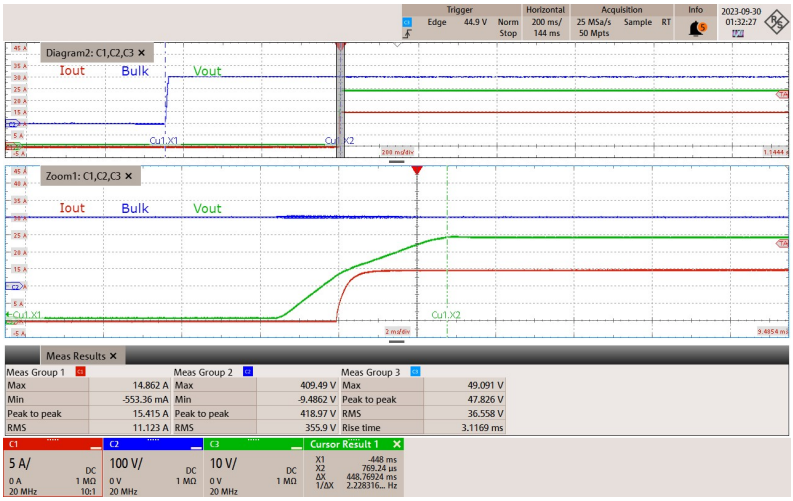


Figure 30 – Output Voltage at Start Up. 400 VDC, Full Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 449 ms.
V_{OUT} Rise Time: 3.12 ms.
CH1: I_{OUT}, 5 A / div.
CH2: V_{BULK}, 100 V / div.
Ch3: V_{OUT}, 10 V / div

11.4 Burst Operation Waveforms

Operation during different burst modes is shown below. For this configuration, the PS resistor R18 is set to 75 kΩ.

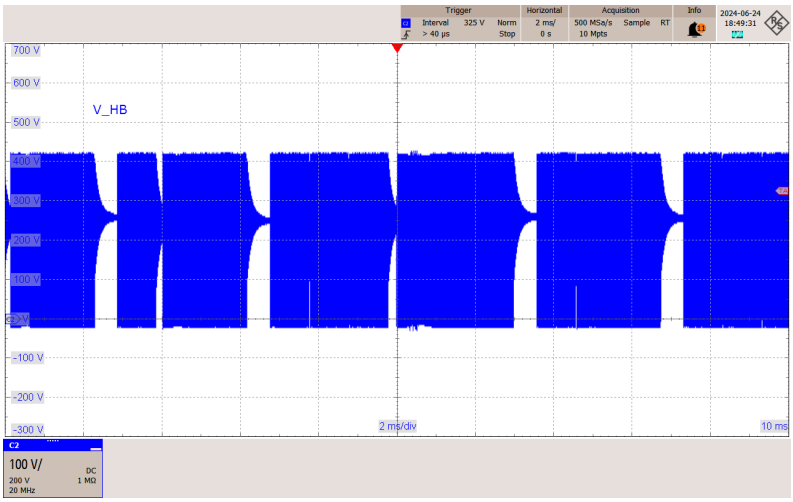


Figure 31 – Burst Profile at 0.95 A. 400 VDC.
Time Division: 2 ms / div.
CH2: V_{HB}, 100 V / div.

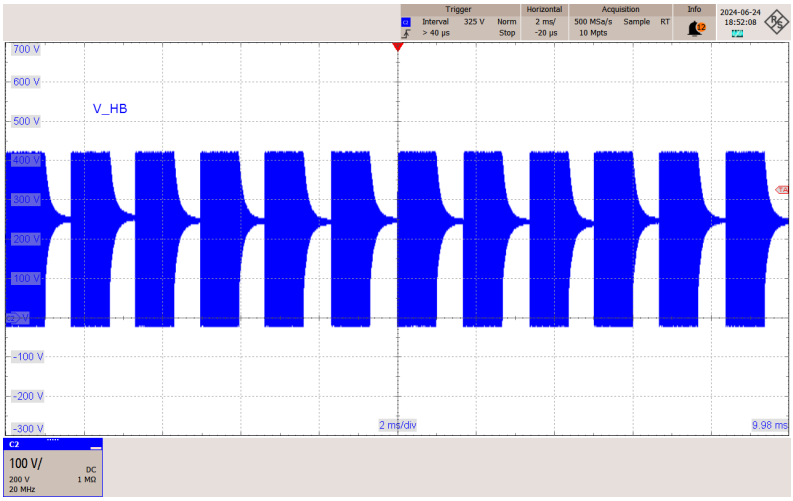


Figure 32 – Burst Profile at 0.54 A. 400 VDC.
Time Division: 2 ms / div.
CH2: V_{HB}, 100 V / div.

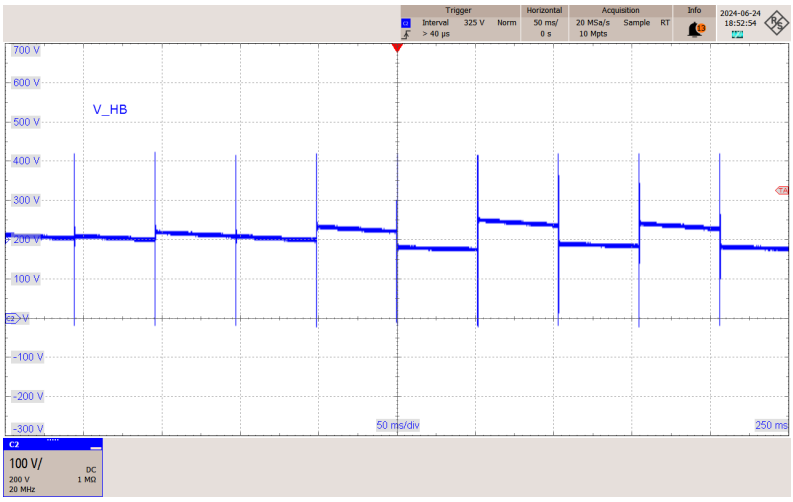


Figure 33 – Burst Profile at No Load. 400 VDC.
Time Division: 50 ms / div.
CH2: V_{HB}, 100 V / div.

11.5 Dynamic Loading

The figures below show the transient response of the UUT and demonstrate the very small change in the output voltage with a 0 – 100% – 0 step load change. Recovery time for the output was approximately 300 µs.

Electronic Load setting is as follows:
Duty Cycle = 50%, Frequency = 50 Hz, Slew Rate = 800 mA/µs.

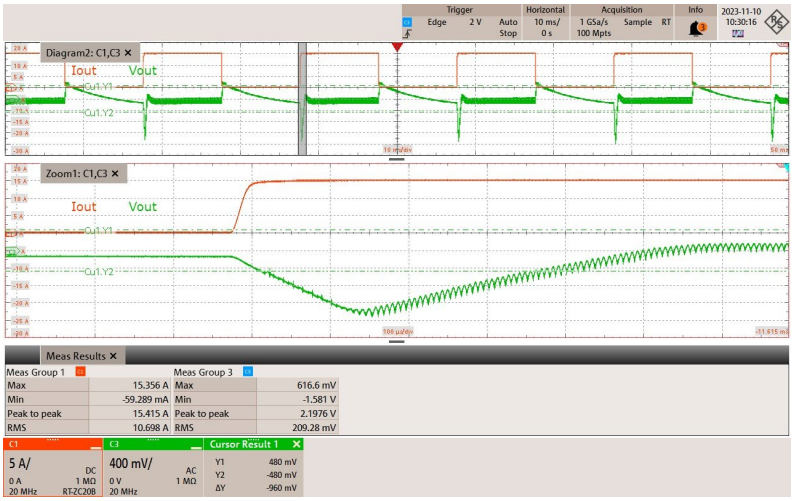


Figure 34 – Dynamic Loading. 400 VDC, 0-100% Load.
Time Division: 10 ms / div.
Zoom Time Division: 100 µs / div.
CH1: I_{OUT}, 5 A / div.
CH3: V_{OUT}, 400 mV / div.

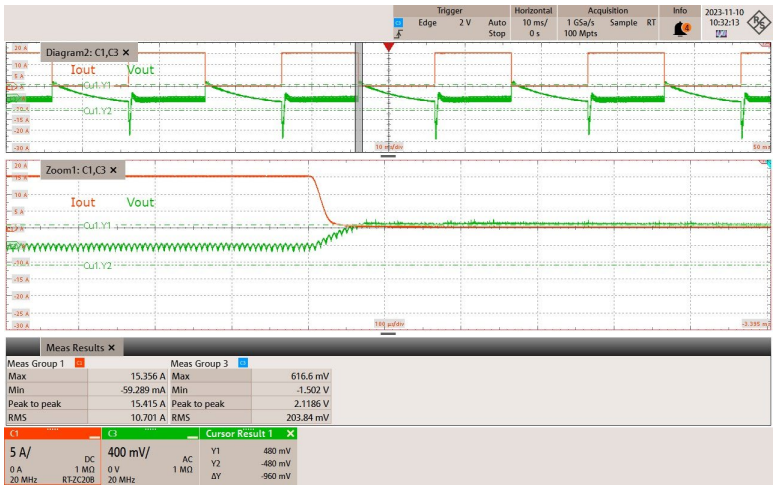


Figure 35 – Dynamic Loading. 400 VDC, 100-0% Load.
Time Division: 10 ms / div.
Zoom Time Division: 100 μs/ div.
CH1: I_{OUT}, 5 A / div.
CH3: V_{OUT}, 400 mV / div.

Note: During no-load burst mode was triggered which increased the output variation when compared to loaded conditions.

12 Output Ripple Measurements

12.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was used to reduce interference. Details of the probe modification are provided below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. A 0.1 μF / 100 V ceramic capacitor and 47 μF / 50 V aluminum electrolytic capacitor were used. The aluminum electrolytic capacitor is polarized, so always check for correct polarity between DC outputs.

Figure 36 – Oscilloscope Probe Prepared for Ripple Measurement (Probe cover and Ground Lead Removed).

Figure 37 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

12.2 Ripple Measurements

Output voltage ripple was measured at 400 VDC input voltage under different load conditions.

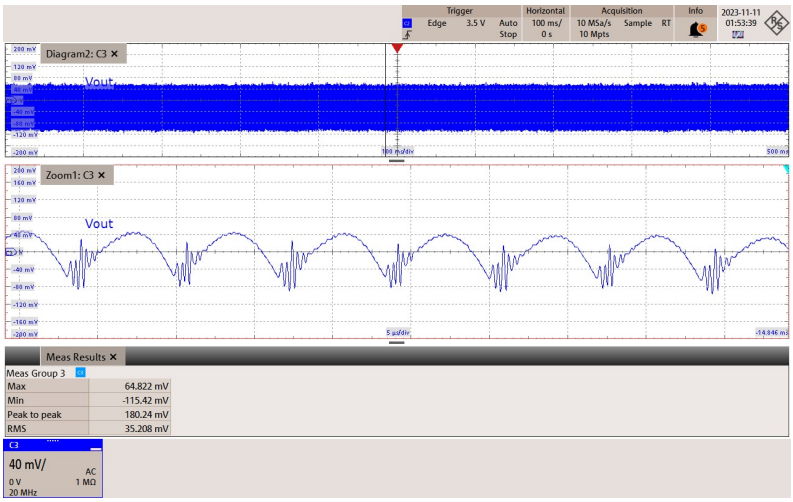


Figure 38 – Output Voltage Ripple. 400 VDC, Full Load.
Time Division: 100 ms / div.
Zoom Time Division: 5 μs / div.
Ripple: 0.38%
CH3: V_{OUT}, 40 mV / div.

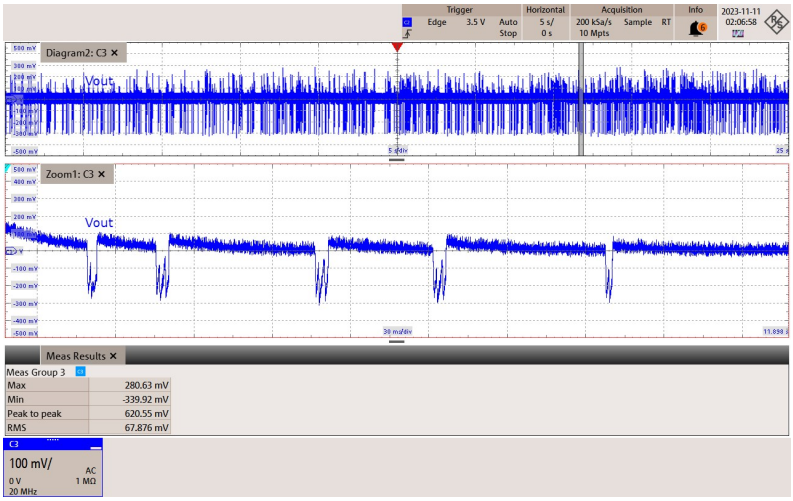


Figure 39 – Output Voltage Ripple. 400 VDC, 1 A Load.
Time Division: 5 s / div.
Zoom Time Division: 30 ms / div.
Ripple: 1.29%
CH3: V_{OUT}, 100 mV / div.

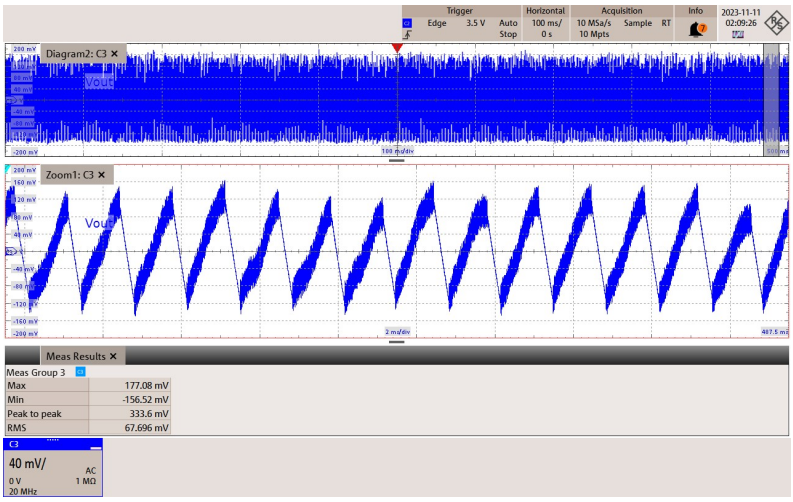


Figure 40 – Output Voltage Ripple. 400 VDC, 0.94 A Load.
Time Division: 100 ms / div.
Zoom Time Division: 5 ms / div.
Ripple: 0.70%
CH3: V_{OUT}, 40 mV / div.

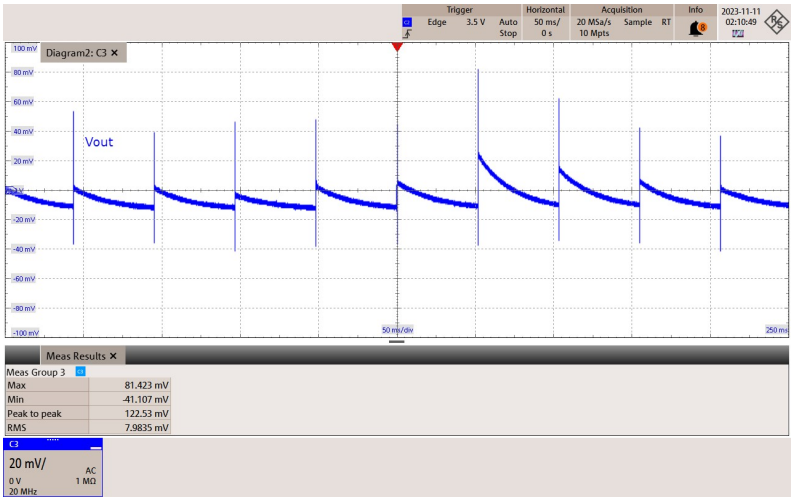
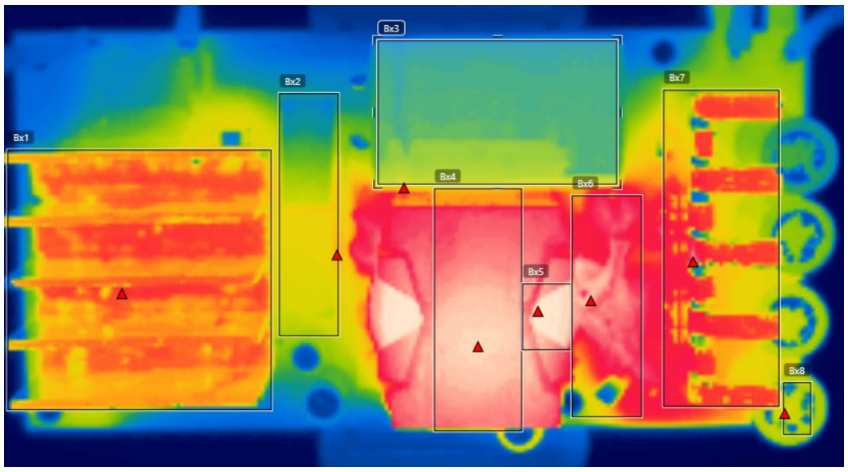


Figure 41 – Output Voltage Ripple. 400 VDC, No-Load.
Time Division: 50 ms / div.
Ripple: 0.26%
CH3: V_{OUT}, 20 mV / div.

13 Temperature Profiles

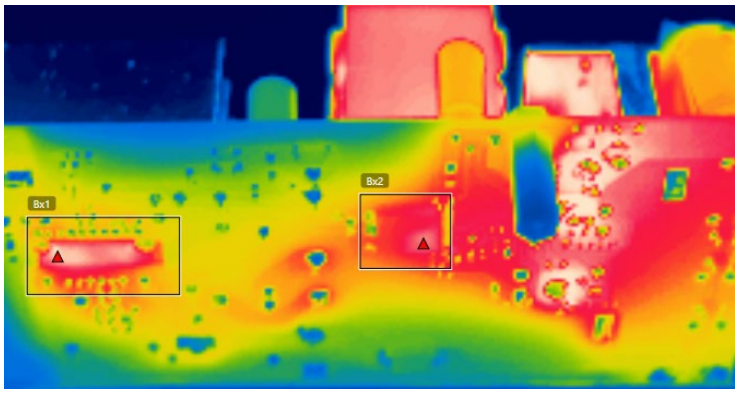
The UUT was powered up with an input voltage of 400 VDC and electronic load set to CCH at full load, 15 A (720 W). The unit was enclosed in an acrylic case to restrict air flow. For this test, the device was soaked for 1 hour before testing was performed.



Measurements		
Bx1	Max	84.0 °C
Bx2	Max	73.6 °C
Bx3	Max	66.3 °C
Bx4	Max	103.0 °C
Bx5	Max	109.9 °C
Bx6	Max	102.6 °C
Bx7	Max	94.6 °C
Bx8	Max	66.2 °C

Legend	Ref Des	Description	Temperature (ºC)
Bx1	Heatsink	PCD Heatsink	84.0
Bx2	C9, C45	Resonant Capacitors	73.6
Bx3	C1	Bulk Capacitor	66.3
Bx4	TRF	TRF Core	103
Bx5	TRF	TRF Primary Winding	110
Bx6	TRF	TRF Secondary Fly Leads	103
Bx7	Q1,Q3	SR FET/ SR Assembly	94.6
Bx8	C26	Output Capacitor	66.2

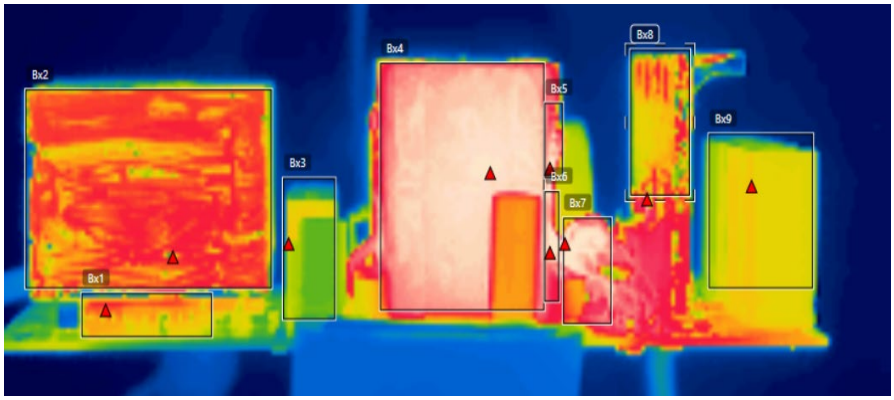
Figure 42 – Thermal Profile (Top), 100% Load, 400 VDC.



Measurements		
Bx1	Max	94.8 °C
Bx2	Max	88.1 °C

Legend	Ref Des	Description	Temperature (ºC)
Bx1	U1	Primary device (PCD)	94.8
Bx2	U2	Secondary device (SCD)	88.1

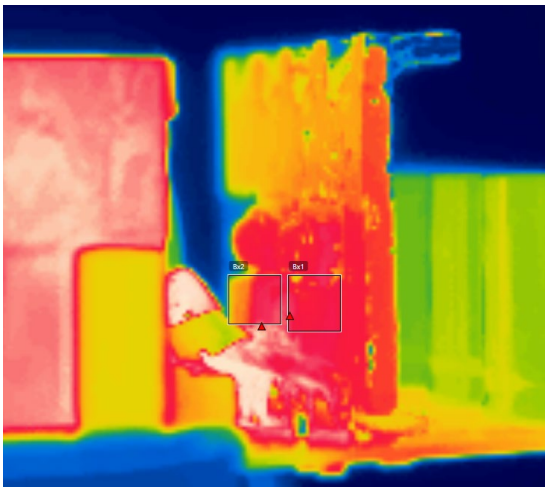
Figure 43 – Thermal Profile (Bottom), 100% Load, 400 VDC.



Measurements		
Bx1	Max	81.4 °C
Bx2	Max	82.7 °C
Bx3	Max	69.0 °C
Bx4	Max	100.9 °C
Bx5	Max	101.4 °C
Bx6	Max	108.0 °C
Bx7	Max	103.7 °C
Bx8	Max	87.6 °C
Bx9	Max	70.1 °C

Legend	Ref Des	Description	Temperature (ºC)
Bx1	U1	Primary device (PCD)	81.4
Bx2	Heatsink	PCD Heatsink	82.7
Bx3	C9, C45	Resonant Capacitors	69.0
Bx4	TRF	TRF Core	101
Bx5	TRF	TRF Primary Winding	101
Bx6	TRF	TRF Secondary Winding	108
Bx7	TRF	TRF Secondary Fly Leads	104
Bx8	Q1, Q3	SR Assembly	87.6
Bx9	C12, C25, C26, C42	Output Capacitors	70.1

Figure 44 – Thermal Profile (Side), 100% Load, 400 VDC.



Measurements		
Bx1	Max	90.3 °C
Bx2	Max	90.9 °C

Legend	Ref Des	Description	Temperature (ºC)
Bx1	Q1	SR MOSFET	90.3
Bx2	Q3	SR MOSFET	90.9

Figure 45 – Thermal Profile (SR MOSFETs), 100% Load, 400 VDC.

Table 6 Summary of Thermal Readings

Component	Temperature (ºC)
Ambient Temperature	32.5
Primary device (PCD)	94.8
Secondary device (SCD)	88.1
Resonant Capacitors	73.6
Bulk Capacitor	66.3
TRF Core	103
TRF Primary Winding	110
TRF Secondary Winding	108
TRF Secondary Fly Leads	104
Output Capacitors	70.1
SR Assembly	87.6
Q1 SR FET	90.3
Q3 SR FET	90.9

14 Revision History

Date	Author	Revision	Description and Changes	Reviewed
15-Jan-2025	AMM / RAC	A	Initial Release	Apps & Mktg

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