Design Example Report

Title	**1650 W DC-DC LLC Resonant Half-bridge Converter with Synchronous Rectification Using HiperLCS™2-HB LCS7269Z and HiperLCS2-SR LSR2000C**
Specification	400 VDC Input; 60 V at 27.5 A Output
Application	High Efficiency Isolated DC-DC Conversion
Author	Applications Engineering Department
Document Number	DER-1060
Date	February 25, 2025
Revision	A

Summary and Features

- Integrated LLC stage reduces component count
- Master controller allows precise control of synchronous rectification to optimize efficiency
- High efficiency across line and load
  - 96.8% full load conversion efficiency
  - 97.5% efficient at 50% load and nominal line
  - 96% efficient at 10% load across line
- High frequency (up to 250 kHz) LLC for small transformer size.
- Secondary-side sensing and feedback control with fast transient response
- Synchronous rectification driver
- No Load Input Power <180 mW

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PATENT INFORMATION

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer to provide the DC input to the prototype board.
Since there is no separate bias converter in this design, ~380-400 VDC is present on bulk capacitor C1 immediately after the supply is powered down. For safety, this capacitor must be discharged with an appropriate resistor (10 kΩ, 2 W resistor is adequate), or the supply must be allowed to stand ~10 minutes before handling.

1 Introduction

This report describes a DC-DC 1650 W, 60 V, 27.5 A power supply. The circuit is designed to operate from a fixed DC input that ranges from 380 VDC to 420 VDC.

The circuit is a resonant half-bridge (LLC) that employs the HiperLCS-2 chipset – a half bridge primary device and a secondary master controller with an integrated SR driver and barrier crossing technology (FluxLink™). In addition, the device provides comprehensive protection and safety features.

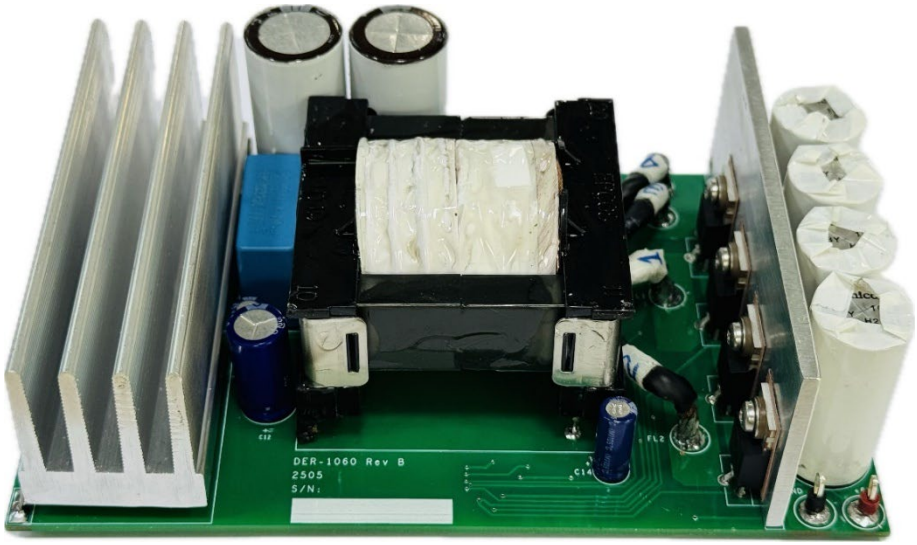


Figure 1 – DER-1060, Front View.

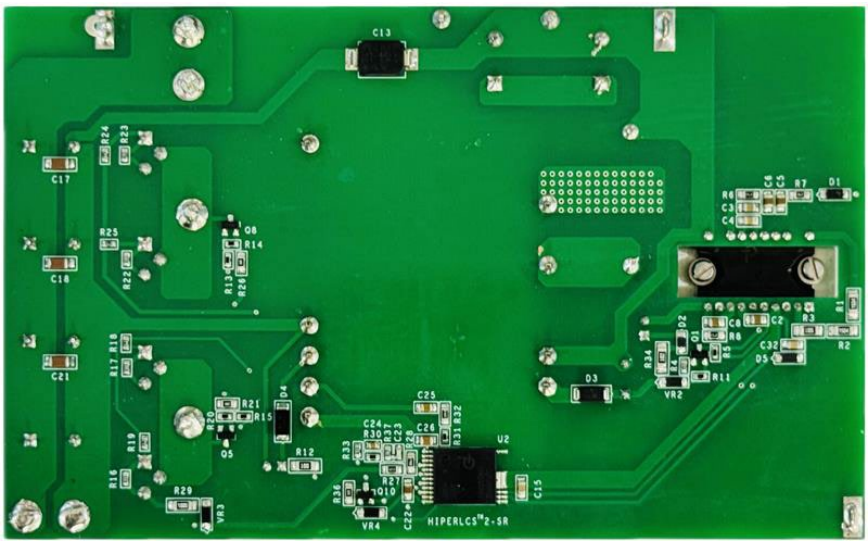


Figure 2 – DER-1060, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min.	Typ.	Max.	Units	Comment
Input						
Voltage	V_{IN}	380	400	420	VDC	DC-Input
No Load Input Power	$P_{IN(NL)}$		163		mW	Measured at 400 VDC
Main Converter Output						
Output Voltage	V_{OUT}		60		V	±1% Output Regulation
Output P-P Ripple Voltage	V_{RIPPLE}			350	mV_{PK-PK}	Within 1% of output at full load
Output Current	I_{OUT}		27.5		A	Full Load
Total Output Power						
Continuous Output Power	P_{OUT}		1.65		kW	Full Load
Efficiency						
100% Load			96.8			Measured at 400 VDC input.
50% Load	η_{Main}		97.5		%	
20% Load			96.4			
Ambient Temperature	T_{AMB}	0		40	°C	See Thermal Section for Conditions.

3 Schematic

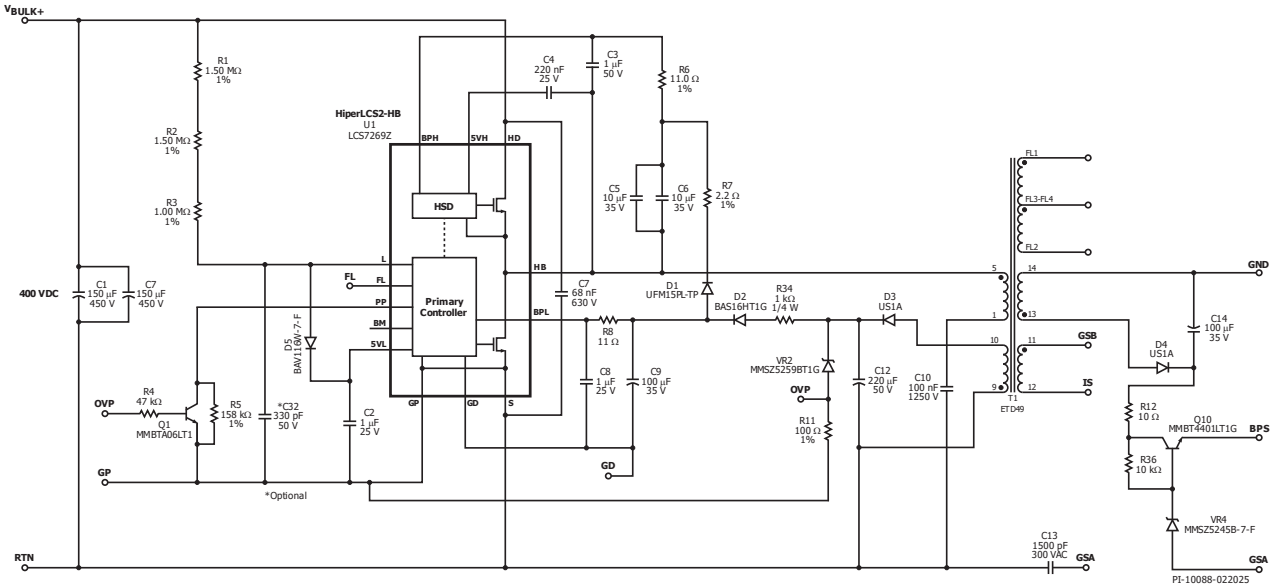


Figure 3 – Schematic of LLC Stage (Primary Side)

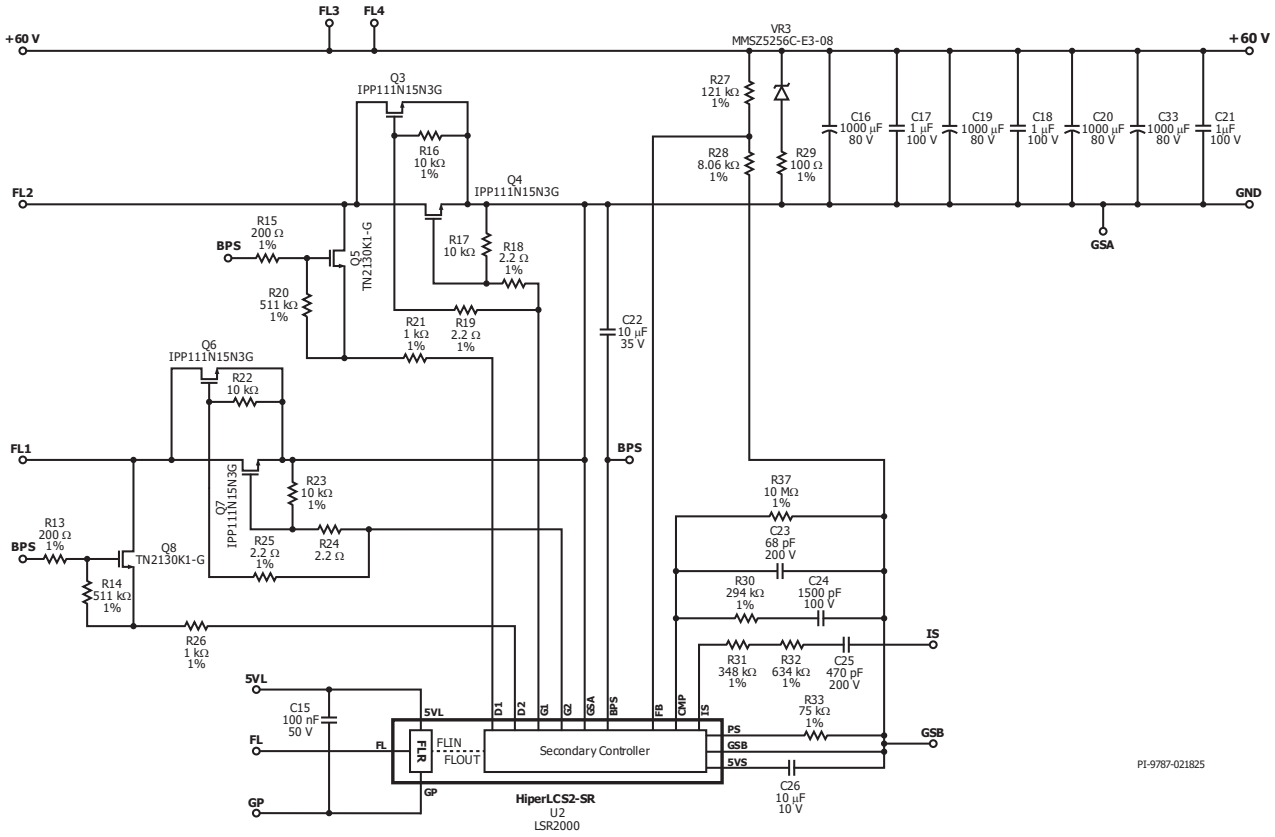


Figure 4 – Schematic of LLC Stage (Secondary Side)

4 Circuit Description

4.1 LLC Converter

The design consists of an LLC converter using HiperLCS2-HB IC, a primary half-bridge with integrated MOSFETs, and HiperLCS2-SR IC, a secondary master controller with secondary-primary communication, integrated reinforced safety isolation and a synchronous rectification driver stage.

4.2 LLC Primary

The high-voltage input bus is filtered through capacitor C1 and C7. Line sense (L-pin) detects the input bus voltage via resistors R1, R2 and R3. HiperLCS2-HB, U1, will initiate soft-start when L-pin goes above UV+ threshold. Capacitor C32 provides local decoupling for L-pin, while D5 clamps L-pin to 5V, these devices are recommended for high power designs to make the L-pin circuit less sensitive to noise. It is recommended that these devices be placed as close as possible to the L pin. Output overvoltage is sensed from the primary bias-winding (pin 8 and pin 9) of transformer T1, via Zener diode VR2 and resistor R11 and coupled to the PP pin via resistor R5 and transistor Q1. When an output over-voltage occurs, Zener VR2 conducts and current will be pulled from PP pin to ground via transistor Q1. Resistor R5 programs the PP pin primary frequency range and fault-response.

Capacitor C2 and C8 decouple the 5VL and BPL pins referencing them to GP and GD respectively. The primary return power-ground, RTN, is connected to the S-pin (SOURCE), primary-bias winding and bias capacitor. It is very important to keep the small signal ground (GP), separate from the system power-ground (RTN). The RTN power-ground offers a low-impedance path for system noise, allowing secondary-coupled noise currents to be safely delivered to the RTN/bulk-capacitor ground without disturbing the small-signal ground (GP pin).

Diode D3 rectifies the primary bias winding voltage and capacitor C12 provides decoupling to the RTN ground. Capacitor C8 provides local high-frequency decoupling at the BPL-pin. During start-up, before switching commences, the BPL pin charges capacitors C8 and C9, via resistor R8. This resistor limits output current from the BPL pin. Capacitor C9 provides energy storage to sustain start-up prior to the primary bias winding coming energized by switching. Capacitor C9 provides boot-strap energy to the HiperLCS2-HB high-side bias via diode D1 and resistor R7. Capacitor C9 should be large enough to provide the necessary bias during startup. As a guide, the capacitance of C6 should be more than 5x the sum of the capacitance of high-side bias capacitors C5 and C6.

Prior to bias winding activation during start-up, diode D2 acts as a blocking diode to prevent the charge current supplied by the BPL pin from being diverted to charge

capacitor C12. During normal operation the bias current flows from the bias winding to capacitor C12. The BPL-pin has an internal shunt regulator to limit the BPL voltage. Resistor R34 limits the BPL shunt-current when BPL shunt-voltage clamping is active thus limits BPL power dissipation. Careful attention should be paid to the steady state bias-winding voltage. If voltage is above the BPL clamp threshold, this will cause additional power dissipation in the BPL circuitry which may induce thermal shutdown of the HiperLCS-2 IC. It is important to recognize that the bias winding voltage may vary by up to 25% when the output load changes from zero to full load. For best no-load performance, the bias should be designed to deliver a minimum of 15 V. The BPL shunt will engage if the bias voltage at the BPL pin exceeds 21 V.

During the on-period of the low-side power MOSFET, the high-side bootstrap is charged via diode D1 and resistor R7 feeding capacitors C5 and C6. For the first few switching cycles at startup, capacitor C5 and C6 typically carry no charge and resistor R7 is required to limit current. Resistor R6 and capacitor C3 provide additional low-frequency filtering to the BPH pin. The high-side 5VH pin is decoupled via capacitor C4. Note that all high-side decoupling is tied to the HB pin.

The resonant tank inductance is the sum of inductance L_R (transformer-integrated resonant inductor) and magnetizing inductance, L_M, which appear in series between the HB pin and C10.

Y-capacitor C13 provides decoupling between primary and secondary grounds to reduce common mode noise on the secondary controller induced by primary-side switching noise.

4.3 LLC Secondary

The HiperLCS2-SR (U2) IC has safety-isolated primary side pins. Pin 5VL on the primary side of the HiperLCS2-SR is connected to the 5 V reference provided by the 5VL pin on the HiperLCS2-HB IC. This connection provides power for the primary side of the HiperLCS2-SR IC. The GP pin on the HiperLCS2-SR IC couples to the primary small signal ground pin of the HiperLCS2-HB IC. Capacitor C15 provides local decoupling to the 5VL and GP pins of U2. The FL pin provides a control signal generated by the master controller on the secondary side of the HiperLCS2-SR IC which is passed to the primary-side via the integrated FluxLink magneto inductive communication link. This control signal is delivered to the HiperLCS2-HB IC.

Transformer T1 output pins FL3/FL4 provide the positive output voltage, which is rectified by SR MOSFET pairs Q3 and Q4, and Q6 and Q7, and filtered by capacitors C16, C17, C18, C19, C20, C21 and C33. These capacitors have low combined ESR, which is the predominant factor in determining output ripple. Their combined capacitance should be chosen to provide the desired off-time in burst-mode. The capacitors are connected to the secondary-side power ground (GND).

Transformer output pins T1 FL1/FL2 provide the return path for synchronous rectifier MOSFET pairs Q3 and Q4 and Q6 and 17 respectively. The secondary power path is from T1 FL3/FL4 through capacitors C16, C17, C18, C19, C20, C21 and C33. To optimize matching of the two secondary power-phases, it is important to ensure that the secondary power path lengths of Q1 and Q3 are equal.

Capacitor C22 decouples the BPS pin, connecting it to the secondary SR-drive ground (GSA pin). Capacitor C26 decouples the 5VS pin connecting it to the secondary small signal ground (GSB pin).

Transformer T1 pin 13 feeds a diode D4 and capacitor C14 to rectify and filter the secondary bias voltage. The bias return is connected to T1 pin 14 and the secondary power ground (GND rail). The Zener diode VR3 and resistor R28 provide a small pre-load to ensure the output maintains regulation during no-load operation.

Output voltage is sensed via feedback resistors R20 and R21 which are referenced to GSB, the secondary small signal ground.

The small signal secondary ground (GSB pin) is used as a reference for feedback and compensation and provides the ground for IS-pin signals. The GSA pin is used to return SR-gate-drive signals. Loop compensation is positioned between the CMP and GSB pins - provide a pole (C24, R30), a zero (C23, R30) and a final pole (C23). The transformer IS winding T1 presented on pins 12 and 11 is grounded to the GSB pin and provides high frequency small-signal information which is capacitor coupled via C25 and resistors R31 and R32 to the IS pin.

Pin D1 and D2 sense the drain voltages on the synchronous rectifier pairs of Q3 and Q4 and Q6 and Q7 via resistors R21 and R26 respectively. The resistors limit the negative sensing current (WRT GND) into both pins. The resistor values can be used to control the SR MOSFET turn-off thresholds. Increasing the resistor value will cause the SR MOSFET to turn off at higher SR current.

Drive for the Q3 and Q4, and Q6 and Q7 synchronous MOSFET pairs is driven by the output of pins G1 and G2 via resistors R18, R19, R24 and R26. The drive resistors are optional and limit high-frequency MOSFET driver ringing. In the event of an FMEA open-connection fault condition between G1/G2 and Q3/Q4, and Q6/Q7 gate, local pull-down resistors R17, R19, R20 and R23 ensure that Q3/Q4 and Q6/Q7 remains off.

The PS pin resistor R33 is used to select burst threshold.

5 PCB Layout

The reference design employs the single layer PCB shown below. The board dimensions are 146.7 x 89.3 mm.

5.1 PCB Specifications

- Layer Count: 2 layers
- Solder Mask: Green
- Silkscreen: White
- Finish: ENIG
- Board Thickness: 1.6 mm
- Copper Thickness: 2 oz (2.8 mils)
- Material: FR4

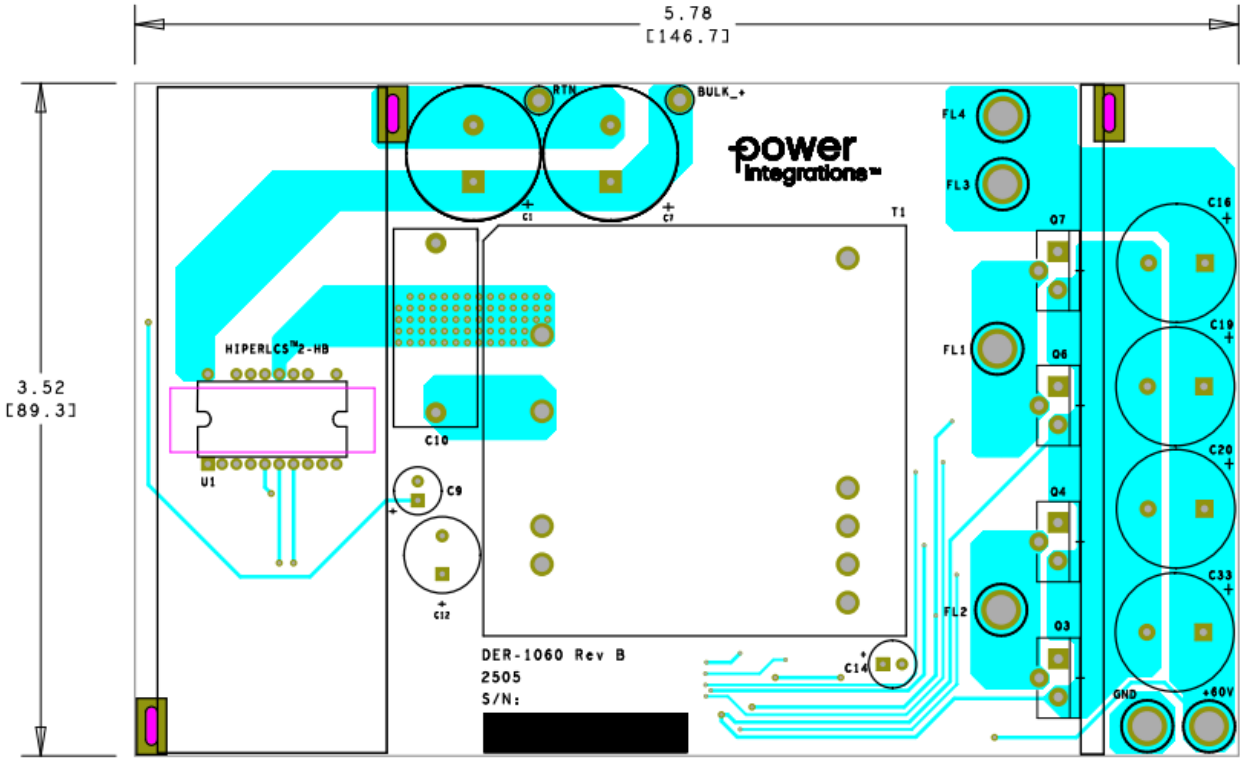


Figure 5 – Printed Circuit Layout, Top Side.

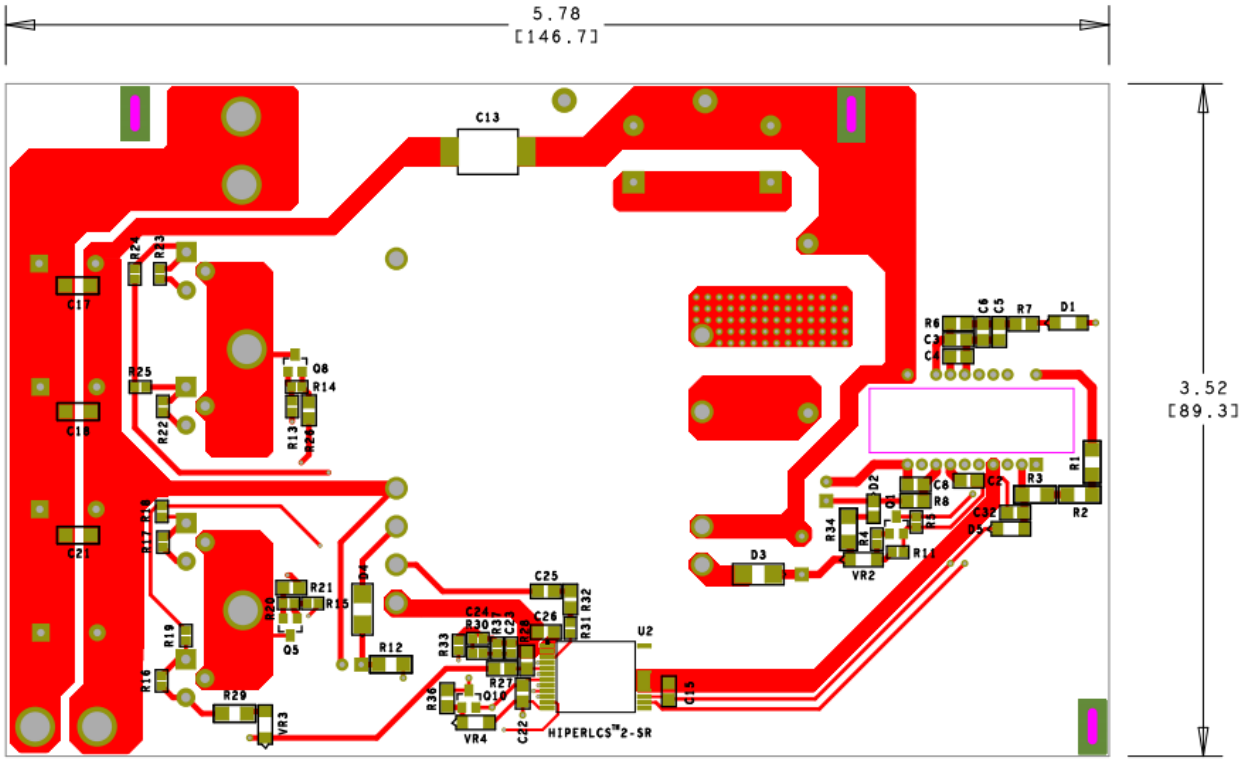


Figure 6 – Printed Circuit Layout, Bottom Side.

6 Bill of Materials

6.1 Electrical Parts

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	2	C1, C7	150 μF, 450 V, Electrolytic, (18 x 40)	UPH2W151MHD	Nichicon
2	2	C2, C8	1 μF, ±10%, 25 V, Ceramic, X7R, 0805 (2012 Metric)	GCM21BR71E105KA56L	Murata Electronics North America
3	1	C3	1 μF, 50 V, Ceramic, X5R, 0805	08055D105KAT2A	AVX Corporation
4	1	C4	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
5	3	C5, C6, C22	10 μF ±10% 35 V Ceramic Capacitor X5R 0805 (2012 Metric)	C2012X5R1V106K125AC	TDK Corporation
6	2	C9, C14	100 μF, 35 V, Electrolytic, Low ESR, 180 mOhm, (6.3 x 15)	ELXZ350ELL101MF15D	Nippon Chemi-Con
7	1	C10	100 nF, 1250 V, Metal Ply Rad	B32653A7104K	Epcos
8	1	C12	220 μF, 50 V, Electrolytic, Gen. Purpose, (10 x 12.5)	ECA1HM221	Panasonic
9	1	C13	Duplicate of 20-01414-00 1500 pF, ±20%, 300 VAC, X1, Y1, Ceramic Capacitor E, Nonstandard SMD	DK1E3EA152M86RBH01	Murata Electronics
10	1	C15	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
11	4	C16, C19, C20, C33	1000 μF, 80 V, ±20%, Aluminum Electrolytic Capacitors, Radial, Can, 27mOhm @ 100 kHz, 3000 Hrs @ 135 °C, (16 x 37)	UBY1K102MHL	Nichicon
12	3	C17, C18, C21	1 μF, 100 V, Ceramic, X7R, 1206	C3216X7R2A105K	TDK Corp
13	1	C23	100 pF 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
14	1	C24	2.2 nF 50 V, Ceramic, X7R, 0603	C0603C222K5RACTU	Yageo
15	1	C25	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
16	1	C26	10 μF, ±10%, 10 V, Ceramic Capacitor, Soft Termination, X7R, 0805 (2012 Metric)	C2012X7R1A106K125AE	TDK Corp
17	1	C32	330 pF, ±10%, 50 V, X7R, Ceramic Capacitor, -55 °C ~ 125 °C, MLCC 0805 (2012 Metric)	CL21B331KBANNNC	Samsung
18	1	D1	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123	UFM15PL-TP	Micro Commercial Co
19	1	D2	75 V, 200 mA, Rectifier, SOD323	BAS16HT1G	ON Semiconductor
20	1	D3	DIODE ULTRA FAST, 1 A, 100 V, SMA	US1B-13-F	Diodes, Inc
21	1	D4	DIODE ULTRA FAST GPP 50 V, 1 A, SMA	US1A-13-F	Diodes, Inc
22	1	D5	130 V, 5%, 250 mW, SOD-123	BAV116W-7-F	Diodes Inc
23	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1	Infineon Tech
24	4	Q3, Q4, Q6, Q7	150 V 83 A MOSFET N-CH TO220-3	IPP111N15N3 G	Infineon Technologies
25	2	Q5, Q8	MOSFET, N-Channel, 300 V, 85 mA (Tj), 360 mW (Tc), Surface Mount TO-236AB (SOT23)	TN2130K1-G	Microchip Technology
26	1	Q10	NPN, Small Signal BJT, GP, 40 V, 600 mA, 250 MHz, 300 mW , SOT-23, SOT-23-3 (TO-236)	MMBT4401LT3G	On Semiconductor
27	2	R1, R2	RES, 1.50 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1504V	Panasonic
28	1	R3	RES, 1.00 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1004V	Panasonic
29	1	R4	RES, 47 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
30	1	R5	RES, 158 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1583V	Panasonic

31	1	R6	RES, 11 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF11R0V	Panasonic
32	1	R7	RES, 2.2 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R2V	Panasonic
33	1	R8	RES, 11 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ110V	Panasonic
34	1	R11	RES, SMD, 100, 1%, 1/10 W, ±100 ppm/°C, -55 °C ~ 155 °C, 0603 (1608 Metric), Moisture Resistant, Thick Film	RC0603FR-07100RL	Yageo
35	1	R12	RES, 10 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J100V	Panasonic
36	2	R13, R15	RES, 200 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2000V	Panasonic
37	2	R14, R20	RES, 511 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF5113V	Panasonic
38	4	R16, R17, R22, R23	RES, 10 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
39	4	R18, R19, R24, R25	RES, 2.2 R, 1%, 1/16 W, Thick Film, 0603	ERJ-3RQF2R2V	Panasonic
40	2	R21, R26	RES, 1 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
41	1	R27	RES, 121 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1213V	Panasonic
42	1	R28	RES, 8.06 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8061V	Panasonic
43	1	R29	RES, 100 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1000V	Panasonic
44	1	R30	RES, 150 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1503V	Panasonic
45	1	R31	RES, 348 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF3483V	Panasonic
46	1	R32	RES, 634 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF6343V	Panasonic
47	1	R33	RES, 75 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ753V	Panasonic
48	1	R34	OPS|RES|1 kOhms ±5% 0.25 W, 1/4 W Chip Resistor 1206 (3216 Metric) Thick Film	CRCW12061K00JNEAC	Vishay Dale
49	1	R36	RES, 10 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
50	1	R37	RES, 10 M, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ106V	Panasonic
51	1	T1	Bobbin, ETD49, Horizontal, 20 pins	B66368B1020T1	EPCOS / TDK
52	1	U1	HiperLCS2-HB, LCS7269Z, POWeDIP-20B	LCS7269Z	Power Integrations
53	1	U2	HiperLCS2-SR, LSR2000C-H002, InSOP-24D	LSR2000C-H002	Power Integrations
54	1	VR2	DIODE ZENER 39 V 500 MW SOD123	MMSZ5259BT1G	ON Semi
55	1	VR3	Zener Diode, 62 V, 500 mW, ±2%, Surface Mount SOD-123	MMSZ5265C-E3-08	Vishay Semiconductor Diodes Division
56	1	VR4	DIODE ZENER 15V 500MW SOD123	MMSZ5245B-7-F	Diodes, Inc

6.2 Mechanical Parts

Item	Qty.	Reference Designator	Description	Manufacturer Part Number	Manufacturer
1	1	HS1	SHTM, HEATSINK, DER1060_SR_MOSFET, DRW, AL, 3003, Extrusion, Custom.	61-00380-00	Custom
2	1	HS2	SHTM, HEATSINK, DER1060_PCD, DRW, AL, 3003, Extrusion, Custom.	61-00381-00	Custom
3	3	TE1, TE2, TE3	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	Zierick

7 Magnetics

7.1 LLC Transformer

7.1.1 Electrical Diagram

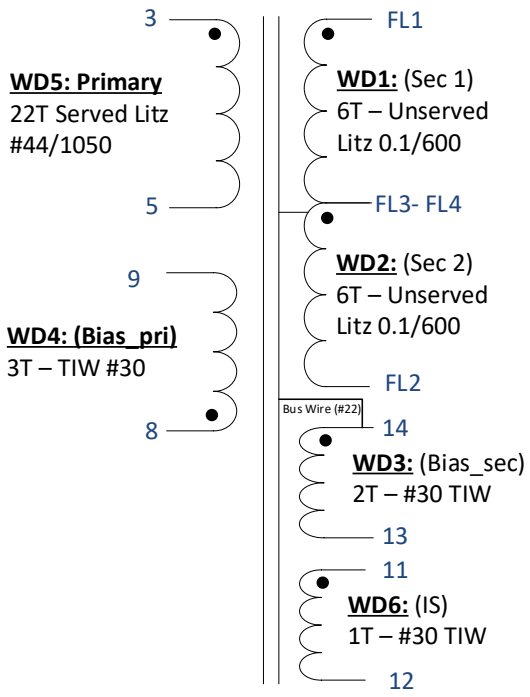


Figure 7 – LLC Transformer Electrical Diagram

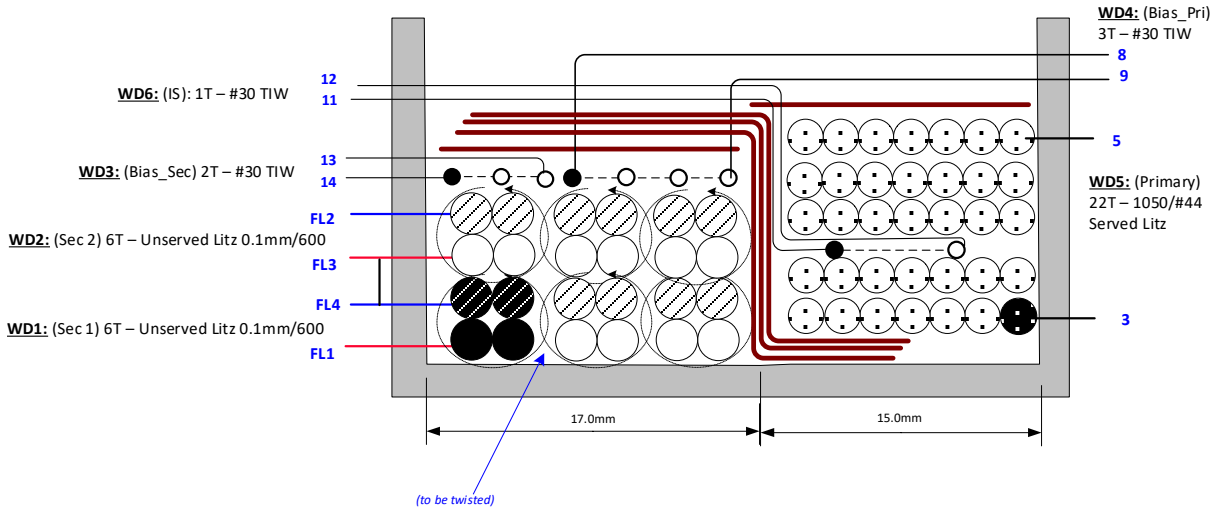
7.1.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 3,5,8,9 to FL1-FL3, FL2-FL4, pins 11,12, 13, 14.	3000 VAC
Primary Inductance (Lpri)	Pins 3-5, all other windings open, measured at 100 kHz, 1 Vrms	122 µH ±5%
Primary Leakage1 (LlkpALL)	Pins 3-5, short ALL other pins except IS-winding Pins 11&12, measured at 100 kHz, 1 Vrms	41 µH ±5%.
Primary Leakage2 (LkpIS)	Measured at Pins 3 - 5 (100 kHz, 1 Vrms), Short ONLY IS-winding Pins 11&12.	53 µH
Primary Leakage3 (LkpSEC1)	Measured at Pins 3-5 (100 kHz, 1 Vrms), Short ONLY FL2, FL3, FL4	41 µH
Primary Leakage4 (LkpSEC2)	Measured at Pins 3-5 (100 kHz, 1 Vrms), Short ONLY FL1, FL3, FL4	41 µH
Primary side Cres		100 nF
Resonant Frequency (fres)	Fseries = 1/ (2.pi*sqrt(LlkpALL.Cres)	78.6 kHz

7.1.3 Material List

Item	Description
[1]	Core: ETD49
[2]	Bobbin: ETD49-H, 20pins
[3]	Litz wire: 1050/#44AWG_Served Litz.
[4]	Litz wire: 0.1/600_Unserved Litz.
[5]	Triple Insulated Wire: #30AWG
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick
[7]	Tape: 3M 1298 Polyester Film, 1 mil thick, 30 mm width.
[8]	Bus wire: #22AWG, Alpha wire, tinned copper.
[9]	Clip: ETD49, Ferroxcube, Farnell P/N: CLI-ETD49.
[10]	Varnish: Dolph BC-359.

7.1.4 LLC Transformer Build Diagram



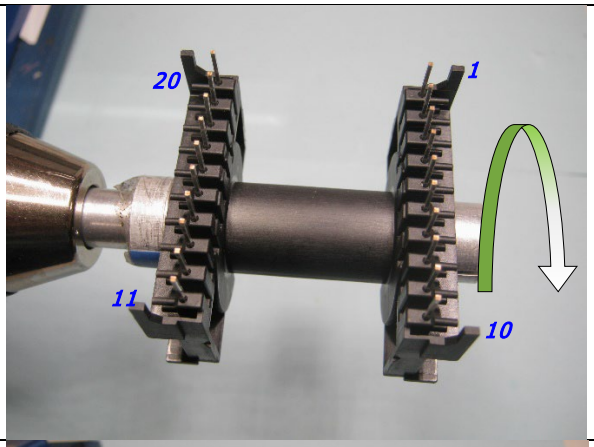
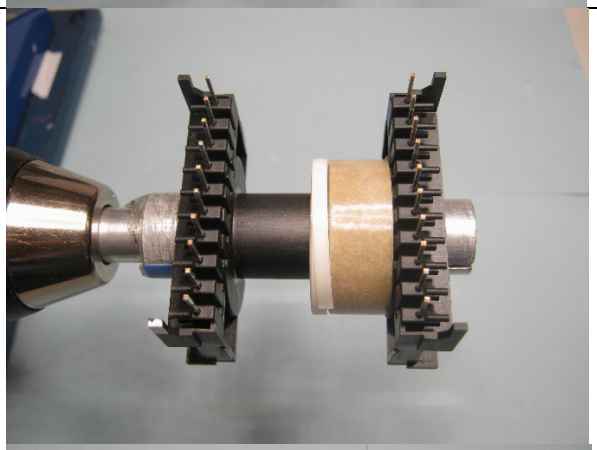
Notes: 1. WD1(SEC1) & WD2(SEC2) must exit at the bottom side of the bobbin.
2. Wire leads 11&12(WD6) should be twisted together before terminating to pins.
3. Wire leads 8 & 9 (WD4) should be twisted together before terminating to pins.

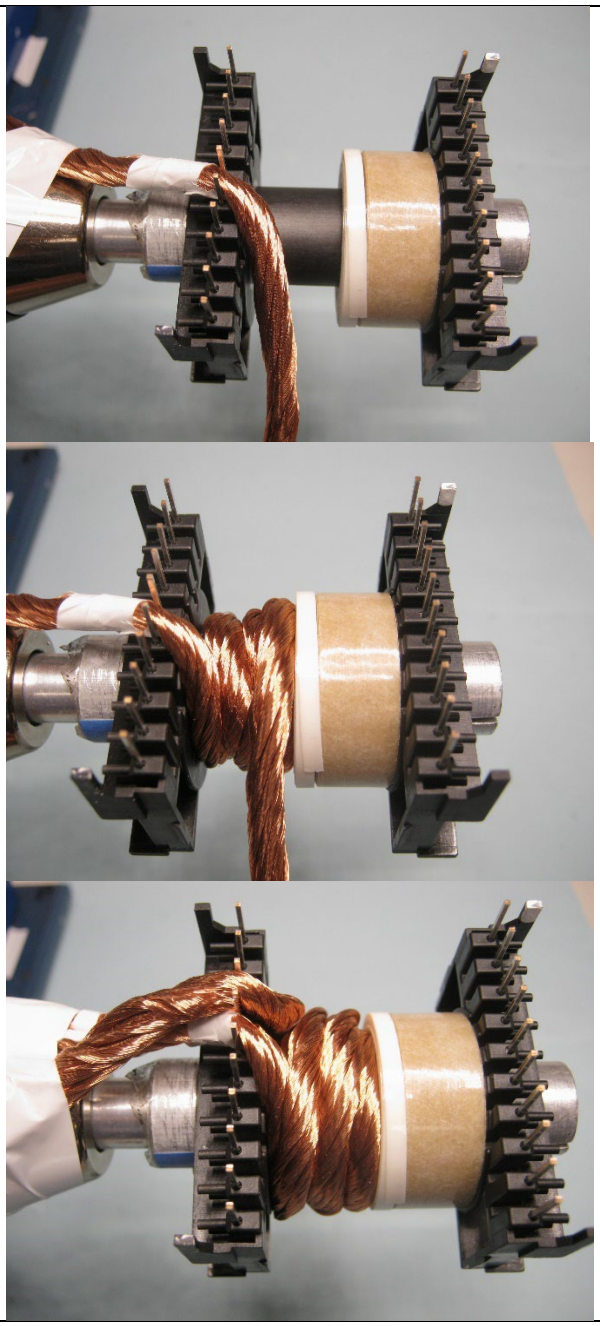
Figure 8 – LLC Transformer Build Diagram

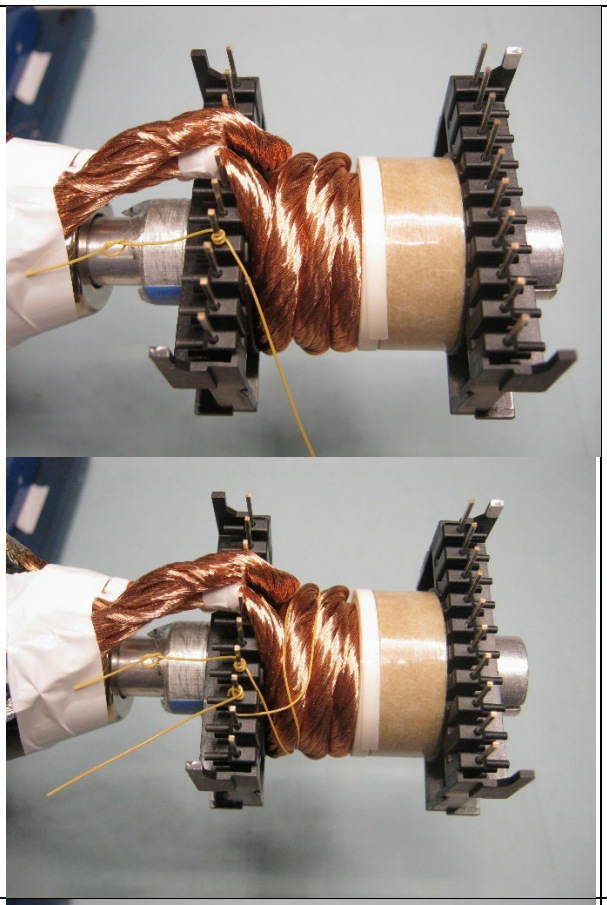
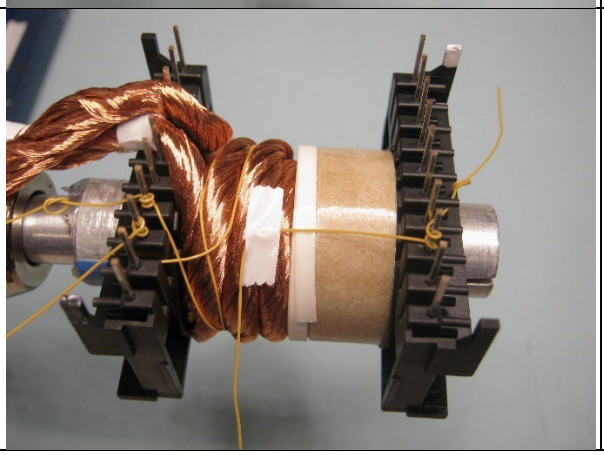
7.1.5 Transformer Preparations

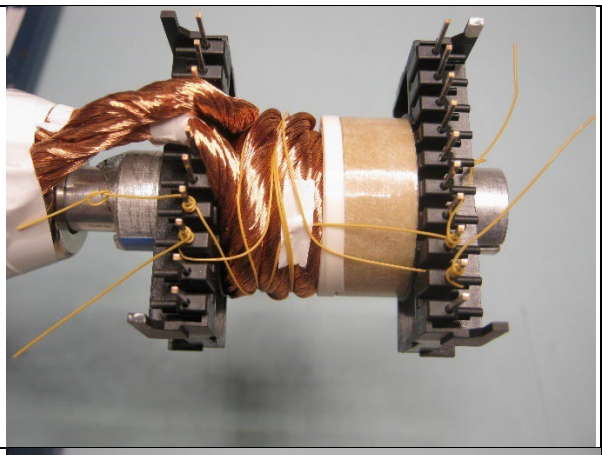
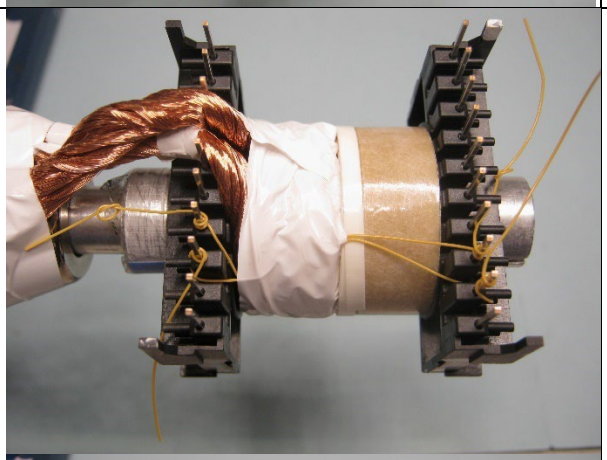
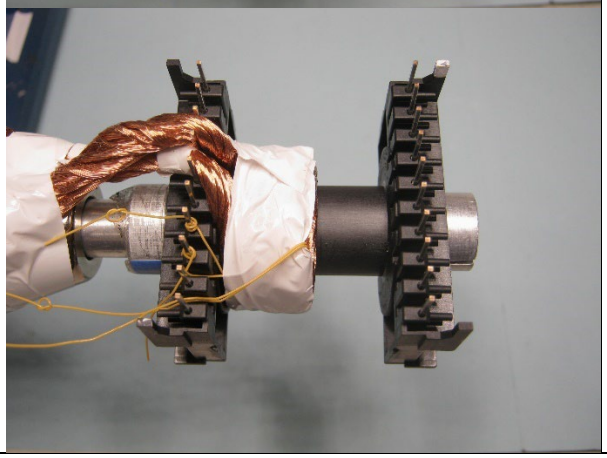
Winding preparation	Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the right side. Winding direction is clockwise direction for forward direction. Place margin tape to fill on the right of bobbin with 15 mm width for the right chamber. Use wire Item [4], cut into wires with 2ft long, tin both sides, and mark FL1, FL3 for 1 wire, FL2 FL4 for another wire. Twist these 2 wires together for secondary winding, (see picture below).
WD1 & WD2 Sec1 & Sec2	Use 2 wires prepared for secondary winding above, start with FL1, FL4, leave 2" of wires floating, wind 6 turns in 2 layers, with tight tension, from left to right, and right to left. At the last turn, exit the bobbin, and end with FL2, FL3 also floating.
WD3 Bias-Sec	Use wire Item [5], start at pin 14, wind 2 turns and end at pin 13 on top secondary winding.
WD4 Bias-Pri	Use wire Item [5], wind 3 turns also on top secondary winding with start and end leads temporarily hang on somewhere (will terminate when finish)
Insulation	Place 1 layer of tape Item [6] to hold secondary winding. Remove margin tape to have right chamber for primary winding. Place 3 layers of tape Item [7] to make divider between secondary and primary windings, (see pictures below).
WD5 Primary **WD6 IS**	Start at pin 3, wind 12 turns of wire Item [3] in 2 layers for WD5-Primary, then at pin 11 start with wire Item [5], wind 1 turn and bring wire back to the left and terminate at pin 12 for IS winding. Now to continue for WD5-Primary, wind another 10 turns and terminate at pin 5.
Insulation and wire terminations	Place 1 layer of tape Item [6] to secure primary winding. Bring start & end leads of WD4 to the right and twist to terminate at pin 8 & 9. Also twist all wires of windings WD3, WD6 before soldering to pins.
Finish	Gap core halves to get 122 μH. Solder pin 14 with bus-wire Item [8] then lean along core halves and secure with clips Item [9]. Varnish with Item [10].

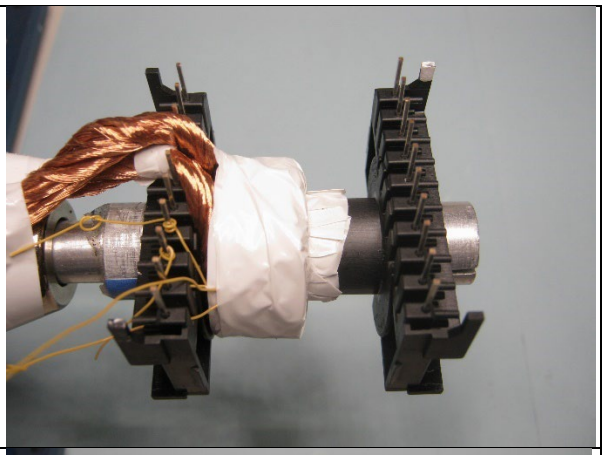
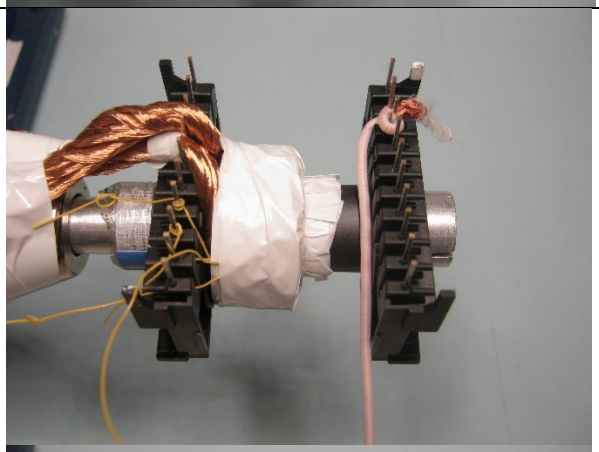
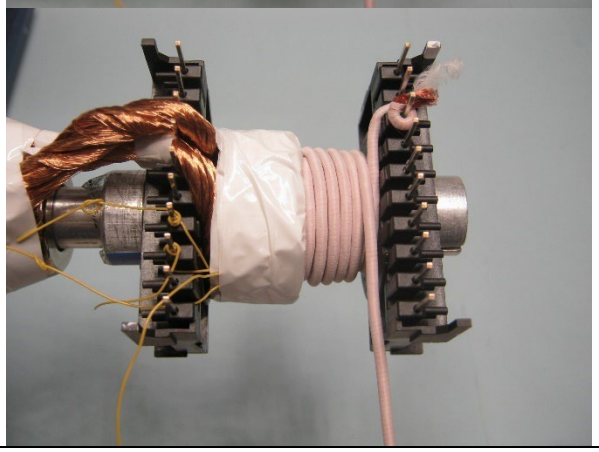
7.1.6 Winding Instructions

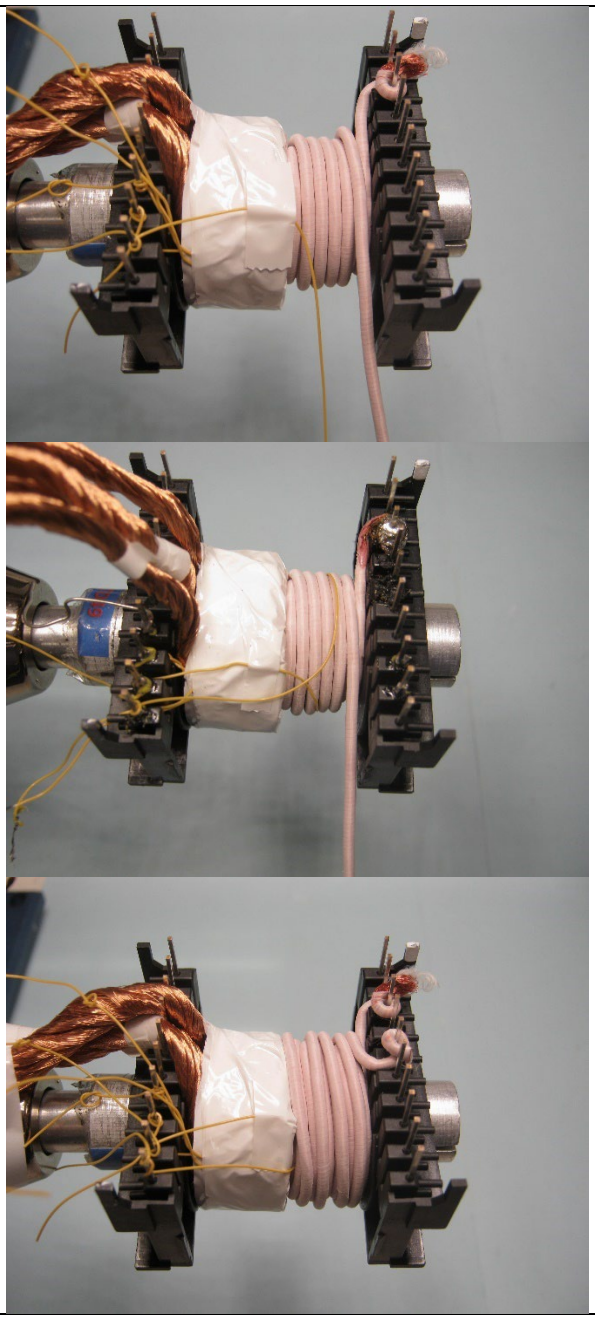
		Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the right side. Winding direction is clockwise direction for forward direction.
	 	Place margin tape to fill on the right of bobbin with 15 mm width for the right chamber. Place margin tape to fill on the right of bobbin with 15 mm width for the right chamber. Use wire Item [4], cut into 2 wires with 2 ft long, tin both sides, and mark FL1, FL3 for 1 wire, FL2 FL4 for another wire. Twist these 2 wires together for secondary winding, (see picture below).

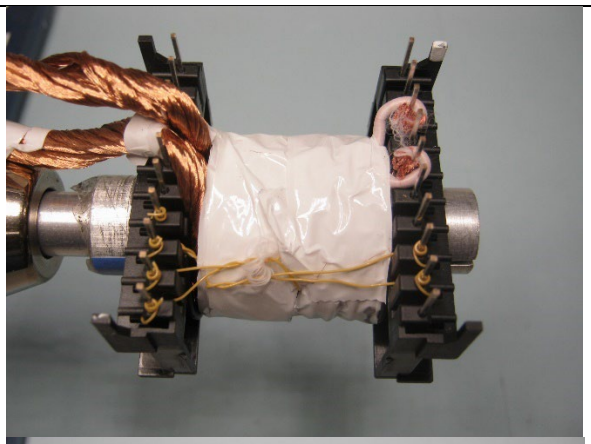
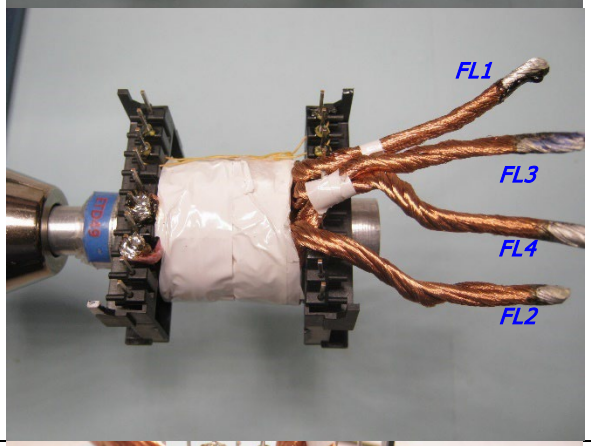
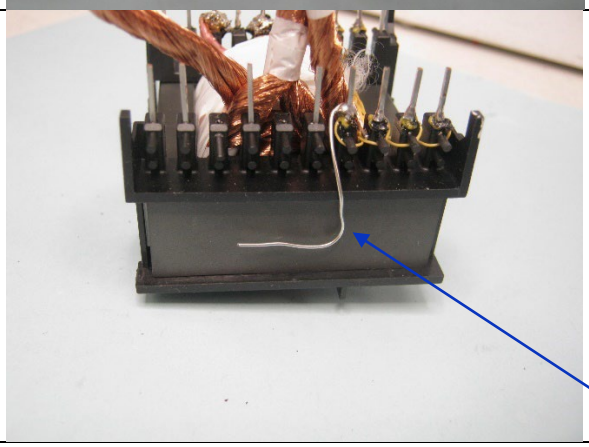
WD1 & WD2 **Sec1 & Sec2**		Use 2 wires prepared for secondary winding above, start with FL1, FL4, leave 2” of wires floating, wind 6 turns in 2 layers, with tight tension, from left to right, and right to left. At the last turn, exit the bobbin, and end with FL2, FL3 also floating.

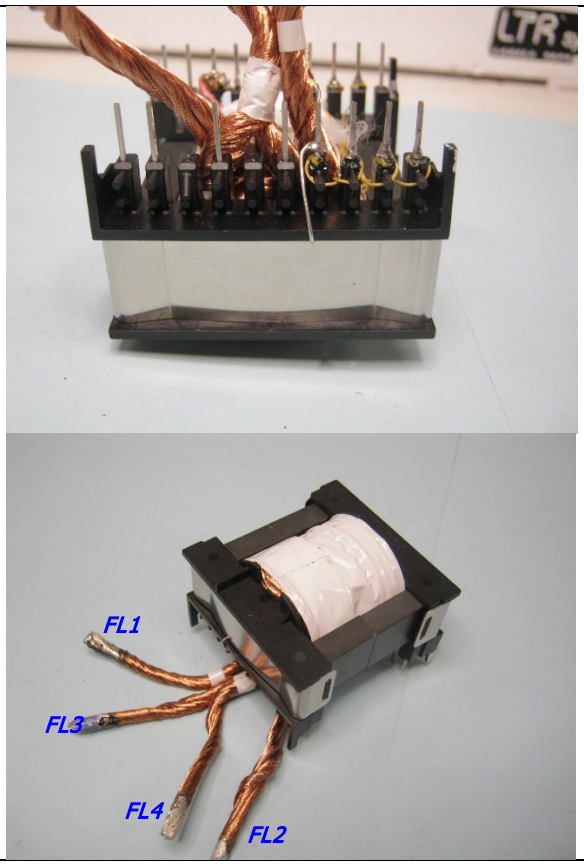
WD3 **Bias-Sec**		Use wire Item [5], start at pin 14, wind 2 turns and end at pin 13.
WD4 **Bias-Pri**		Use wire Item [5], wind 3 turns also on top secondary winding with start and end leads temporarily hang on somewhere (will terminate when finish)

		
Insulation	 	Place 1 layer of tape Item [6] to hold secondary winding. Remove margin tape to have right chamber for primary winding. Place 3 layers of tape Item [7] to make divider between secondary and primary windings, (see pictures beside).

		
WD5 **Primary** **WD6** **IS**	 	Start at pin 3, wind 12 turns of wire Item [3] in 2 layers for WD5-Primary, then at pin 11 start with wire Item [5], wind 1 turn and bring wire back to the left and terminate at pin 12 for IS winding. Now to continue for WD5-Primary, wind another 10 turns and terminate at pin 5.



Insulation and wire terminations	 	Place 1 layer of tape Item [6] to secure primary winding. Bring start & end leads of WD4 to the right and twist to terminate at pin 8 & 9. Also twist all wires of windings WD3, WD6 before soldering to pins.
Finish		Gap core halves to get 122 µH. Solder pin 14 with bus-wire Item [8] then lean along core halves and secure with clips Item [9]. Varnish with Item [10].


FL1
FL3
FL4
FL2

8 LLC Transformer Design Spreadsheet

1	ACDC_HiperLCS2_090324; Rev.2.0; Copyright Power Integrations 2024	INPUT	INFO	OUTPUT	UNITS	HiperLCS-2 Design Spreadsheet
2	General					
3	Description			>		LCS7269Z-1950W-60V-32.5A-SynchRF-22T-6T-81μH-41μH-100nF-83kHz
4	Input Parameters					
5	VIN MIN	320		320	V	Brownout Threshold Voltage
6	VIN RES	395		395	V	Input Voltage at Resonance - lower Vres to lower Npri
7	VIN NOM	400		400	V	Nominal Input Voltage - default CRM Vres=Vnom (or DCM Vres>Vnom, CCM Vres<Vnom)
8	VIN MAX	430		430	V	Maximum Input Voltage - decrease Vmax to lower Fmax
9	PFC	YES		YES		Input Option
10	Output Parameters					
11	Vout1	60.00		60.00	V	Main Output Voltage
12	Iout1 PK	32.5		32.5	A	Peak Main Output Current - default = 200% of Iout1Cont - used to select device size - increasing (IOUT1 PK) peak power will lower (LRES)
13	Pout1 PK			1950.0	W	Main Output Peak Power
14	Iout1 CONT	27.5		27.5	A	Continuous Main Output Current - default 50% of Ppeak - used to select device size - losses calculated at this power level
15	Pout1 CONT			1650.0	W	Continues Main Output Power
16	External CC	NO		NO		Use external CC operation
17	Vout1 Min (CC)				V	Minimum Output Voltage when operating in CC - lower VoutMin lowers Lm and also lowers efficiency
18	VCC				V	Output current sense resistor voltage when operating at CC-threhsold
19	RCC				mΩ	Output current sense resistor value
20	RCC Rated Power				W	Output current sense resistor rated power
21	Estimated Parameters, Design					

	Choices and Selections					
22	FS Range	Auto		1		Frequency Range
23	FS Vnom (Target)	75.0		75.0	kHz	Switching Frequency at VinNom
24	Output Rectifier	SynchRF		SynchRF		Output Rectifier
25	Ron_SR1			5.0	mΩ	Sync. Rectifier ON Resitance
26	VF_SR1				V	Output Diode Average Voltage Drop
27	Design Results					
28	DESIGN RESULT			Design Passed		Current Design Status
29	Device Variables					
30	DEVNAME	LCS7269Z		LCS7269Z		PI Device Name
31	QOSS			588	nC	Equivalent Combined Half-bridge charge (Qoss) at 480 V
32	RDSON			0.130	Ω	RDSON of selected device
33	Fault Responce	NON_LATCHING		NON_LATCHING		..
34	Tank Circuit Components & Operation Frequency Range					
35	Integrated Magnetics	YES		YES		Integrated Transformer Requirements
36	LP Nominal			121.86	μH	Nominal Primary Inductance
37	Lm			81.0	μH	Magnetizing inductance of transformer - modified by Kz, Device size and frequency
38	Lres			40.9	μH	Series resonant or primary leakage inductance - modified by Pmax
39	Cres	100.00		100.00	nF	Series resonant capacitor.
40	f_calc@Vbrownout			74.3	kHz	Frequency at PoutCont at Vbrownout, full load - adjust VinBrownout
41	f_calc@resonance			78.7	kHz	Frequency at PoutCont at Vres (defined by Lres and Cres) - adjust Vres)
42	f_calc@Vnom			83.5	kHz	Frequency at PoutCont at Vnom - adjust FS Vnom Target or Vnom
43	f_calc@Vinmax			87.4	kHz	Expected frequency at maximum input voltage and full load; Heavily influenced by n_eq and primary turns
44	VINGmaxInversion			278.0	V	Minimum Input Voltage for negative Gain at 100% load. Below this voltage the Gain

						becomes positive (unstable loop)
45	Core Dimensions/TRF Mechanical Parameters					
46	AE			211.00	mm^2	Transformer Core Cross-sectional area
47	VE			0.0	cm^3	Transformer Core Volume
48	MLT			86.71	mm	Middle Length of a Turn
49	AW			271.41	mm^2	Core Window area
50	BW			32.70	mm	Bobbin Winding Width
51	Bobbin Chambers			2		Bobbin Chambers
52	ChambDist			0.00	mm	Width of bobbin with no windings - empty space between primary/secondary generates leakage inductance
53	Bobbin Height			8.30	mm	Height of the bobbin, maximum Stack height
54	Prim. Bobbin Chamber Width			15.37	mm	Part of the bobbin allocated for primary
55	Sec. Bobbin Chamber Width			17.33	mm	Part of the bobbin allocated for secondary
56	K-PD			0.35		Penetration Depth multiplier (for Single Strand LITZ calculation)
57	Transformer Generic Parameters					
58	CR_TYPE	ETD49		ETD49		Transformer Core Type
59	FR_TYPE			N97		Magnetic material used
60	BACmax Actual			301.53	mT	Estimated Flux Density at Vnom - increase Ns to reduce Bmax
64	kSecChamb	0.53		0.53		Percentage of Bobbin Chamber Width used for Secondary Windings - Adjust to change Used Percentage of Primary/Secondary Windows
65	Transformer Primary Parameters					
66	Npri			22		Calculated Primary Winding Total Number of Turns
67	Iprim RMS			13.91	A	Transformer Primary Winding RMS Current at PoutCont and VinNom
79	Main Output Parameters					
80	NSec	6		6		Secondary Number of Turns
81	ISRMS			46.10	A	Transformer Secondary

						Winding RMS Current
93	Circuit Losses					
97	CO ESR Loss			1.37	W	Output Capacitor ESR Loss at VinNom and PoutCont
98	PLOSS Switch			12.57	W	Single Primary Switch Conduction Loss at VinNom and PoutCont
99	PLOSS Output Rectifier			2.33	W	Single Output Rectifier Conduction Loss at VinNom and PoutCont
100	PLOSS RCC			0.00	W	Current sense resistor power loss at VinNom and PoutCont
102	PLOSS Circuit Total			31.18	W	Circuit Total Loss at VinNom and PoutCont
103	Circuit Components					
104	RZ1			150	kΩ	Control Zero (boost high-frequency gain)
105	CP2			100	pF	Control Pole2 (roll-off high-frequency gain)
106	Cp1			2.2	nF	Control Pole1 (roll-off low-frequency gain)
107	Resr CO			1.00	mOhms	ESR of the output capacitor
108	COmin			1403	µF	Min CO to satisfy burst conditions
109	RD1			500	Ω	RD1 Resistor value
110	RD2			500	Ω	RD2 Resistor value
111	CBPL			1	µF	CBPL Capacitor Value /25 V
112	CBPH			1	µF	CBPH Capacitor Value /25 V
113	C5VL			1	µF	C5VL Capacitor Value /10 V
114	C5VH			220	nF	C5VH Capacitor Value /10 V
115	C5VFL			100	nF	C5VLFL Capacitor Value /10 V
116	C5VS			10	µF	C5VS Capacitor Value /10 V
117	CBPS			10	µF	CBPS Capacitor Value /35 V
118	RL_Up			open	kΩ	L-pin Input Voltage (Vin) Sense Resistor
119	RL_Down			shorted	Ω	L-pin to Ground Resistor
120	RPP			158	kΩ	RPP Resistor /1% E96 series
121	RPS			75	kΩ	RPS Resistor /1% E96 series
122	Bias, IS Circuit & Feedback Components					
123	NPB			2		Primary Bias Turns
124	NSB			2		Secondary Bias Turns
125	NVIS			2		Secondary (Is) Sense Turns
126	RIS			1681	kΩ	Rrs Resistor Value
127	CIS			470	pF	IS sense winding coupling capacitor
128	RFBH			360.6	kΩ	Calulated value of top

						feedback resistor. use series closest resistor 1% E96
129	RFBL			24.0	kΩ	Calculated value of low feedback resistor. use series closest resistor 1% E96
130	Currents and Winding loss elements					
131	Iprim RMS			13.91	A	Transformer Primary Winding RMS Current at PoutCont at VinNom
132	ISRMS			46.10	A	Transformer Secondary Winding RMS Current at PoutCont at VinNom
133	Irms_SR			21.60	A	Secondary Rectifier RMS Current at PoutCont at VinNom
134	Irms_CO1			36.99	A	Output Capacitor RMS Current at PoutCont at VinNom
139	Advanced Settings					
140	Kz	2.1		2.1		coefficient of surplus ZVS energy @ Vnom - raise Kz to lower Vin (GmaxInv) - Kz should be >= 1.0 to ensure ZVS operation
141	Tdd1_Vinnom	125		125	ns	Half-bridge slew at 100% load @ Vnom - raise Tdd1 to lower ZVS currents
142	Coupling			0.89		Transformer Coupling
143	Cpri			40.00	pF	Stray Capacitance at transformer primary
144	PP or Lpin	PP		PP		HB Startup current selection
145	R_L_UP_ACT				kΩ	Actual Value of L-pin Input Voltage (Vin) Sense Resistor
146	VLUV-				V	..
147	VLUV+				V	..
148	VLOV-				V	..
149	VLOV+				V	..
150	External Resonant Inductor (Ext.Lres) Calculations					
172	Errors, Warnings, Information					
173	Information			0		Number of variables required bench functionality check. Check the variables with "Info" in the third column.
174	Design Warnings			0		Number of variables whose values exceed electrical/datasheet

						specifications. Check the variables with "Err" in the third column .
175	Design Errors			0		The list of design variables which result in an infeasible design.

9 Heatsinks

Two heatsinks are used for the design. One is for the primary side HiperLCS2-HB IC and the other is for the synchronous rectifier MOSFETs on the output.

9.1 Primary Device Heatsink

The HiperLCS2-HB IC on the primary side uses an aluminum heatsink with fins.

Note: When tightening the fixing screws for the primary IC, a torque screwdriver should be used set to 1 pound-inch.

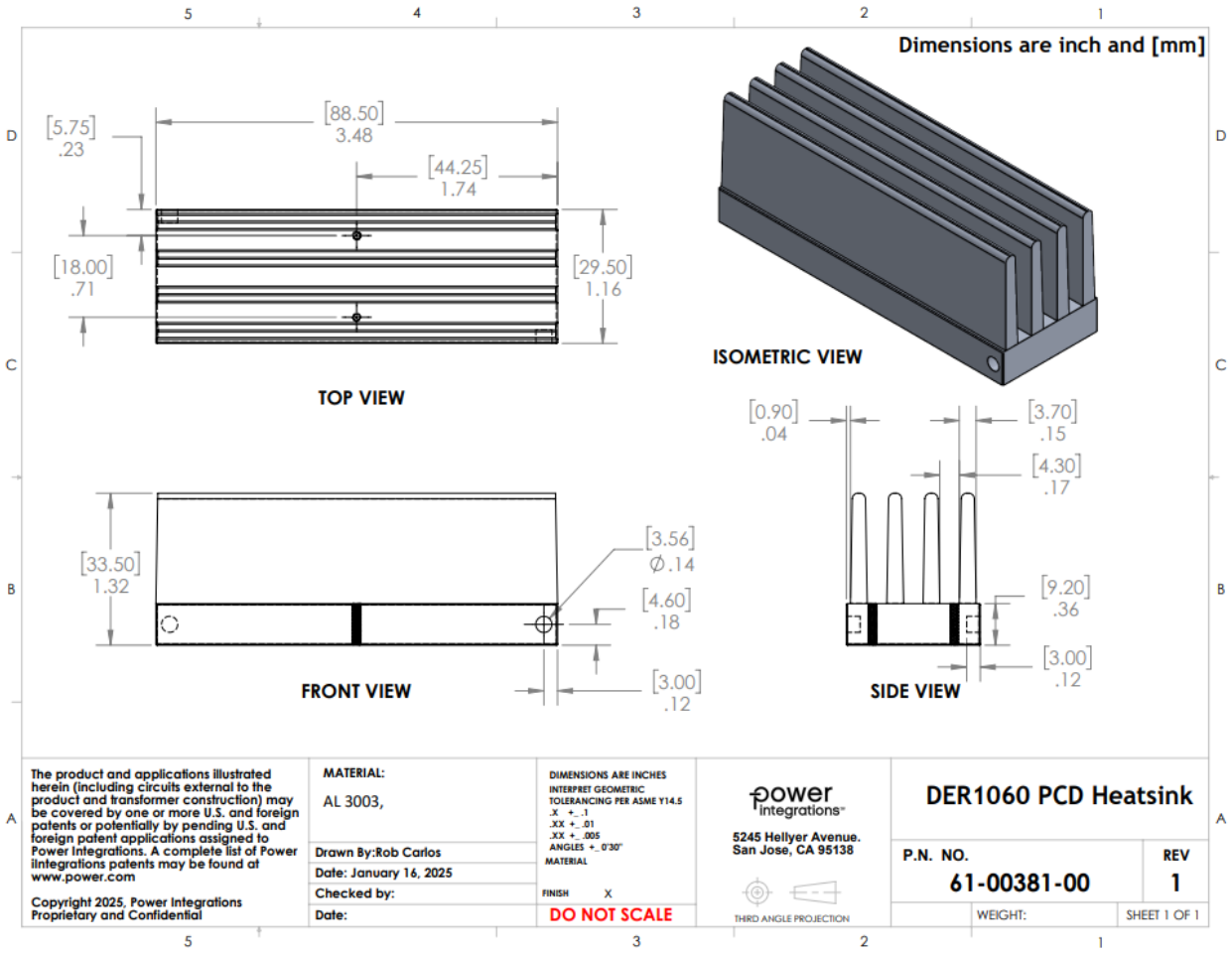
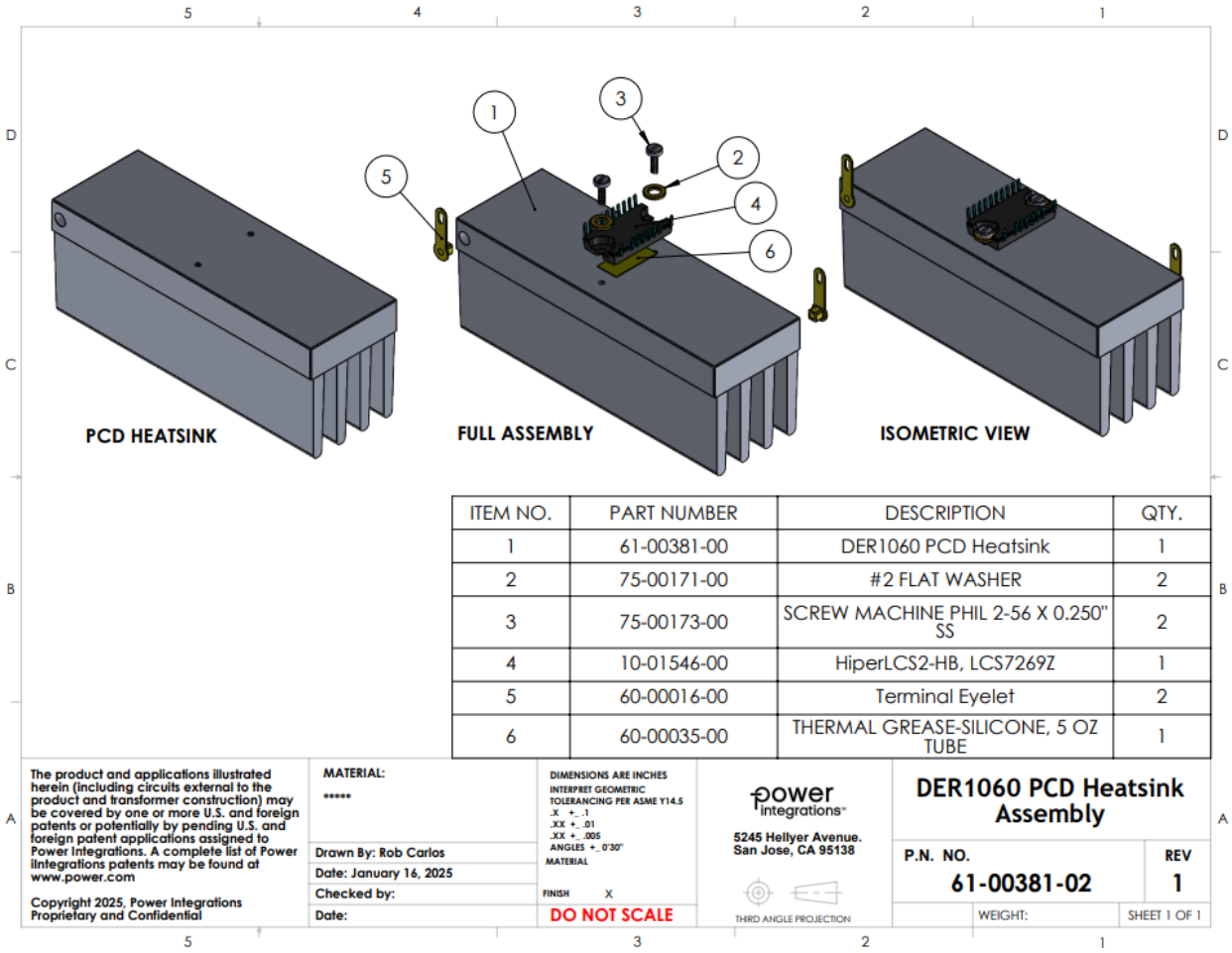


Figure 9 – Primary Device Heatsink Drawing.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00381-00	DER1060 PCD Heatsink	1
2	75-00171-00	#2 FLAT WASHER	2
3	75-00173-00	SCREW MACHINE PHIL 2-56 X 0.250" SS	2
4	10-01546-00	HiperLCS2-HB, LCS7269Z	1
5	60-00016-00	Terminal Eyelet	2
6	60-00035-00	THERMAL GREASE-SILICONE, 5 OZ TUBE	1

The product and applications illustrated herein (including circuits external to the product and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com

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MATERIAL: *****

Drawn By: Rob Carlos
Date: January 16, 2025
Checked by:
Date:

DIMENSIONS ARE INCHES
INTERPRET GEOMETRIC TOLERANCING PER ASME Y14.5
.X +_.1
.XX +_.01
.XX +_.005
ANGLES +_0°30"
MATERIAL
FINISH X
DO NOT SCALE

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138
THIRD ANGLE PROJECTION

DER1060 PCD Heatsink Assembly

P.N. NO. 61-00381-02 REV 1
WEIGHT: SHEET 1 OF 1

Figure 10 – Primary Device Heatsink Assembly Drawing.

9.2 Synchronous Rectifier Heatsink

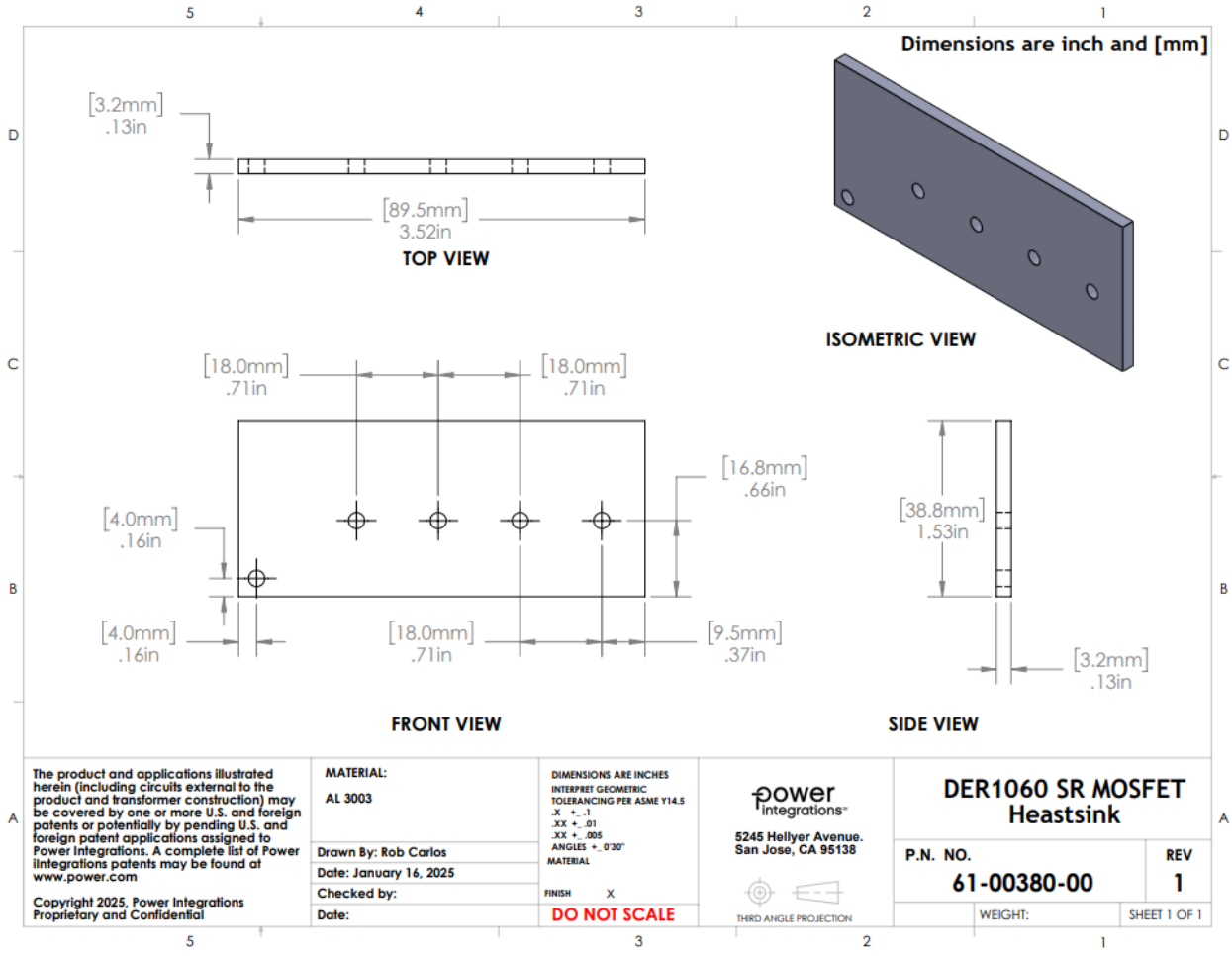
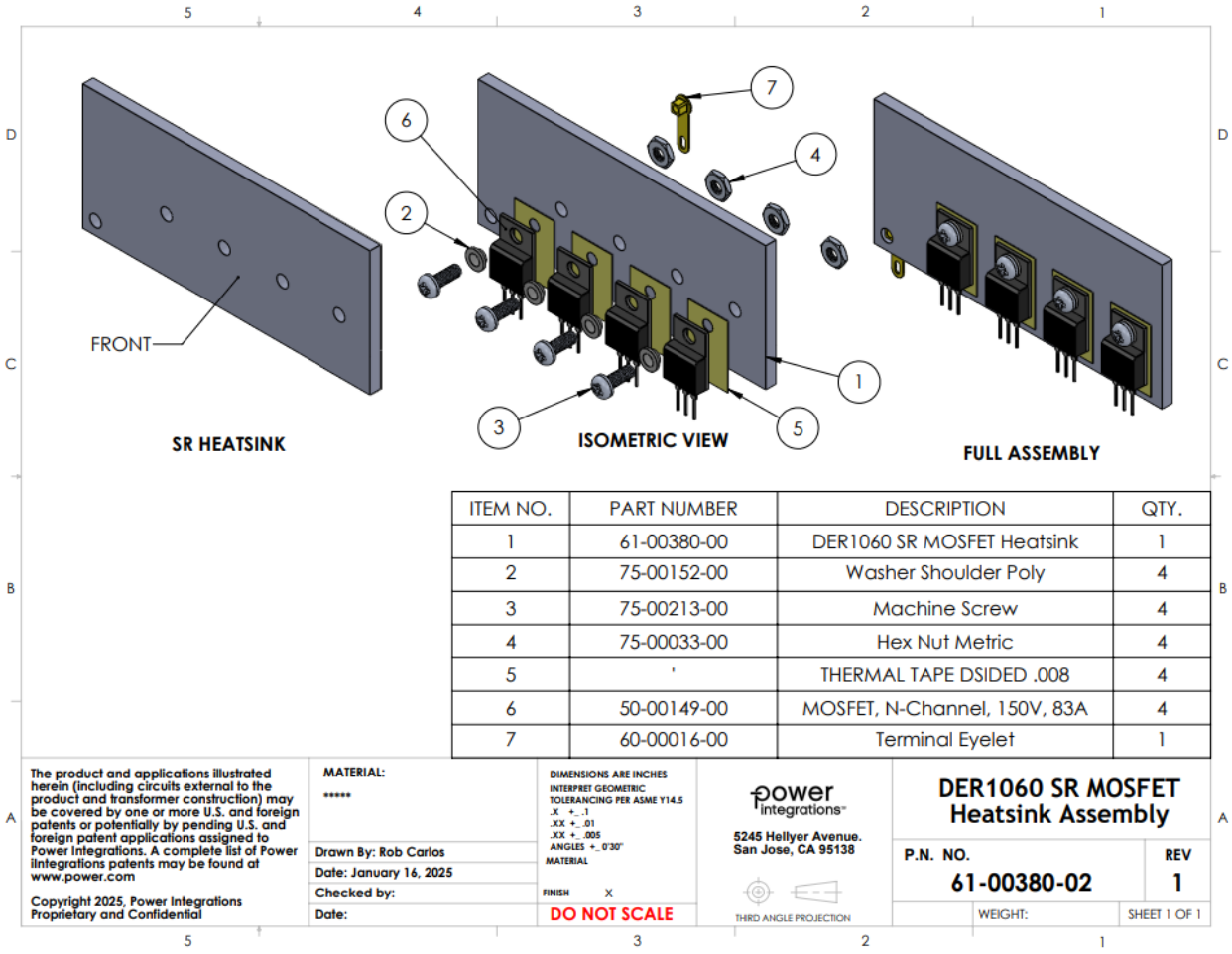


Figure 11 – SR MOSFET Heatsink Drawing.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	61-00380-00	DER1060 SR MOSFET Heatsink	1
2	75-00152-00	Washer Shoulder Poly	4
3	75-00213-00	Machine Screw	4
4	75-00033-00	Hex Nut Metric	4
5	'	THERMAL TAPE DSIDED .008	4
6	50-00149-00	MOSFET, N-Channel, 150V, 83A	4
7	60-00016-00	Terminal Eyelet	1

MATERIAL: *****

Drawn By: Rob Carlos
Date: January 16, 2025
Checked by:
Date:

DIMENSIONS ARE INCHES
INTERPRET GEOMETRIC TOLERANCING PER ASME Y14.5
.X +_.1
.XX +_.01
.XX +_.005
ANGLES +_ 0°30"
MATERIAL
FINISH X
DO NOT SCALE

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138
THIRD ANGLE PROJECTION

DER1060 SR MOSFET Heatsink Assembly

P.N. NO. 61-00380-02
REV 1
WEIGHT:
SHEET 1 OF 1

Figure 12 – SR MOSFET Heatsink Assembly Drawing.

10 Performance Data

In this section, the power supply's performance under different line and load conditions is described. Tests include DC-DC efficiency, no load input power, line and load regulation, operating waveforms, and thermal measurements. The set-up and test conditions are described for each section.

10.1 Efficiency

DC-DC efficiency of the unit is shown in Figure 13. The efficiency was tested for three different line conditions. A high-power DC source was used to supply the DC input and a DC electronic load set to CCH mode was used for output.

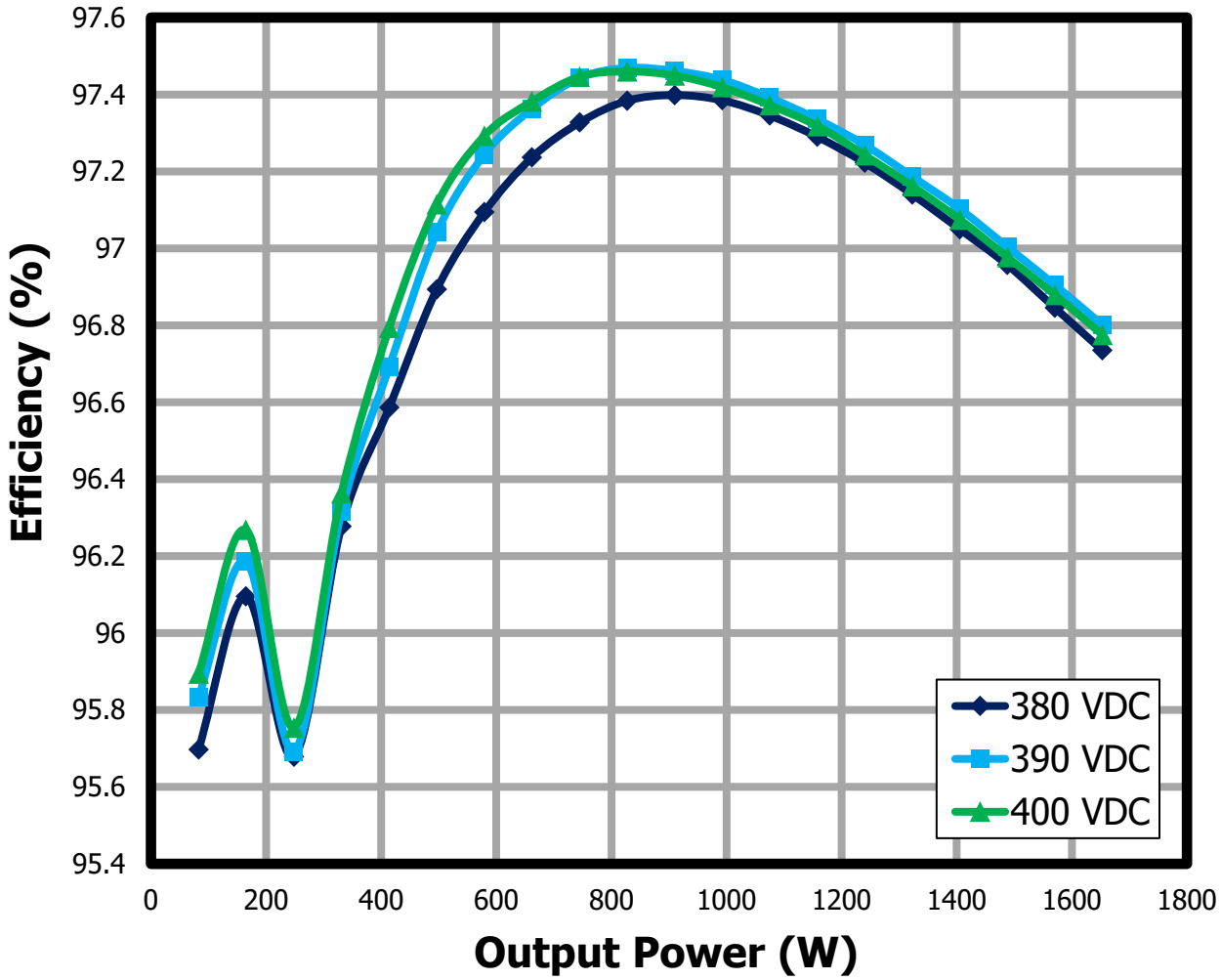


Figure 13 – Total Efficiency vs. Load, Output Power.

Table 1 – Efficiency Data

Input	Load (%)	V_{IN} (V)	I_{IN} (A)	P_{IN} (kW)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (kW)	Efficiency (%)
380 VDC	100	380	4.50	1.71	60.1	27.5	1.65	96.7
	95.0	380	4.27	1.62	60.1	26.1	1.57	96.8
	90.0	380	4.04	1.53	60.2	24.7	1.49	97.0
	85.0	380	3.81	1.45	60.2	23.4	1.41	97.0
	80.0	380	3.58	1.36	60.2	22.0	1.32	97.1
	75.0	380	3.36	1.28	60.2	20.6	1.24	97.2
	70.0	380	3.13	1.19	60.2	19.2	1.16	97.3
	65.0	380	2.91	1.10	60.2	17.9	1.08	97.3
	60.0	380	2.68	1.02	60.2	16.5	0.993	97.4
	55.0	380	2.46	0.934	60.2	15.1	0.910	97.4
	50.0	380	2.24	0.850	60.2	13.7	0.827	97.4
	45.0	380	2.01	0.765	60.2	12.4	0.745	97.3
	40.0	380	1.79	0.681	60.2	11.0	0.662	97.2
	35.0	380	1.57	0.597	60.2	9.62	0.579	97.1
	30.0	380	1.35	0.512	60.2	8.25	0.497	96.9
	25.0	380	1.13	0.428	60.2	6.87	0.414	96.6
	20.0	380	0.905	0.344	60.2	5.50	0.331	96.3
	15.0	380	0.683	0.260	60.2	4.13	0.248	95.7
	10.0	380	0.452	0.172	60.0	2.75	0.165	96.1
	5.00	380	0.227	0.086	60.0	1.38	0.083	95.7

Input	Load (%)	V_{IN} (V)	I_{IN} (A)	P_{IN} (kW)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (kW)	Efficiency (%)
390 VDC	100	390	4.38	1.71	60.1	27.5	1.65	96.8
	95.0	390	4.16	1.62	60.2	26.1	1.57	96.9
	90.0	390	3.93	1.54	60.2	24.7	1.49	97.0
	85.0	390	3.71	1.45	60.2	23.4	1.41	97.1
	80.0	390	3.49	1.36	60.2	22.0	1.32	97.2
	75.0	390	3.27	1.28	60.2	20.6	1.24	97.3
	70.0	390	3.05	1.19	60.2	19.2	1.16	97.3
	65.0	390	2.83	1.10	60.2	17.9	1.08	97.4
	60.0	390	2.61	1.02	60.2	16.5	0.993	97.4
	55.0	390	2.39	0.933	60.2	15.1	0.910	97.5
	50.0	390	2.18	0.848	60.2	13.7	0.827	97.5
	45.0	390	1.96	0.763	60.2	12.4	0.745	97.4
	40.0	390	1.74	0.679	60.2	11.0	0.662	97.4
	35.0	390	1.53	0.594	60.2	9.62	0.579	97.2
	30.0	390	1.31	0.511	60.2	8.25	0.497	97.0
	25.0	390	1.10	0.426	60.2	6.87	0.414	96.7
	20.0	390	0.881	0.342	60.2	5.50	0.331	96.3
	15.0	390	0.665	0.258	60.2	4.13	0.248	95.7
	10.0	390	0.440	0.171	60.0	2.75	0.165	96.2
	5.00	390	0.221	0.086	60.0	1.38	0.083	95.8

Input	Load (%)	V_{IN} (V)	I_{IN} (A)	P_{IN} (kW)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (kW)	Efficiency (%)
400 VDC	100	400	4.27	1.71	60.2	27.5	1.65	96.8
	95.0	400	4.05	1.62	60.2	26.1	1.57	96.9
	90.0	400	3.84	1.54	60.2	24.7	1.49	97.0
	85.0	400	3.62	1.45	60.2	23.4	1.41	97.1
	80.0	400	3.40	1.36	60.2	22.0	1.32	97.2
	75.0	400	3.19	1.28	60.2	20.6	1.24	97.2
	70.0	400	2.97	1.19	60.2	19.2	1.16	97.3
	65.0	400	2.76	1.10	60.2	17.9	1.08	97.4
	60.0	400	2.55	1.02	60.2	16.5	0.993	97.4
	55.0	400	2.33	0.933	60.2	15.1	0.910	97.4
	50.0	400	2.12	0.848	60.2	13.7	0.827	97.5
	45.0	400	1.91	0.763	60.2	12.4	0.745	97.4
	40.0	400	1.70	0.679	60.2	11.0	0.662	97.4
	35.0	400	1.49	0.594	60.2	9.62	0.579	97.3
	30.0	400	1.28	0.511	60.2	8.25	0.497	97.1
	25.0	400	1.07	0.426	60.2	6.87	0.414	96.8
	20.0	400	0.859	0.342	60.2	5.50	0.331	96.4
	15.0	400	0.648	0.258	60.2	4.13	0.248	95.8
	10.0	400	0.429	0.171	60.0	2.75	0.165	96.3
	5.00	400	0.215	0.086	60.0	1.38	0.083	95.9

10.2 No-Load Input Power

No-load input power was measured with only the DC source connected to the input. The unit under test (UUT) was turned on and allowed to stabilize for 5 minutes then measured with an integration time of 15 minutes.

Note: To more accurately determine the no-load input power, no output connections were attached to the UUT.

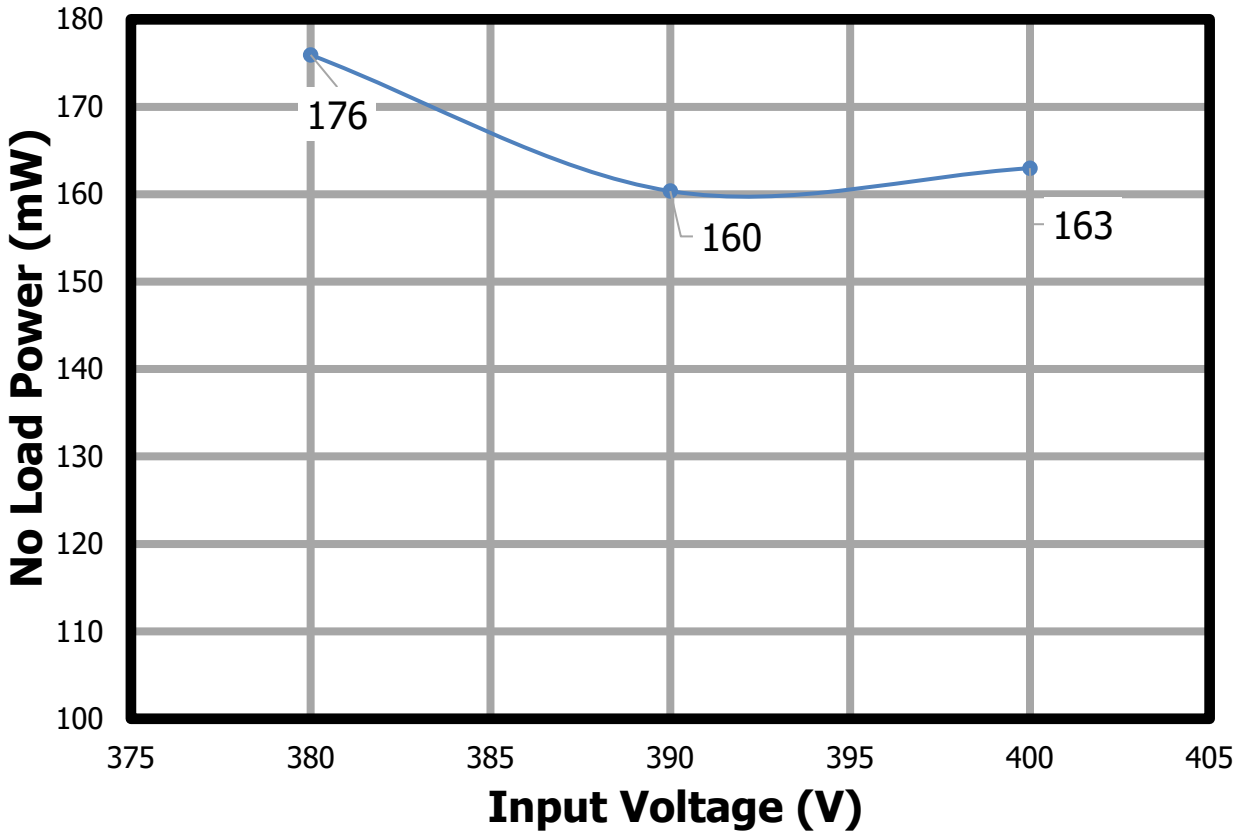


Figure 14 – No-Load Input Power vs. Input Voltage.

Table 2 – No Load Input Power

V_{IN} (V)	P_{no_load} (mW)
380	176
390	160
400	163

10.3 Line Regulation

Line regulation describes the relationship between the DC input voltages and the output voltage. The output regulation was monitored from 380 VDC to 400 VDC at full load, half load, and no-load conditions.

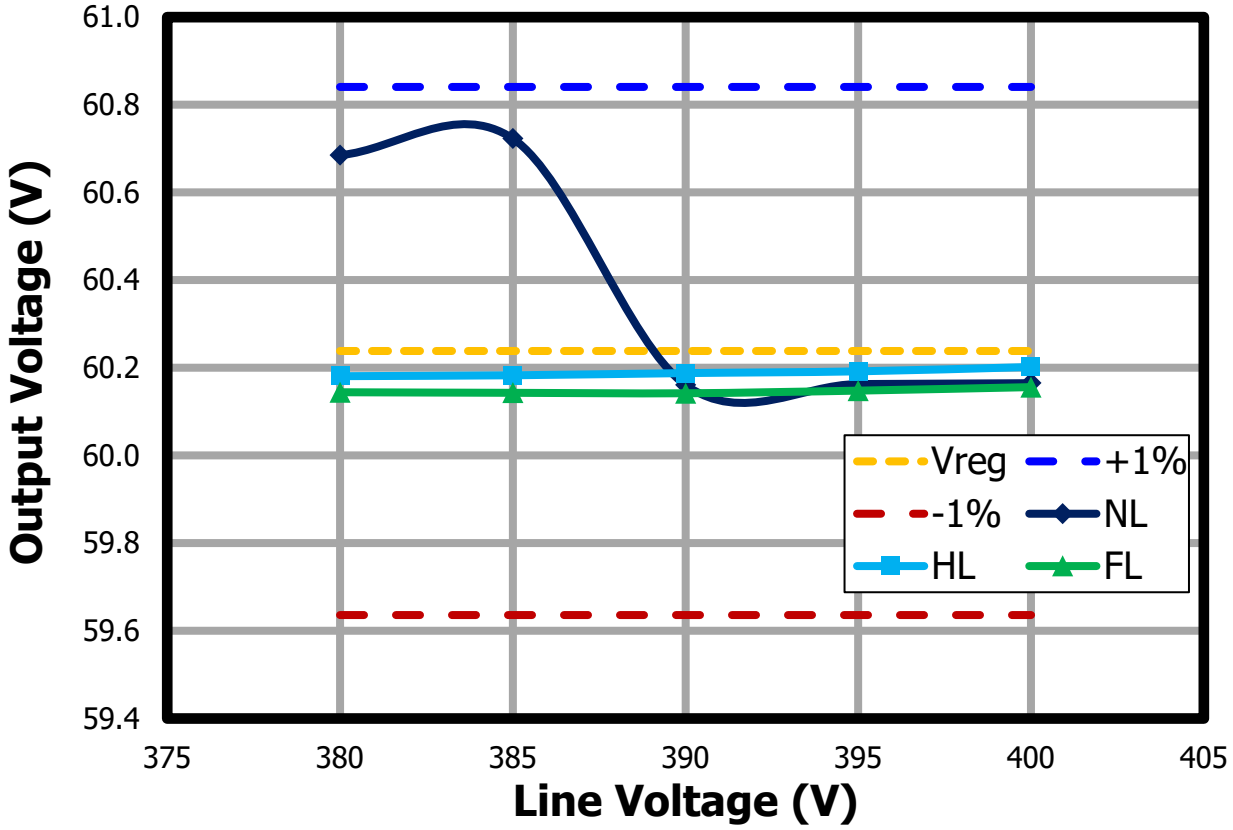


Figure 15 – Line Regulation.

Table 3 – Line Regulation

V_{IN}	NL	HL	FL	Vreg	+1%	-1%
380	60.7	60.2	60.1	60.2	60.8	59.6
385	60.7	60.2	60.1	60.2	60.8	59.6
390	60.2	60.2	60.1	60.2	60.8	59.6
395	60.2	60.2	60.1	60.2	60.8	59.6
400	60.2	60.2	60.2	60.2	60.8	59.6

10.4 Load Regulation

The graph describes output power against output voltage. Output voltage was measured between 0 - 100% for three different DC line voltages.

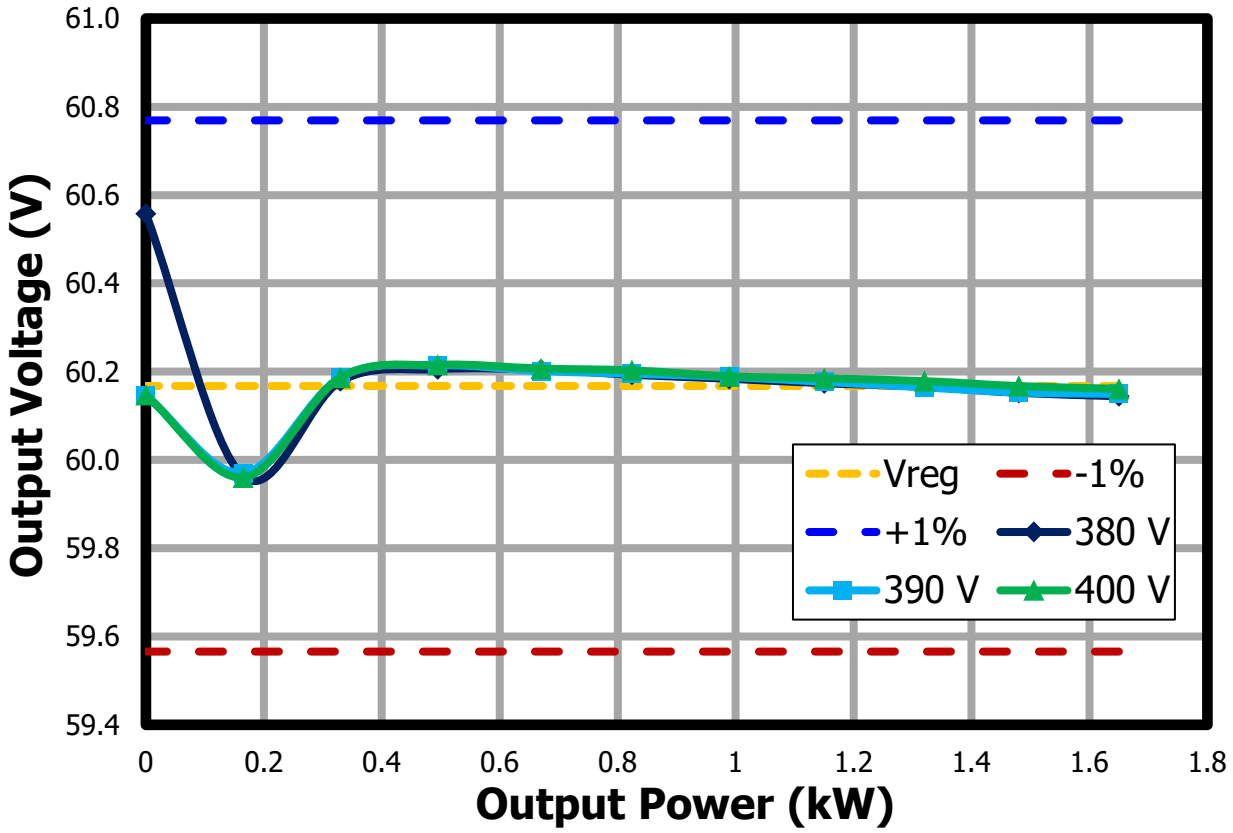


Figure 16 – Load Regulation.

Table 4 – Load Regulation

P_{OUT} (kW)	V_{IN}			+1%	-1%	Vreg
	380 V	390 V	400 V			
1.65	60.1	60.1	60.2	60.8	59.6	60.2
1.48	60.2	60.2	60.2	60.8	59.6	60.2
1.32	60.2	60.2	60.2	60.8	59.6	60.2
1.15	60.2	60.2	60.2	60.8	59.6	60.2
0.989	60.2	60.2	60.2	60.8	59.6	60.2
0.824	60.2	60.2	60.2	60.8	59.6	60.2
0.670	60.2	60.2	60.2	60.8	59.6	60.2
0.495	60.2	60.2	60.2	60.8	59.6	60.2
0.330	60.2	60.2	60.2	60.8	59.6	60.2
0.165	60.0	60.0	60.0	60.8	59.6	60.2
0.000	60.6	60.1	60.1	60.8	59.6	60.2

11 Waveforms

Waveforms were recorded for different DC input voltage and output loading conditions set for the UUT.

11.1 LLC Primary Voltage and Current

The figures below show the primary voltage and current waveforms with the UUT operating from 400 VDC. The load used was an electronic load set at CCH mode. Waveforms were recorded at full load, half load, and no load.

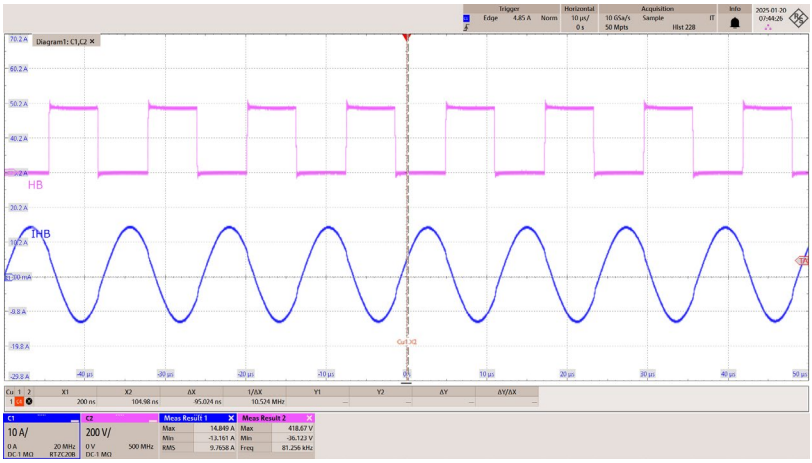


Figure 17 – LLC Stage Primary Voltage and Current, 100% Load.
Time Division: 10 μs / div.
Frequency: 81.3 kHz
HB Current (RMS): 9.77 A
CH1: HB Current, 10 A / div.
CH2: HB Voltage, 200 V / div.

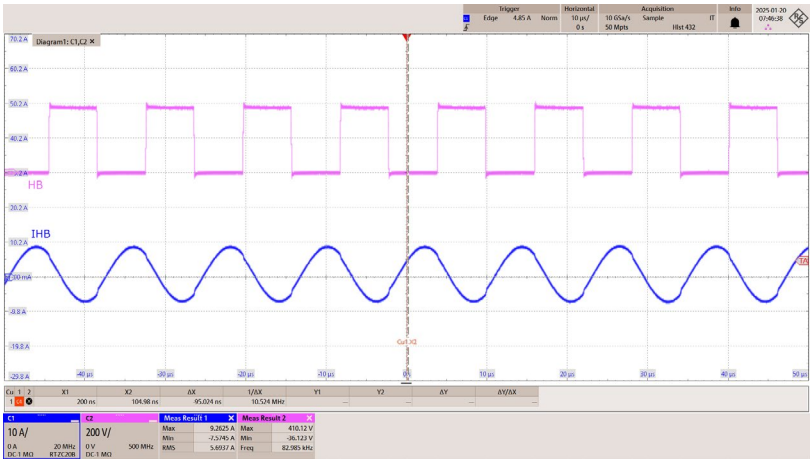


Figure 18 – LLC Stage Primary Voltage and Current, 50% Load.
Time Division: 10 μs / div.
Frequency: 83.0 kHz
HB Current (RMS): 5.69 A
CH1: HB Current, 10 A / div.
CH2: HB Voltage, 200 V / div.

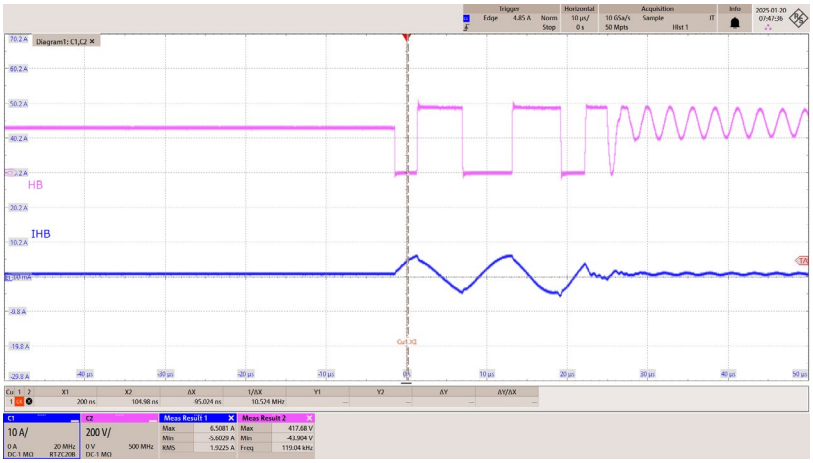


Figure 19 – LLC Stage Primary Voltage and Current, No-Load.
Time Division: 10 μs / div.
CH1: HB Current, 4 A / div.
CH2: HB Voltage, 100 V / div.

11.2 SR Waveforms

11.2.1 Drain-Source Voltage

Drain-source voltage waveforms across the synchronous rectifiers Q3/Q4 and Q6/Q7 were measured with input voltage of 400 VDC, at full load.

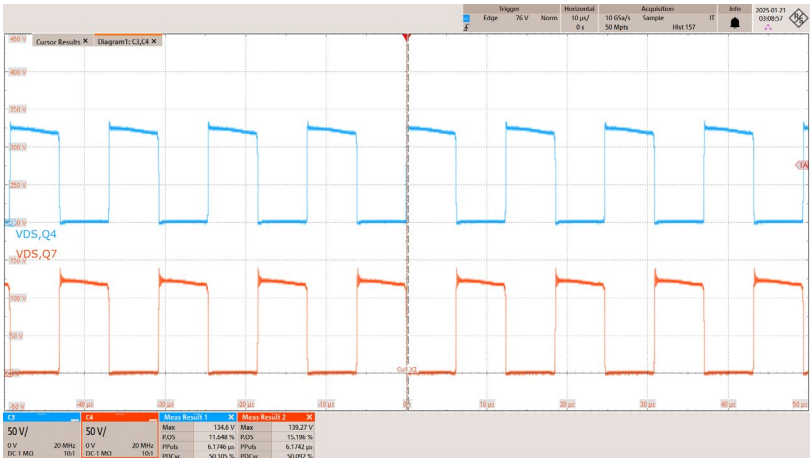


Figure 20 – Output Synchronous Rectifier Peak Reverse Voltage. 400 VDC, Full Load.
Time Division: 10 µs / div.
CH3: $Q_{3,}Q_4$ V_{DS}, 50 V / div.
CH4: Q_6,Q_7 V_{DS}, 50 V / div.

11.2.2 Gate-Source Voltage

SR Gate drive was measured from the gate to source pins of the SR MOSFETs Q3/Q4 and Q6/Q7.

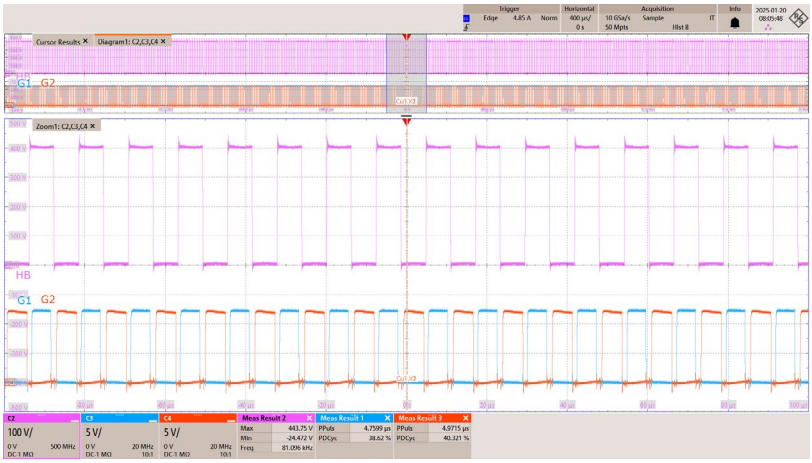


Figure 21 – Synchronous Rectifier Gate Drive. 400 VDC, Full Load.
Time Division: 400 µs / div.
Zoom Time Division: 20 µs / div.
CH2: HB, 100 V / div.
CH3: $Q_{3,}Q_4$ V_{GS}, 5 V / div.
Ch4: Q_6,Q_7 V_{GS}, 5 V / div.

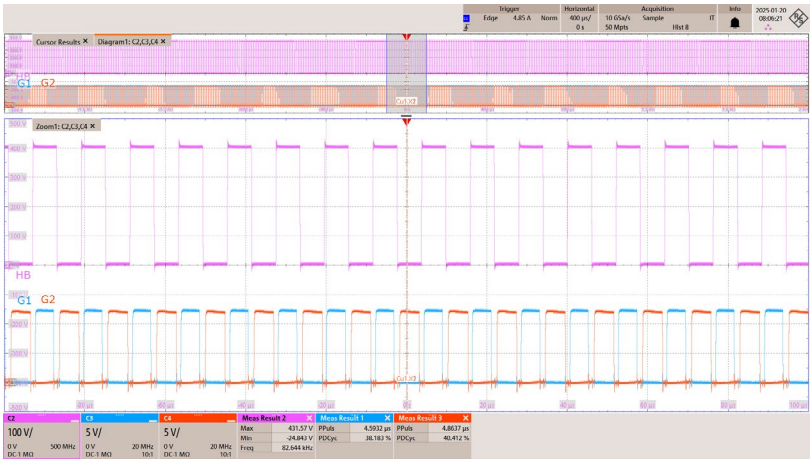


Figure 22 – Synchronous Rectifier Gate Drive. 400 VDC, Half Load.
Time Division: 400 µs / div.
Zoom Time Division: 20 µs / div.
CH2: HB, 100 V / div.
CH3: Q_3,Q_4 V_{GS}, 5 V / div.
Ch4: Q_6,Q_7 V_{GS}, 5 V / div.

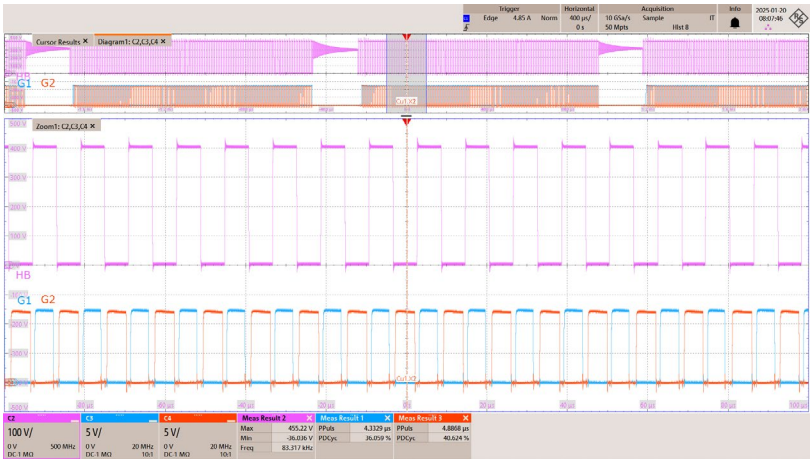


Figure 23 – Synchronous Rectifier Gate Drive. 400 VDC, 20% (5.5 A) Load.
Time Division: 400 µs / div.
Zoom Time Division: 20 µs / div.
CH2: HB, 100 V / div.
CH3: Q_3,Q_4 V_{GS}, 5 V / div.
Ch4: Q_6,Q_7 V_{GS}, 5 V / div.

11.3 Start Up Waveforms

Startup waveforms were captured with a DC input voltage adjusted between 380 VDC and 400 VDC. Loads were set to no load and full load for each input voltages.

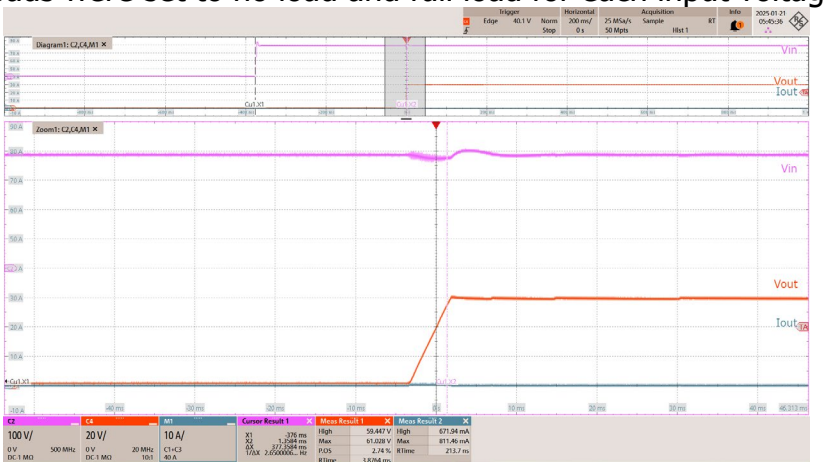


Figure 24 – Output Voltage at Start Up. 380 VDC, No Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 377 ms.
V_{OUT} Rise Time: 3.88 ms.
M1: I_{OUT}, 10 A / div.
CH2: V_{BULK}, 100 V / div.
Ch4: V_{OUT}, 20 V / div.

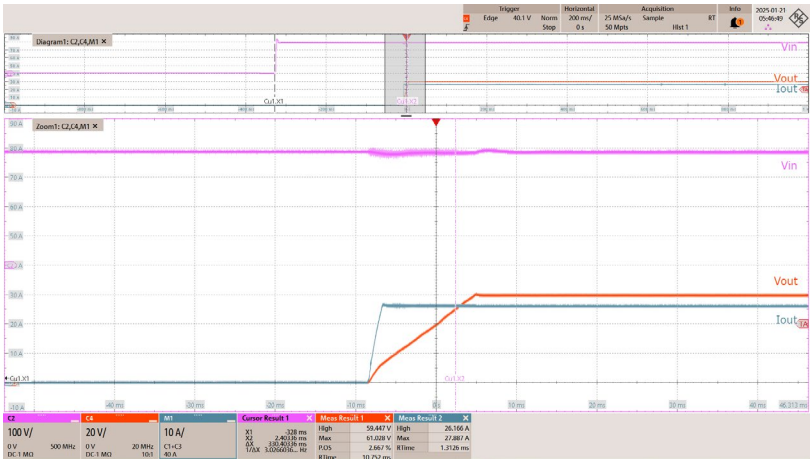


Figure 25 – Output Voltage at Start Up. 380 VDC, Full Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 330 ms.
V_{OUT} Rise Time: 10.8 ms.
M1: I_{OUT}, 10 A / div.
CH2: V_{BULK}, 100 V / div.
Ch4: V_{OUT}, 20 V / div.

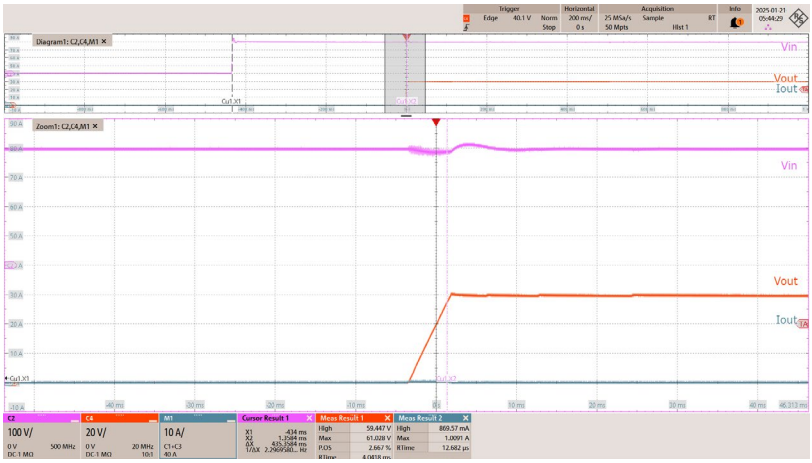


Figure 26 – Output Voltage at Start Up. 390 VDC, No Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 435 ms.
V_{OUT} Rise Time: 4.04 ms.
M1: I_{OUT}, 10 A / div.
CH2: V_{BULK}, 100 V / div.
Ch4: V_{OUT}, 20 V / div.

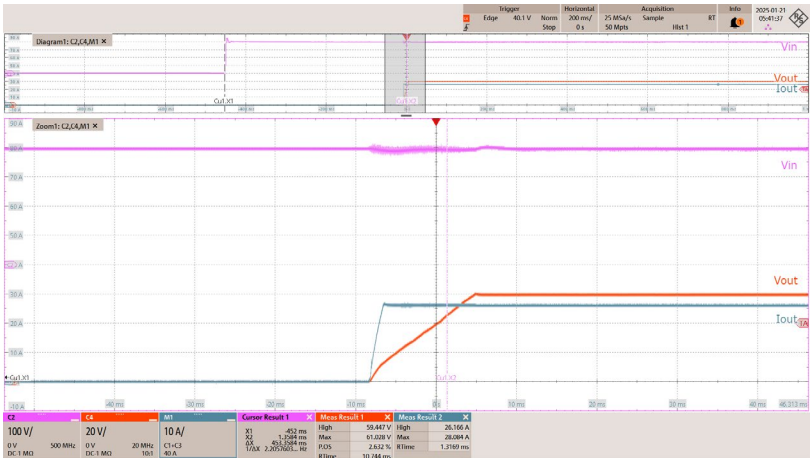


Figure 27 – Output Voltage at Start Up. 390 VDC, Full Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 453 ms.
V_{OUT} Rise Time: 10.7 ms.
M1: I_{OUT}, 10 A / div.
CH2: V_{BULK}, 100 V / div.
Ch4: V_{OUT}, 20 V / div.

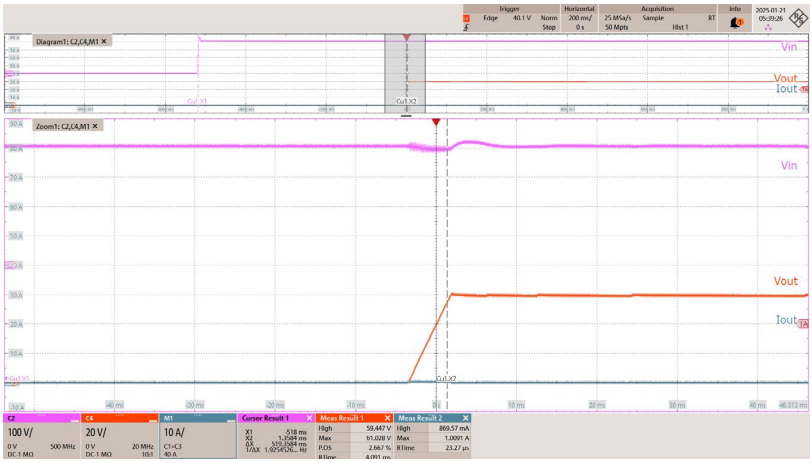


Figure 28 – Output Voltage at Start Up. 400 VDC, No Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 519 ms.
V_{OUT} Rise Time: 4.09 ms.
M1: I_{OUT}, 10 A / div.
CH2: V_{BULK}, 100 V / div.
Ch4: V_{OUT}, 20 V / div.

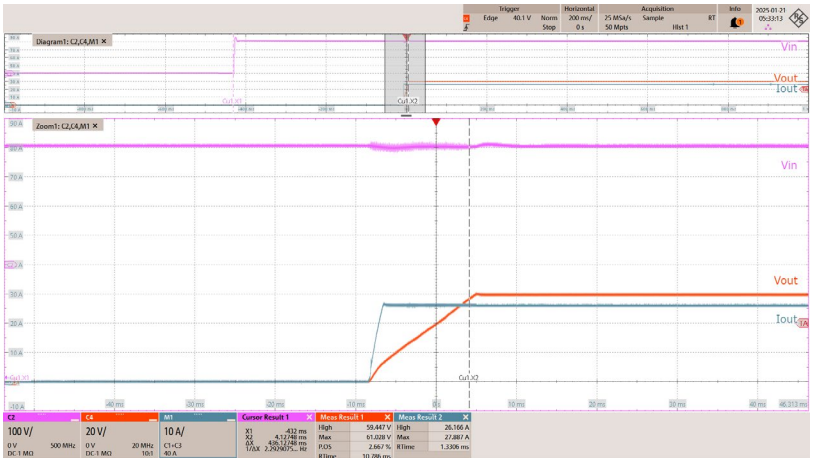


Figure 29 – Output Voltage at Start Up. 400 VDC, Full Load.
Time Division: 200 ms / div.
Zoom Time Division: 2 ms / div.
Regulation Time: 436 ms.
V_{OUT} Rise Time: 10.8 ms.
M1: I_{OUT}, 10 A / div.
CH2: V_{BULK}, 100 V / div.
Ch4: V_{OUT}, 20 V / div.

11.4 Burst Operation Waveforms

Operation during different burst modes is shown below. For this configuration, the PS resistor R18 is set to 75 kΩ.

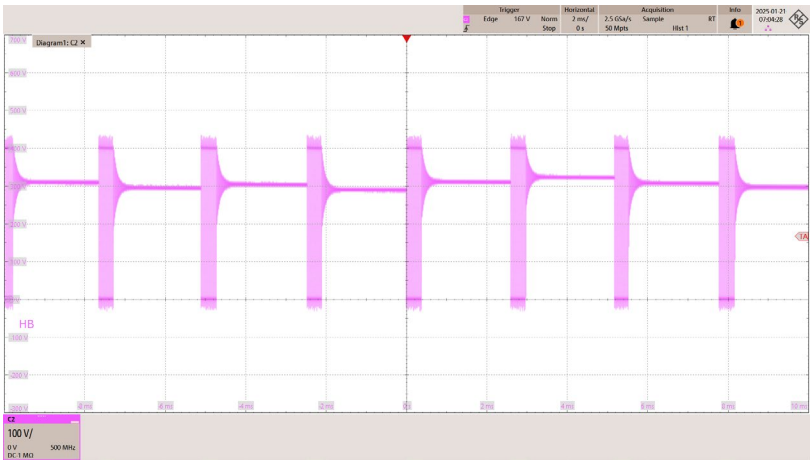


Figure 30 – Burst Profile at 0.95 A. 400 VDC.
Time Division: 2 ms / div.
CH2: V_{HB}, 100 V / div.

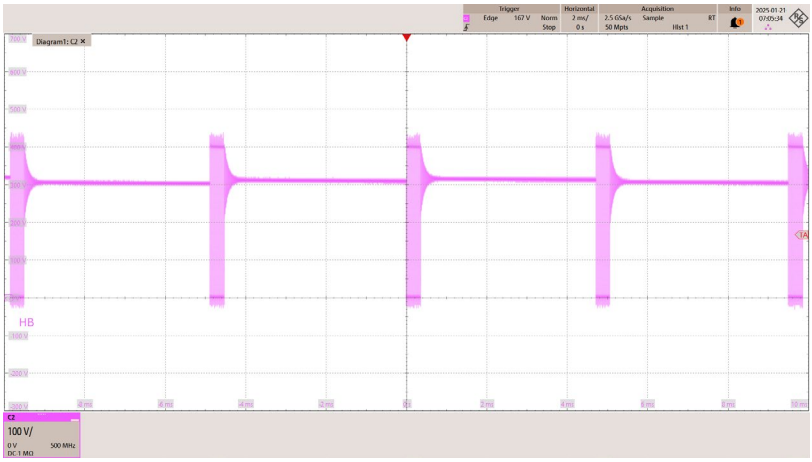


Figure 31 – Burst Profile at 0.5 A. 400 VDC.
Time Division: 2 ms / div.
CH2: V_{HB}, 100 V / div.

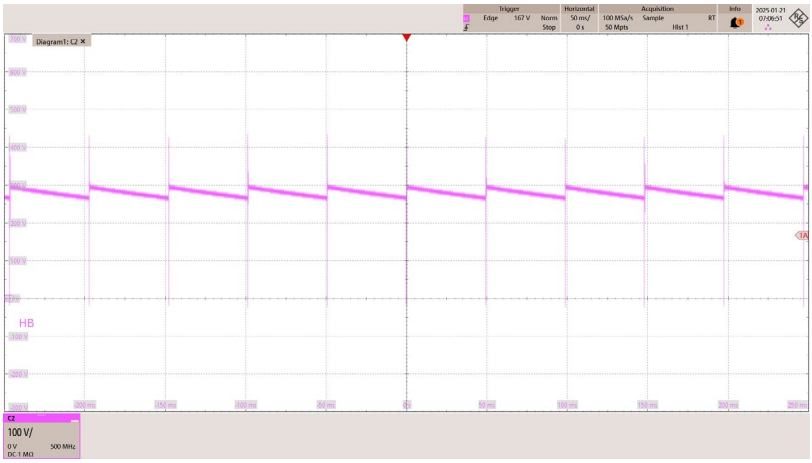


Figure 32 – Burst Profile at No Load. 400 VDC.
Time Division: 50 ms / div.
CH2: V_{HB}, 100 V / div.

11.5 Dynamic Loading

The figures below show the transient response of the UUT and demonstrate the very small change in the output voltage with a 0 – 100% – 0 step load change. Recovery time for the output was approximately 300 µs.

Electronic Load setting is as follows:
Duty Cycle = 50%, Frequency = 50 Hz, Slew Rate = 800 mA/µs.

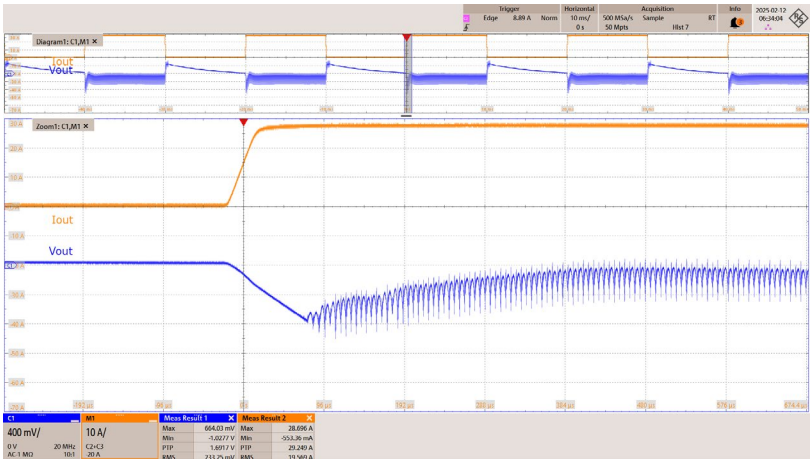


Figure 33 – Dynamic Loading. 400 VDC, 0 - 100% Load.
Time Division: 10 ms / div.
Zoom Time Division: 100 µs / div.
M1: I_{OUT}, 10 A / div.
CH1: V_{OUT}, 400 mV / div.

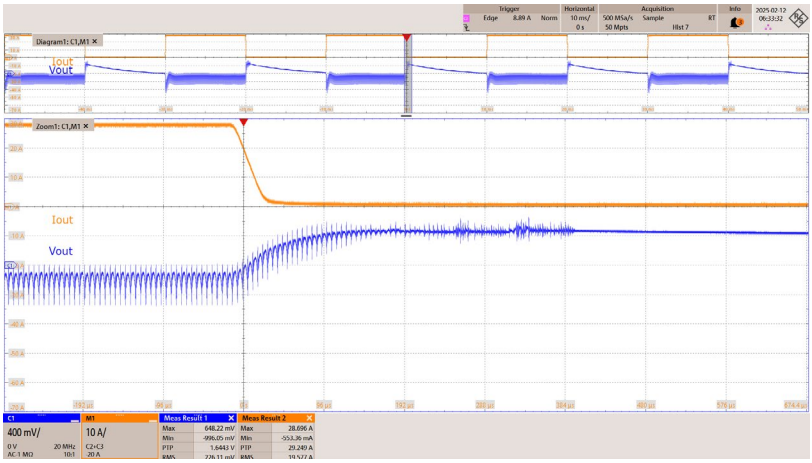


Figure 34 – Dynamic Loading. 400 VDC, 100 - 0% Load.
Time Division: 10 ms / div.
Zoom Time Division: 100 μs/ div.
M1: I_{OUT}, 10 A / div.
CH1: V_{OUT}, 400 mV / div.

Note: During no-load burst mode was triggered which increased the output variation when compared to loaded conditions.

12 Output Ripple Measurements

12.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe was used to reduce interference. Details of the probe modification are provided below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. A 0.1 μF / 100 V ceramic capacitor and 47 μF / 80 V aluminum electrolytic capacitor were used. The aluminum electrolytic capacitor is polarized, so always check for correct polarity between DC outputs.

Figure 35 – Oscilloscope Probe Prepared for Ripple Measurement (Probe cover and Ground Lead Removed).

Figure 36 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

12.2 Ripple Measurements

Output voltage ripple was measured at 400 VDC input voltage under different load conditions.

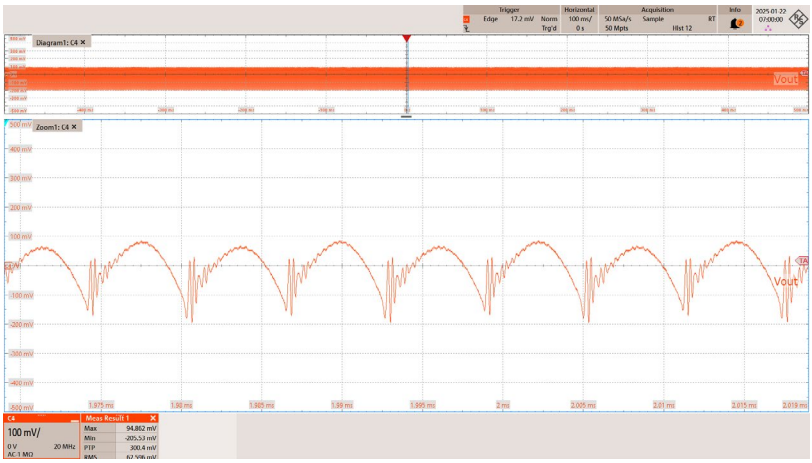


Figure 37 – Output Voltage Ripple. 400 VDC, Full Load.
Time Division: 100 ms / div.
Zoom Time Division: 5 μs / div.
Ripple: 0.501%
CH4: V_{OUT}, 100 mV / div.

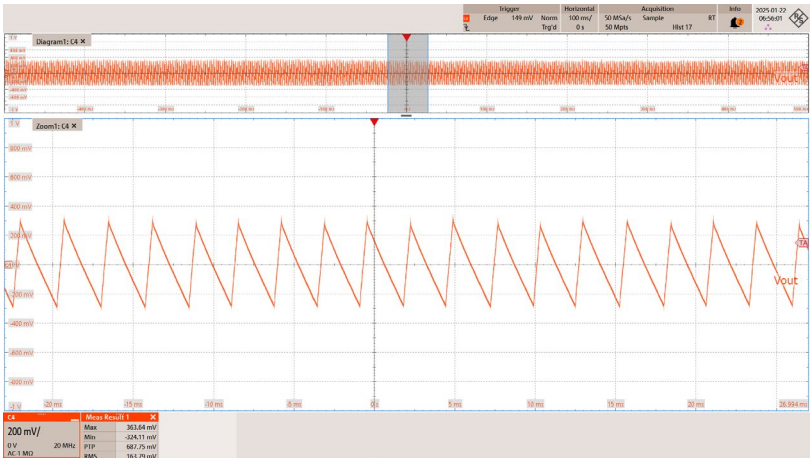


Figure 38 – Output Voltage Ripple. 400 VDC, 1 A Load.
Time Division: 100 ms / div.
Zoom Time Division: 5 ms / div.
Ripple: 1.15%
CH4: V_{OUT}, 200 mV / div.

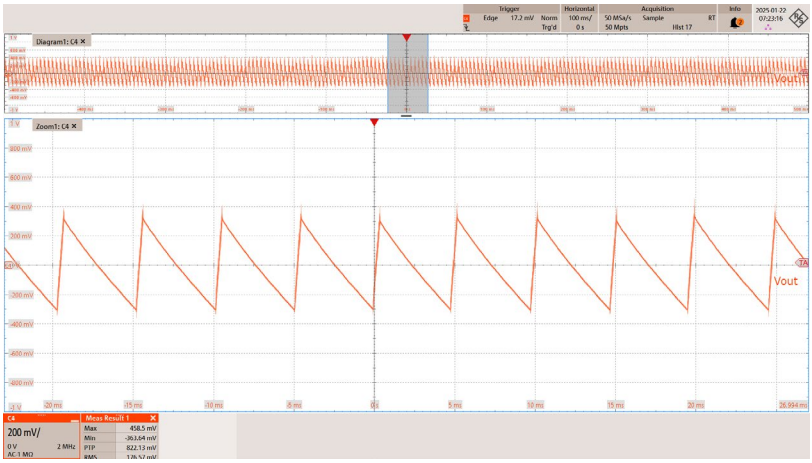


Figure 39 – Output Voltage Ripple. 400 VDC, 0.5 A Load.
Time Division: 100 ms / div.
Zoom Time Division: 5 ms / div.
Ripple: 1.37%
CH4: V_{OUT}, 200 mV / div.

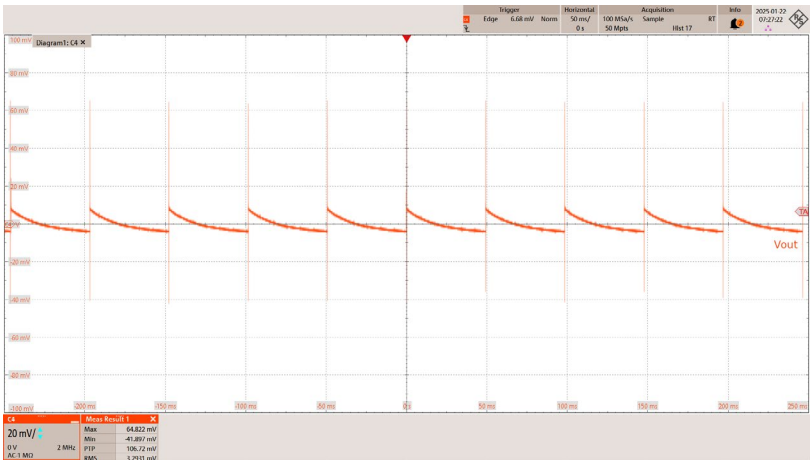


Figure 40 – Output Voltage Ripple. 400 VDC, No-Load.
Time Division: 50 ms / div.
Ripple: 0.178%
CH4: V_{OUT}, 20 mV / div.

13 Temperature Profiles

The UUT was powered up with an input voltage of 400 VDC and electronic load set to CCH at full load, 27.5 A (1.65 kW). The unit was tested open case under room temperature and cooled by a 220 V / 0.11 A fan. The fan was placed 15 cm to the side of the UUT.

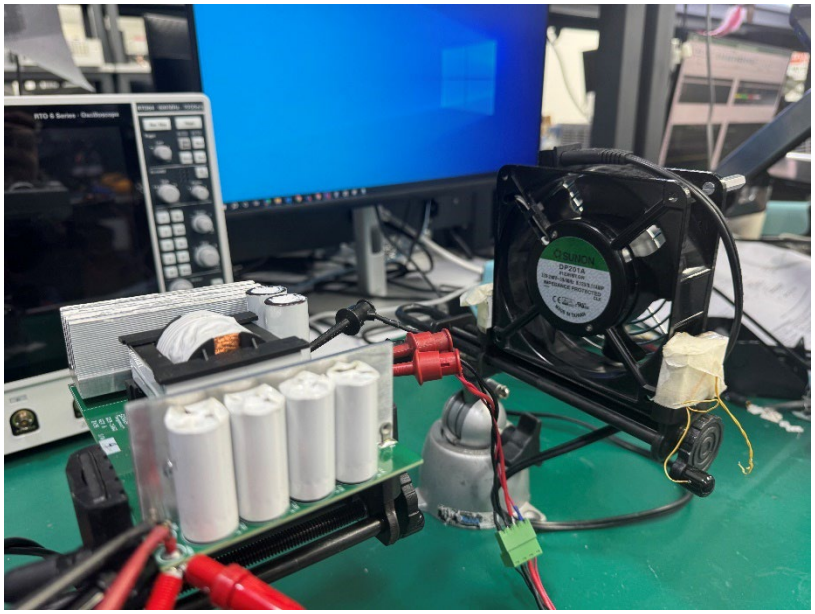
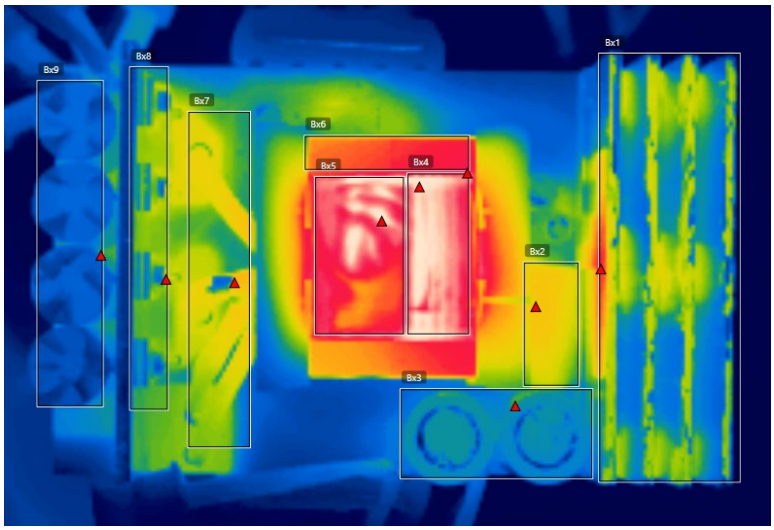


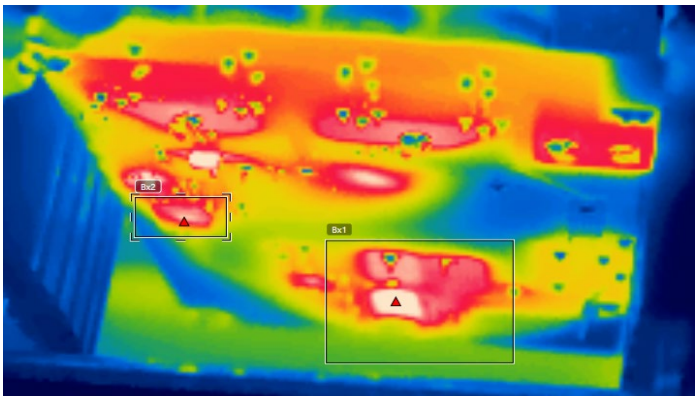
Figure 41 – Thermal Set-up with External Fan



Measurements		
Bx1	Max	71.8 °C
Bx2	Max	56.2 °C
Bx3	Max	42.1 °C
Bx4	Max	99.7 °C
Bx5	Max	105.5 °C
Bx6	Max	75.5 °C
Bx7	Max	58.6 °C
Bx8	Max	52.2 °C
Bx9	Max	39.7 °C

Legend	Ref Des	Description	Temperature (ºC)
Bx1	Heatsink	PCD Heatsink	71.8
Bx2	C10	Resonant Capacitor	56.2
Bx3	C1, C7	Bulk Capacitors	42.1
Bx4	TRF	TRF Primary Winding	99.7
Bx5	TRF	TRF Secondary Winding	106
Bx6	TRF	TRF Core	75.5
Bx7	TRF	TRF Secondary Fly Leads	58.6
Bx8	Q1,Q3	SR FET/ SR Assembly	52.2
Bx9	C16, C19, C20, C33	Output Capacitors	39.7

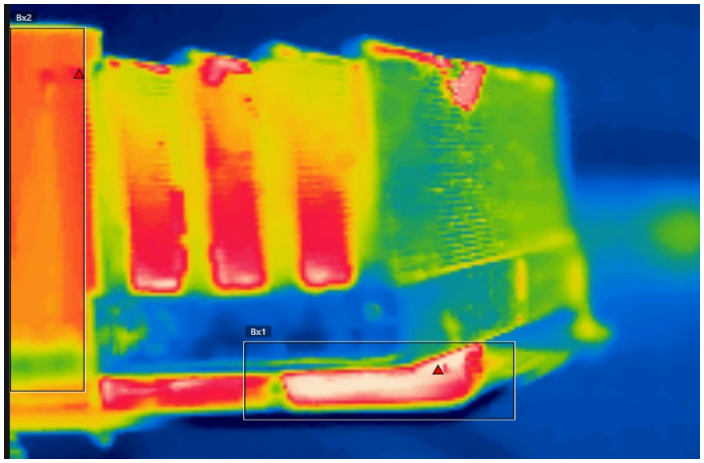
Figure 42 – Thermal Reading Top, 100% Load, 400 VDC.



Measurements		
Bx1	Max	62.3 °C
Bx2	Max	47.3 °C

Legend	Ref Des	Description	Temperature (ºC)
Bx1	U1	Primary device (PCD)	62.3
Bx2	U2	Secondary device (SCD)	47.3

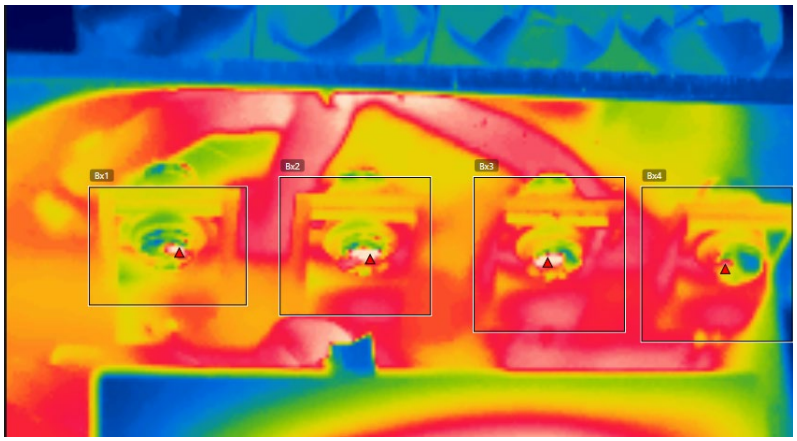
Figure 43 – Thermal Reading Bottom, 100% Load, 400 VDC.



Measurements		
Bx1	Max	50.4 °C
Bx2	Max	39.3 °C

Legend	Ref Des	Description	Temperature (ºC)
Bx1	U1	Primary device (PCD)	50.4
Bx2	C1	Bulk Cap	39.3

Figure 44 – Thermal Reading Side PCD, 100% Load, 400 VDC.



Measurements		
Bx1	Max	53.7 °C
Bx2	Max	58.7 °C
Bx3	Max	56.7 °C
Bx4	Max	46.7 °C

Legend	Ref Des	Description	Temperature (ºC)
Bx1	Q7	SR MOSFET	53.7
Bx2	Q6	SR MOSFET	58.7
Bx3	Q4	SR MOSFET	56.7
Bx4	Q3	SR MOSFET	46.7

Figure 45 – Thermal Reading SR MOSFETs, 100% Load, 400 VDC.

Table 5 – Summary of Thermal Readings

Component	Temperature (ºC)
Ambient Temperature	25.4
Primary device (PCD)	62.3
Secondary device (SCD)	47.3
Resonant Capacitors	56.2
Bulk Capacitor	42.1
TRF Core	75.5
TRF Primary Winding	99.7
TRF Secondary Winding	105.5
TRF Secondary Fly Leads	58.6
Output Capacitors	39.7
SR Assembly	52.2
Q6, Q7 SR FET	58.7
Q3, Q4 SR FET	56.7

14 Revision History

Date	Author	Revision	Description and Changes	Reviewed
25-Feb-2025	RAC	A	Initial Release	Apps & Mktg

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