Design Example Report

Title	**82 W Multi-Output Flyback with High Power Factor with Two CV and One CC Outputs Using InnoMux™2-EP IMX2270F**
Specification	Input: 180 VAC – 265 VAC Outputs: 5 V / 500 mA, 24 V / 2.4 A_{NOM} / 5.8 A_{PK}, 36 V / 600 mA
Application	Smart Clothes-Dryer Rack
Author	Applications Engineering Department
Document Number	DER-1050
Date	October 29, 2024
Revision	A

Summary and Features

- Unique single-stage conversion, multiple-output, flyback architecture
- High power factor, >0.9 at 230 VAC during light load (≤ 24.1 W)
- Low THD, <10% THD at 230 VAC
- >88% efficiency at 230 VAC at nominal load (82 W)
- High regulation accuracy - independently regulated, CV1: 5 V / 0.5 A, CV2: 24 V / 2.4 A_{NOM} - 5.8 A_{PK}, CC: 36 V / 600 mA
  - ±1% CV and ±5% CC accuracy across line and load
- CC (LED) output with 1-wire filtered PWM dimming input
- Safety features
  - Output overvoltage protection (OVP)
  - Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection

InnoMux2-EP provides accurate and efficient single stage conversion providing multiple independently regulated outputs.

Provisional Report
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The InnoMux2-EP IC incorporates safety-rated barrier crossing feedback and communication channels, combining all the benefits of secondary-side control with the simplicity of primary-side regulation.

The architecture achieves accurate line, load and cross regulation across multiple outputs while simplifying the overall system by removing the need for post-regulation. The single-stage converter improves efficiency, reduces board size significantly and part count compared to conventional multiple-stage topologies.

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This report describes a Switch Mode Power Supply (SMPS) designed for a Smart Clothes-Dryer Rack applications. The SMPS utilizes the InnoMux2-EP switcher IC from Power Integrations. The InnoMux-2 IC family employs a multiplexing output control algorithm. Energy is stored in the transformer during primary conduction and transferred to the outputs during the flyback (off period) cycle. The delivered energy is shared between the converter's outputs (CV1, CV2 or LED) according to their respective load requirements. This is achieved by controlling the SR FET, SEL1 and SEL2 (Figure 3) during each flyback period. The control technique utilizes a single magnetic component (transformer TX 2) where each output is driven from the single stacked secondary output winding. When the controller directs energy to the CV1 output, the SR FET and SEL1 are turned ON. Similarly, if the energy pulse needs to be delivered to the CV2 output, SR FET and SEL2 are turned ON. If SEL1 and SEL2 are OFF energy is delivered to the LED output via the rectification diode.

The design has two Constant Voltage (CV) outputs, 5 V / 0.5 A, 24 V / 2.4 A_{NOM} / 5.8 A_{PK} and one Constant Current (CC) output, capable of delivering maximum of 0.6 A into an LED string with a nominal voltage of 36 V. The current through the LED string is controlled from zero to maximum by a single-wire filtered PWM dimming signal (DIM1). The Power Supply can deliver a total maximum continuous power of 82 W and thermally limited peak power of 163.3 W, with high line mains input (from 180 VAC to 265 VAC).

Figure 1 – PCB, Top View.

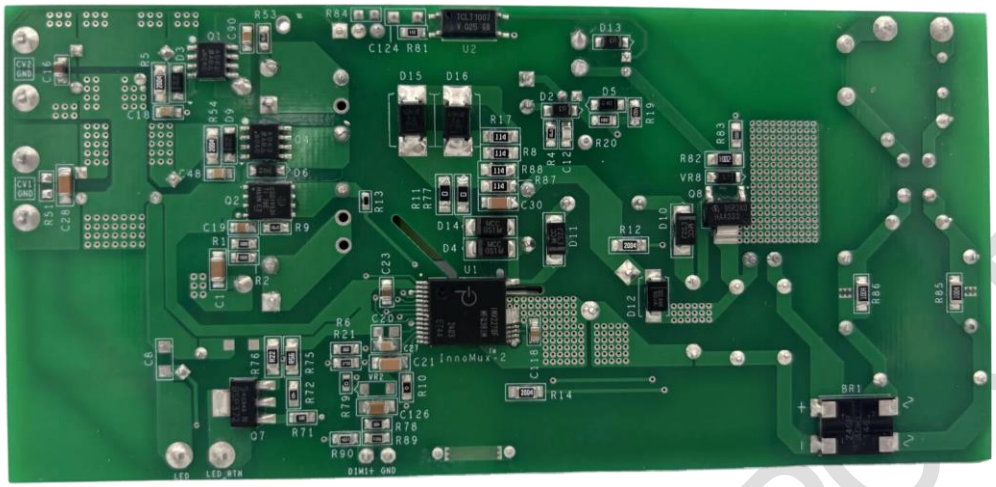


Figure 2 – PCB, Bottom View.

2 Output-stage Block Diagram

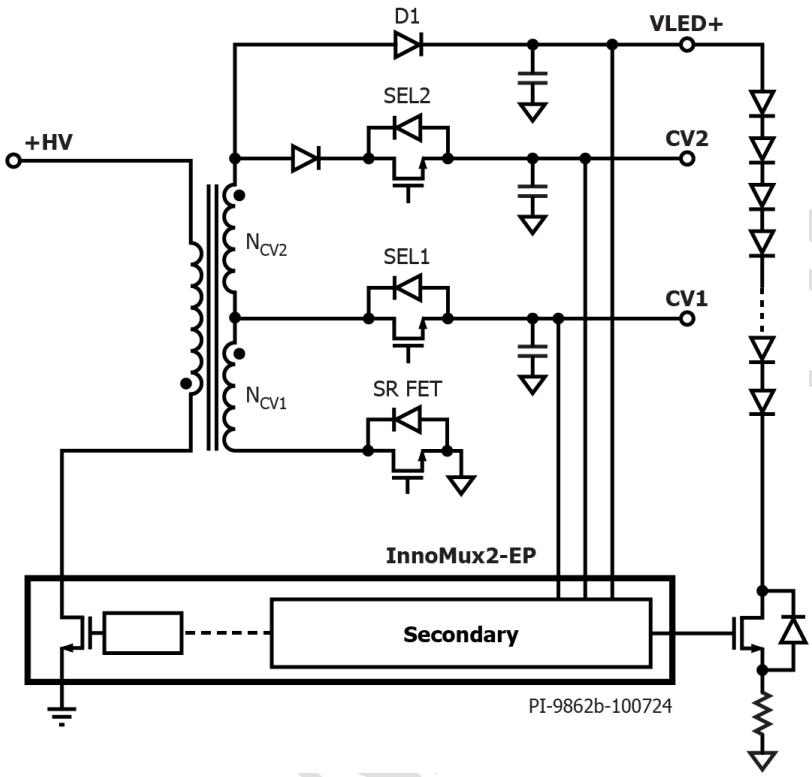


Figure 3 – DER-1050 Block Diagram of Secondary Side.

The VCV1 and VCV2 and VLED pins continuously sense the output voltages. If the voltage of any of the outputs drops below their minimum regulation level, the multi-output controller in the InnoMux2-EP IC sends a request for a switching cycle to primary-side via the FluxLink™ communication channel. For the multiplexing algorithm to work correctly and effectively steer the power, it is essential that the reflected voltage for each winding must be higher than that of the preceding (lower output voltage) winding:

$$\frac{V_{CV1}}{N_{CV1}} < \frac{V_{CV2}}{N_{CV1} + N_{CV2}} < \frac{V_{LED}}{N_{CV1} + N_{CV2}}$$

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

3 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						2 Wire – no P.E.
Voltage	V_{IN}	180		265	VAC	180 VAC – 265 VAC
Frequency	f_{LINE}		50		Hz	
No Load Input Power						Measured at 230 VAC, SVF Enabled
SVF Enabled				150	mW	V_{OUT1} = 5 V, I_{OUT1} = 0.5 A, V_{OUT2} = 24 V, I_{OUT2} = 0 A, V_{OUT3} = 36 V, I_{OUT3} = 600 mA
SVF Disabled				100	mW	Measured at 230 VAC, full load
Output						
Output Voltage 1	V_{OUT1}		5		V	±1%
Output Voltage Ripple 1	$V_{RIPPLE1}$			200	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}	0		500	mA	
Output Voltage 2	V_{OUT2}		24		V	±1%
Output Voltage Ripple	$V_{RIPPLE2}$			410	mV	20 MHz Bandwidth
Output Current 2	I_{OUT2}	0		2.4	A	
Output Peak Current 2	$I_{OUT2,PK}$			5.8	A	
LED Voltage	V_{OUT3}		36		V	
LED Current	I_{OUT3}		600		mA	±5%
Total Output Power						Switched Valley-Fill (SVF) Enabled:
Continuous Output Power	$P_{OUT(NOM)}$		82		W	V_{OUT1} = 5 V, I_{OUT1} = 0.5 A, V_{OUT2} = 24 V, I_{OUT2} = 2.4 A V_{OUT3} = 36 V, I_{OUT3} = 600 mA
Peak Output Power	$P_{OUT(PEAK)}$			163.3	W	SVF Disabled: V_{OUT1} = 5 V, I_{OUT1} = 0.5 A V_{OUT2} = 24 V, I_{OUT2} = 5.8 A V_{OUT3} = 36 V, I_{OUT3} = 600 mA
Efficiency						
SVF Disabled, Full Load Efficiency	η		88		%	230 VAC, Vout measured on the board
SVF Enabled, Efficiency			83		%	Measured at 230 VAC, SVF Enabled V_{OUT1} = 5 V, I_{OUT1} = 0.5 A V_{OUT2} = 24 V, I_{OUT2} = 0 A V_{OUT3} = 36 V, I_{OUT3} = 600 mA
Power Factor		0.9				Measured at 230 VAC, SVF Enabled V_{OUT1} = 5 V, I_{OUT1} = 0.5 A V_{OUT2} = 24 V, I_{OUT2} = 0 A V_{OUT3} = 36 V, I_{OUT3} = 600 mA
ATHD				10	%	Measured at 230 VAC, SVF Enabled V_{OUT1} = 5 V, I_{OUT1} = 0.5 A V_{OUT2} = 24 V, I_{OUT2} = 0 A V_{OUT3} = 36 V, I_{OUT3} = 600 mA
Environmental						
Conducted EMI		Meets CISPR 15B / EN55015B				
Safety						

4 Schematic

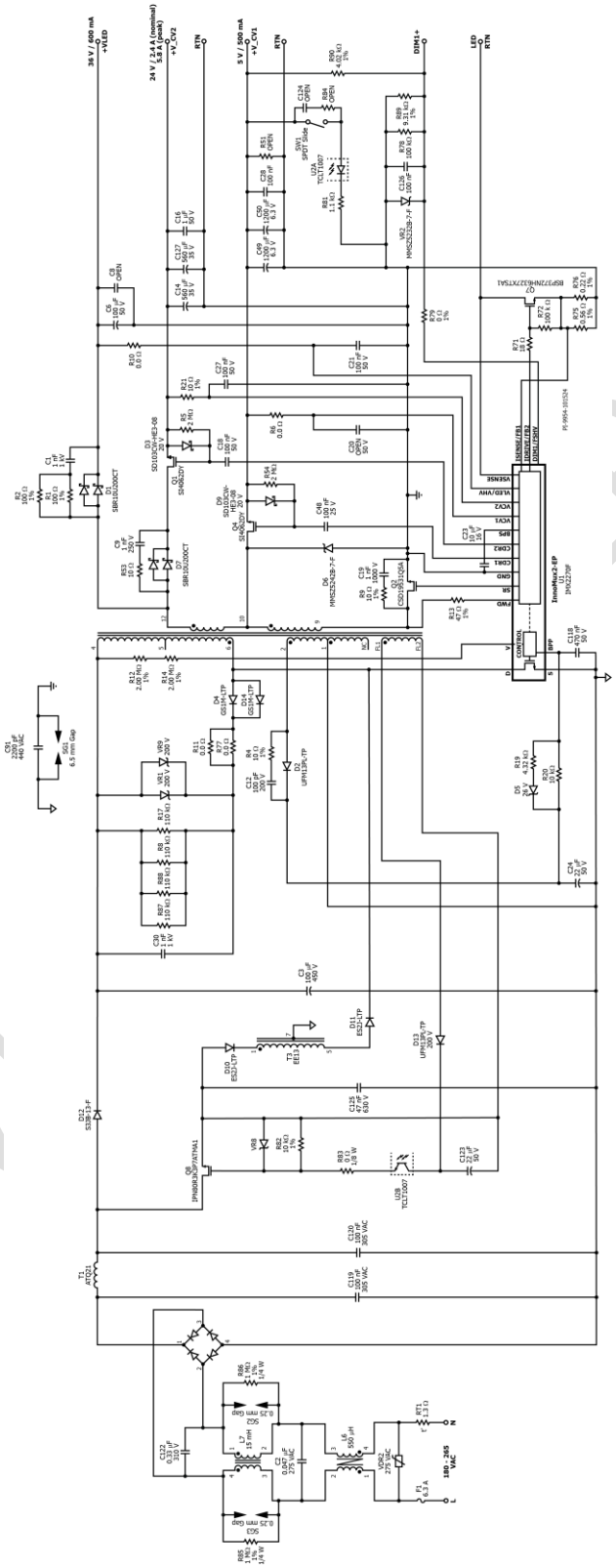


Figure 4 – Schematic.

5 Circuit Description

5.1 Input Rectification and EMI Filtering

Fuse F1 isolates the PSU circuitry and provides protection from primary-side component failure. Thermistor RT1 reduces inrush current at startup. Varistor VDR2 protects against line surges by clamping the input voltage seen by the power supply. Common-mode chokes L6 and L7, along with X-capacitors C2 and C122, attenuate both common-mode and differential-mode noise. Resistor R85 and R86 damps the self-resonance of the inductors.

Bridge rectifier BR1 rectifies the AC line voltage into full wave rectified DC, high frequency noise is rejected by a pi filter - capacitors C119, C120, and inductor T1. These components also provide differential-mode noise suppression along with Y-capacitor C91. Capacitor C3 stores excess energy generated by the PFC during the off time of the power switch.

5.2 Primary-Side

5.2.1 Power Switch

The transformer primary is connected between the input DC bus (TXPRI+) and the drain of the integrated primary switch of InnoMux2-EP IC (U1 DRAIN pin).

A clamp comprising an RCD plus a TVS diode (C30, R87, R88, R8, R17, VR1, VR9, D4, D14, R11, R77) is used to limit the peak drain voltage across the primary switch at turn-off. During normal operation C30 absorbs leakage energy and dissipates it through R87, R88, R8 and R17. TVS diodes VR1 and VR9 operate as a clamp and protect the InnoMux-2 IC from excessive drain voltage during abnormal conditions.

5.2.2 Primary-Side Controller Power Source and OV Protection

The primary side controller is part of the InnoMux2-EP IC (U1). It is self-starting, using an internal high-voltage current source (derived from the DRAIN pin) to charge the BPP capacitor C118, when voltage is first applied to the converter. During normal operation (steady-state) the primary-side is powered from an auxiliary winding on the main transformer. The voltage across this winding is rectified and filtered using diode D2 and capacitor C24, and then connected to the BPP pin via a current limiting resistor R20. Resistor R4 and capacitor C12 form a snubber across diode D2 to help reduce EMI.

5.2.3 Primary-Side OVP, Brown-In and Brown-Out Protection

Primary-side output overvoltage protection (OVP) is implemented by Zener diode D5 and the series resistor R19. In the event of an uncontrolled overvoltage at the output, the auxiliary winding voltage increases and causes D5 to break down which allows current to flow into the BPP pin of IC U1. If this current exceeds the I_{SD} threshold, the primary-side controller in the InnoMux2-EP IC will latch off - protecting the outputs.

Resistor R12 and R14 provide input voltage information to the V pin which provides protection from line undervoltage and overvoltage.

5.2.4 Primary Peak Current Limit

The value of capacitor C118 is used to set the maximum primary current to STANDARD or to INCREASED level. In this case 470 nF capacitance sets the primary-side controller peak current limit to its STANDARD level of 3.39 A.

5.3 Secondary-Side

The secondary-side of the InnoMux2-EP IC (U1) is powered from the 5 V BPS rail which is generated internally. Capacitor C23 is a local decoupling capacitor.

5.3.1 Primary to Secondary-Side Communication

The secondary-side of the InnoMux2-EP IC (U1) sends a request to the primary-side controller to initiate a switching cycle via FluxLink™, the safety-rated galvanically isolated communication channel.

5.3.2 InnoMux2-EP Power Supply

During start-up, the InnoMux2-EP secondary-side BPS rail is generated from energy supplied from the LED rail via R10 or from the FWD pin. There is a local decoupling capacitor C21 connected close to the VLED pin of U1. An internal regulator reduces the LED+ voltage to 5 V and outputs it to the BPS bus (U1 pin 6).

In steady state, the voltage on VCV1 (U1 pin 11) is 5 V and BPS direct-power-mode is enabled. The BPS pin voltage is supplied by CV1 if it is within a suitable range (4.75 V to 5.5 V). Directly powering the BPS rail from VCV1 minimizes power dissipation which becomes very important when the user equipment is in standby (low power) mode. In the event where the CV1 voltage falls out of the allowable BPS range (4.75 V to 5.5 V), the next suitable BPS source is automatically selected.

5.3.3 Drive for the Selection MOSFETs

The gate drive amplitude for the selection MOSFET Q4 is approximately equal to the voltage on the BPS rail (5 V). Consequently, logic level selection MOSFETs are used. Capacitor C48 is charged up to V_{CV1} from the CV1 output via a diode (D9) connected to the CDR1 pin. When the selection MOSFET needs to be turned on, the CDR1 pin voltage is raised from GND to BPS potential, and the selection MOSFET gate voltage (the other terminal of the capacitor C48) is lifted to V_{CV1}+V_{BPS}. R54 serves as a gate discharge path for the selection MOSFET (Q4).

Similarly, the gate drive amplitude for the selection MOSFET Q1 is approximately equal to the voltage on the BPS rail (5 V). Capacitor C18 is charged to V_{CV2} from the CV2 output via diode (D3) which is connected to the CDR2 pin. When the selection MOSFET needs to be turned on, the CDR2 pin voltage is raised from GND to BPS potential, and the selection

MOSFET gate voltage (the other terminal of the capacitor C18) is lifted to $V_{CV2}+V_{BPS}$. R5 serves as a gate discharge path for the selection MOSFET (Q1).
The secondary control circuit in the InnoMux2-EP IC needs to monitor the secondary-side idle ring to determine SR timing and facilitate valley switching or zero voltage switching (ZVS). This information is provided by the FWD pin, measurement is facilitated by keeping Q2 on after the secondary conduction time has expired.

5.3.4 Output Control

Output rectification for the CV1 output is provided by the SR MOSFET Q2 and the CV1 selection MOSFET (Q4). The low ESR capacitors (C49, C50 and C28) ensure low output ripple voltage. Zener diode D6 is used as a voltage clamp for the transformer CV1 winding.

Similarly, output rectification for the CV2 output is provided by the SR MOSFET Q2, D7, and the CV2 selection MOSFET (Q1). A small multilayer ceramic (MLCC) capacitor C16 is connected across the CV2 output terminals and provides low impedance bypass for any high frequency noise. The RC snubber network comprised of R53 and C90 damps high-frequency ringing across the rectifier diode D7.

For the CC LED output, output rectification is provided by the SR MOSFET Q2 and diode D1. Capacitor C6 is used to provide energy storage and filtering at the LED output. The RC snubber network comprised of R1, R2 and C1 damps high-frequency ringing across the rectifier diode D1. The RC snubber network comprised of R9 and C19 damps high-frequency ringing across the SR MOSFET Q2.

When the selection MOSFETs (Q4) and (Q1) are turned off and the SR MOSFET (Q2) is turned on, the voltage on the anode of D1 rises until it is forward biased. In this condition, all the transformer energy is directed to the LED Output.

When the selection MOSFET (Q4) is turned off while selection MOSFET (Q1) is turned on, the secondary turns of the transformer are selected such that the voltage on the anode of D1 is below the lowest working LED string voltage. Therefore, D1 will remain reverse biased, and all transformer energy is directed to CV2.

When the selection MOSFET (Q4) is turned on while selection MOSFET (Q1) is turned off, the secondary turns of the transformer are selected such that the voltage on the anode of D1 is below the lowest working LED string voltage. Therefore, D1 will remain reverse biased, and all transformer energy is directed to CV1.

When both selection MOSFETs are turned on, only one output is serviced. If multiple outputs require energy at the same time, the output scheduler chooses the next requesting output in the series based on which output received the last energy pulse. The selection order is CV1 then CV2 then LED then back to CV1.

5.4 Switched-Valley Fill Single Stage PFC

Without the added PFC circuit, the power factor of the flyback power supply is approximately 0.5 to 0.6 under full load. The input of the flyback power supply circuit usually consists of the full wave bridge rectifier (BR1) followed by a storage bulk capacitor (C3) capable of sustaining the voltage to approximately equal to the peak voltage of the input sine wave until the peak of the next AC cycle. The input charging pulse current must be sufficient to sustain the load until the next peak. In practice this means that the charging pulse current is around 5-10 times higher than the average current with significant phase lead from the input voltage sine wave.

The Switched Valley-Fill Single Stage PFC (SVF S^2PFC) is composed of an inductor T3, and diodes (D10 and D11) connected directly to the DRAIN (D) pin of the Innomux-2 IC. The Innomux2 IC primary switch will draw an additional high frequency pulse current from the full wave rectified input. This will reduce the rms input current and reduce the phase angle difference from the input line voltage; hence power factor will increase and THD will improve.

The PFC inductor T3 operates in DCM mode. When the power MOSFET is on, current drawn from the rectified input ramps through the boost inductor (T3) storing energy. When the primary switch turns off, the stored energy in T3 is delivered to the load via direct energy transfer between the primary and secondary winding of the flyback transformer T2. The variability of the PFC inductor peak current (set by primary switch on time) will be compensated for by the Innomux2 IC primary and secondary-side controllers.

Leakage energy stored on the leakage inductance of transformer T2 during on time will be delivered to the storage bulk capacitor C3 during power MOSFET off time. The expected voltage stress across the bulk capacitor C3 will be higher than the peak input voltage. 2 PFC diodes D10 and D11 are connected in series to prevent voltage overstress caused by the resonant ring of inductor T2 during the turn off of the primary power MOSFET.

5.5 Switched-Valley Fill Single Stage PFC Switch Operation

The Switched Valley-Fill (SVF) Single Stage PFC is activated when switch SW1 connects the CV1 output to the optocoupler U2A. Once switch SW1 is closed, current flows through the optocoupler U2A, which allows U2B to conduct. The primary bias circuit comprising D13 and C12, drives MOSFET on Q8 when U2B is conducting allowing current to flow to the SVF circuit.

When SW1 is disabled, no current flows through optocoupler U2A, keeping U2B open, and MOSFET Q8 remains off deactivating the SVF circuit.

When the optocoupler U2B is not conducting, resistor R82 ensures that the gate-source voltage of MOSFET (Q8) is pulled to 0 V. Diode VR8 clamps transient voltage spikes, protecting MOSFET (Q8).

6 SVF Operation Control

The connection diagram below describes SVF and dimming configuration.

6.1 SVF Configuration Switch Location and Slide Operation

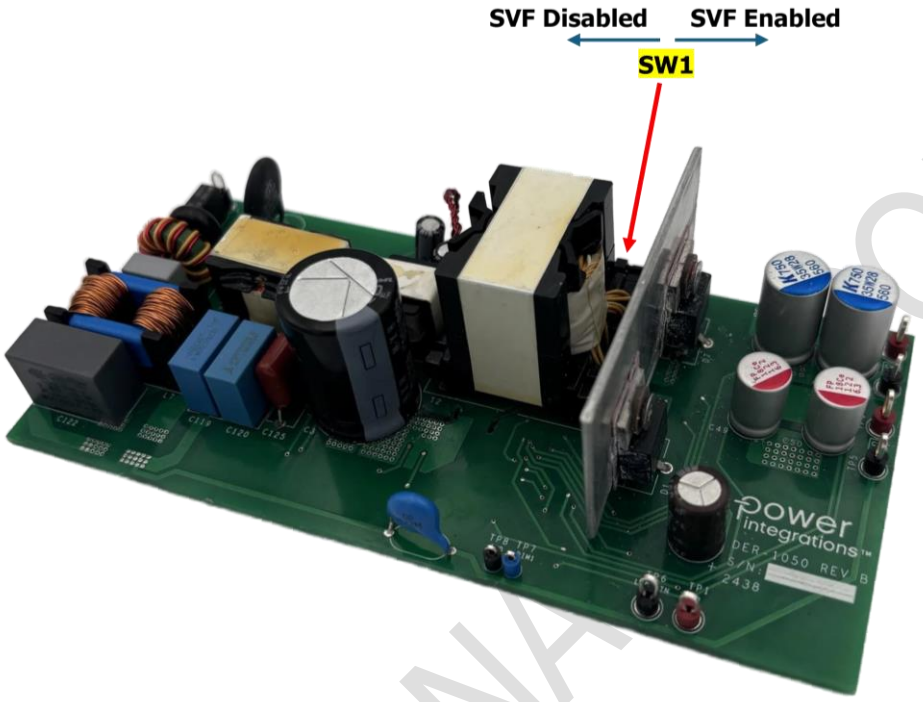


Figure 5 – SVF Configuration.

This design incorporates a manual control for power factor correction (PFC), simulating microcontroller-based control in a clothes-dryer rack application. The PFC is only enabled when the 21.6 W LED load is in use while the motor remains off. This is to comply with certification agencies like CCC in China, which classify the clothes-dryer rack as a lighting appliance effective January 1, 2025.

SVF State	Load Configuration	Remarks
SVF Disabled	LED: 36 V / 0.6 A CV1: 5 V / 0.5 A CV2: 24 V / 2.4 A_{NOM} / 5.8 A_{PK}	Supports full load on all outputs
SVF Enabled	LED: 36 V / 0.6 A CV1: 5 V / 0.5 A **CV2: 24 V / 0 A – Unloaded**	CV2 (heating element) unloaded

6.2 Dimming Configuration

6.2.1 Summary of Dimming Configuration

Dimming Mode	Configuration	Description
Default mode (100% Dimming)	Resistor R89 and R90 are populated	In this configuration, R89 and R90 create a voltage divider that provides 3.4 VDC to the dimming input corresponding to maximum LED current
With Dimming Control	Resistor R89 and R90 are unpopulated; 1-wire filtered PWM applied	1-wire filtered PWM is applied between DIM+ and GND terminals with the following parameters: • V_{PEAK} = 3.3 Vp • F_{SW} = 10 kHz – 30 kHz • Duty Cycle = 0 – 100% (Proportional to LED current)

6.2.2 Default mode (100% Dimming)

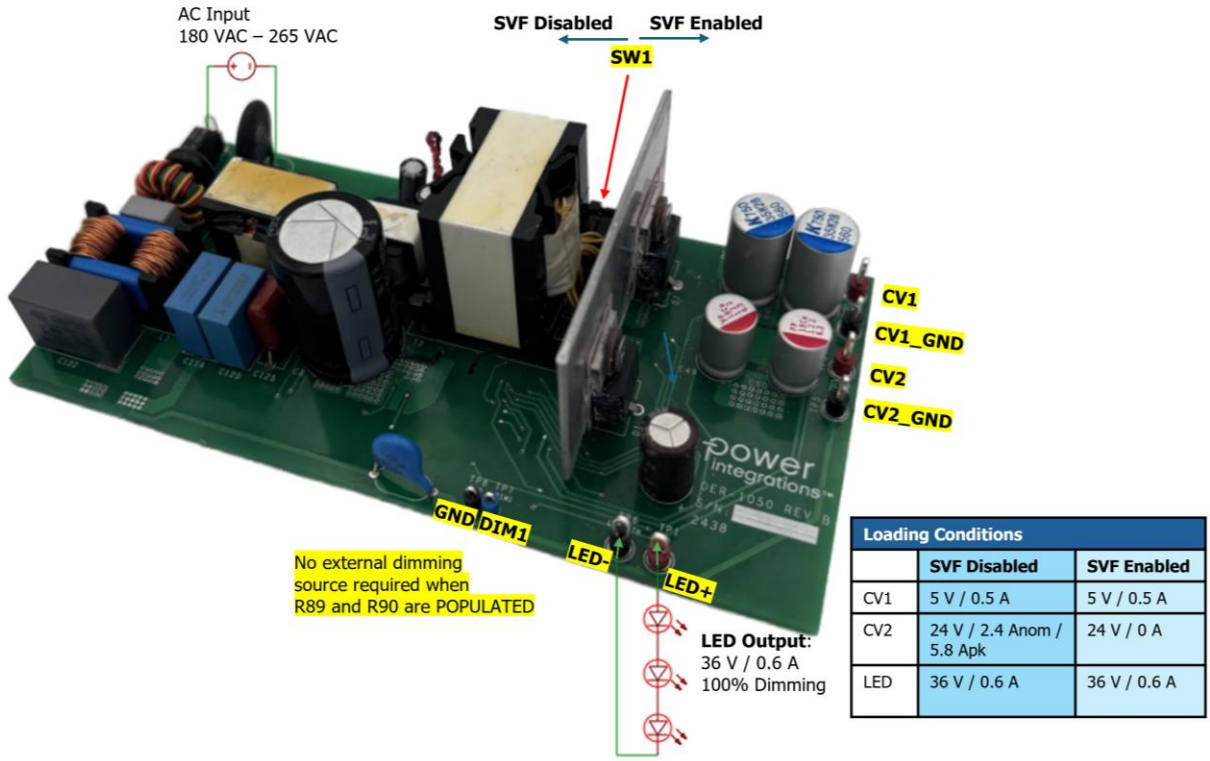


Figure 6 – Default Mode (100% Dimming), R89 and R90 are populated.

6.2.3 With Dimming Control

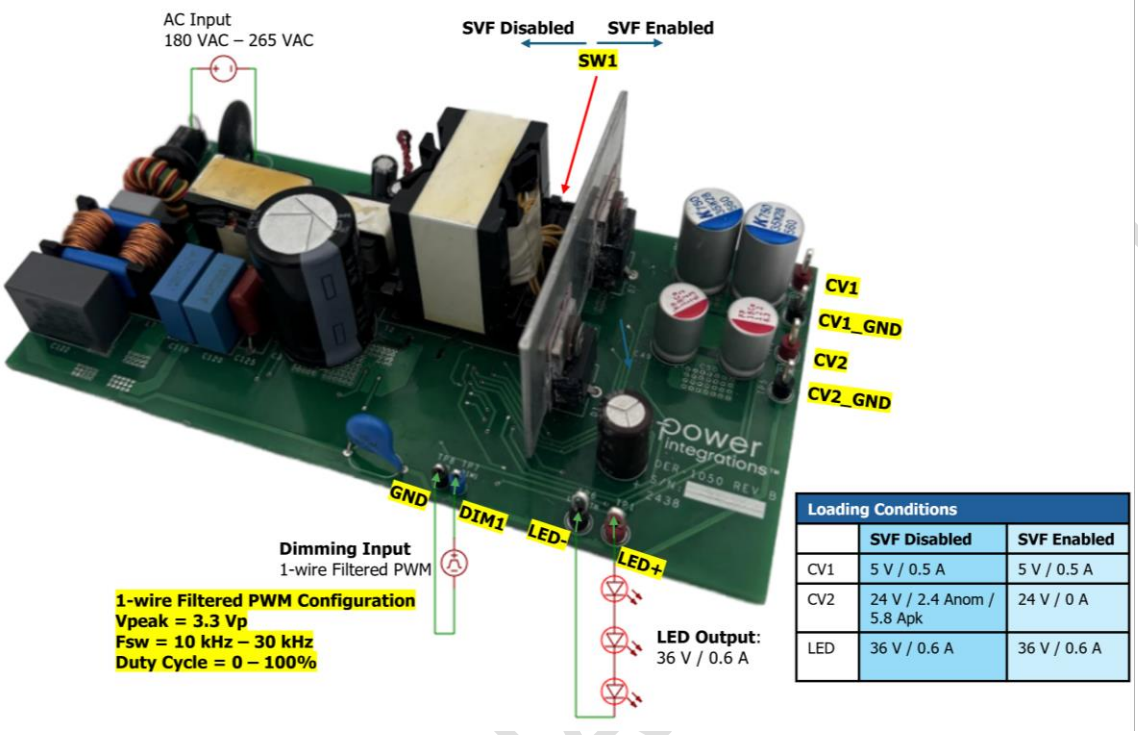


Figure 7 – 1-wire Filtered PWM Dimming Configuration, R89 and R90 are unpopulated.

7 PCB Layout

The PCB uses FR4 material with a thickness of 1.6 mm and a double-sided copper layer with a thickness of 2.0 oz.

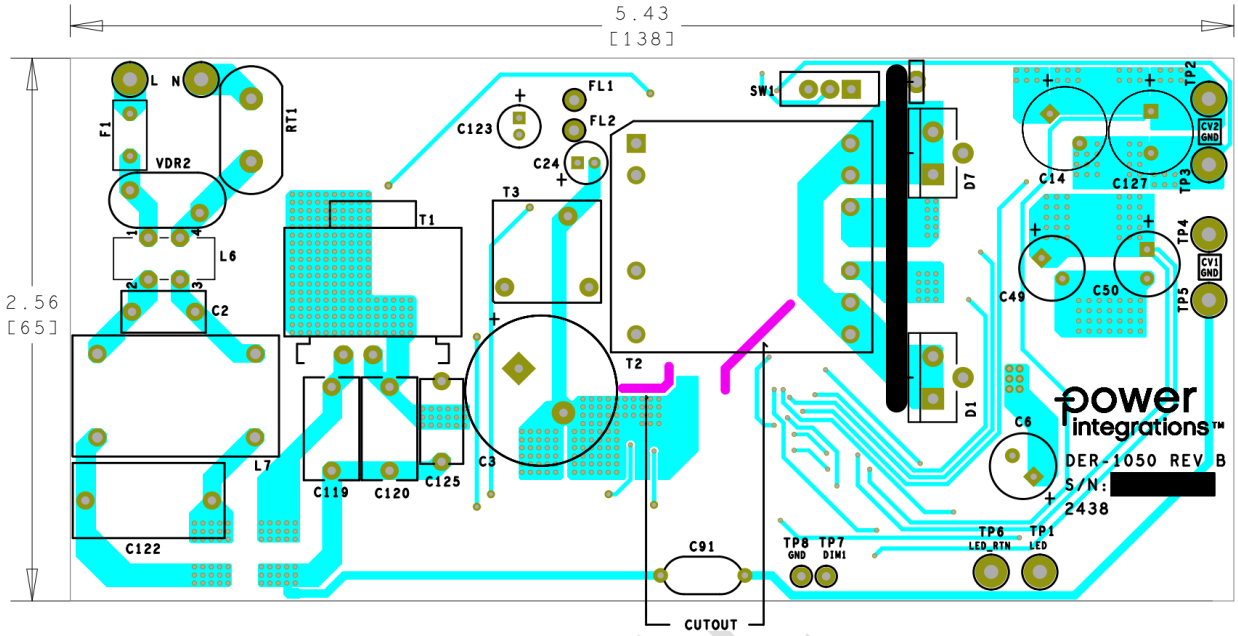


Figure 8 – Printed Circuit Layout, Top.

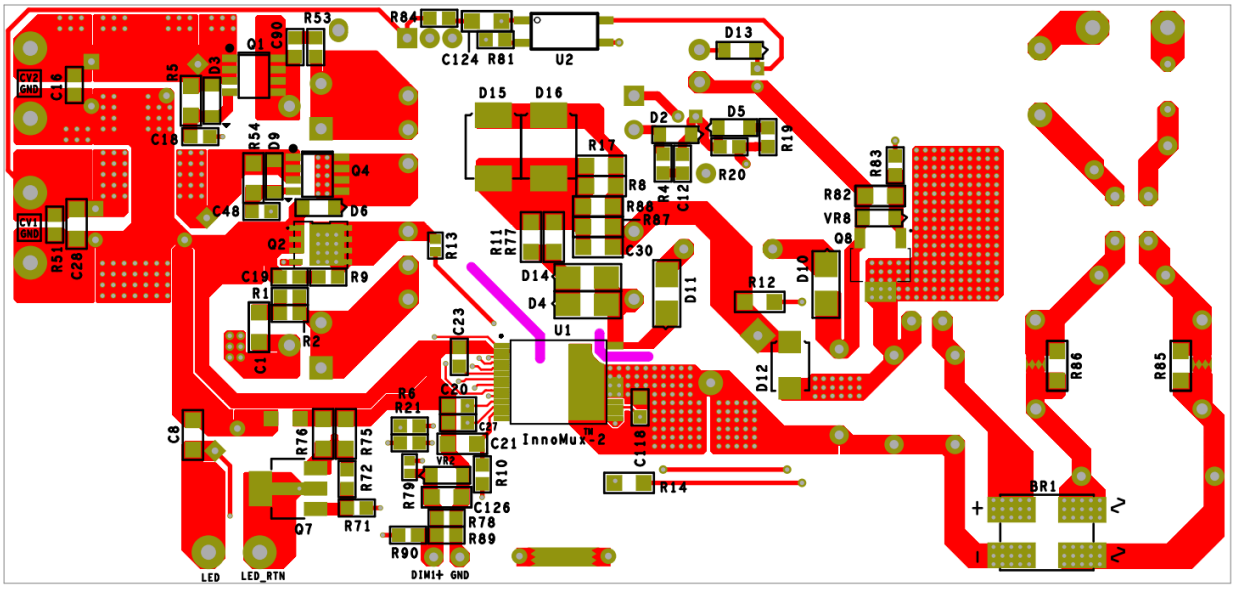


Figure 9 – Printed Circuit Layout, Bottom.

8 Bill of Materials

Item Number	Part Reference	QTY	Description	Mfg Part Number	Mfg
1	BR1	1	RECT BRIDGE, GP, 800V, 4A, Z4-D	Z4DGP408L-HF	Comchip Technology
2	C1 C30	2	1 nF, 1000 V, Ceramic, X7R, 1206	CC1206KKX7RCBB102	Yageo
3	C2	1	0.047 µF, Film Capacitor, X2, 310V 630V, Polypropylene (PP), Metallized Radial	BFC233820473	Vishay Beyschlag/Draloric/BC Components
4	C3	1	100 µF, 450 V, Electrolytic, (18 x 25).	450HXW100MEFR18X25	Rubycon
5	C6	1	100 µF, 50 V, Electrolytic, Very Low ESR, 74 mOhm, (8 x 11.5)	EKZE500ELL101MHB5D	Nippon Chemi-Con
6	C8	1	OPEN		
7	C12	1	100 pF, 200 V, Ceramic, COG, 0805	08052A101JAT2A	AVX Corp
8	C14 C127	2	560 µF, ±20%, 35 V, Aluminum – Polymer Capacitors, (10 x 18)	A750MW567M1VAAE018	KEMET
9	C16	1	1 µF, ±20% ,50 V, Ceramic, X7R, Boardflex Sensitive, 0805 (2012 Metric)	CGA4J3X7R1H105M125AE	TDK Corp
10	C18 C27	3	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
11	C20	1	OPEN		
12	C19	1	1 nF, 10%, 1000 V, Ceramic, X7R, 0805	C0805C102KDRACTU	Kemet
13	C21	1	0.1 µF, 250V, ±10%, Ceramic, X7R, 1206 (3216 Metric)	C3216X7R2E104K160AA	TDK Corporation
14	C23	1	10 µF, ±10%, 16V, X7R, Ceramic Capacitor, Surface Mount, MLCC 0805 (2012 Metric)	CL21B106KOQNNNE	Samsung
15	C24 C123	2	22 µF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
16	C28	1	100 nF, 25 V, Ceramic, X7R, 1206	C1206F104K3RACTU	Kemet
17	C48	1	100 nF, 25 V, Ceramic, X7R, 0805	08053C104KAT2A	AVX Corp
18	C49 C50	2	1200 µF, 6.3 V, Aluminum – Polymer Capacitors Radial, Can, 9mOhm, 2000 Hrs @ 105°C, (8 x 13mm) x 3.5mmLS	RNU0J122MDN1KX	Nichicon
19	C90	1	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
20	C91	1	2200pF ±20% 440VAC Ceramic Capacitor E Radial, Disc, X1, Y1	CD45-E2GA222M-NKA	TDK Corporation
21	C118	1	470 nF, ±10%,50 V, Ceramic, X7R, 0805	CL21B474KBFVPNE	Samsung Electro-Mechanics
22	C119 C120	2	100 nF, 305 VAC, Film, X2	B32921C3104M	Epcos
23	C122	1	0.33 µF, ±10%, Film Capacitor X2, 310V 630V, AEC-Q200, Polypropylene (PP), Metallized Radial	R523I3330DQP1K	KEMET
24	C124	1	OPEN		
25	C125	1	47 nF, 630 V, Film	MEXPD24704JJ	Duratech
26	C126	1	OPEN		
27	D1 D7	2	200 V, 10 A, Dual Schottky, TO-220AB	SBR10U200CT	Diodes Incorporated
28	D2 D13	2	DIODE, GEN PURP, 200V, 1A, SOD-123F, SOD123FL	UFM13PL-TP	Micro Commercial Co.
29	D3 D9	2	Diode, Schottky, 20 V, 350mA (DC), Surface Mount SOD-123, SC-76	SD103CW-HE3-08	"
30	D4 D14	2	1000 V, 1 A, DO-214AC	GS1M-LTP	Micro Commercial Co
31	D5	1	26 V, 3%, 500 mW, SOD 123	DDZ26-7	Diodes, Inc
32	D6	1	DIODE ZENER 12V 500MW SOD123	MMSZ5242B-7-F	Diodes, Inc
33	D10 D11	2	600 V, 2 A, Super-Fast, 35 ns, DO-214AC, SMA	ES2J-LTP	Micro Commercial Co.
34	D12	1	600 V, 1 A, General Purpose, SMB Case	MURS160-13-F	Diodes, Inc.
35	F1	1	FUSE BRD MNT 6.3A 350VAC 72VDC	0697H6300-02	Belfuse
36	FL1 FL2	2	Flying Lead, Hole size 50mils	N/A	N/A
37	HS_POST?	1	Post, Heatsink, SS, Nickel Plated ,5 mm W x 9.1mm T	Custom	Custom
38	L TP3 TP5 TP6	4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
39	L6	1	CMC, 300 µH @ 100KHz, Toroidal, wound on 32-00315-00 toroidal core, using 10 turns #24 AWG wire per side	32-00429-00	Power Integrations

40	L7	1	15 mH @ 10 kHz, 2 Line Common Mode Choke, Through Hole ,1.3A, DCR 430mOhm (Typ), 24.5 x 14.5 mm x 13.5mm height	B82732F2132B001	Epcos
41	N	1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
42	Q1 Q4	2	MOSFET, N-Channel, 60V, 32.1A (Tc), 7.8W (Tc), 4.2 mOhm @ 20A, 10V, 8-SO, SO-8, 8-SOIC (0.154", 3.90mm Width)	SI4062DY-T1-GE3	Vishay Siliconix
43	Q2	1	MOSFET, N-ch, Enhancement mode, 100V, 110A, 5.3mOhm Pwr MOSFET, 150C Tmax, 8-VSON (5x6)	CSD19531Q5A	Texas Instruments
44	Q7	1	"MOSFET, N-Channel, 100 V ,1.8A (Ta), 1.8W (Ta), Surface Mount PG-SOT223-4, TO-261-4, TO-261AA,	SOT223"	BSP372NH6327XTSA1
45	Q8	1	MOSFET, N-Channel, 800 V, 1.9A (Tc), 6.1W (Tc), Surface Mount PG-SOT223, SOT-223, TO-261-4, TO-261AA	IPN80R3K3P7ATMA1	Infineon Technologies
46	R1 R2	2	RES, 100 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1000V	Panasonic
47	R4 R9 R21 R53	5	RES, 10 R, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF10R0V	Panasonic
48	R5 R12 R14 R54	4	RES, 2.00 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
49	R6 R10	2	RES, 0 R, 5%, 1/8 W, Thick Film, 0805	RMCF0805ZT0R00	Stackpole Electronics Inc
50	R8 R17 R87 R88	4	RES, 110 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J114V	Panasonic
51	R11 R77	2	RES, 0 R, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic
52	R13	1	RES, 47.0 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF47R0V	Panasonic
53	R19	1	RES, 4.32 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4321V	Panasonic
54	R20	1	RES, 10.0 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
55	R51	1	OPEN		
56	R71	1	RES, 18 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ180V	Panasonic
57	R72 R78	2	RES, 100 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
58	R75	1	RES, SMD, 0.56 OHM, 1%, 1/4W, 1206	ERJ-8RQFR56V	Panasonic
59	R76	1	RES, 0.22 OHM 1/4W, 1%, Thick Film, 1206	ERJ-8RQFR22V	Panasonic
60	R79	1	RES,0 Ohms Jumper 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	RC0603FR-070RL	Yageo
61	R81	1	RES, 1.1 k, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ112V	Panasonic
62	R82	1	RES,10 kOhms, ±1%, ±200ppm/°C, 0.5W, 1/2W Chip Resistor 1206 (3216 Metric), Moisture Resistant, Thick Film	RC1206FR-7W10KL	Yageo
63	R83	1	RES, 0 Ohms, Jumper, 0.25W, 1/4W Chip Resistor, 0805 (2012 Metric), Anti-Sulfur, Moisture Resistant Thick Film	RK73Z2ARTTD	KOA Speer Electronics, Inc.
64	R84	1	OPEN		
65	R85 R86	2	RES, 1 MOhms, ±1%, 0.25W, 1/4W Chip Resistor, 1206 (3216 Metric), Automotive AEC-Q200, Thick Film	RMCF1206FT1M00	Stackpole Electronics Inc
66	R89	1	RES, 9.31 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF9311V	Panasonic
67	R90	1	RES, 4.02 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4021V	Panasonic
68	RT1	1	NTC Thermistor, 1.3 Ohms, 7 A	MF72-001.3D13	Cantherm
69	SG1	1	Spark Gap 6.5mm 2 pin		
70	SG2 SG3	2	Spark Gap 0.25mm		
71	SW1	1	SWITCH SLIDE SPDT 30V.2A PC MNT	EG1218	E-Switch
72	T1	1	Bobbin, ATQ21/16.8 Vertical, 5 pins. Mates with core 99-00088-00.	ATQ21-16.8A-5P-TH-H-17	TBI (Transformer Bobbin Industrial Co. ltd
73	T2	1	Bobbin, PQ26/25, Vertical, 12 pins	PQ26X25	Pin Shine
74	T3	1	Bobbin, EE13, Vertical, 10 pins	P-1302-2	Pin Shine
75	TP1 TP2 TP4	3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
76	TP7	1	Test Point, BLUE, Miniature THRU-HOLE MOUNT	5117	Keystone
77	TP8	1	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
78	U1	1	MINNO-2 test symbol with 28 pins, InSOP-T28B		Power Integrations
79	U2	1	OPTOISOLATOR, 5KV, TRANSISTOR, 4-SOP	TCLT1007	Vishay

80	VDR2	1	275Vac, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
81	VR2	1	DIODE ZENER 5.6V 500MW SOD123	MMSZ5232B-7-F	Diodes, Inc
82	VR8	1	DIODE ZENER 20V 500MW SOD123	MMSZ5250B-7-F	Diodes, Inc
83	VR1 VR9	2	324V Clamp, 4.6A Ipp, 1500W (1.5kW), BIDIRECTIONAL TVS Diode, Surface Mount DO-214AB (SMC)	SMCJ200CA	Bourns Inc.

9 Flyback Transformer Design Spreadsheet

1	***InnoMux2_EP_071724; Rev.1.5; Copyright Power Integrations 2024***	***INPUT***	***INFO***	***OUTPUT***	***UNITS***	***DESCRIPTION***
2	Power Supply Basic Parameters					
3	OUTPUT CONFIGURATION	CV1_CV2_LED		CV1_CV2 LED		Output configuration
4	DC INPUT VOLTAGE	NO		NO		Yes = DC input; No = AC input
5	VAC MIN	180		180	V	Minimum AC input voltage
6	VAC NOM	230		230	V	Nominal AC input voltage
7	VAC MAX	265		265	V	Maximum AC input voltage
11	PO PK			163.30	W	Total output power @ peak load condition
12	PO			81.70	W	Total output power @ nominal load condition
13	PIN PK			185.57	W	Input power @ peak load condition
14	PIN			92.84	W	Input power @ nominal load condition
15	PTRF PK			175.55	W	Power processed by the transformer @ peak load condition
16	PTRF			87.83	W	Power processed by the transformer @ nominal load condition
17	FL	50		50	Hz	AC line frequency
18	VMAX			374.8	V	Maximum rectified input voltage
19	N			0.88		Estimated converter efficiency
20	Z			0.55		Secondary loss allocation
21	USE SR	YES		YES		Use synchronous rectification
22	**Input Section**					
23	CIN	100		100	µF	Input capacitance
24	VMIN			222.8	V	Minimum DC input voltage calculated at VAC MIN and nominal power
25	VMIN AVG			239.9	V	Rectified average input voltage calculated at VAC MIN and nominal power
26	VMIN [PEAK POWER]			192.8	V	Minimum DC input voltage calculated at VAC MIN and peak power
27	VMIN AVG [PEAK POWER]			227.5	V	Rectified average input voltage calculated at VAC MIN and peak power
54	**CV1 Specification**					
55	OUTPUT TYPE			CV		Output control type
56	VOUT CV1	5.00		5.00	V	CV1 voltage
57	IOUT CV1	0.500		0.500	A	CV1 current
58	IOUT CV1 [PEAK POWER]			0.500	A	CV1 current for peak power requirement
59	CONNECTION TYPE CV1	Auto		AC_STACK		Winding connection type
60	CV2 Specification					
61	OUTPUT TYPE			CV		Output control type
62	VOUT CV2	24.00		24.00	V	CV2 voltage
63	IOUT CV2	2.400		2.400	A	CV2 current
64	IOUT CV2 [PEAK POWER]	5.800		5.800	A	CV2 current for peak power requirement

65	CONNECTION TYPE CV2	Auto		AC_STACK		Winding connection type
66	**LED Specification**					
67	OUTPUT TYPE			CC		Output control type
68	VOUT LED MAX	36.00		36.00	V	LED maximum voltage
69	VOUT LED MIN			36.00	V	LED minimum voltage
70	IOUT LED	0.600		0.600	A	Total LED current
71	IOUT LED [PEAK POWER]			0.600	A	Total LED current for peak power requirement
72	CONNECTION TYPE LED	Auto		AC_STACK		Winding connection type
91	Other Design Conditions					
92	FS TARGET	100.00		100.00	kHz	Target maximum frequency at VMIN and peak power
94	KP TARGET	0.400		0.400		Minimum KP target at VMIN and peak power
95	VOR MARGIN LED-CV2	30.0		30.0	V	Minimum VOR margin between LED/CVHV and CV2 output
97	VOR MARGIN CV2-CV1			0.0	V	Minimum VOR margin between CV2 and CV1 Output
99	BP MAX			0.33	T	Maximum allowed peak flux density at VMIN and peak power
100	MAXIMUM VOR	136.0		136.0	V	Reflected output voltage maximum limit
101	**PI Device Variables**					
102	DEVNAME	IMX2270F		IMX2270F		Device name
103	BVDSS			750	V	Drain to source breakdown voltage
104	PACKAGE			InSOP 28D		Device package
105	DEVICE_MODE	Standard		Standard		Device current limit mode
106	ILIMIT TOL			7.00	%	Current limit tolerance
107	ILIMIT MIN			3.153	A	Minimum current limit
108	ILIMIT TYP			3.390	A	Typical current limit
109	ILIMIT MAX			3.627	A	Maximum current limit
111	FS LIMIT			155.00	kHz	Controller maximum switching frequency in steady-state condition
112	FS ABS MAX			194.00	kHz	Controller absolute maximum switching frequency in transitory condition
113	RDSON			0.41	Ohm	Drain to source on-time resistance
114	VDS			0.16	V	On-state drain to source voltage
118	**Transformer Parameters**					
119	Core and Bobbin Parameters					
120	CR TYPE	Custom		Custom		Core type (Compare transformer values against datasheet as it may differ per manufacturer.)
122	CR PN	ePC95		ePC95		Core part number
123	BB TYPE	PQ26/25		PQ26/25		Bobbin type
124	PRIMARY PINS	6		6		Number of primary pins in the bobbin
125	SECONDARY PINS	6		6		Number of secondary pins in the bobbin
126	BW	12.70		12.70	mm	Bobbin width
127	BFW	4.47		4.47	mm	Bobbin height
128	AE	122.2		122.2	mm^2	Core cross-sectional area
129	LE	53.5		53.5	mm	Core magnetic path length

130	VE	6540.0		6540.0	mm^3	Core volume
131	AL	5700		5700	nH/T^2	Ungapped core specific inductance
132	Inductance and Core Gap					
133	LP TOL			5.00	%	Primary inductance tolerance
134	LP MIN			551.6	µH	Minimum primary inductance
135	LP TYP			580.6	µH	Nominal primary inductance
136	LP MAX			609.6	µH	Maximum primary inductance
137	LG			0.773	mm	Estimated gap length
138	Construction Parameters					
139	NP	55		55		Primary winding total number of turns
141	NS CV1	3		3		CV1 output number of turns
143	NS STACK CV1			3		CV1 output stack number of turns
149	NS CV2	15		15		CV2 output number of turns
151	NS STACK CV2			12		CV2 output stack number of turns
153	NS LED	15		15		LED output number of turns
155	NS STACK LED			0		LED output stack number of turns
161	BM			0.266	T	Maximum flux density in steady-state conditions (@FS MAX) and nominal power condition
162	BM [PEAK POWER]			0.316	T	Maximum flux density in steady-state conditions (@FS MAX) and peak power condition
163	BP			0.344	T	Peak flux density in transitory conditions (@FS ABS MAX)
164	VOR CV1			91.7	V	Primary reflected output voltage during CV1 output conduction
165	VOR CV2			91.7	V	Primary reflected output voltage during CV2 output conduction
168	VOR LED at VO MAX			135.7	V	Maximum primary reflected output voltage during LED output conduction
169	VOR LED at VO MIN			135.7	V	Minimum primary reflected output voltage during LED output conduction
170	VOR MARG LED-CV2 ACTUAL			44.00	V	Minimum actual VOR margin between LED output and CV2 output reflected voltage
174	VOR MARG CV2-CV1 ACTUAL			0.00	V	Minimum actual VOR margin between CV2 output and CV1 output reflected voltage
175	**Operating Parameters Worst (Nominal Power)**					
176	FS MAX			42	kHz	Maximum operating switching frequency across all tolerance corners
177	FS MIN			33	kHz	Minimum operating switching frequency across all tolerance corners
178	KP			1.043		Minimum current continuity factor across all tolerance corners
179	KP LED ONLY			5.143		Minimum current continuity factor when CV outputs deliver no power and LED delivers full power
180	VOR MAX			135.7	V	Actual maximum reflected voltage
181	DMAX			0.291		Maximum duty cycle
182	TON MIN			6.757	us	Minimum controller ON time
183	TON			7.996	us	Maximum controller ON time

184	TOFF			21.934	us	Minimum controller OFF time
185	VDRAIN PEAK			580	V	Estimated off-state drain to source peak voltage (considers 70 V spike)
186	VDRAIN PLATEAU			510	V	Off-state drain to source plateau voltage
187	VDS ON			0.16	V	On-state drain to source voltage
188	IAVG PRIMARY			0.39	A	Primary switch average current
189	IAVG DIODE BRIDGE			0.38	A	Average diode bridge current (DC input current)
190	OUTPUTS HANDOVER TIME MARGIN			4.34		Ratio of CV conduction time and required controller blanking time
191	**Peak Currents (Nominal Power)**					
192	PRIMARY IP			3.00	A	Peak primary current @ nominal load condition
193	CV1 OUTPUT IP			47.49	A	CV1 output peak current @ nominal load condition
195	CV2 OUTPUT IP			9.50	A	CV2 output peak current @ nominal load condition
196	LED OUTPUT IP			10.99	A	LED output peak current @ nominal load condition
198	**RMS Currents (Nominal Power)**					
199	INPUT IRMS			1.06	A	Input RMS current @ nominal load condition
200	PRIMARY IRMS			0.89	A	Primary winding RMS current @ nominal load condition
201	CV1 OUTPUT IRMS			2.71	A	CV1 RMS current @ nominal load condition
202	CV1 OUTPUT WINDING IRMS			5.46	A	CV1 winding RMS current @ nominal load condition
205	CV2 OUTPUT IRMS			4.04	A	CV2 RMS current @ nominal load condition
206	CV2 OUTPUT WINDING IRMS			4.74	A	CV2 winding RMS current @ nominal load condition
207	LED OUTPUT IRMS			2.48	A	LED RMS current @ nominal load condition
208	LED OUTPUT WINDING IRMS			2.48	A	LED winding RMS current @ nominal load condition
211	**Ripple Currents (Nominal Power)**					
212	INPUT I RIPPLE RMS			0.99	A	Input capacitor RMS ripple current @ nominal load condition
213	CV1 I RIPPLE RMS			2.66	A	CV1 output RMS ripple current @ nominal load condition
215	CV2 I RIPPLE RMS			3.25	A	CV2 output RMS ripple current @ nominal load condition
216	LED I RIPPLE RMS			2.41	A	LED output RMS ripple current @ nominal load condition
218	**Operating Parameters Worst case (Peak Power)**					
219	FS MAX [PEAK POWER]			124	kHz	Maximum operating switching frequency across all tolerance corners
220	FS MIN [PEAK POWER]			71	kHz	Minimum operating switching frequency across all tolerance corners
221	KP [PEAK POWER]			0.281		Minimum current continuity factor across all tolerance corners
222	DMAX [PEAK POWER]			0.328		Maximum duty cycle
223	TON MIN [PEAK POWER]			2.636	us	Minimum controller ON time
224	TON [PEAK POWER]			4.599	us	Maximum controller ON time
225	TOFF [PEAK POWER]			9.454	us	Minimum controller OFF time

226	IAVG [PEAK POWER]			0.80	A	Average diode bridge current (DC input current)
227	**Peak Currents (Peak Power)**					
228	PRIMARY IP [PEAK POWER]			3.52	A	Peak primary current @ peak load condition
229	CV1 OUTPUT IP [PEAK POWER]			61.64	A	CV1 output peak current @ peak load condition
231	CV2 OUTPUT IP [PEAK POWER]			12.33	A	CV2 output peak current @ peak load condition
232	LED OUTPUT IP [PEAK POWER]			12.89	A	LED output peak current @ peak load condition
234	**RMS Currents (Peak Power)**					
235	INPUT IRMS [PEAK POWER]			1.86	A	Input RMS current @ peak load condition
236	PRIMARY IRMS [PEAK POWER]			1.59	A	Primary winding RMS current @ peak load condition
237	CV1 OUTPUT IRMS [PEAK POWER]			5.21	A	CV1 RMS current @ peak load condition
238	CV1 OUTPUT WINDING IRMS [PEAK POWER]			9.75	A	CV1 winding RMS current @ peak load condition
241	CV2 OUTPUT IRMS [PEAK POWER]			7.77	A	CV2 RMS current @ peak load condition
242	CV2 OUTPUT WINDING IRMS [PEAK POWER]			8.25	A	CV2 winding RMS current @ peak load condition
243	LED OUTPUT IRMS [PEAK POWER]			2.75	A	LED RMS current @ peak load condition
244	LED OUTPUT WINDING IRMS [PEAK POWER]			2.75	A	LED winding RMS current @ peak load condition
247	Ripple Currents (Peak Power)					
248	INPUT I RIPPLE RMS [PEAK POWER]			0.97	A	Input capacitor RMS current ripple @ peak load condition
249	CV1 I RIPPLE RMS [PEAK POWER]			5.18	A	CV1 Output RMS ripple current @ peak load condition
251	CV2 I RIPPLE RMS [PEAK POWER]			5.17	A	CV2 output RMS ripple current @ peak load condition
252	LED I RIPPLE RMS [PEAK POWER]			2.68	A	LED output RMS ripple current @ peak load condition
254	**Bias Parameters**					
255	Primary Bias					
256	NB	6		6	turns	Primary bias winding turns
257	V BIAS MIN			9.3	V	Minimum primary bias voltage
258	V BIAS MAX			14.1	V	Maximum primary bias voltage
259	VFD BIAS PRI			0.70	V	Primary bias rectifier voltage forward drop
260	PIV BIAS PRI			55.0	V	Primary bias rectifier peak inverse voltage
261	R BIAS			3.07	kOhms	Bias resistor
262	IBPP MIN			1.40	mA	Bias current at V BIAS MIN
263	IBPP MAX			2.96	mA	Bias current at V BIAS MAX
264	USE OUTPUT OVP	YES		YES		Use output overvoltage protection on primary bias
265	OV ZENER VOLTAGE			12.27	V	Minimum zener voltage
266	VO LED @ OVP			44.81	V	LED output voltage at OVP detection
268	RZ OV			47.00	Ohms	OV resistor
277	**Component Ratings**					
278	Secondary Switches					
279	USE CV1 ZENER CLAMP	Auto		YES		Use zener clamp on CV1 output

280	CV1 ZENER VOLTAGE			11.1	V	CV1 zener clamping voltage
283	SR PRV			31.5	V	Synchronous rectifier maximum peak reverse voltage
284	SR IRMS			5.46	A	Synchronous rectifier RMS current
285	SF CV1			11.1	V	CV1 selection FET maximum peak reverse voltage
298	OBD CV2			77.2	V	CV2 output blocking diode maximum peak reverse voltage
299	OBD VF CV2			1.00	V	CV2 output blocking diode forward voltage drop
301	SF CV2			93.8	V	CV2 output selection FET maximum peak reverse voltage
302	OBD LED			117.8	V	LED blocking diode maximum peak reverse voltage
303	OBD VF LED			1.00	V	LED output blocking diode forward voltage drop
308	Output Capacitors					
309	CV1 Output					
310	CV1 VOUT RIPPLE			1.0	%	CV1 output voltage ripple
311	CV1 VOUT UNDERSHOOT			5.0	%	CV1 output maximum voltage undershoot (at peak power)
312	CV1 COUT NUM			1		CV1 output number of parallel capacitors
316	CV1 COUT			8073	µF	CV1 output capacitor – minimum capacitance per capacitor
317	CV1 COUT VOLTAGE RATING			6.25	V	CV1 output capacitor – minimum voltage rating
318	CV1 COUT ESR			0.7	mOhm	CV1 output capacitor – maximum ESR per capacitor
319	CV1 COUT I RATING			2661	mA	CV1 output capacitor – minimum current rating per capacitor
321	CV2 Output					
332	CV2 VOUT RIPPLE			1.0	%	CV2 output voltage ripple
333	CV2 VOUT UNDERSHOOT			5.0	%	CV2 output maximum transient voltage undershoot (at peak power)
334	CV2 COUT NUM			1		CV2 output number of parallel capacitors
338	CV2 COUT			474	µF	CV2 output capacitor – minimum capacitance per capacitor
339	CV2 COUT VOLTAGE RATING			30.00	V	CV2 output capacitor – minimum voltage rating
340	CV2 COUT ESR			17.7	mOhm	CV2 output capacitor – maximum ESR per capacitor
341	CV2 COUT I RATING			3251	mA	CV2 output capacitor – minimum current rating per capacitor
342	LED Output					
343	LED VOUT RIPPLE			1.0	%	LED output voltage ripple
344	LED VOUT UNDERSHOOT			1.0	%	LED output maximum transient voltage undershoot (at peak power)
345	LED COUT NUM			1		LED output number of parallel capacitors
349	LED COUT			311	µF	LED output capacitor – minimum capacitance per capacitor
350	LED COUT VOLTAGE RATING			45.00	V	LED output capacitor – minimum voltage rating
351	LED COUT ESR			22.9	mOhm	LED output capacitor – maximum ESR per capacitor
352	LED COUT I RATING			2408	mA	LED output capacitor – minimum current rating per capacitor
364	Power Limit					

365	SHOW POWER LIMITS	NO		NO		Display power limit calculations
375	LED Driver Components					
376	R SENSE			166.7	mOhm	LED current sense resistor
377	RDSON MAX LED MOSFET			417	mOhm	Maximum LED MOSFET RDSON
382	Charts					
383	SHOW PLOTS	OFF		OFF		Enable or disable plotting functionality
391	Errors, Warnings, Information					
392	DESIGN_RESULT			Design Passed		Design result status
393	# Design Info			0		Number of design variables whose values might need user attention. Although the design has passed, the user should validate functionality on the bench. Please check the variables listed.
394	# Design Warnings			0		Number of design variables whose values exceed electrical/datasheet specifications.
395	# Design Errors			0		Number of design variables which result in an infeasible design.

10 Boost Inductor Design Spreadsheet

Note: LYTSwitch-6 PIXLS spreadsheet was used for the calculation of boost inductor. The boost inductor was designed at 24.1 W which is the power during light load when SVF is enabled.

1	ACDC_Flyback_PF_LYTSwitch-6_070820; Rev.1.9; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNITS	Switched Valley-Fill Single Stage PFC (SVF S^2PFC)
2	Application Variables					
3	VACMIN	180		180	V	Minimum Input AC Voltage
4	VACNOM	230		230	V	Nominal Input AC Voltage
5	VACMAX	265		265	V	Maximum Input AC Voltage
6	VACRANGE			HIGH LINE		Input Voltage Range
7	FL	50		50	Hz	Line Frequency
8	CIN	100.00		100.00	µF	Minimum Input Capacitance
9	V_CIN			450	V	Input Capacitance Recommended Voltage Rating
10	VO	24.10		24.10	V	Output Voltage
11	IO	1.00		1.00	A	Output Current
12	PO			24.10	W	Total Output Power
13	N			88.00	%	Estimated Efficiency
14	Z			0.50		Loss Allocation Factor
15	Calculations Basis					
16	PARcalcBASIS	VACNOM		VACNOM		Calculated Results Based on Selected VAC - VACNOM, VACMAX, VACMIN or Worst Case only
17	Flyback_Ind_Basis	Nom		Nom		Calculated Results Based on Selected LP - Min = LP_MIN, Nom = LP_NOM, Max = LP_MAX
18	Boost_Ind_Basis	Nom		Nom		Calculated Results Based on Selected LBOOST - Min = LBOOSTMIN, Nom = LBOOSTNOM,Max = LBOOSTMAX
19	Primary Controller Section					
20	DEVICE_MODE	Increased		Increased		Device Current Limit Mode
21	DEVNAME	LYT6079C-H125		LYT6079C-H125		PI Device Name
22	RDSON			0.62	Ohm	Device RDSON at 100degC
23	ILIMITMIN			3.160	A	Minimum Current Limit
24	ILIMITTYP			3.472	A	Typical Current Limit
25	ILIMITMAX			3.784	A	Maximum Current Limit
26	POUT_MAX			85.000	W	Power Capability of the Device based on Thermal Performance
27	BVDSS	Auto		750	V	Peak Drain to Source Breakdown Voltage
28	VDS			2.00	V	On state Drain to Source Voltage
29	VDRAIN			580.77	V	Peak Drain to Source Voltage during Fet turn off
30	Calculated Electrical Parameters Based on Specified Basis					
31	Boost Converter					
32	IBOOSTRMS			286.11	mA	Boost RMS current
33	IBOOSTMAX			1473.44	mA	Boost PEAK current
34	IBOOSTAVG			93.42	mA	Boost AVG current
35	IINRMS			105.77	mA	Input RMS current
36	PF_est			0.9990		Estimated Power Factor
37	Flyback Converter					
38	FSMIN	19650	Warning	19650	Hz	FSMIN must be between 30kHz and 70kHz

39	FSMAX			31117.33	Hz	Maximum Switching Frequency in a Line Period
40	KPmin			4.4174		Minimum KP in a Line Period for VAC specified by PARcalcBASIS
41	IFETRMS			416.04	mA	Fet RMS current
42	IFETMAX			2737.85	mA	Fet PEAK current
43	IPRIRMS			0.3321	A	Primary Winding RMS current
44	IPRIMAX			2.1337	A	Primary Winding PEAK current
45	IPRIAVG			0.0366	A	Primary Winding AVG current
46	IPRIMIN			1176.59	mA	Primary Winding Minimum current
47	ISECRMS			2.86	A	Secondary RMS current
48	ISECMAX			14.21	A	Secondary PEAK current
49	Boost Choke Construction Parameters					
50	RATIO_LBST_LFB	0.8000		0.8000		Boost Inductance and Flyback Primary Inductance Ratio
51	LBOOSTMIN			421.78	µH	Minimum Boost Inductance
52	LBOOSTNOM			468.64	µH	Nominal Boost Inductance
53	LBOOSTMAX			515.51	µH	Maximum Boost Inductance
54	LBOOSTTOL			10.00	%	Boost Inductance Tolerance
55	Boost Core and Bobbin Selection					
56	CR_TYPE_BOOST	EE13		EE13		Boost Core
57	CR_PN_BOOST			PC40EE13-Z		Boost Core Code
58	AE_BOOST			17.10	mm^2	Boost Core Cross Sectional Area
59	LE_BOOST			30.20	mm	Boost Core Magnetic Path Length
60	AL_BOOST			1130.00	nH/turns^2	Boost Core Ungapped Core Effective Inductance
61	VE_BOOST			517.00	mm^3	Boost Core Volume
62	BOBBINID_BOOST			548		Bobbin
63	AW_BOOST			22.20	mm^2	Window Area of Bobbin
64	BW_BOOST			7.40	mm	Bobbin Width
65	MARGIN_BOOST			0.00	mm	Safety Margin Width
66	BOBFILLFACTOR_Boost			74.75	%	Boost Bobbin Fill Factor
67	Boost Winding Details					
68	NBOOST			118.00		Boost Choke Turns
69	BP_BOOST			3767.56	Gauss	Boost Peak Flux Density
70	ALG_BOOST			33.66	nH/turns^2	Boost Core Ungapped Core Effective Inductance
71	LG_BOOST			0.62	mm	Boost Core Gap Length
72	L_BOOST			5.98		Number of Boost Layers
73	AWG_BOOST	28		28		Boost Winding Wire AWG
74	OD_BOOST_INSULATED			0.375	mm	Boost Winding Wire Output Diameter with Insulation
75	OD_BOOST_BARE			0.321	mm	Boost Winding Wire Output Diameter without Insulation
76	CMA_BOOST		Info	526.27	Circular Mils/A	CMA_BOOST is above recommended upper limit of 500 CMA
77	Flyback Transformer Construction Parameters					
78	VOR	136.00		136.00	V	Secondary Voltage Reflected in the Primary Winding
79	LP_MIN			527.22	µH	Minimum Flyback Inductance
80	LP_NOM			585.80	µH	Nominal Flyback Inductance
81	LP_MAX			644.38	µH	Maximum Flyback Inductance
82	LP_TOL			10.00	%	Flyback Inductance Tolerance
83	Flyback Core and Bobbin Selection					
84	CR_TYPE	PQ26/25		PQ26/25		Flyback Core
85	CR_PN			PQ26/25-3F3		Flyback Core Code
86	AE			120.00	mm^2	Flyback Core Cross Sectional Area
87	LE			54.30	mm	Flyback Core Magnetic Path Length

88	AL			4390.00	nH/turns^2	Flyback Core Ungapped Core Effective Inductance
89	VE			6530.00	mm^3	Flyback Core Volume
90	BOBBINID			PQ26X25		Flyback Bobbin
91	AW			47.50	mm^2	Flyback Window Area of Bobbin
92	BW			13.60	mm	Flyback Bobbin Width
93	MARGIN			0.00	mm	Safety Margin Width
94	Flyback Winding Details					
95	NP			61.00		Primary Turns
96	BP			3431.07	Gauss	Flyback Peak Flux Density
97	BM			2611.28	Gauss	Flyback Maximum Flux Density
98	BAC			853.79	Gauss	Flyback AC Flux Density
99	ALG			157.43	nH/turns^2	Flyback Core Ungapped Core Effective Inductance
100	LG			0.92	mm	Flyback Core Gap Length
101	L			2.00		Number of Flyback Layers
102	NB			6.00		Bias Turns
103	NS			11.00		Secondary Turns

11 Flyback Transformer (T2) Specification

11.1 Electrical Diagram

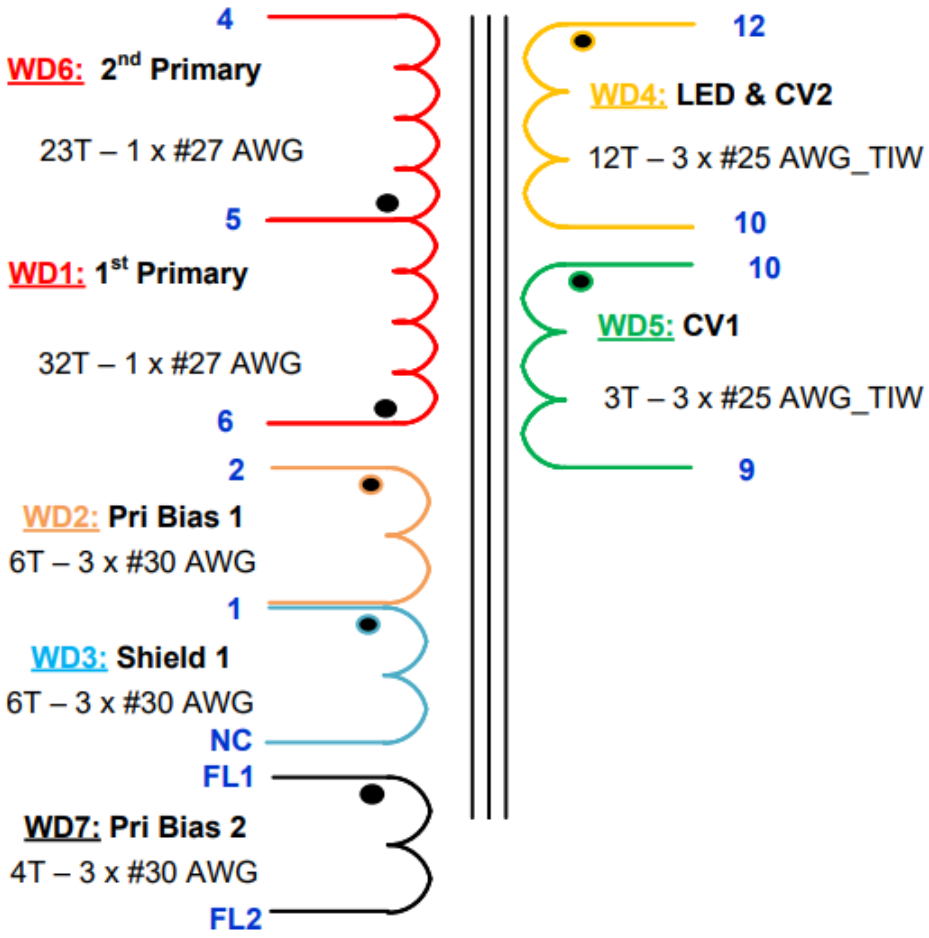


Figure 10 – Transformer Schematic.

11.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 4 and 6, with all other windings open.	580.6 µH ± 5%
Resonant Frequency	Between pin 4 and 6, other windings open	100 kHz (min)
Primary Leakage Inductance	Measure inductance across Pin 4-6, other windings shorted	6 µH (Max.)

11.3 Materials

Item	Description
[1]	Core: PC95
[2]	Bobbin: PQ26/25, 12 pins, 6pri, 6sec, PI#: 25-01149-00
[3]	Magnet wire: #27 AWG, double coated.
[4]	Magnet wire: #30 AWG, double coated.
[5]	TIW: #25 AWG
[6]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 13 mm Width.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 11.5 mm Width.
[8]	Varnish: Dolph BC-359.

11.4 Transformer Build Diagram

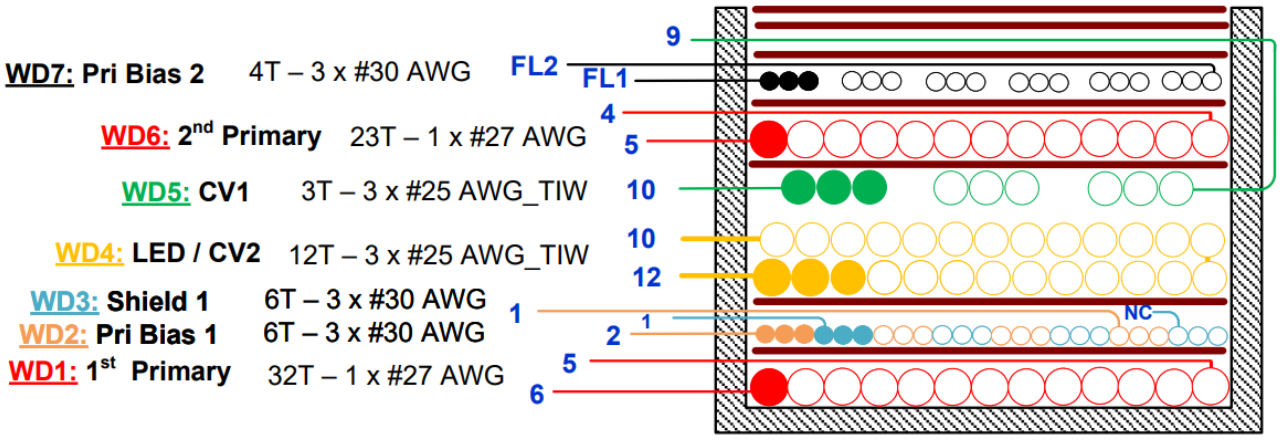
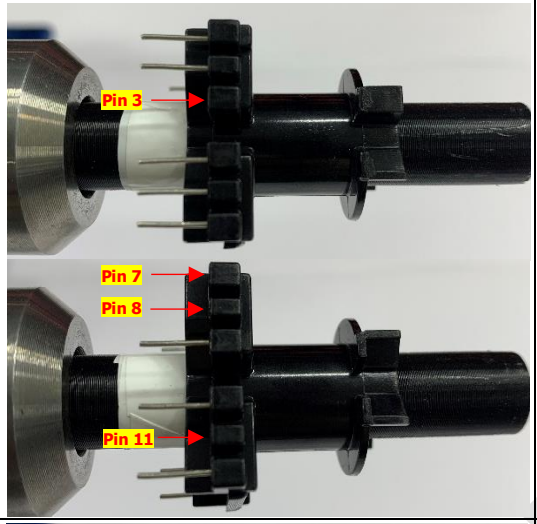
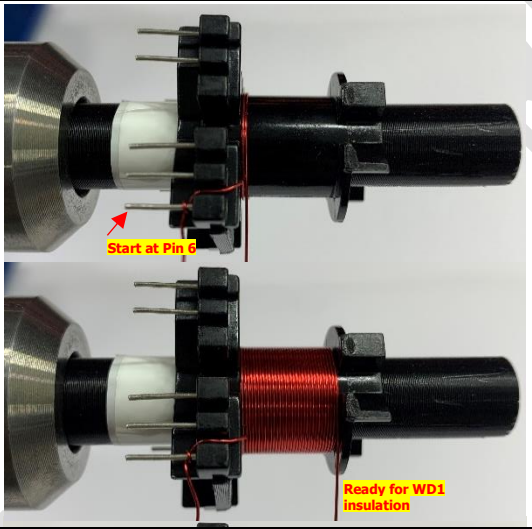
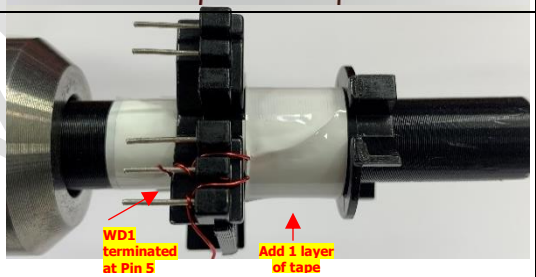
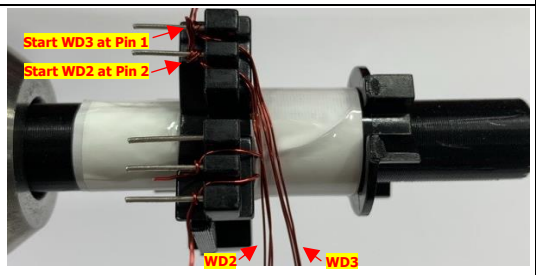
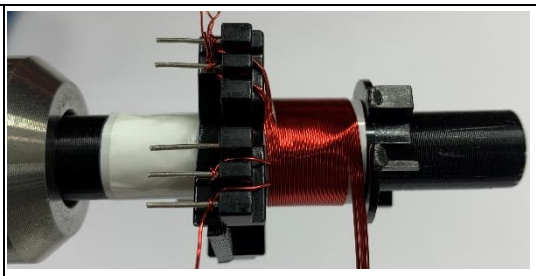
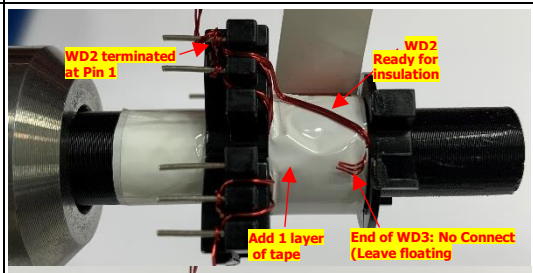
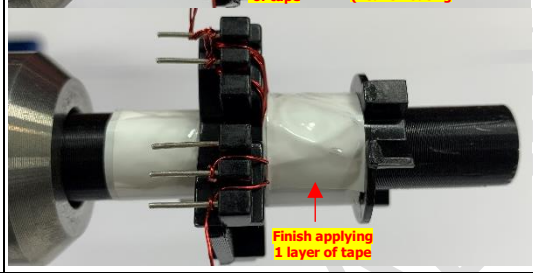
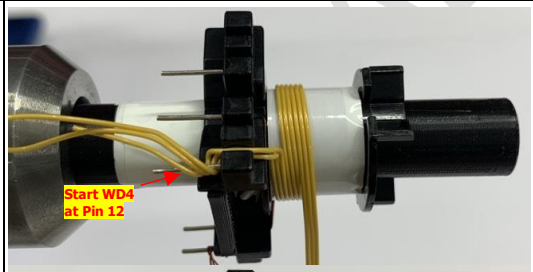
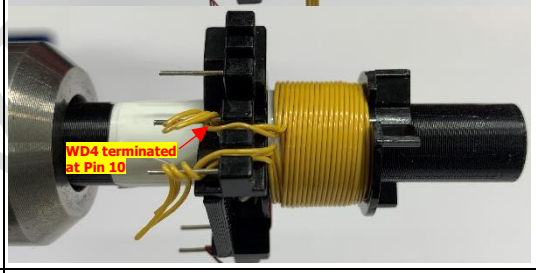
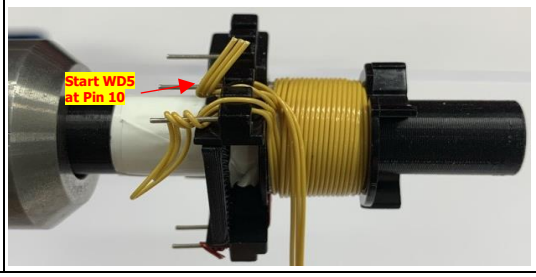
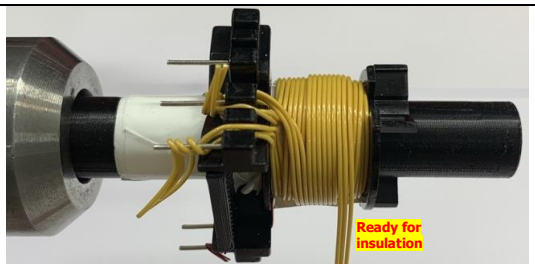
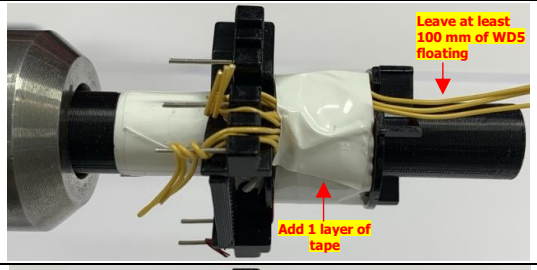
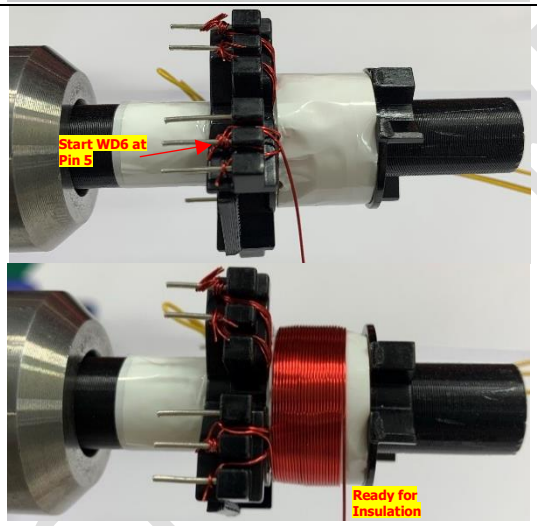
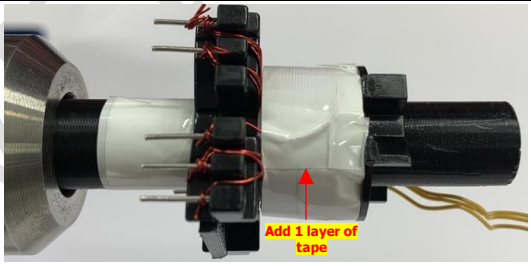
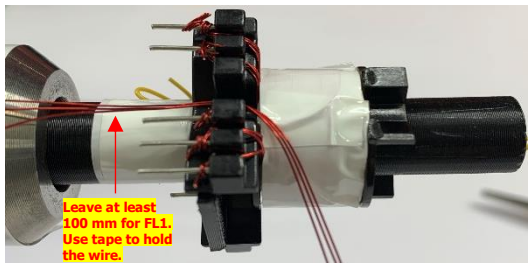


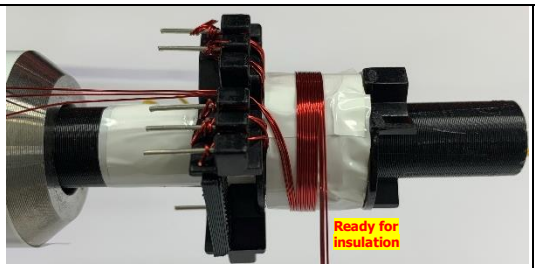
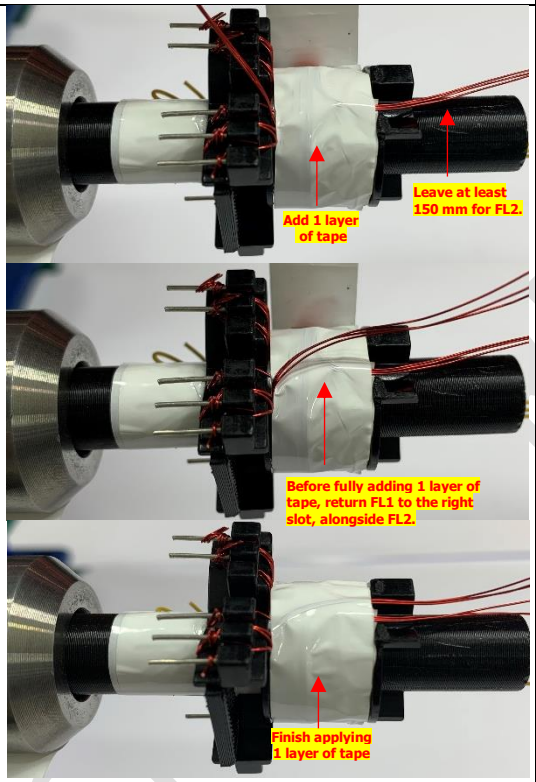
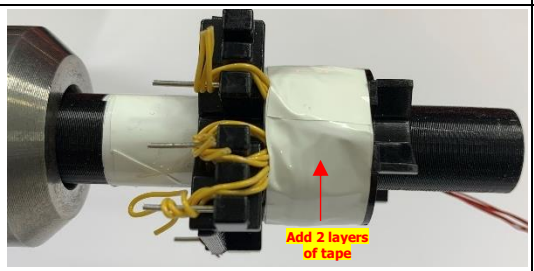
Figure 11 – Transformer Build Diagram.

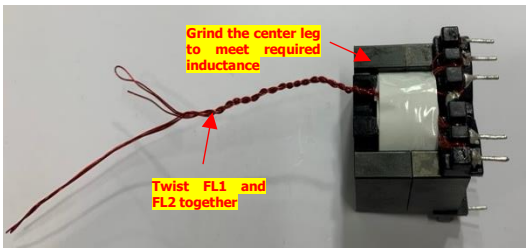
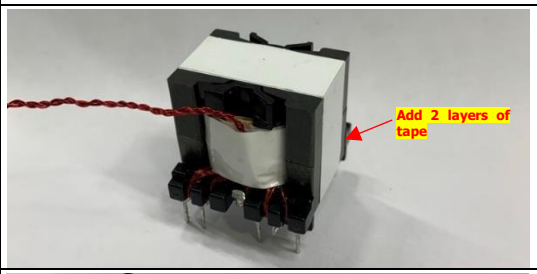
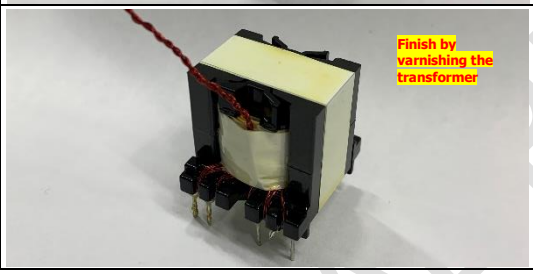
11.5 Winding Illustrations

Bobbin Preparation		Use PQ26/25 bobbin Item [2]. Position bobbin on the winding jig such that pin 1-12 is on the left side. Winding direction is clockwise. Remove terminal pins 3, 7, 8 and 11.
WD1 1st Primary		Use AWG #27 magnet wire Item [3] long enough for WD1 and WD6. Starting at pin 6, wind 32 turns, with tight tension, from left to right, for 1 layer. At the last turn of WD1, bring the wire back to left and terminate it to Pin 5.
Insulation		Apply 13 mm Item [6] 1-layer polyester tape for insulation.
WD2: Primary Bias 1 & WD3: Shield 1		Use 3 wires item [4] start at pin 2 for Bias winding, also use 3 wires same item [4] start at pin 1 for Shield1 winding. Wind all 6 wires in parallel, at the 6th turn: - Bring 3 wires for Bias winding to the left and terminate at pin 1,

		- For Shield 1 winding, cut short 3 wires as No-Connect.
Insulation	 	Apply 13 mm Item [6] 1-layer polyester tape for insulation.
WD4: LED/CV2 Secondary	 	Use AWG #25 TIW Item [5]. Prepare trifillar wire of AWG #25 TIW Item [5] for WD4 and WD5. Using 3 wires of AWG #25 TIW Item [5], start at pin 12 wind 12 turns in 2 layers, from left to right and then right to left. Finish winding at pin 10.
WD5: CV1 Secondary		Use AWG #25 TIW Item [5]. Using 3 wires of AWG #25 TIW Item [5], start at pin 10 wind 3 turns in 1 layer, from left to right.

		
Insulation		Apply 13 mm Item [6] 1-layer polyester tape for insulation, make sure it is not too tight. At the last turn of WD5, exit at the right slot of the bobbin and leave at least 100 mm of wires floating for WD5 termination.
WD6: **2nd Primary**		Use AWG #27 magnet wire Item [3]. Starting at pin 5, wind 23 turns, from left to right, for 1 layer. At the last turn of WD6, bring the wire back to left and terminate it to Pin 4.
Insulation		Apply 13 mm Item [6] 1-layer polyester tape for insulation.
WD7: Pri Bias 2		Use 3 wires item [4]. Before starting to wind, secure FL1 on the left slot of the bobbin by using tape, leaving a 100 mm wire for FL1. Mark the wire as FL1 for identification.

		Starting at the slot on the left side of the bobbin, wind 4 turns from left to right.
Insulation		Apply 13 mm Item [6] 1-layer polyester tape for insulation. At the last turn of WD7, exit wire to the right slot of the bobbin and mark it as FL2. Return FL1 to the right slot, alongside FL2.
WD5 Termination		Use AWG #25 TIW Item [5] that was set aside on the left from WD5. Terminate WD5 to Pin 9.
Insulation		Apply 13 mm Item [6] 2-layer polyester tape for insulation.

Gap Core and Install		Use PQ26/25 Core Item [1]. Grind the center leg of the ferrite evenly to meet the required inductance. Twist FL1 and FL2 with total length of at least 100 mm.
Core Insulation		Apply 11.5 mm Item [7] 2 - layer polyester tape at the perimeter of the core.
Varnish		Dip the whole transformer in a pure varnish solution Item [8] for 10 minutes. Cure the varnished transformer in hot (100 ºC) oven for 30 minutes.

12 Boost Inductor (T3) Specification

12.1 Electrical Diagram

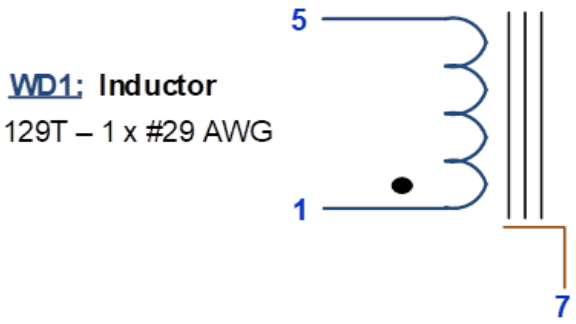


Figure 12 – Electrical Diagram.

12.2 Electrical Specification

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and 5	468.64 µH ± 5%

12.3 Materials

Item	Description
[1]	Transformer Bobbin: Bobbin, EE13, Vertical, 10 pins, 25-01023-00
[2]	Transformer Core: Magnetic Core, EE13, PC40
[3]	Magnet Wire: #29 AWG.
[4]	Bus Wire: #30 AWG, Alpha Wire, Tinned Copper
[5]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 8 mm Width.
[6]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 4 mm Width.
[7]	Varnish: Dolph BC-359.

12.4 Inductor Winding Diagram

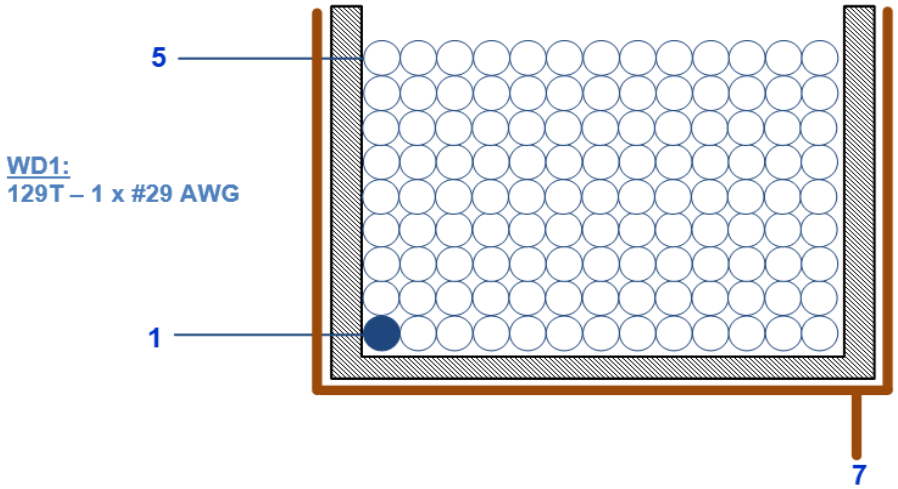
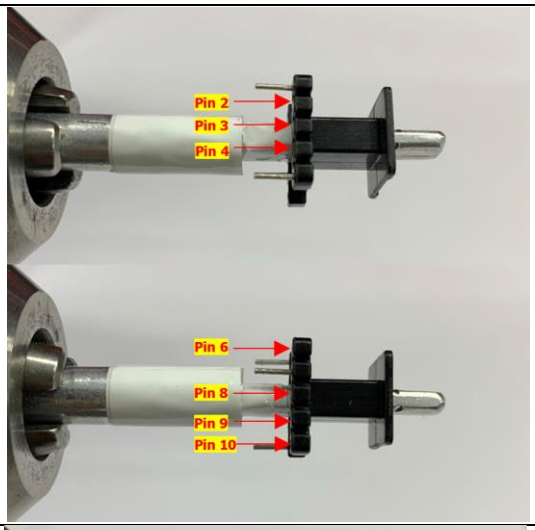
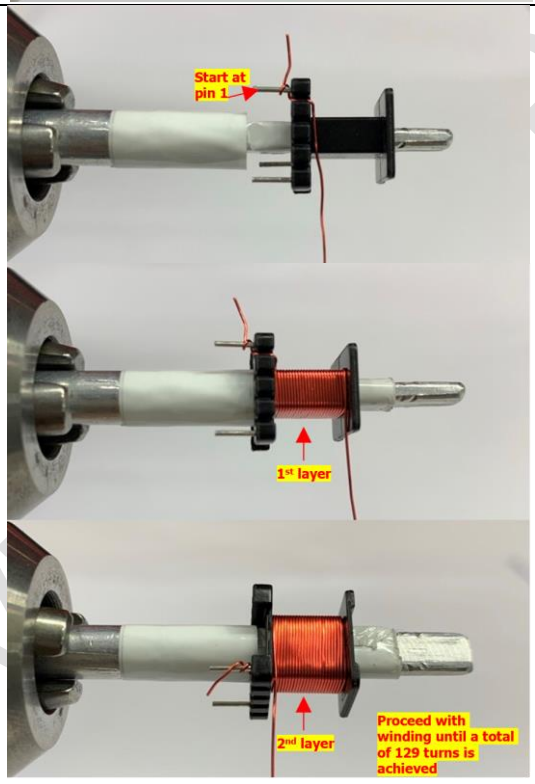
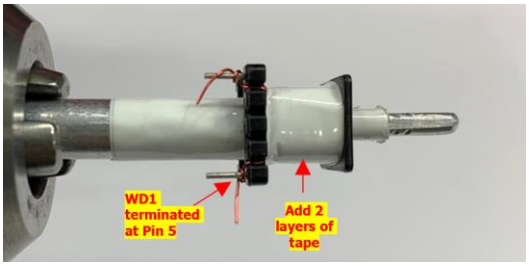
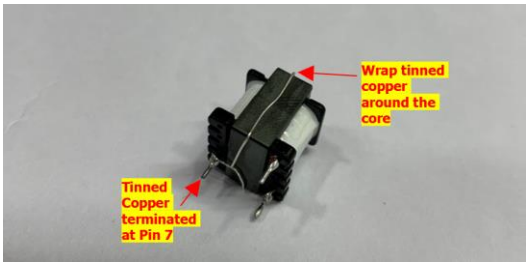
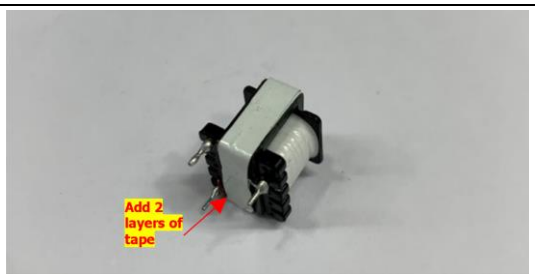


Figure 13 – Inductor Build Diagram.

12.5 Inductor Winding Illustration

Bobbin Preparation		Use EE13 bobbin Item [1]. Position bobbin on the winding jig such that pin 1-10 is on the left side. Winding direction is clockwise. Remove terminal pins 2, 3, 4, 6, 8, 9 and 10.
WD1: Inductor		Use AWG #29 magnet wire Item [3] long enough for WD1. Starting at pin 1, wind 129 turns, from left to right and right to left for 6 layers. At the last turn of WD1, bring the wire back to left and terminate it to Pin 5.
Insulation		Apply 8 mm Item [5] 2-layer polyester tape for insulation.

Core Termination		Prepare a copper strip, Item [4}. Wrap a copper strip around the core and terminate the magnetic wire at Pin 7.
Core Tape		Apply 4 mm Item [6] 2-layer polyester tape for insulation.
Varnish		Dip the whole inductor in a pure varnish solution Item [7] for 10 minutes. Cure the varnished transformer in hot (100 ºC) oven for 30 minutes.

13 Differential Mode Filter Inductor (T1) Specification

13.1 Electrical Diagram

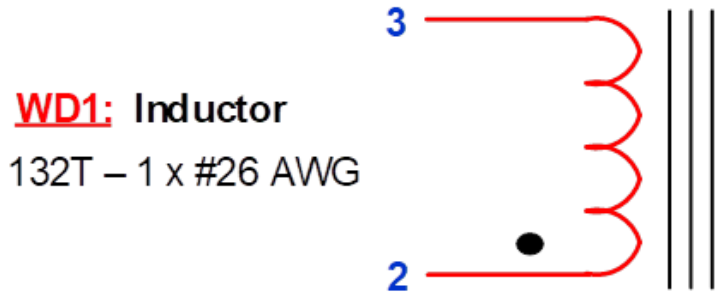


Figure 14 – Electrical Diagram.

13.2 Electrical Specification

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 2 and 3	3.01 mH ± 5%

13.3 Materials

Item	Description
[1]	Transformer Bobbin: Bobbin, ATQ21/16.8 Vertical, 5 pins, 25-01181-00
[2]	Transformer Core: Magnetic Core, ATQ21, 99-00088-00
[3]	Magnet Wire: #26 AWG.
[4]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 10 mm Width.
[5]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 6 mm Width.
[6]	Varnish: Dolph BC-359.

13.4 Winding Diagram

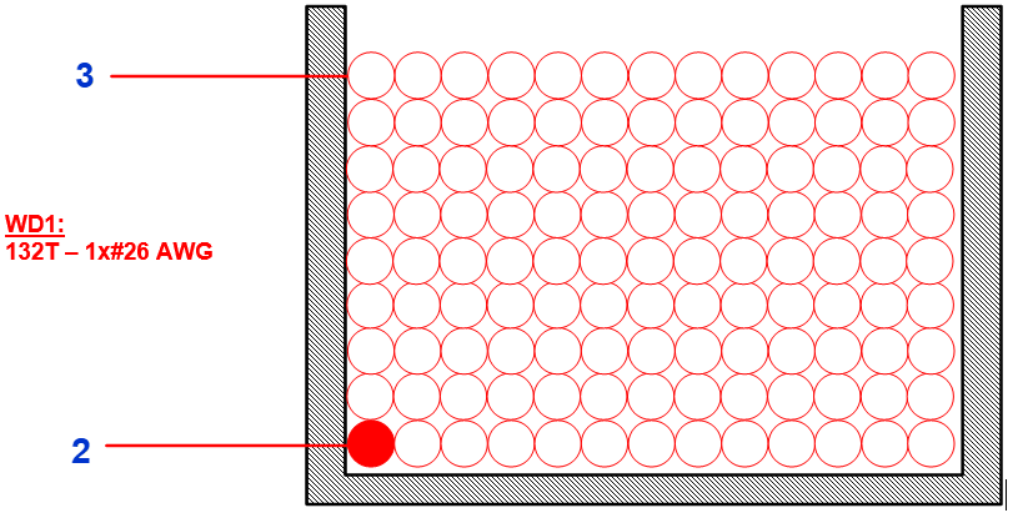
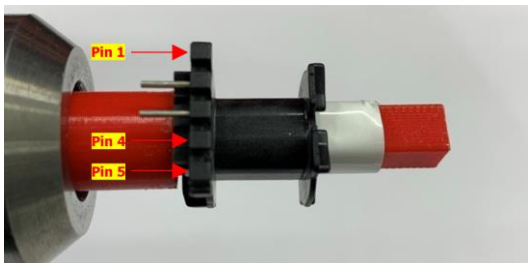
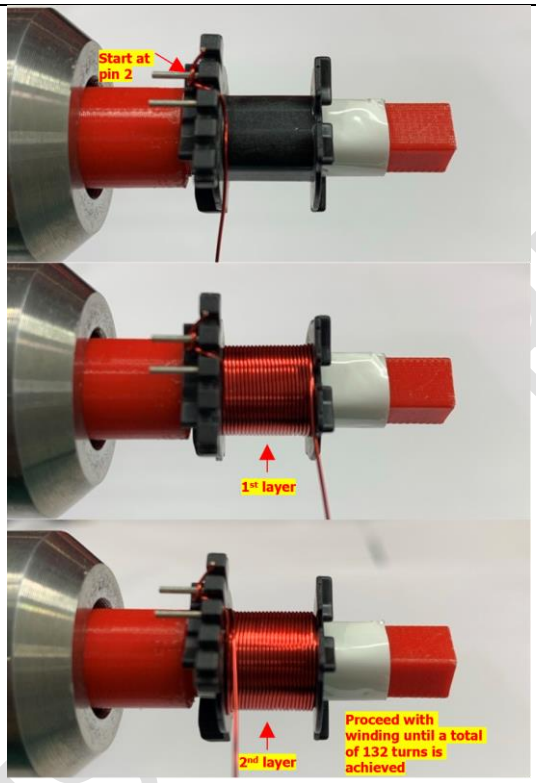
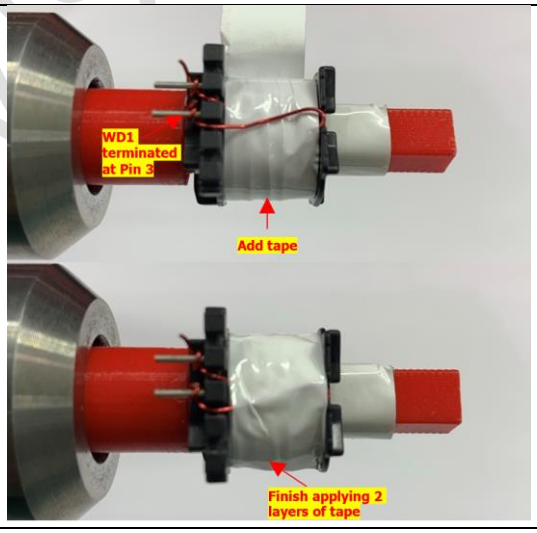
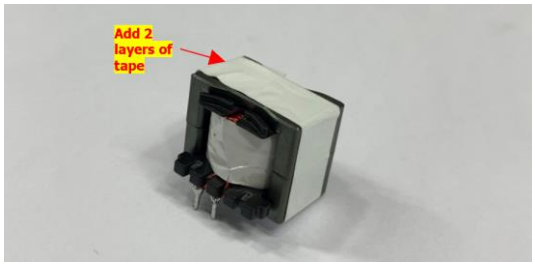
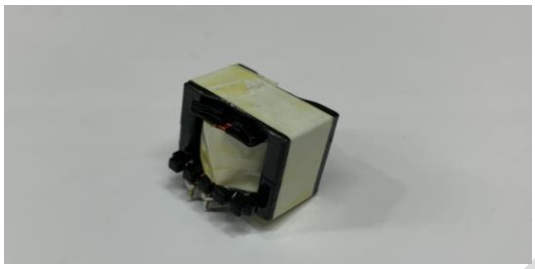


Figure 15 – Inductor Build Diagram.

13.5 Inductor Winding Illustration

Bobbin Preparation		Use ATQ21/16.8 bobbin Item [1]. Position bobbin on the winding jig such that pin 1-5 is on the left side. Winding direction is clockwise. Remove terminal pins 1, 4 and 5.
WD1: Inductor		Use AWG #26 magnet wire Item [3] long enough for WD1. Starting at pin 2, wind 132 turns, from left to right and right to left for 7 layers. At the last turn of WD1, bring the wire back to left and terminate it to Pin 3.
Insulation		Apply 10 mm Item [4] 2-layer polyester tape for insulation.

Core Tape		Apply 6 mm Item [5] 2-layer polyester tape for insulation.
Varnish		Dip the whole inductor in a pure varnish solution Item [6] for 10 minutes. Cure the varnished transformer in hot (100 ºC) oven for 30 minutes.

14 Common Mode Choke (L6) Specification

14.1 Electrical Diagram

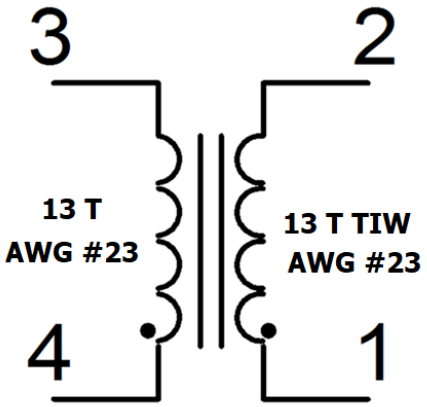


Figure 16 – Inductor Electrical Diagram.

14.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 1 and pin 2 or pin 3 and pin 4 with all other windings open.	550 µH ±20%

14.3 Materials List

Item	Description
[1]	Toroid Core: 32-00315-00 (Green Color)
[2]	Magnet Wire: #23 AWG.
[3]	TIW Wire: #23 AWG.

14.4 Inductor Build Diagram

Figure 17 – Inductor Build Diagram.

14.5 Inductor Construction

Winding 1 - Wind 13 turns of item 2 and 3 in bifilar wound as shown in figure 17.

15 Secondary Heat Sink

15.1 Secondary Heat Sink Sheet Metal

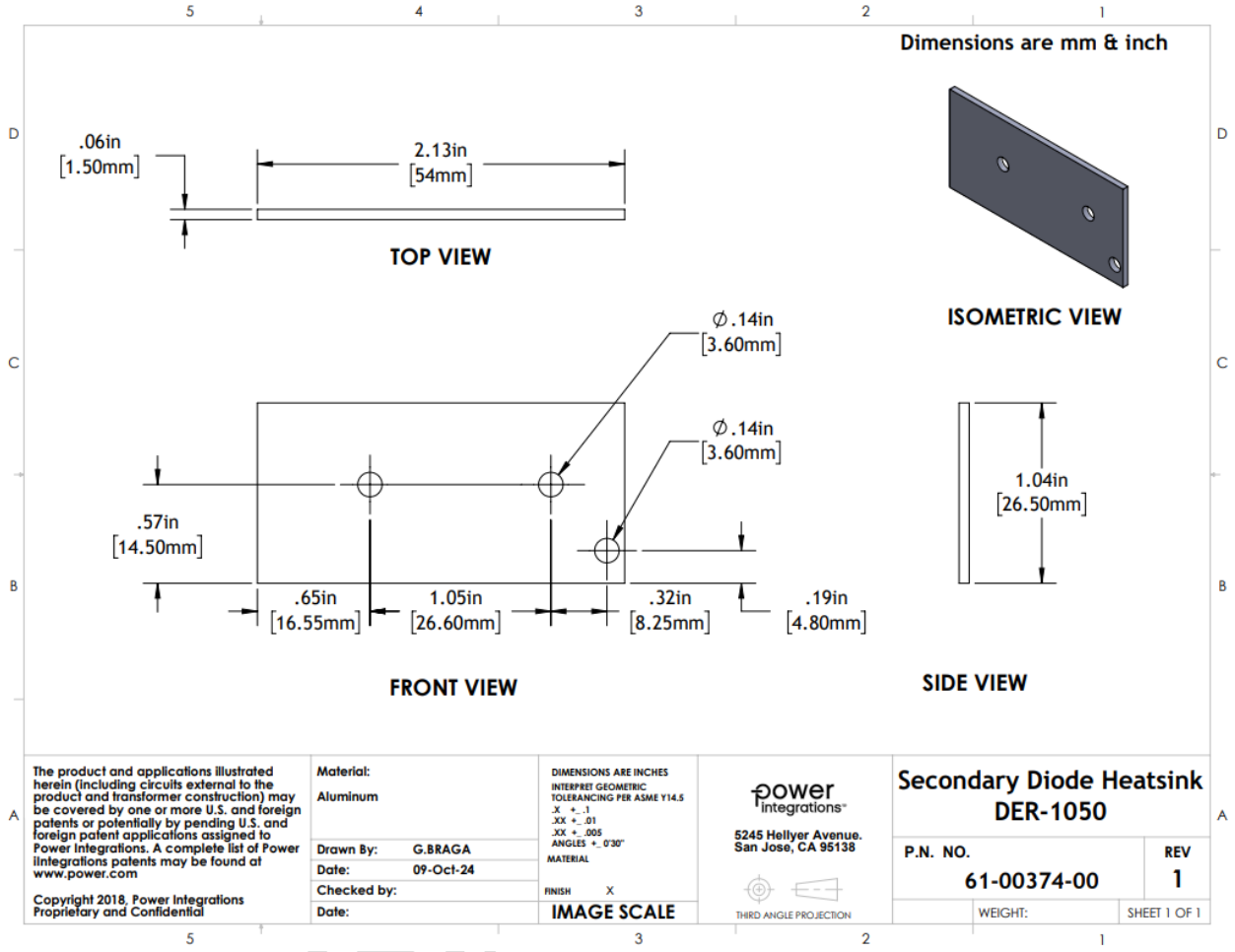
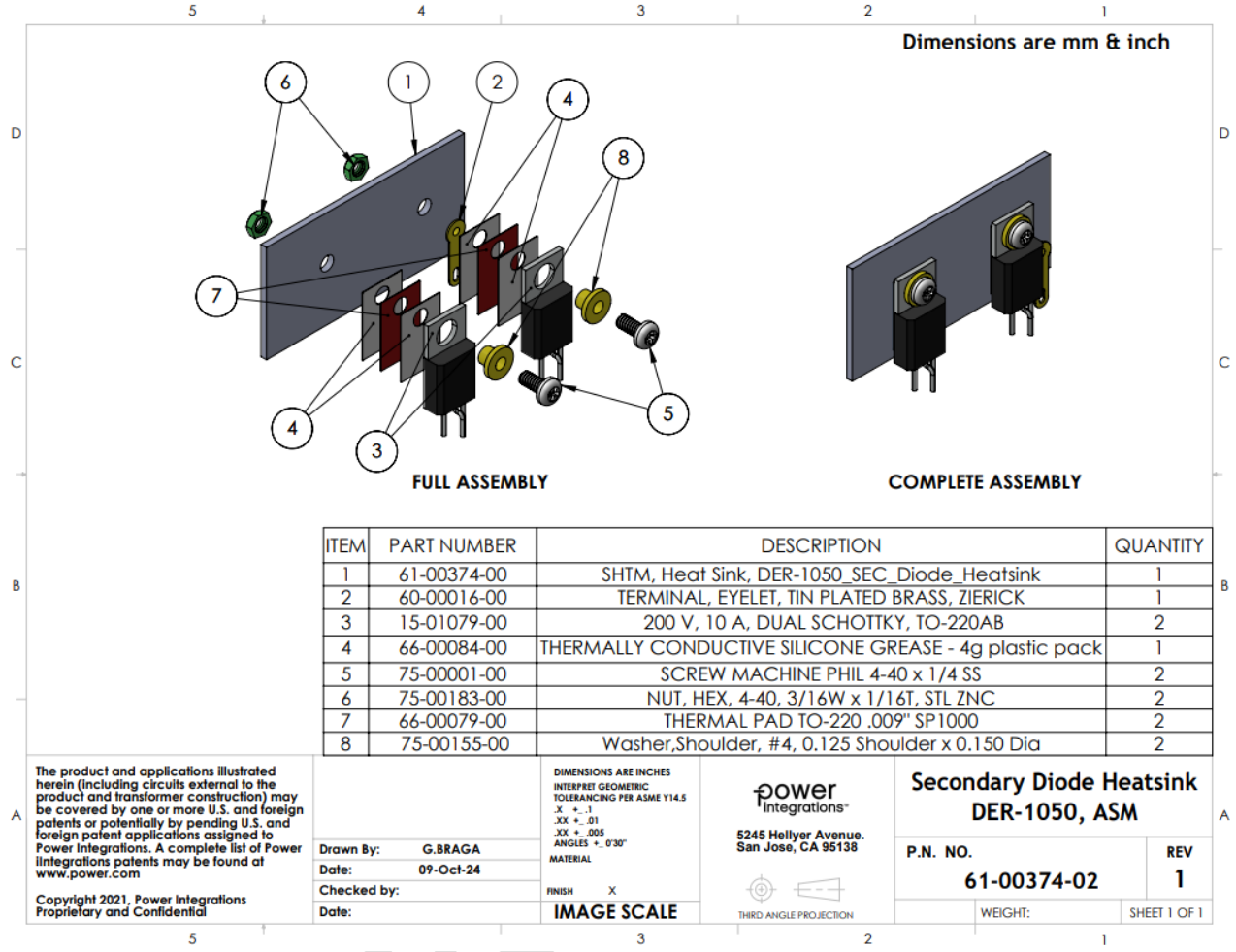


Figure 18 – Secondary Heat Sink Drawing.

15.2 Secondary Heat Sink Assembly



ITEM	PART NUMBER	DESCRIPTION	QUANTITY
1	61-00374-00	SHTM, Heat Sink, DER-1050_SEC_Diode_Heatsink	1
2	60-00016-00	TERMINAL, EYELET, TIN PLATED BRASS, ZIERICK	1
3	15-01079-00	200 V, 10 A, DUAL SCHOTTKY, TO-220AB	2
4	66-00084-00	THERMALLY CONDUCTIVE SILICONE GREASE - 4g plastic pack	1
5	75-00001-00	SCREW MACHINE PHIL 4-40 x 1/4 SS	2
6	75-00183-00	NUT, HEX, 4-40, 3/16W x 1/16T, STL ZNC	2
7	66-00079-00	THERMAL PAD TO-220 .009" SP1000	2
8	75-00155-00	Washer,Shoulder, #4, 0.125 Shoulder x 0.150 Dia	2

Drawn By: G.BRAGA
Date: 09-Oct-24
Checked by:
Date:

DIMENSIONS ARE INCHES
INTERPRET GEOMETRIC TOLERANCING PER ASME Y14.5
.X +-.1
.XX +-.01
.XX +-.005
ANGLES +-.0'30"
MATERIAL
FINISH X
IMAGE SCALE

power integrations
5245 Hellyer Avenue.
San Jose, CA 95138
THIRD ANGLE PROJECTION

Secondary Diode Heatsink
DER-1050, ASM
P.N. NO. 61-00374-02
REV 1
WEIGHT:
SHEET 1 OF 1

Figure 19 – Secondary Heat Sink Drawing.

16 Performance Data

Performance data was measured at room temperature, with voltages taken on the input and output terminals of the PCB unless noted otherwise.

16.1 Efficiency

The efficiency test was conducted on power supply under the following test conditions:

- Input line voltages: 180 VAC, 200 VAC, 230 VAC, 240 VAC, 265 VAC
- During SVF Disabled (LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A, CV1: 5 V / 0.5 A)
- During SVF Enabled (LED: 36 V / 0.6 A, CV2: 24 V / 0 A, CV1: 5 V / 0.5 A)

The results are presented in figures 20 and 21.

16.1.1 Full Load Efficiency vs Input Voltage, SVF Disabled

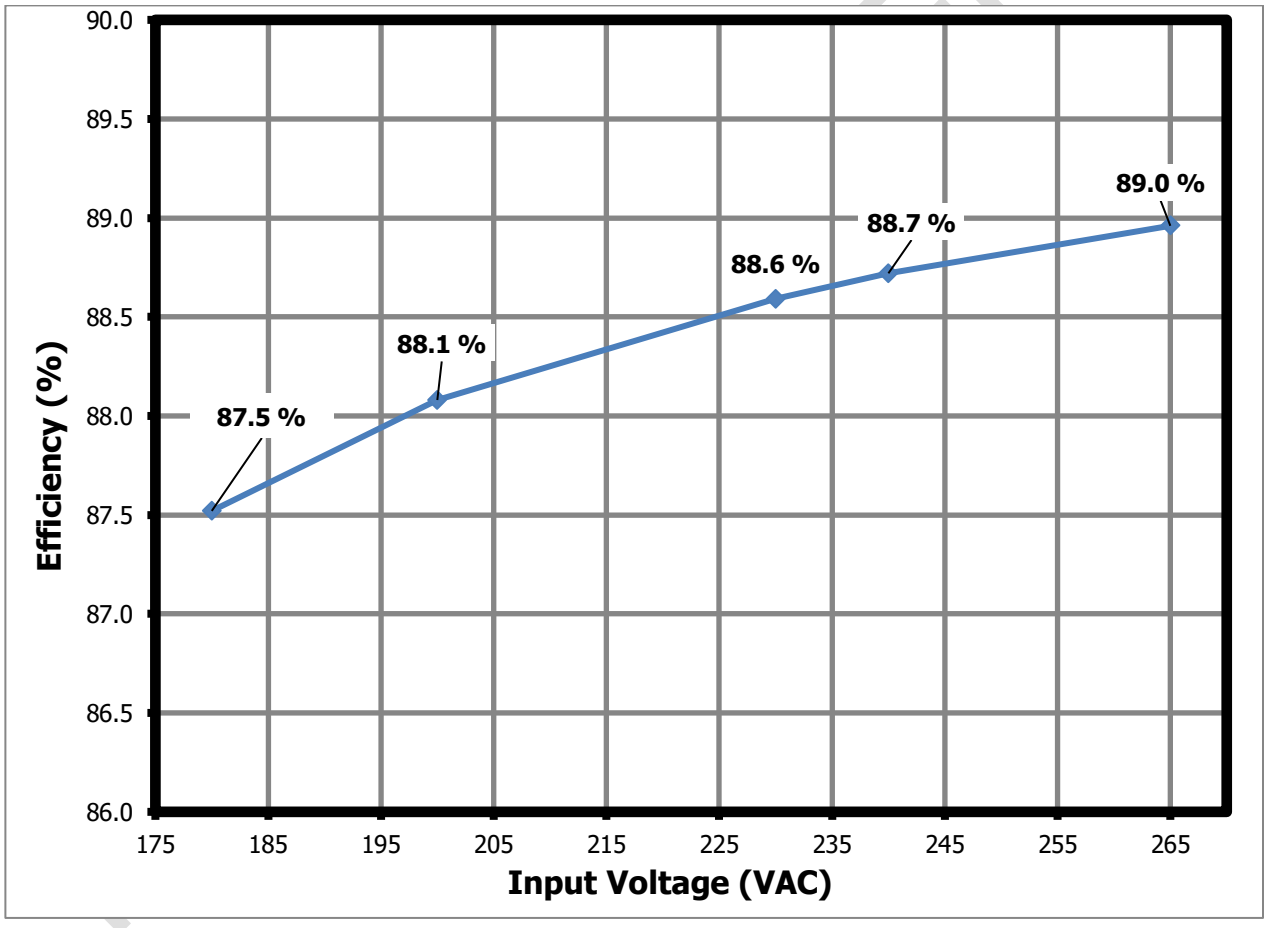


Figure 20 – Full Load Efficiency vs. Input Line Voltage, SVF Disabled.

16.1.2 Efficiency vs Input Voltage, SVF Enabled

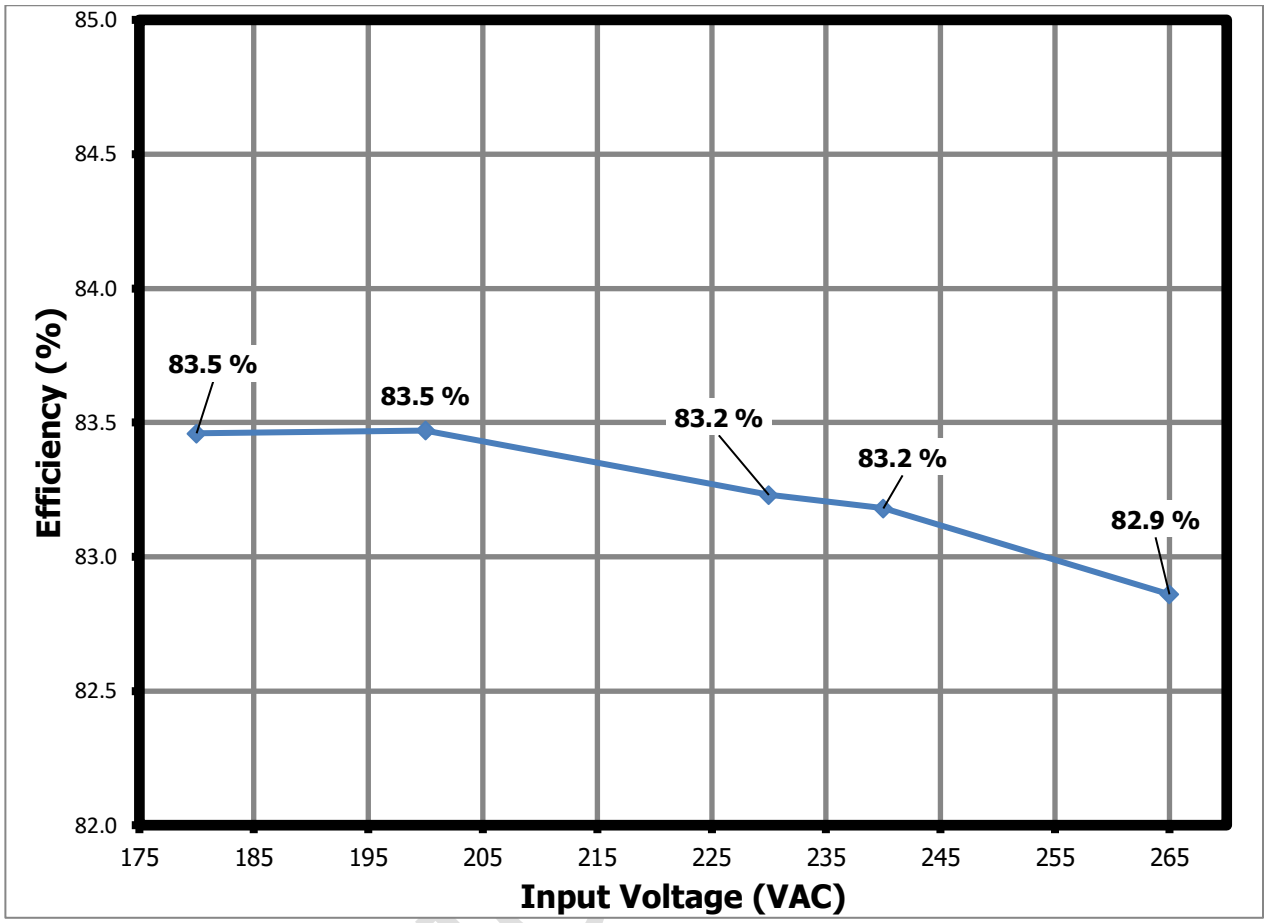


Figure 21 – Efficiency vs. Input Line Voltage, SVF Enabled.

16.1.3 Efficiency vs Output Load, SVF Disabled

The efficiency vs. load measurements are shown below. Results were obtained for all combinations of:

- Input line voltages: 180 V, 230 V, 265 V
- LED full current of 600 mA with 11 steps for each line voltage
- CV1 full current of 0.5 A with 11 steps for each line voltage
- CV2 full current of 2.4 A with 11 steps for each line voltage

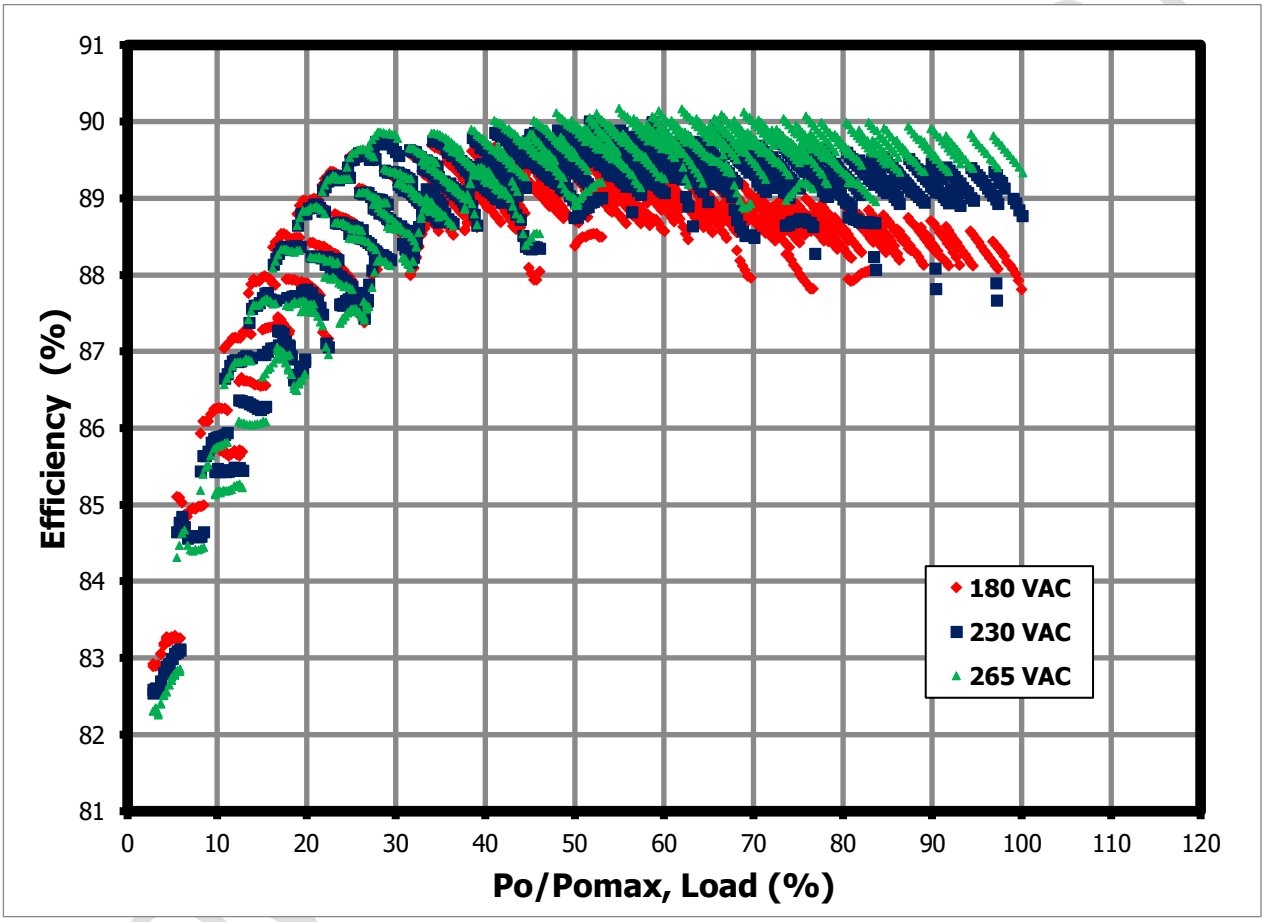


Figure 22– Efficiency vs Load, SVF Disabled.

16.2 Power Factor

16.2.1 Power Factor vs Input Line Voltage, SVF Enabled (P_{OUT} = 24.1 W)

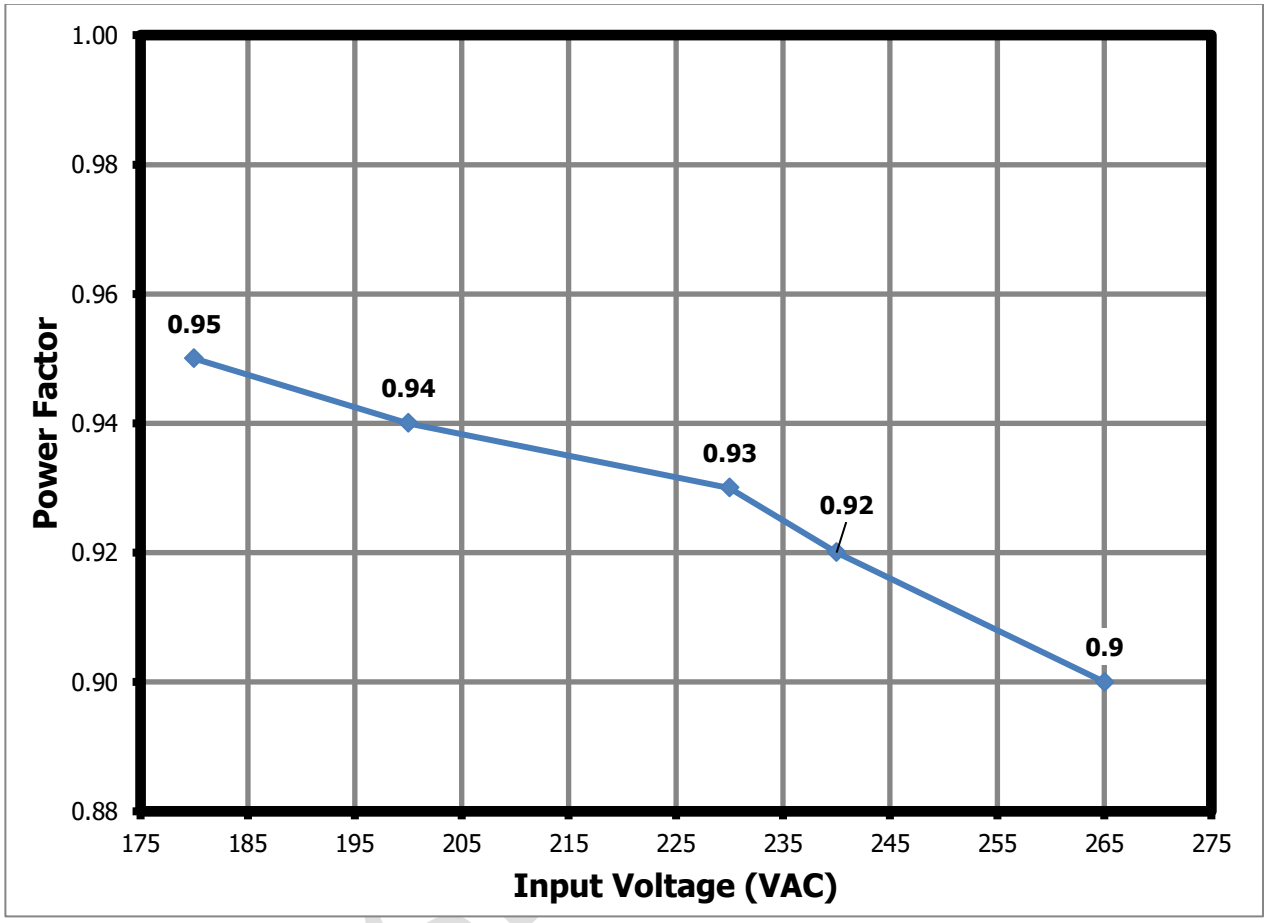


Figure 23 – Power Factor vs Input Line, SVF Enabled, P_{OUT} = 24.1 W.

16.3 Total Harmonic Distortion (THD)

16.3.1 Total Harmonic Distortion (THD) vs Input Line, SVF Enabled (P_{OUT} = 24.1 W)

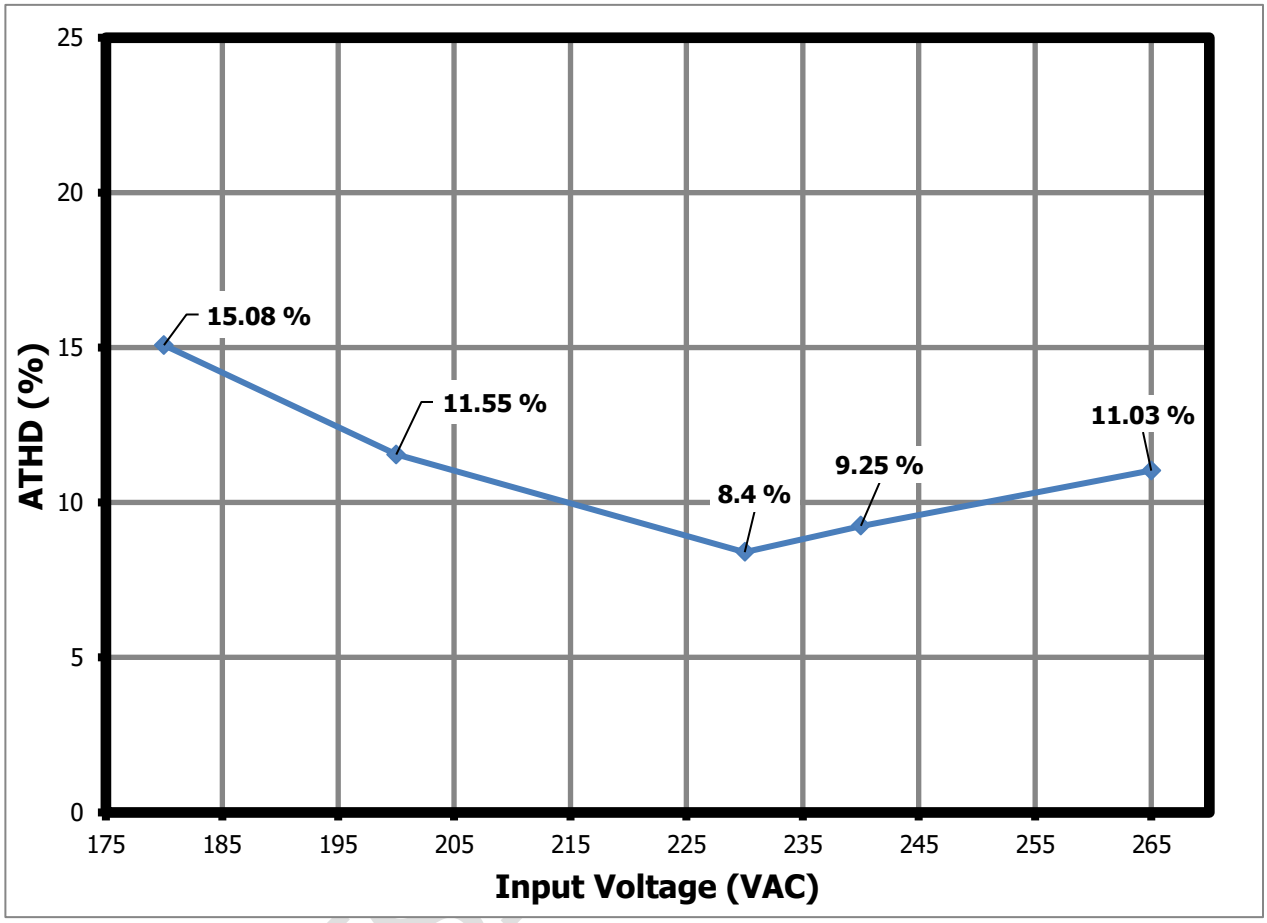


Figure 24 – THD vs Input Line, SVF Enabled, P_{OUT} = 24.1 W.

16.4 Output Voltage Regulation

16.4.1 Output Voltage Regulation vs Input Line at Full Load, SVF Disabled

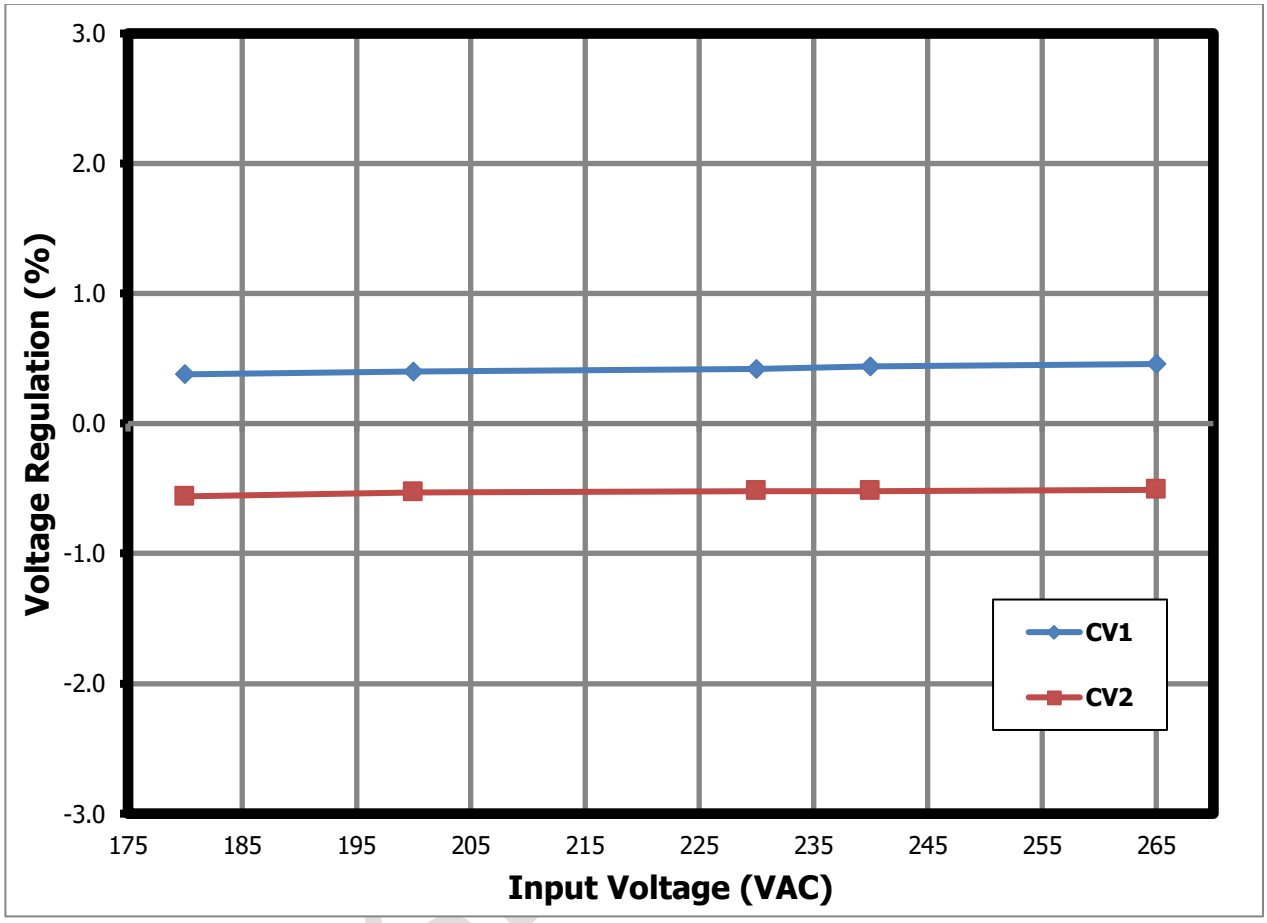


Figure 25 – Output Voltage Regulation vs Input Line, SVF Disabled.

16.4.2 Output Voltage Regulation vs Input Line, SVF Enabled

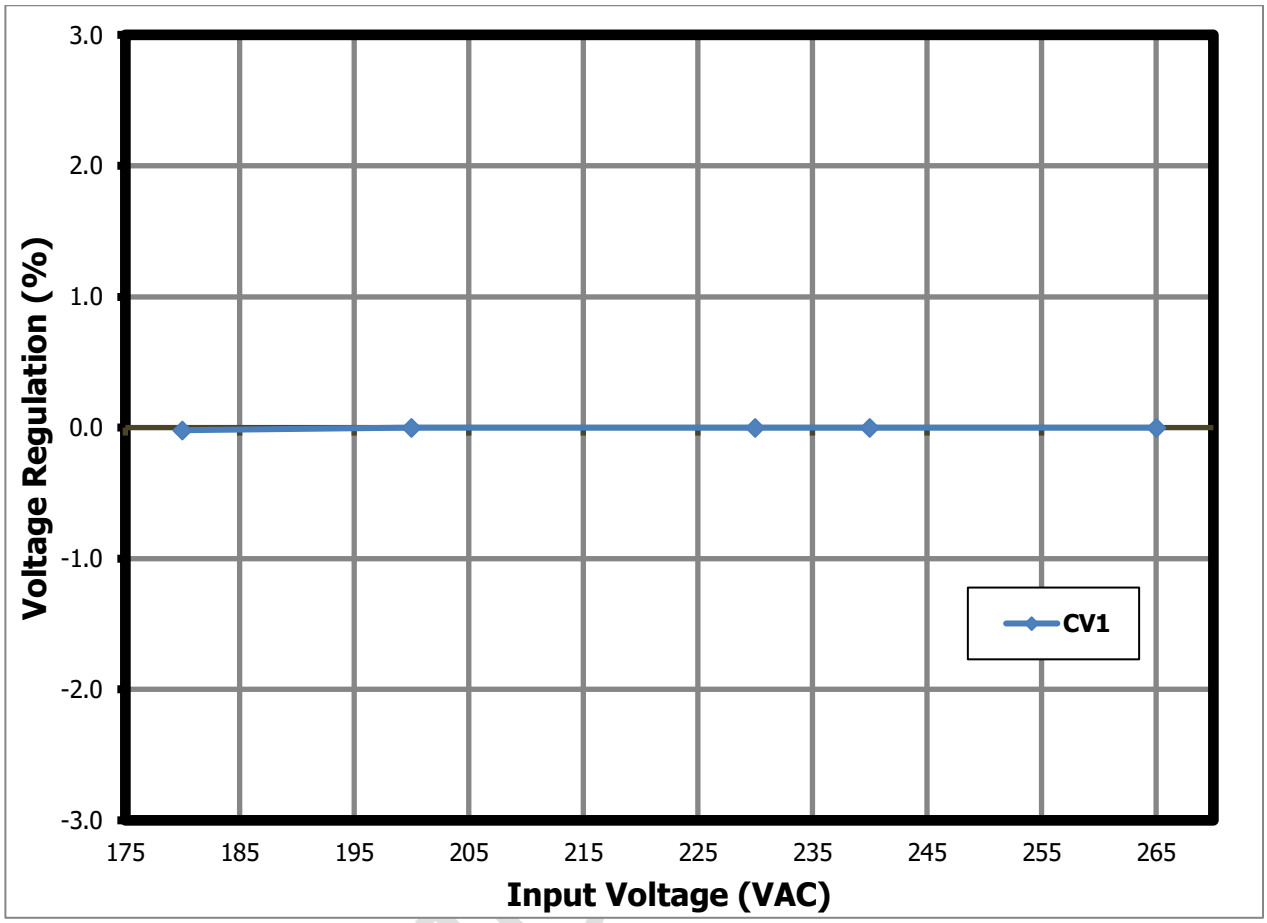


Figure 26 – Output Voltage Regulation vs Input Line, SVF Enabled.

16.4.3 Output Current Regulation vs Input Line at Full Load, SVF Disabled

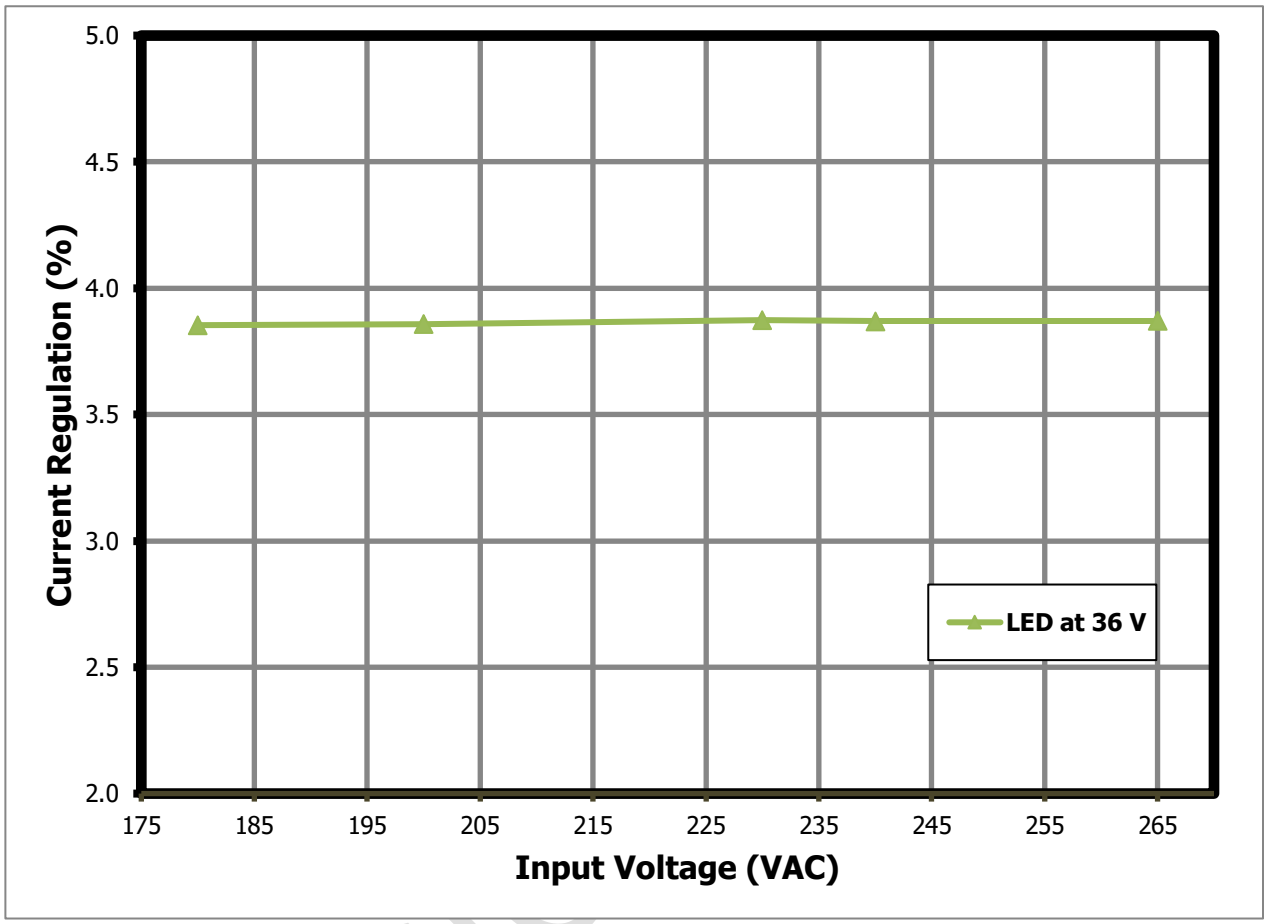


Figure 27 – Output Current Regulation vs Input Line, SVF Disabled.

16.4.4 Output Current Regulation vs Input Line, SVF Enabled

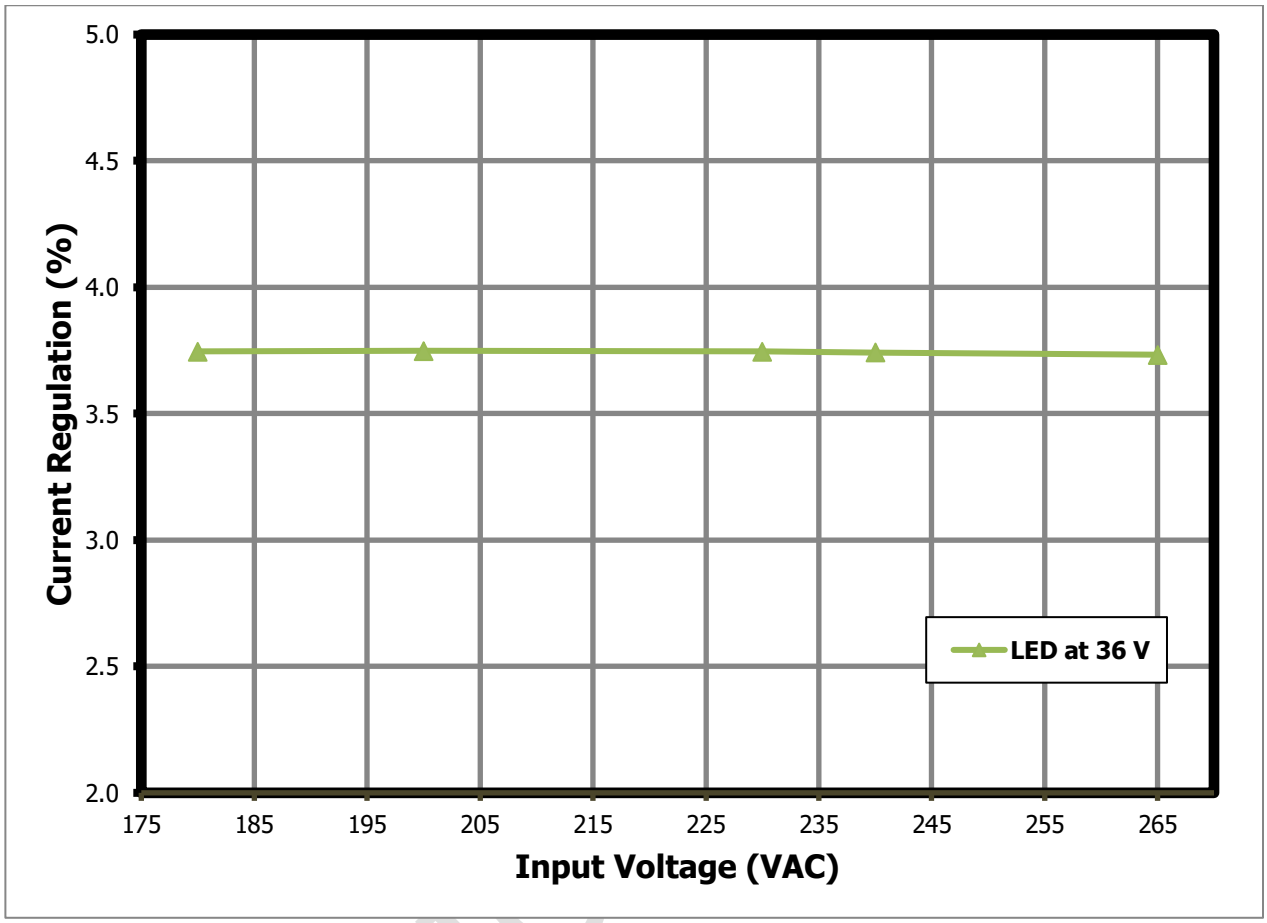


Figure 28 – Output Current Regulation vs Input Line, SVF Enabled.

16.4.5 Output Voltage Regulation vs Output Power

The output regulation was measured for both CV output. The current at the CV outputs and LED output was increased from 0% to 100% of its rating in 11 steps. The test was conducted under the following conditions:

- Input line voltages: 180 VAC, 230 VAC, 265 VAC
- During SVF Disabled (LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A, CV1: 5 V / 0.5 A)

The results for CV outputs are presented in figures 29 and 30.

16.4.5.1 CV1 Output Voltage Regulation vs Output Power, SVF Disabled

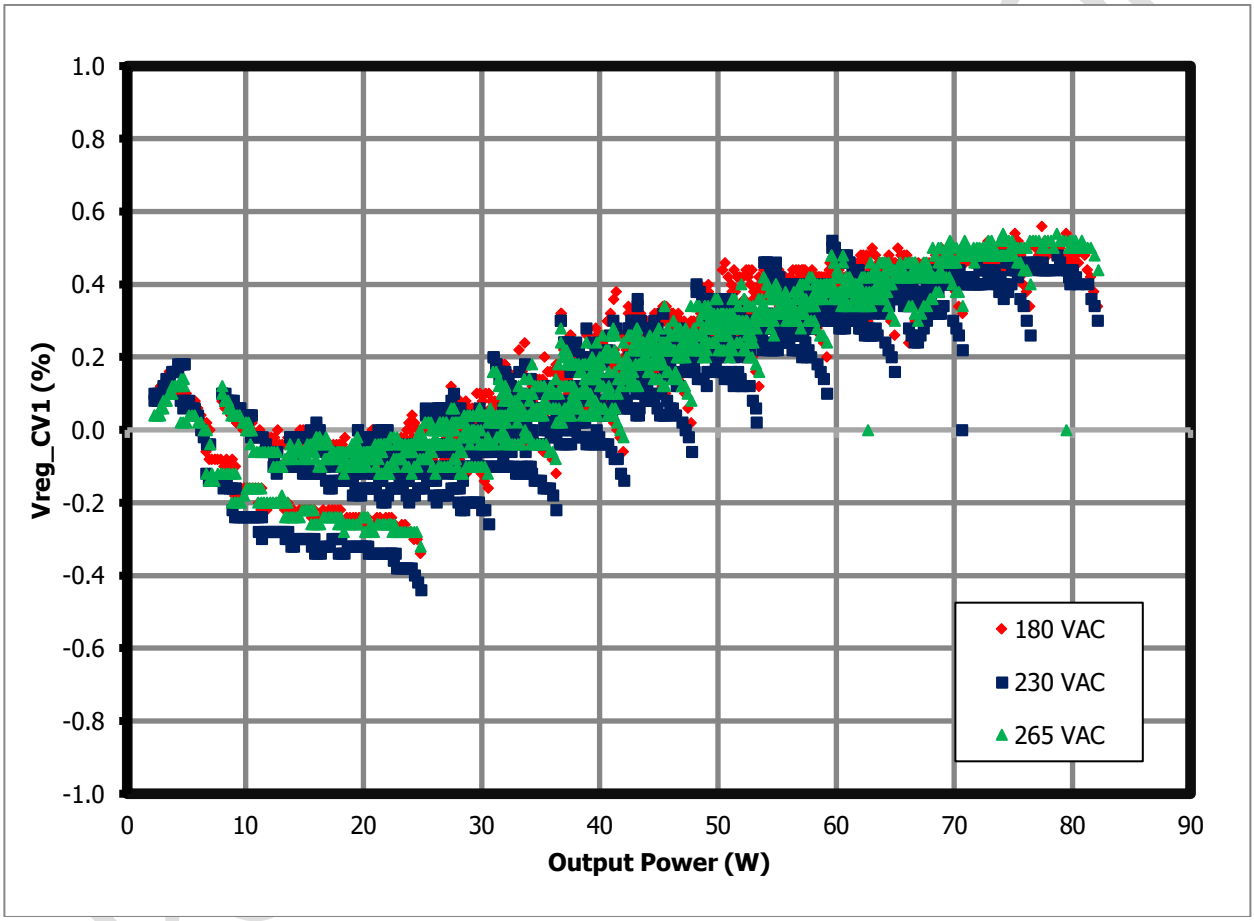


Figure 29 – VCV1 Output Voltage Regulation vs. Output Power, SVF Disabled.

16.4.5.2 CV2 Output Voltage Regulation vs Output Power, SVF Disabled

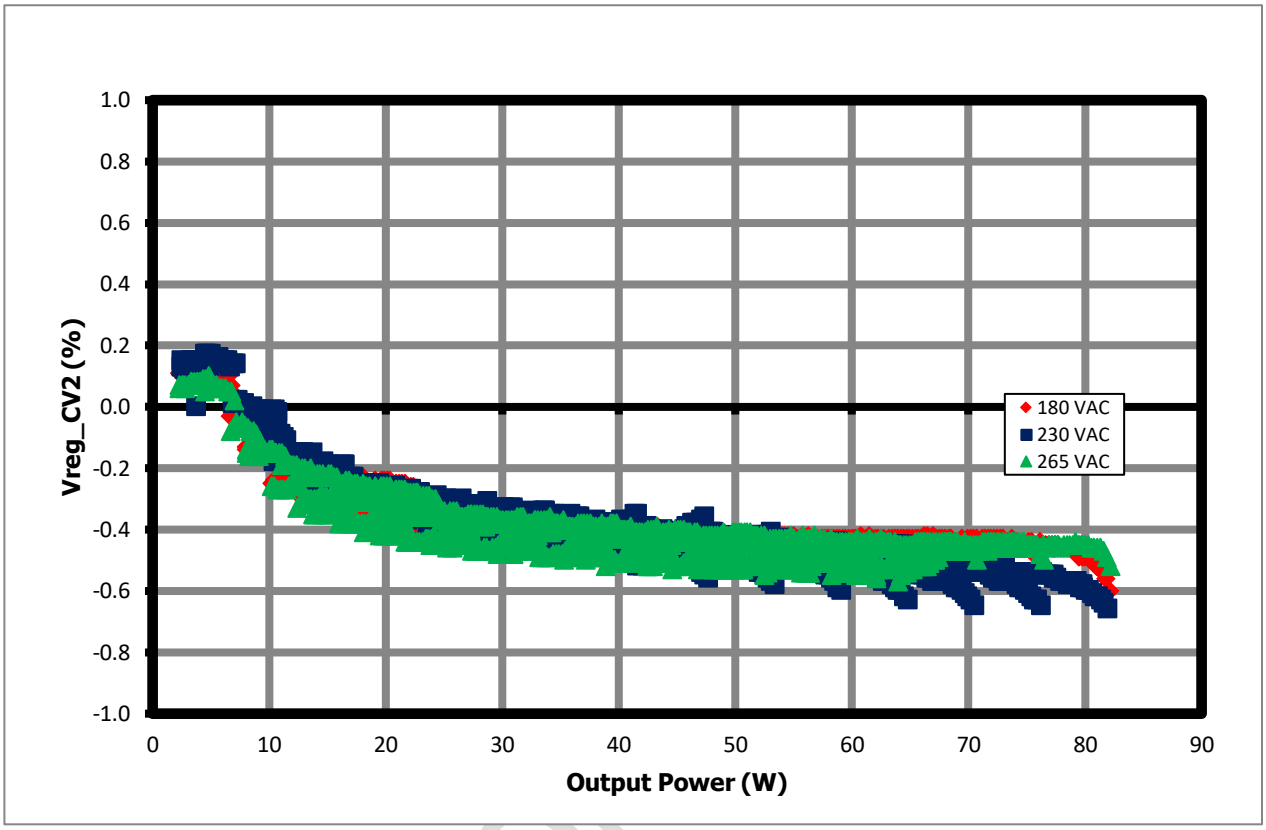


Figure 30 – VCV2 Output Voltage Regulation vs. Output Power, SVF Disabled.

16.5 No-Load Input Power

No-load input power was measured using a Yokogawa WT310E power meter. The power meter was set to its no-load measurement setting to gather the data shown in Figure 31. The no-load input power test was conducted on the power supply under the following test conditions:

- Input line voltages: 180 VAC, 200 VAC, 220 VAC, 230 VAC, 240 VAC, 265 VAC
- During SVF Disabled (LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A, CV1: 5 V / 0.5 A)
- During SVF Enabled (LED: 36 V / 0.6 A, CV2: 24 V / 0 A, CV1: 5 V / 0.5 A)

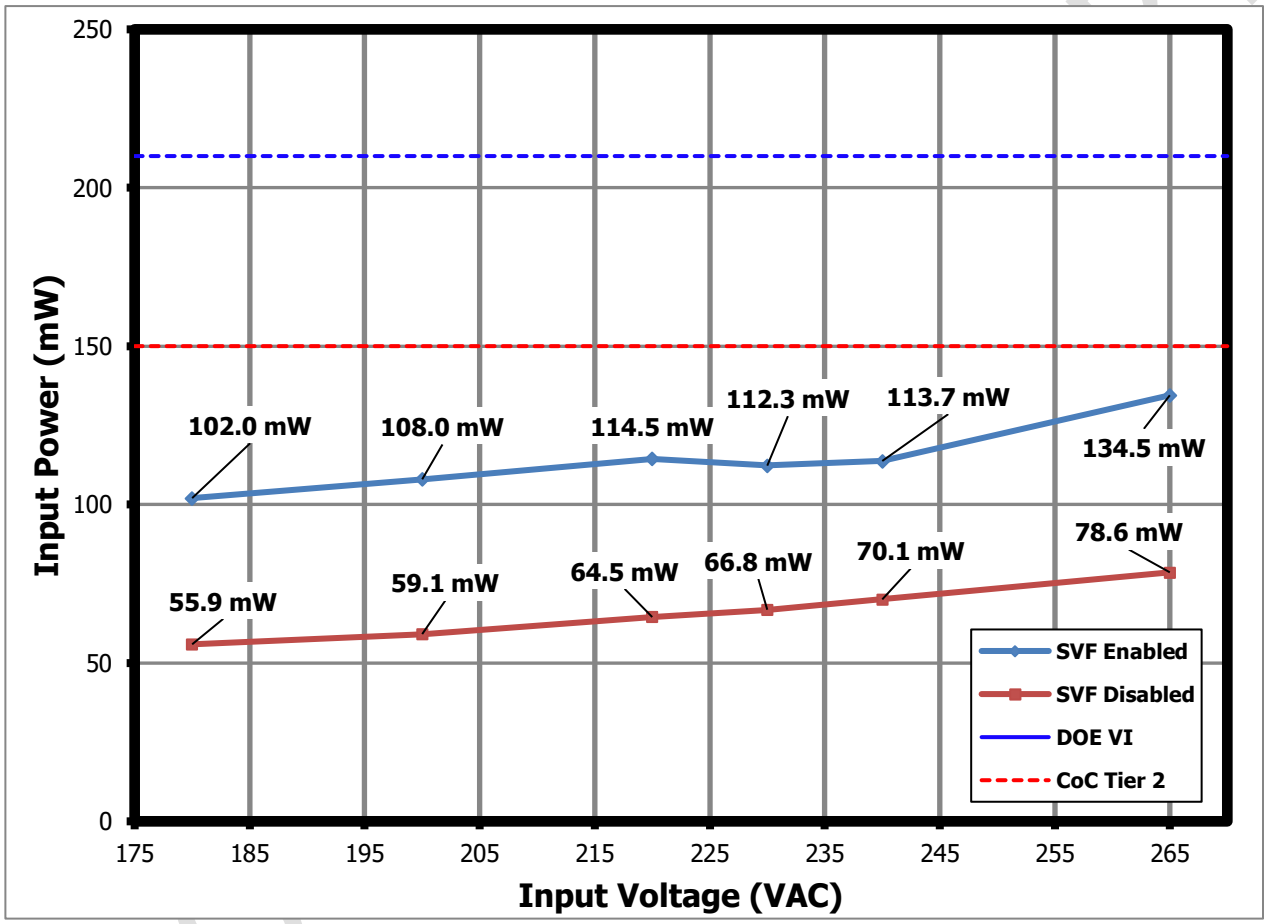


Figure 31 – No-Load Input Power.

16.6 Line Input Harmonic Content

Harmonic content was measured on the power supply under the following test conditions:

- Input line voltage: 230 VAC
- During SVF Enabled
  - **Test 1:** LED + CV1, LED: 36 V / 0.6 A, CV2: 24 V / 0 A, CV1: 5 V / 0.5 A
  - **Test 2**: LED only, LED: 36 V / 0.6 A, CV2: 24 V / 0 A, CV1: 5 V / 0 A

16.6.1 Test 1: LED + CV1, Line Frequency Harmonic Content, SVF Enabled

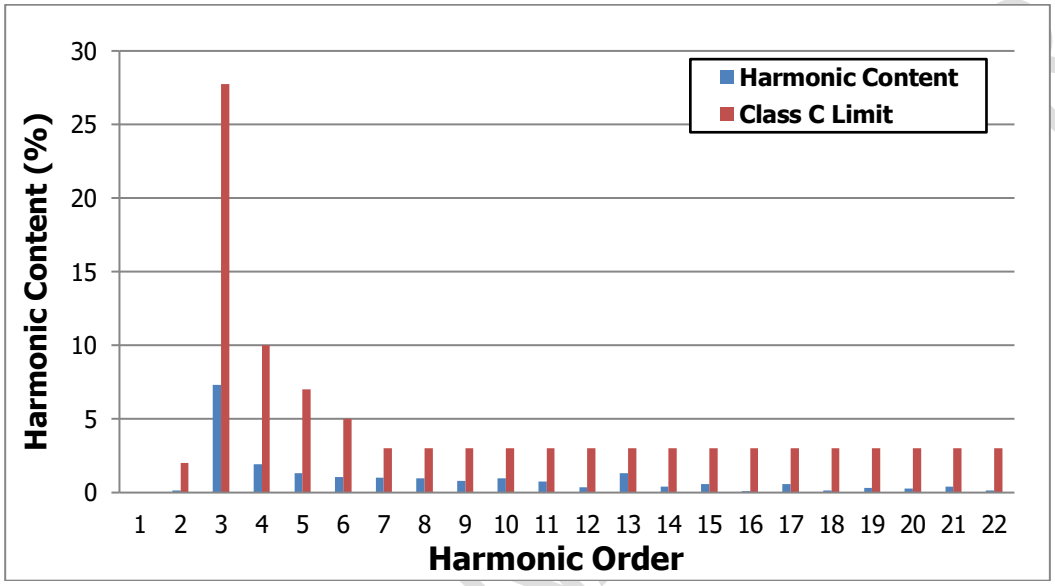


Figure 32 – Harmonic Content, SVF Enabled, P_{OUT} = 24.1 W, Test 1, 230 VAC.

16.6.1 Test 2: LED only, Harmonic Content, SVF Enabled

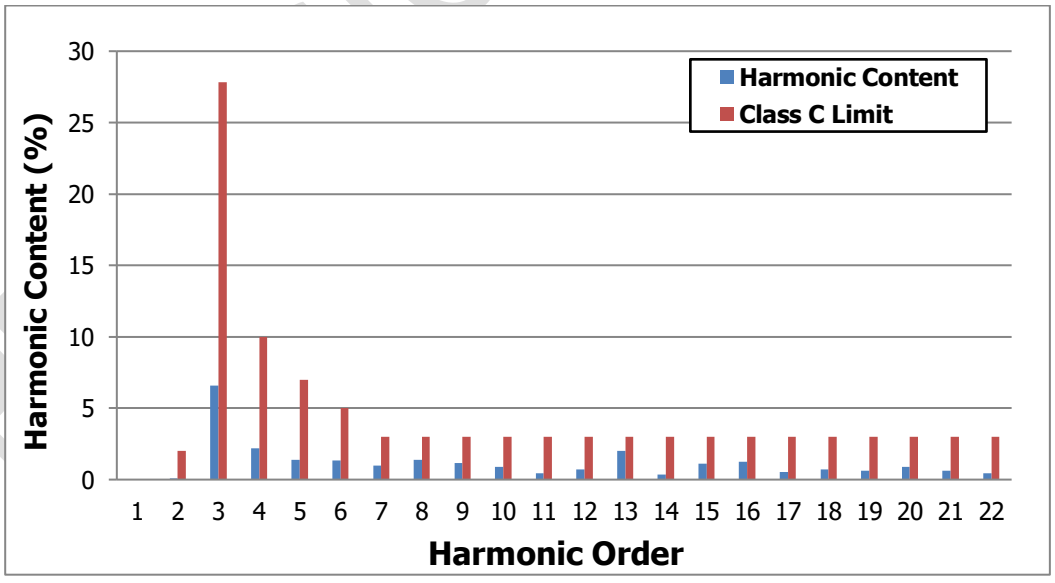


Figure 33 – Harmonic Content, SVF Enabled, P_{OUT} = 21.6 W, Test 2, 230 VAC.

16.7 LED Dimming Test

The PSU was configured for 1-wire filtered PWM dimming. The value of the LED current was measured as the duty cycle of the PWM was increased from 0 to 100% in 1% steps. The measurements were taken at the LED stack voltage of 36 V and repeated for the following conditions:

- Input line voltages: 180 VAC, 230 VAC, 265 VAC
- During SVF Disabled (LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A, CV1: 5 V / 0.5 A)
- During SVF Enabled (LED: 36 V / 0.6 A, CV2: 24 V / 0 A, CV1: 5 V / 0.5 A)

The results are shown in Figure 34 and Figure 35.

16.7.1 LED Dimming, SVF Disabled

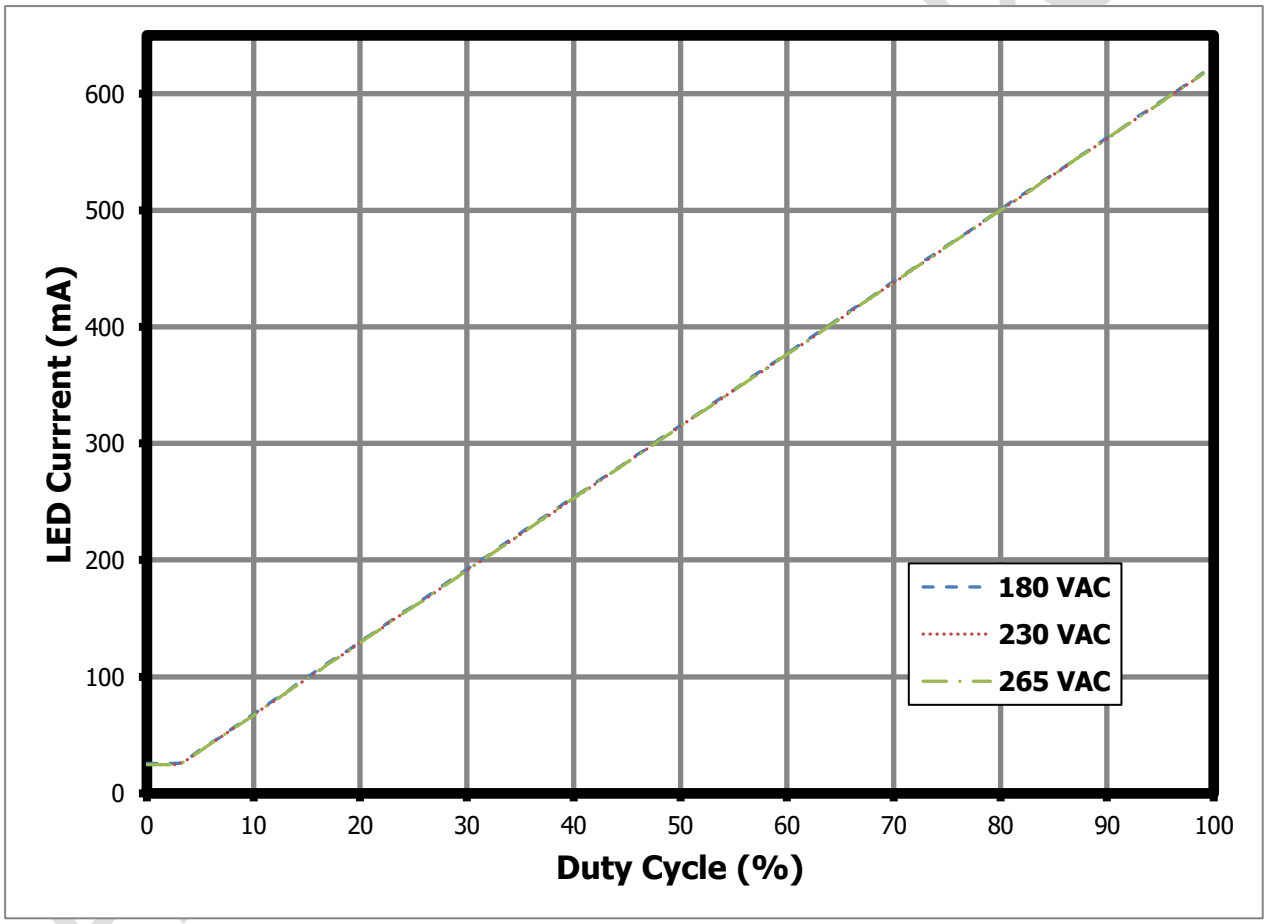


Figure 34 – LED Dimming, SVF Disabled.

16.7.2 LED Dimming, SVF Enabled

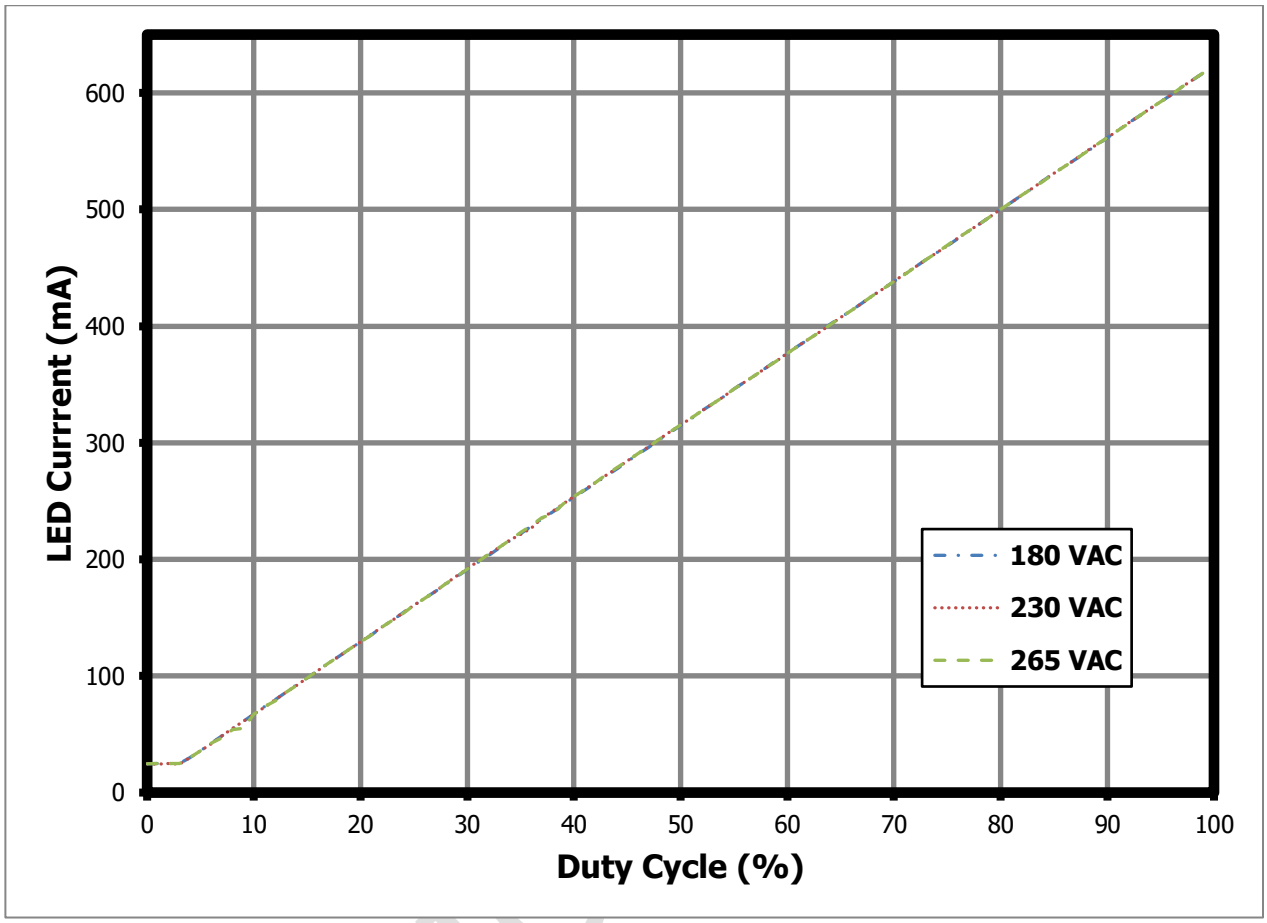


Figure 35 – LED Dimming, SVF Enabled.

16.8 Thermal Test

16.8.1 Thermal testing at Room Temperature

The open frame was placed inside a large enclosure to restrict convective airflow that might affect the thermal measurements. No forced air-cooling was deployed during the test.

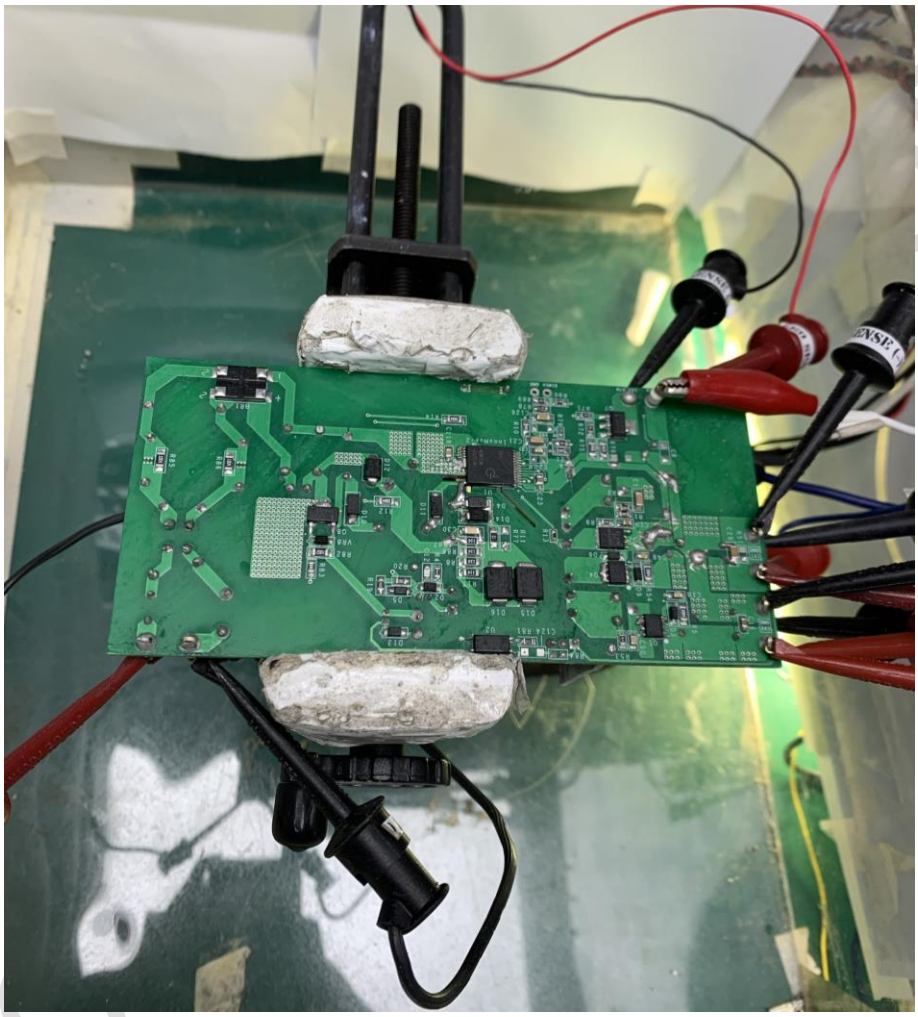


Figure 36 – Thermal Scan Test Set-up.

16.8.1.1 Thermal Scan at 180 VAC, SVF Disabled, Full-Load

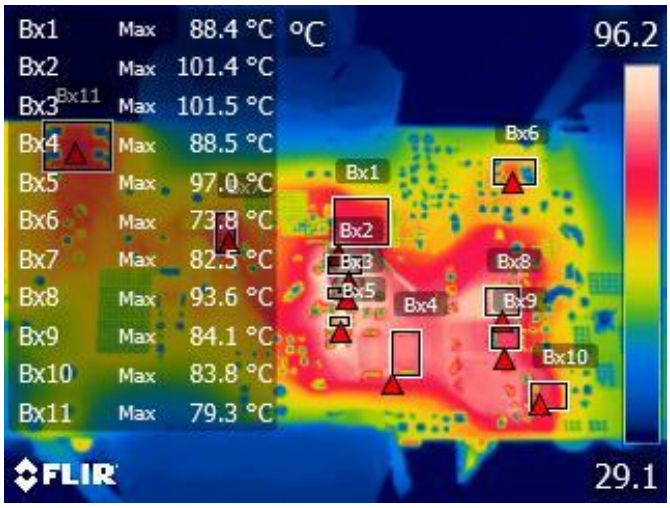


Figure 37 – Thermal Scan 180 VAC, Full Load, SVF Disabled, Bottom View.

Bx11	U1	Innomux2-EP IC	88.4 ºC
Bx2	D4	Pri Snubber Diode	101.4 ºC
Bx3	C30	Pri Snubber Capacitor	101.5 ºC
Bx4	VR9	Pri Snubber TVS Clamp	88.5 ºC
Bx5	R87	Pri Snubber Resistor	97.0 ºC
Bx6	Q7	LED Driver MOSFET	73.8 ºC
Bx7	D12	Blocking Diode	82.5 ºC
Bx8	Q2	SR MOSFET	93.6 ºC
Bx9	Q4	CV1 Selection FET	84.1 ºC
Bx10	Q1	CV2 Selection FET	83.8 ºC
Bx11	BR1	Bridge Rectifier	79.3 ºC
AMBIENT			33.8 ºC

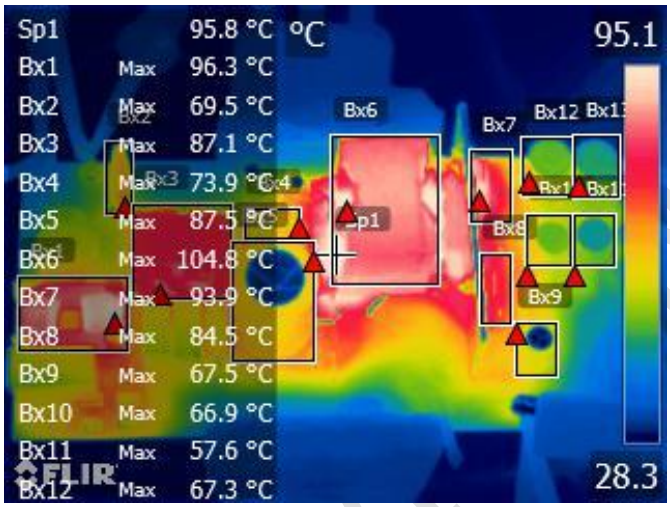


Figure 38 – Thermal Scan 180 VAC, Full Load, SVF Disabled, Top View.

Bx11	L7	Input CMC	95.8ºC
Bx2	RT1	Thermistor	96.3 ºC
Bx3	T1	SVF L-Filter	69.5 ºC
Bx4	T3	SVF Boost Inductor	87.1 ºC
Bx5	C3	Bulk Capacitor	73.9 ºC
Bx6	T2	Flyback Transformer	87.5 ºC
Bx7	D7	CV2 Blocking Diode	104.8 ºC
Bx8	D1	LED Blocking Diode	93.9 ºC
Bx9	C6	LED Output Capacitor	84.5 ºC
Bx10	C49	CV1 Output Capacitor	67.5 ºC
Bx11	C50	CV1 Output Capacitor	66.9 ºC
Bx12	C14	CV2 Output Capacitor	57.6 ºC
Bx13	C127	CV2 Output Capacitor	67.3 ºC
AMBIENT			33.7 ºC

16.8.1.2 Thermal Scan at 230 VAC, SVF Disabled, Full-Load

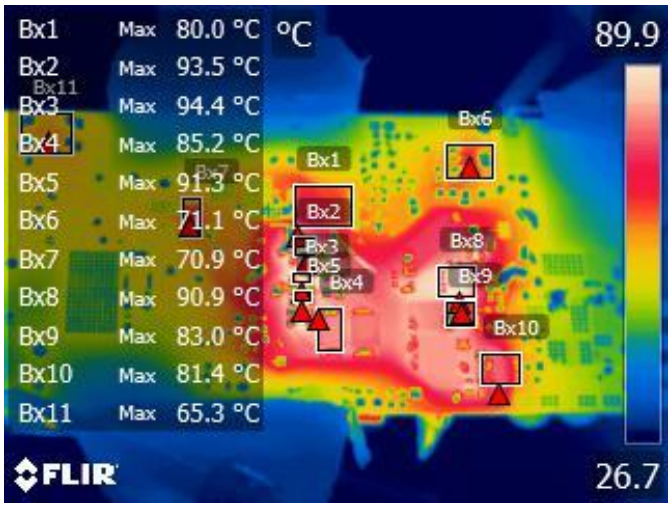


Figure 39 – Thermal Scan 230 VAC, Full Load, SVF Disabled, Bottom View.

Bx11	U1	Innomux2-EP IC	80 ºC
Bx2	D4	Pri Snubber Diode	93.5 ºC
Bx3	C30	Pri Snubber Capacitor	94.4 ºC
Bx4	VR9	Pri Snubber Zener Clamp	85.2 ºC
Bx5	R87	Pri Snubber Resistor	91.3 ºC
Bx6	Q7	LED Driver MOSFET	71.1 ºC
Bx7	D12	Blocking Diode	70.9 ºC
Bx8	Q2	SR MOSFET	90.9 ºC
Bx9	Q4	CV1 Selection FET	83.0 ºC
Bx10	Q1	CV2 Selection FET	81.4 ºC
Bx11	BR1	Bridge Rectifier	65.3 ºC
AMBIENT			33.1 ºC

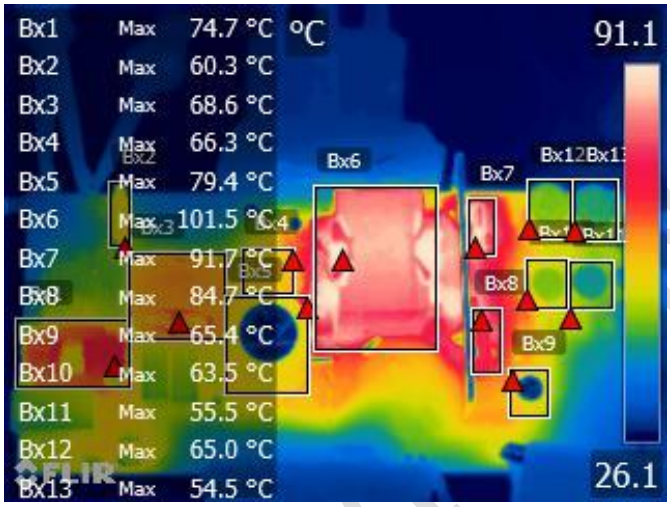


Figure 40 – Thermal Scan 230 VAC, Full Load, SVF Disabled, Top View.

Bx11	L7	Input CMC	74.7 ºC
Bx2	RT1	Thermistor	60.3 ºC
Bx3	T1	SVF L-Filter	68.6 ºC
Bx4	T3	SVF Boost Inductor	66.3 ºC
Bx5	C3	Bulk Capacitor	79.4 ºC
Bx6	T2	Flyback Transformer	101.5 ºC
Bx7	D7	CV2 Blocking Diode	91.7 ºC
Bx8	D1	LED Blocking Diode	84.7 ºC
Bx9	C6	LED Output Capacitor	65.4 ºC
Bx10	C49	CV1 Output Capacitor	63.5 ºC
Bx11	C50	CV1 Output Capacitor	55.5 ºC
Bx12	C14	CV2 Output Capacitor	65 ºC
Bx13	C127	CV2 Output Capacitor	54.5 ºC
AMBIENT			30.6 ºC

16.8.1.3 Thermal Scan at 265 VAC, SVF Disabled, Full-Load

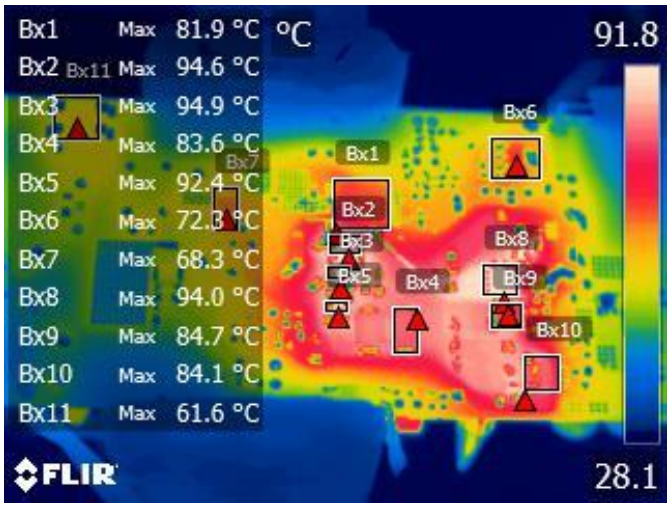


Figure 41 – Thermal Scan 265 VAC, Full Load, SVF Disabled, Bottom View.

Bx11	U1	Innomux2-EP IC	81.9 ºC
Bx2	D4	Pri Snubber Diode	94.6 ºC
Bx3	C30	Pri Snubber Capacitor	94.9 ºC
Bx4	VR9	Pri Snubber Zener Clamp	83.6 ºC
Bx5	R87	Pri Snubber Resistor	92.4 ºC
Bx6	Q7	LED Driver MOSFET	72.3 ºC
Bx7	D12	Blocking Diode	68.3 ºC
Bx8	Q2	SR MOSFET	94 ºC
Bx9	Q4	CV1 Selection FET	84.7 ºC
Bx10	Q1	CV2 Selection FET	84.1 ºC
Bx11	BR1	Bridge Rectifier	61.6 ºC
AMBIENT			34 ºC

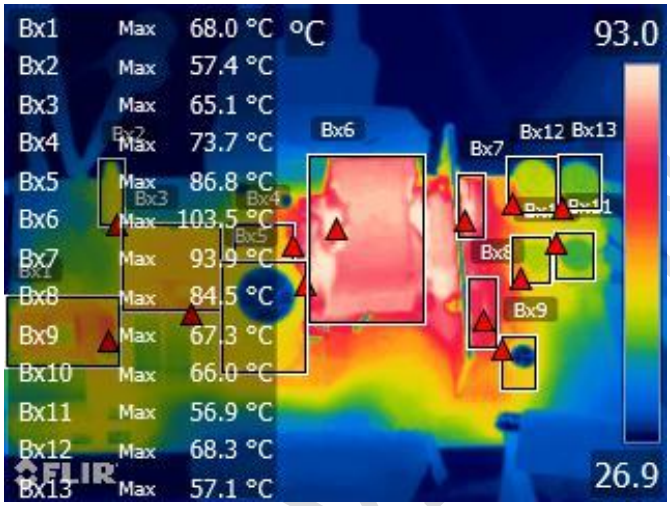


Figure 42 – Thermal Scan 265 VAC, Full Load, SVF Disabled, Top View.

Bx11	L7	Input CMC	68 ºC
Bx2	RT1	Thermistor	57.4 ºC
Bx3	T1	SVF L-Filter	65.1 ºC
Bx4	T3	SVF Boost Inductor	73.7 ºC
Bx5	C3	Bulk Capacitor	86.8 ºC
Bx6	T2	Flyback Transformer	103.5 ºC
Bx7	D7	CV2 Blocking Diode	93.9 ºC
Bx8	D1	LED Blocking Diode	84.5 ºC
Bx9	C6	LED Output Capacitor	67.3 ºC
Bx10	C49	CV1 Output Capacitor	66 ºC
Bx11	C50	CV1 Output Capacitor	56.9 ºC
Bx12	C14	CV2 Output Capacitor	68.3 ºC
Bx13	C127	CV2 Output Capacitor	57.1 ºC
AMBIENT			33 ºC

16.8.1.4 Thermal Scan at 230 VAC, SVF Enabled

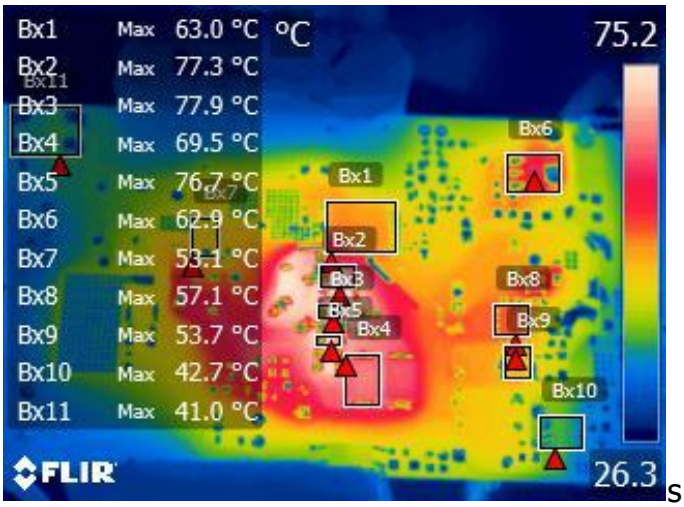


Figure 43 – Thermal Scan 230 VAC, Full Load, SVF Enabled, Bottom View.

Bx11	U1	Innomux2-EP IC	63 ºC
Bx2	D4	Pri Snubber Diode	77.3 ºC
Bx3	C30	Pri Snubber Capacitor	77.9 ºC
Bx4	VR9	Pri Snubber Zener Clamp	69.5 ºC
Bx5	R87	Pri Snubber Resistor	76.7 ºC
Bx6	Q7	LED Driver MOSFET	62.9 ºC
Bx7	D12	Blocking Diode	53.1 ºC
Bx8	Q2	SR MOSFET	57.1 ºC
Bx9	Q4	CV1 Selection FET	53.7 ºC
Bx10	Q1	CV2 Selection FET	42.7 ºC
Bx11	BR1	Bridge Rectifier	41.0 ºC
AMBIENT			28.6 ºC

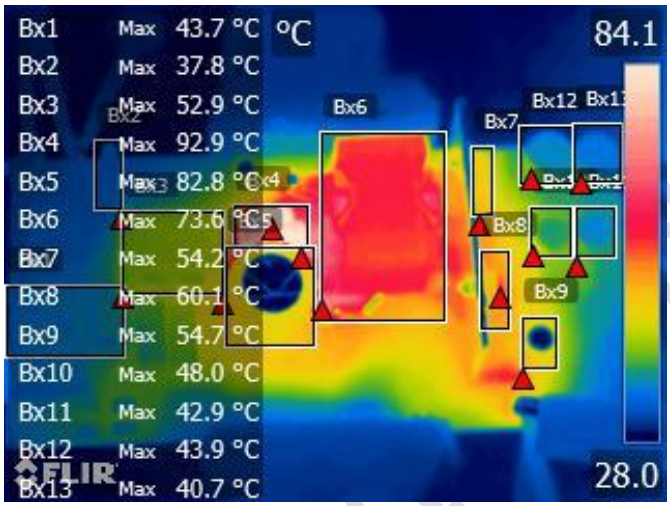


Figure 44 – Thermal Scan 230 VAC, Full Load, SVF Enabled, Top View.

Bx11	L7	Input CMC	43.7 ºC
Bx2	RT1	Thermistor	37.8 ºC
Bx3	T1	SVF L-Filter	52.9 ºC
Bx4	T3	SVF Boost Inductor	92.9 ºC
Bx5	C3	Bulk Capacitor	82.8 ºC
Bx6	T2	Flyback Transformer	73.6 ºC
Bx7	D7	CV2 Blocking Diode	54.2 ºC
Bx8	D1	LED Blocking Diode	60.1 ºC
Bx9	C6	LED Output Capacitor	54.7 ºC
Bx10	C49	CV1 Output Capacitor	48 ºC
Bx11	C50	CV1 Output Capacitor	42.9 ºC
Bx12	C14	CV2 Output Capacitor	43.9 ºC
Bx13	C127	CV2 Output Capacitor	40.7 ºC
AMBIENT			29.7 ºC

17 Waveforms

17.1 Start-up Profile

A full load start-up test was conducted on the power supply under the following test conditions:

- Input line voltages: 180 VAC, 230 VAC, 265 VAC
- During SVF Disabled (LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A, CV1: 5 V / 0.5 A)
- During SVF Enabled (LED: 36 V / 0.6 A, CV2: 24 V / 0 A, CV1: 5 V / 0.5 A)

17.1.1 SVF Disabled

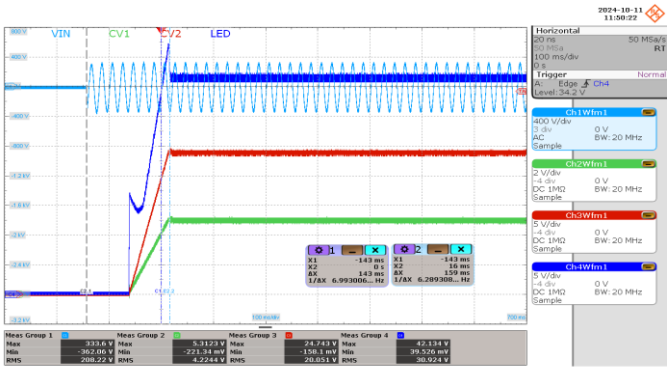


Figure 45 – Start-up Profile
180 VAC, Full-Load, Start-up, SVF Disabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div.
Time Scale: 100 ms / div.
$t_{ON\ Delay}$: 143 ms

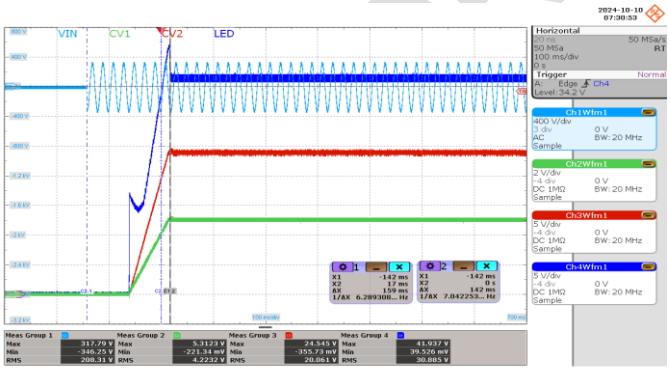


Figure 46 – Start-up Profile
230 VAC, Full-Load, Start-up, SVF Disabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div.
Time Scale: 100 ms / div.
$t_{ON\ Delay}$: 159 ms

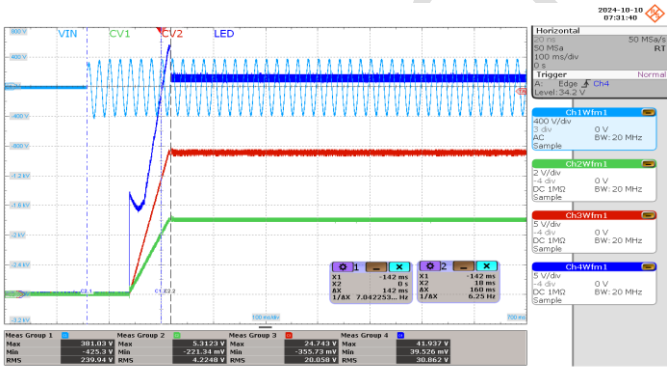


Figure 47 – Start-up Profile
265 VAC, Full-Load, Start-up, SVF Disabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div.
Time Scale: 100 ms / div.
$t_{ON\ Delay}$: 142 ms

17.1.2 SVF Enabled

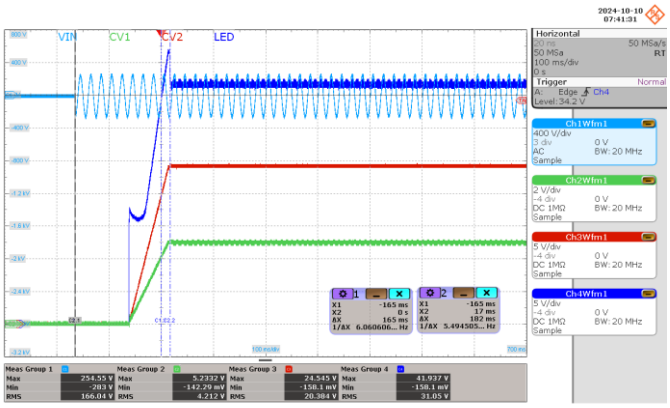


Figure 48– Start-up Profile
180 VAC, Start-up, SVF Enabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div.
Time Scale: 100 ms / div.
$t_{ON\ Delay}$: 165 ms

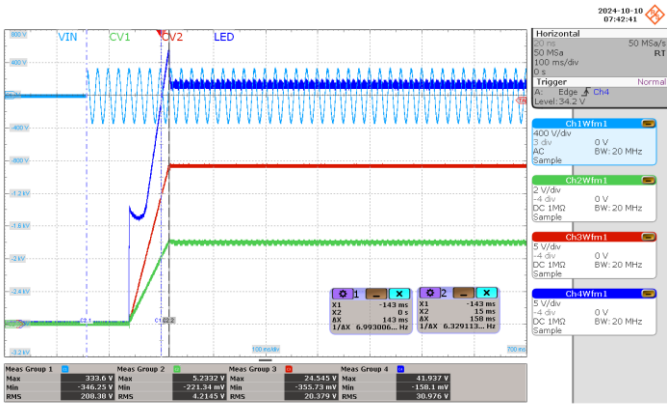


Figure 49– Start-up Profile
230 VAC, Start-up, SVF Enabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div.
Time Scale: 100 ms / div.
$t_{ON\ Delay}$: 143 ms

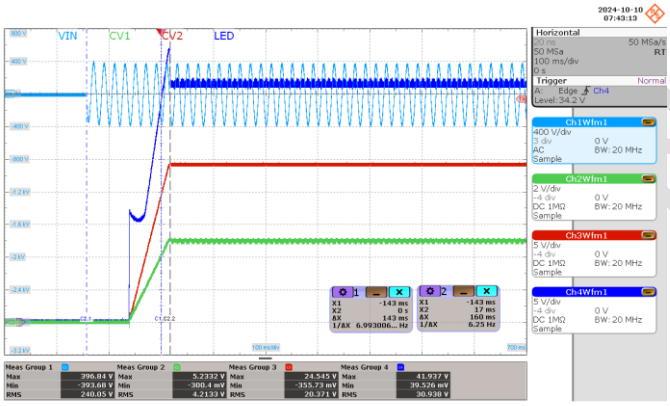


Figure 50– Start-up Profile
265 VAC, Start-up, SVF Enabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div.
Time Scale: 100 ms / div.
$t_{ON\ Delay}$: 143 ms

17.2 No-Load Start-Up

A no load start-up test was conducted on power supply covering under the following test conditions:

- Input line voltages: 180 VAC, 230 VAC, 265 VAC
- During SVF Disabled (LED: 36 V / 0 A, CV2: 24 V / 0 A, CV1: 5 V / 0 A)
- During SVF Enabled (LED: 36 V / 0 A, CV2: 24 V / 0 A, CV1: 5 V / 0 A)

17.2.1 SVF Disabled

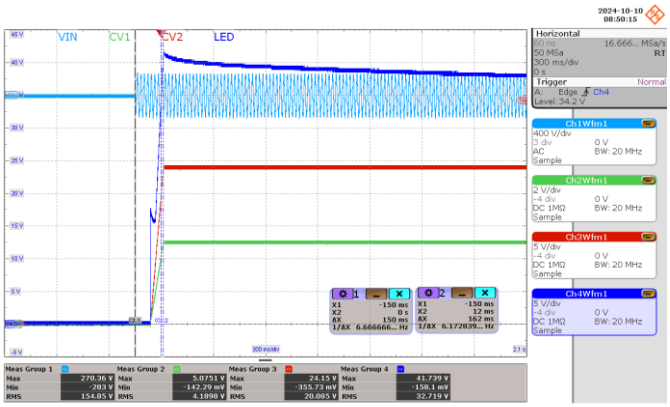


Figure 51 – Start-up Profile
180 VAC, No-Load, Start-up, SVF Disabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div., 300 ms / div.
$t_{ON\ Delay}$: 150 ms

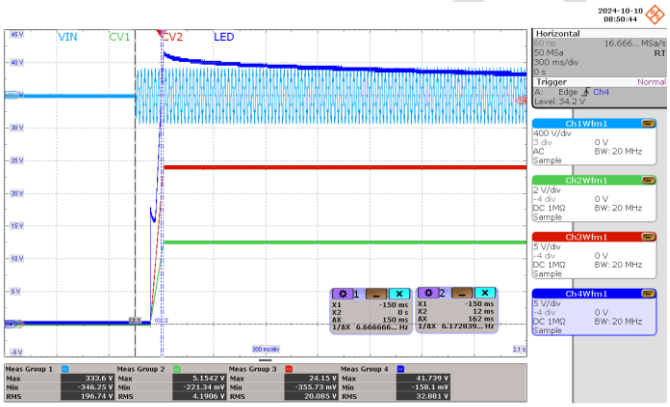


Figure 52 – Start-up Profile
230 VAC, No-Load, Start-up, SVF Disabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div., 300 ms / div.
$t_{ON\ Delay}$: 150 ms

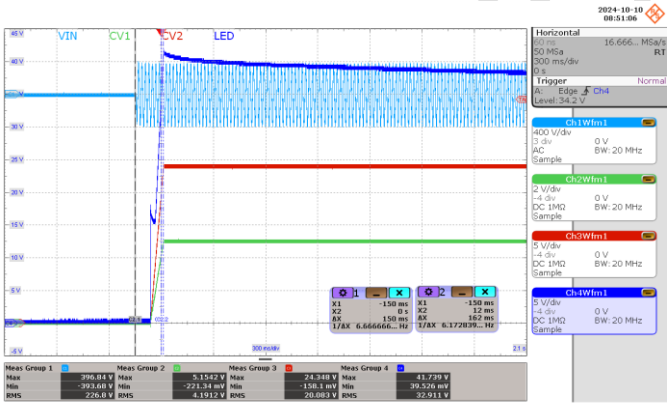


Figure 53 – Start-up Profile
265 VAC, No-Load, Start-up, SVF Disabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div., 300 ms / div.
$t_{ON\ Delay}$: 150 ms

17.2.2 SVF Enabled

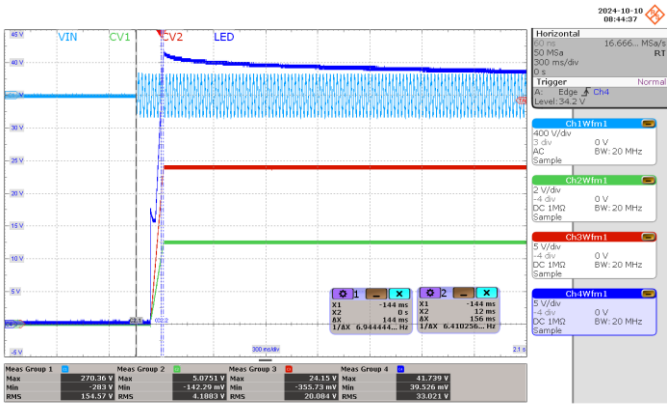


Figure 54 – Start-up Profile
180 VAC, No-Load, Start-up, SVF Enabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div., 300 ms / div.
$t_{ON\ Delay}$: 144 ms

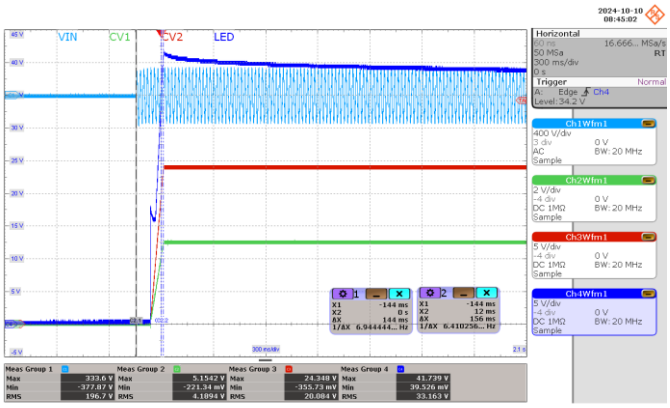


Figure 55 – Start-up Profile
230 VAC, No-Load, Start-up, SVF Enabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div., 300 ms / div.
$t_{ON\ Delay}$: 144 ms

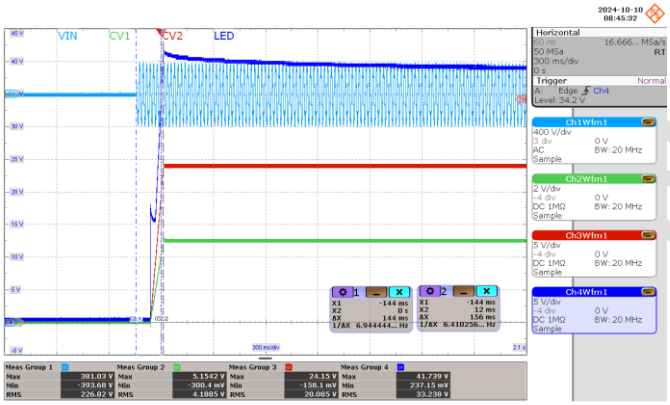


Figure 56 – Start-up Profile
265 VAC, No-Load, Start-up, SVF Enabled.
CH1: V_{IN}, 400 V / div.
CH2: V_{CV1}, 2 V / div.
CH3: V_{CV2}, 5 V / div.
CH4: V_{LED}, 5 V / div., 300 ms / div.
$t_{ON\ Delay}$: 144 ms

17.3 Switching Waveforms

17.3.1 Flyback Primary Drain Voltage and Current at Start-up Full Load, SVF Disabled.

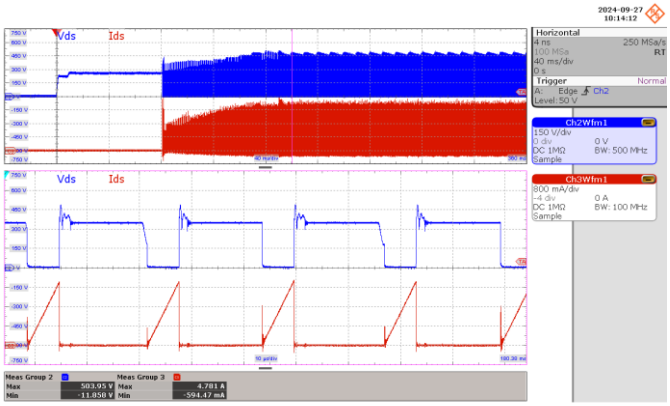


Figure 57 – Primary Drain Voltage and Current
180 VAC, Full-Load, Start-up
CH2: V_{DRAIN}, 150 V / div.
CH3: I_{DRAIN}, 800 mA / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
V_{DSMAX}: 503.95 V; I_{DSMAX}: 4.78 A

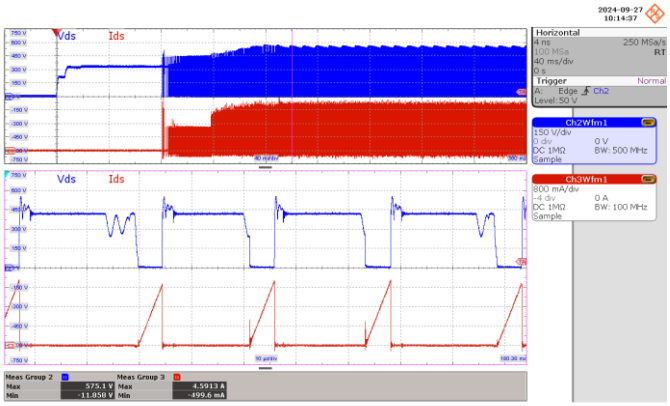


Figure 58 – Primary Drain Voltage and Current
230 VAC, Full-Load, Start-up
CH2: V_{DRAIN}, 150 V / div.
CH3: I_{DRAIN}, 800 mA / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
V_{DSMAX}: 575.1 V; I_{DSMAX}: 4.59 A

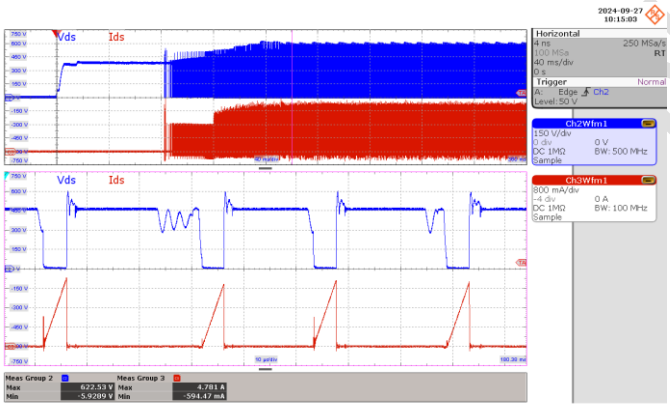


Figure 59 – Primary Drain Voltage and Current
265 VAC, Full-Load, Start-up
CH2: V_{DRAIN}, 150 V / div.
CH3: I_{DRAIN}, 800 mA / div.
Time Scale: 40 ms / div. (10 µs / div. Zoom)
V_{DSMAX}: 622.53 V; I_{DSMAX}: 4.78 A

17.3.2 Flyback Primary Drain Voltage and Current at Full Load Steady State, SVF Disabled.

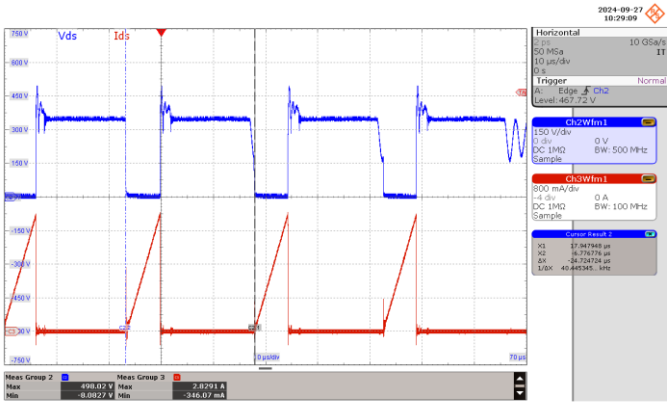


Figure 60 – Primary Drain Voltage and Current
180 VAC, Full-Load, Steady-State
CH2: V_{DRAIN}, 150 V / div.
CH3: I_{DRAIN}, 800 mA / div.
V_{DSMAX}: 498.02 V; I_{DSMAX}: 2.83 A;
f_{SW}: 40.44 kHz
Time Scale: 10 µs / div.

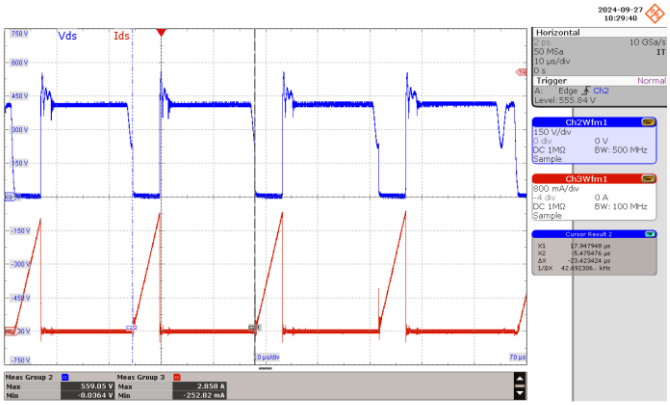


Figure 61 – Primary Drain Voltage and Current
230 VAC, Full-Load, Steady-State
CH2: V_{DRAIN}, 150 V / div.
CH3: I_{DRAIN}, 800 mA / div.
V_{DSMAX}: 559.05 V; I_{DSMAX}: 2.86 A;
f_{SW}: 42.49 kHz
Time Scale: 10 µs / div.

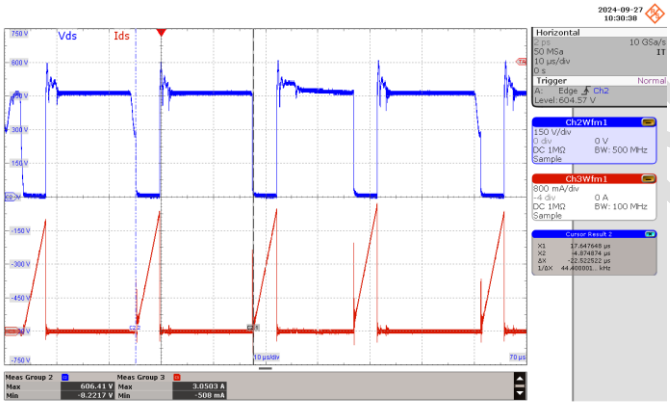


Figure 62 – Primary Drain Voltage and Current
265 VAC, Full-Load, Steady-State
CH2: V_{DRAIN}, 150 V / div.
CH3: I_{DRAIN}, 800 mA / div.
V_{DSMAX}: 606.41 V; I_{DSMAX}: 3.05 A;
f_{SW}: 44.40 kHz
Time Scale: 10 µs / div.

17.3.3 Flyback Primary Drain Voltage and Current at Transient Load, SVF Disabled

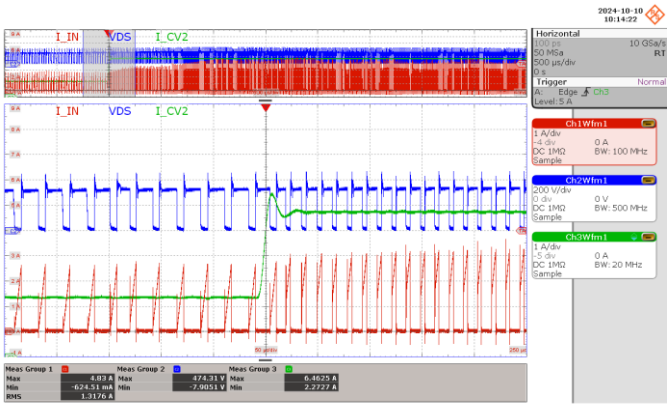


Figure 63 – CV2 Output-Load Transient at 180 VAC;
LED: 36 V / 0.6 A, CV2: 24 V 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A
CH1: I_{DS}, 1 A / div.
CH2: V_{DRAIN}, 200 V / div.
CH3: I_{CV2}, 1 A / div.
V_{DSMAX}: 474.31 V; I_{DSMAX}: 4.83 A
Time Scale: 500 µs / div. (50 µs / div. Zoom)

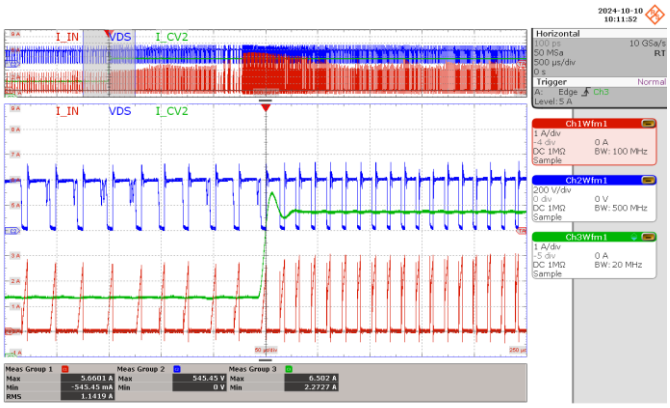


Figure 64 – CV2 Output-Load Transient 230 VAC;
LED: 36 V / 0.6 A, CV2: 24 V 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A
CH1: I_{DS}, 1 A / div.
CH2: V_{DRAIN}, 200 V / div.
CH3: I_{CV2}, 1 A / div.
V_{DSMAX}: 545.45 V; I_{DSMAX}: 5.66 A
Time Scale: 500 µs / div. (50 µs / div. Zoom)

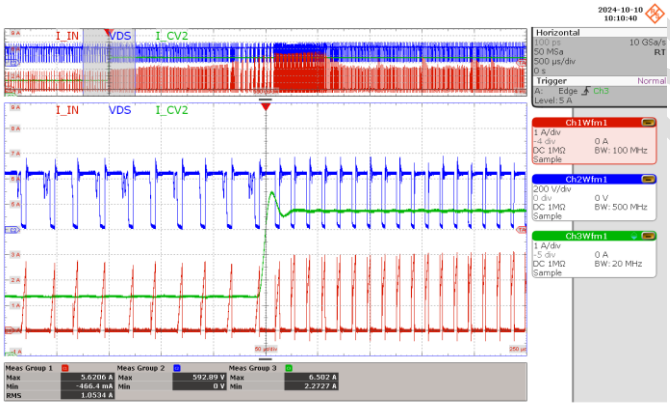


Figure 65– CV2 Output-Load Transient at 265 VAC;
LED: 36 V / 0.6 A, CV2: 24 V 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A
CH1: I_{DS}, 1 A / div.
CH2: V_{DRAIN}, 200 V / div.
CH3: I_{CV2}, 1 A / div.
V_{DSMAX}: 592.89 V; I_{DSMAX}: 5.62 A
Time Scale: 500 µs / div. (50 µs / div. Zoom)

17.4 Flyback SR FET (Q2) Voltage Waveforms

A flyback start-up test was conducted on the power supply under the following test conditions:

- Input line voltages: 180 VAC, 230 VAC, 265 VAC
- During SVF Disabled (LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A, CV1: 5 V / 0.5 A)

17.4.1 Flyback SR FET (Q2) Voltage at Full Load Start-up

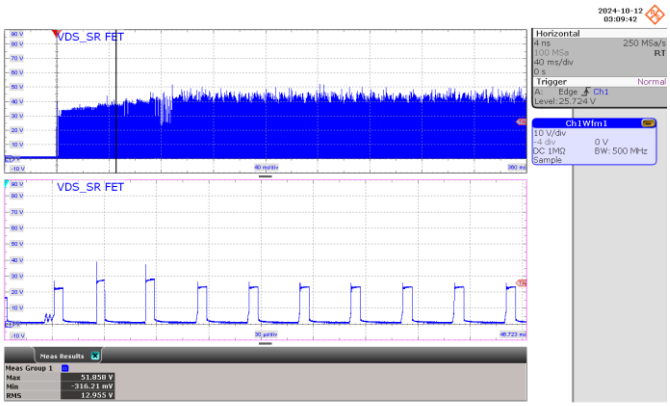


Figure 66 – SR FET Drain Voltage
180 VAC, Full-Load, Start-up, SVF Disabled.
CH2: V_{DRAIN_SR}, 10 V / div.
Time Scale: 40 ms / div. (30 µs / div. Zoom)
V_{DSMAX}: 51.86 V

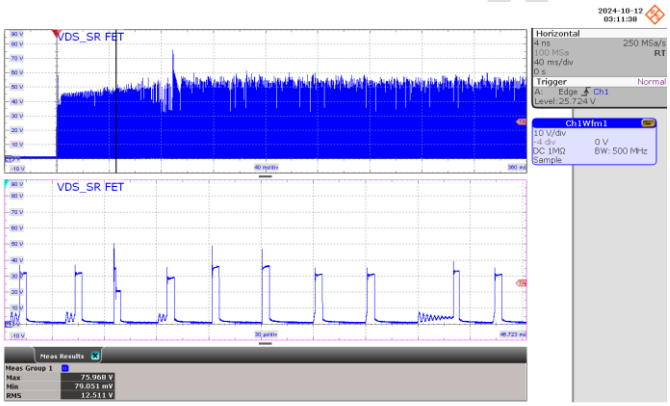


Figure 67 – SR FET Drain Voltage
230 VAC, Full-Load, Start-up, SVF Disabled.
CH2: V_{DRAIN_SR}, 10 V / div.
Time Scale: 40 ms / div. (30 µs / div. Zoom)
V_{DSMAX}: 75.97 V

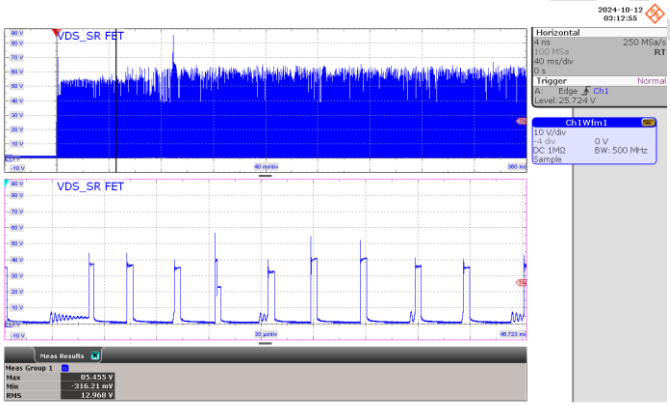


Figure 68 – SR FET Drain Voltage
265 VAC, Full-Load, Start-up, SVF Disabled.
CH2: V_{DRAIN_SR}, 10 V / div.
Time Scale: 40 ms / div. (30 µs / div. Zoom)
V_{DSMAX}: 85.46 V

17.4.2 Flyback SR FET (Q2) Voltage at Full Load Steady-State

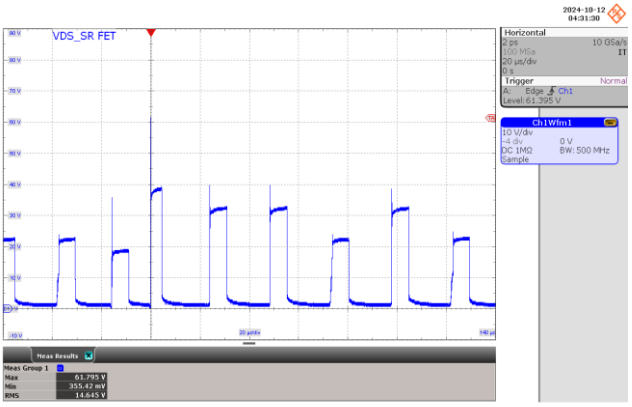


Figure 69 – SR FET Drain Voltage
180 VAC, Full-Load, Steady-State, SVF Disabled.
CH2: V_{DRAIN_SR}, 10 V / div.
Time Scale: 20 µs / div.
V_{DSMAX}: 61.80 V

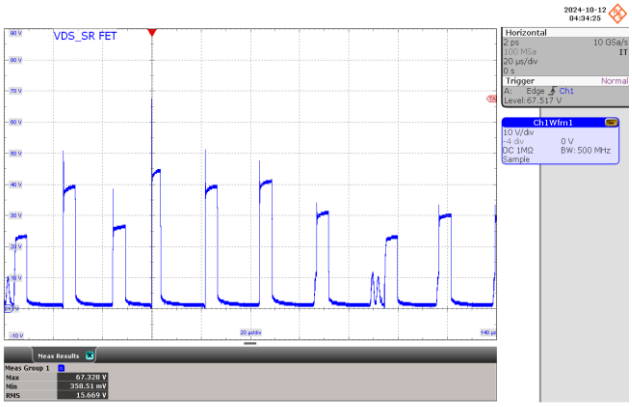


Figure 70 – SR FET Drain Voltage
230 VAC, Full-Load, Steady-State, SVF Disabled.
CH2: V_{DRAIN_SR}, 10 V / div.
Time Scale: 20 µs / div.
V_{DSMAX}: 67.33 V

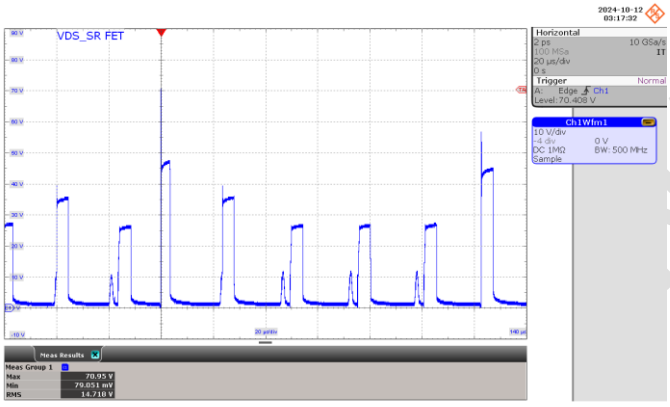


Figure 71 – SR FET Drain Voltage
265 VAC, Full-Load, Steady-State, SVF Disabled.
CH2: V_{DRAIN_SR}, 10 V / div.
Time Scale: 20 µs / div.
V_{DSMAX}: 70.95 V

17.5 Load Transient Response

CV output voltages and LED current were measured for a load step of 2.4 A to 5.8 A for CV2 with SVF disabled. Measurements were taken at 180 VAC, 230 VAC, and 265 VAC, with full load on CV1 and the LED output.

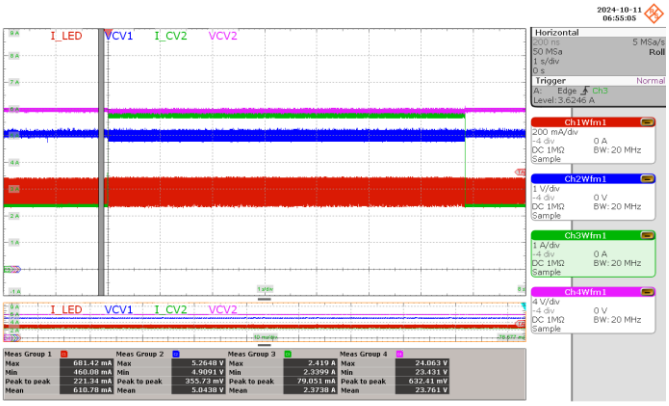


Figure 72 – Load Transient during Nominal Load at 180 VAC, LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A,
CH1: $I_{(LED)}$, 200 mA / div.
CH2: $V_{(CV1)}$, 1 V / div.
CH3: $I_{(CV2)}$, 1 A / div.
CH4: $V_{(CV2)}$, 4 V / div.
Time Scale: 1 s / div.

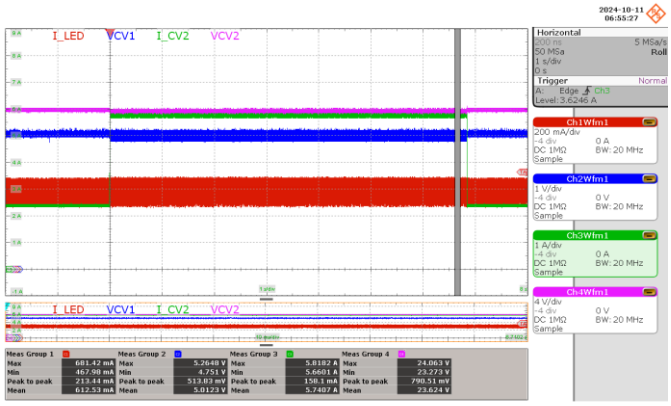


Figure 73 – Load Transient during Peak Load at 180 VAC, LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A,
CH1: $I_{(LED)}$, 200 mA / div.
CH2: $V_{(CV1)}$, 1 V / div.
CH3: $I_{(CV2)}$, 1 A / div.
CH4: $V_{(CV2)}$, 4 V / div.
Time Scale: 1 s / div.

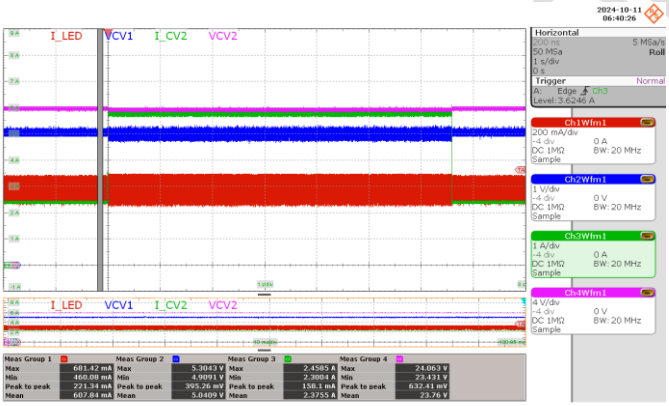


Figure 74 – Load Transient during Nominal Load at 230 VAC, LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A,
CH1: $I_{(LED)}$, 200 mA / div.
CH2: $V_{(CV1)}$, 1 V / div.
CH3: $I_{(CV2)}$, 1 A / div.
CH4: $V_{(CV2)}$, 4 V / div.
Time Scale: 1 s / div.

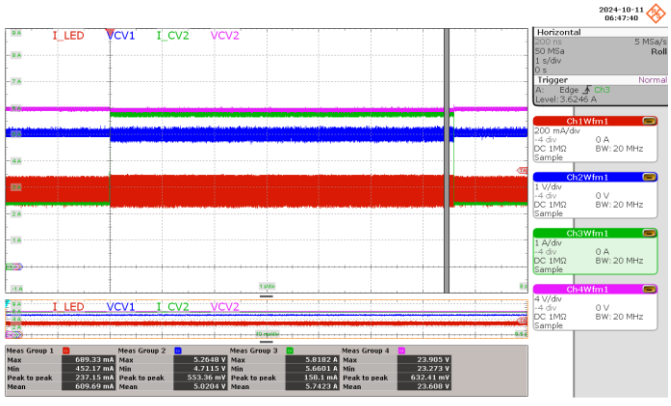


Figure 75 – Load Transient during Peak Load at 230 VAC, LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A,
CH1: $I_{(LED)}$, 200 mA / div.
CH2: $V_{(CV1)}$, 1 V / div.
CH3: $I_{(CV2)}$, 1 A / div.
CH4: $V_{(CV2)}$, 4 V / div.
Time Scale: 1 s / div.

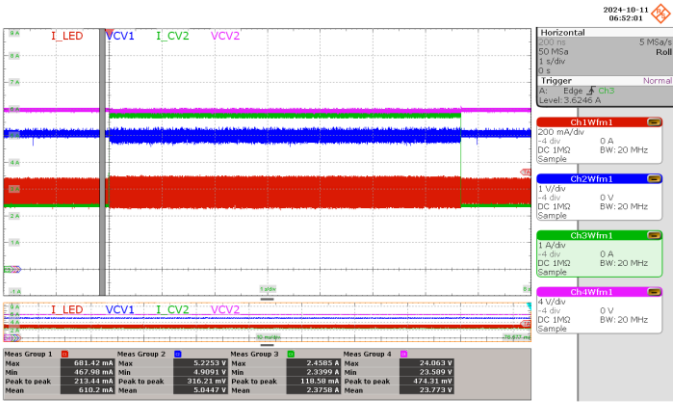


Figure 76 – Load Transient during Nominal Load at 265 VAC, LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A,
CH1: $I_{(LED)}$, 200 mA / div.
CH2: $V_{(CV1)}$, 1 V / div.
CH3: $I_{(CV2)}$, 1 A / div.
CH4: $V_{(CV2)}$, 4 V / div.
Time Scale: 1 s / div.

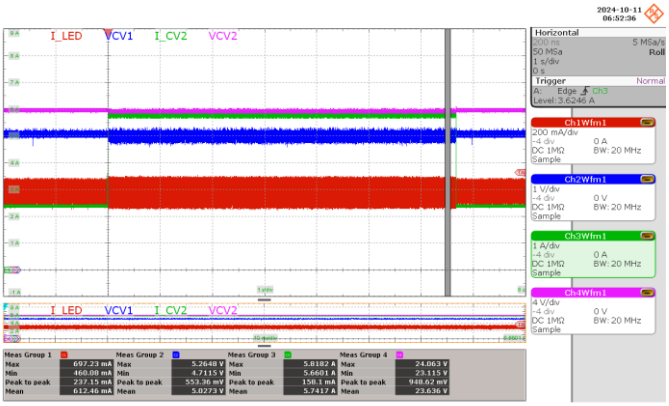


Figure 77 – Load Transient during Peak Load at 265 VAC, LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A – 5.8 A Transient, CV1: 5 V / 0.5 A,
CH1: $I_{(LED)}$, 200 mA / div.
CH2: $V_{(CV1)}$, 1 V / div.
CH3: $I_{(CV2)}$, 1 A / div.
CH4: $V_{(CV2)}$, 4 V / div.
Time Scale: 1 s / div.

17.6 Output Ripple Voltage Waveforms

17.6.1 Ripple Measurement Technique

To conduct output ripple measurements, a modified oscilloscope test probe must be used prevent spurious noise pickup from offsetting results.

The 4987BA probe adapter was equipped with two capacitors connected in parallel across the probe tip. These capacitors consisted of one (1) 0.1 µF/50 V ceramic type and one (1) 10 µF/50 V aluminum electrolytic type. Since the aluminum electrolytic capacitor is polarized, proper polarity was maintained across DC outputs (refer to the diagram below).

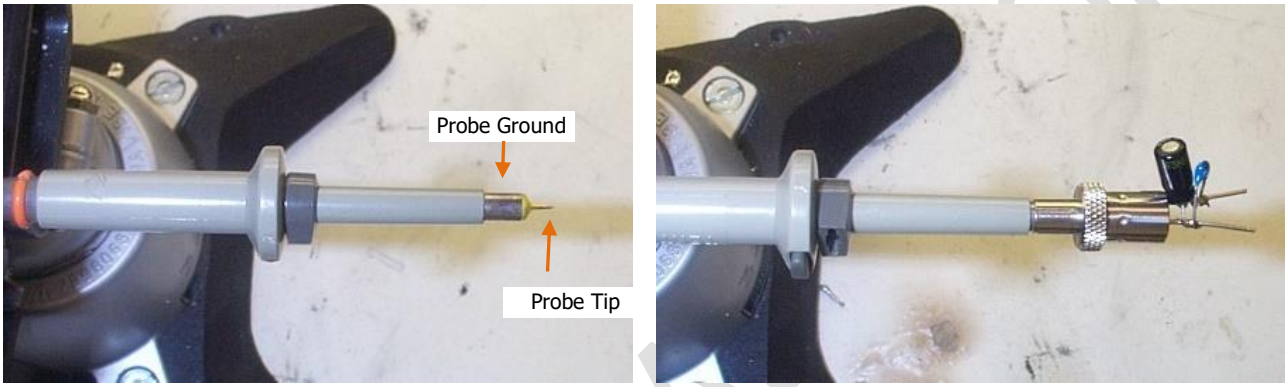


Figure 78 – Ripple voltage probe using Probe Master 4987A BNC Adapter

17.6.2 Output Ripple Voltage

The following test conditions used for measuring the output ripple voltage:

- Input line voltages: 180 VAC, 230 VAC, 265 VAC
- SVF Disabled
- Test 1 - LED: 36 V / 0.6 A (100% Load), CV2: 24 V / 2.4 A (100% Load), CV1: 5 V / 0.5 (100% Load)
- Test 2 - LED: 36 V / 0 A (0% Load), CV2: 24 V / 2.4 A (0% Load), CV1: 5 V / 0.5 (0% Load)

17.6.2.1 SVF Disabled

17.6.2.1.1 Test 1, LED: 100% Load, CV1: 100% Load, CV2: 100% Load

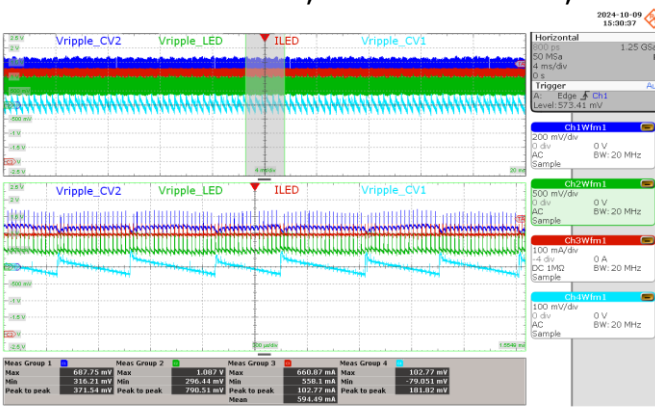


Figure 79 – Output Ripple Voltage
180 VAC, CV1: 100% Load, CV2: 100% Load, LED: 100% Load
CH1: $V_{RIPPLE(CV2)}$, 200 mV / div.
$V_{RIPPLE(CV2)}$: 371.54 mVpp
CH2: $V_{RIPPLE(LED)}$, 500 mV / div.
$V_{RIPPLE(LED)}$: 790.51 mVpp
CH3: I_{LED}, 100 mA / div
CH4: $V_{RIPPLE(CV1)}$, 100 mV / div.
$V_{RIPPLE(CV1)}$: 181.82 mVpp
Time Scale: 300 µs / div. (Zoom)

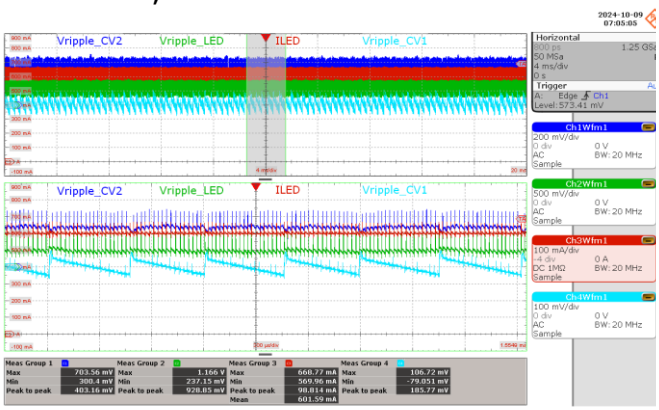


Figure 80 – Output Ripple Voltage
230 VAC, CV1: 100% Load, CV2: 100% Load, LED: 100% Load
CH1: $V_{RIPPLE(CV2)}$, 200 mV / div.
$V_{RIPPLE(CV2)}$: 403.16 mVpp
CH2: $V_{RIPPLE(LED)}$, 500 mV / div.
$V_{RIPPLE(LED)}$: 928.85 mVpp
CH3: I_{LED}, 100 mA / div
CH4: $V_{RIPPLE(CV1)}$, 100 mV / div.
$V_{RIPPLE(CV1)}$: 185.77 mVpp
Time Scale: 300 µs / div. (Zoom)

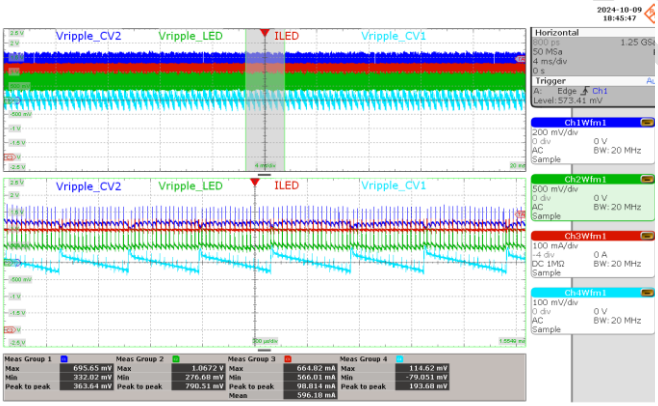


Figure 81 – Output Ripple Voltage
265 VAC, CV1: 100% Load, CV2: 100% Load, LED: 100% Load
CH1: $V_{RIPPLE(CV2)}$, 200 mV / div.
$V_{RIPPLE(CV2)}$: 363.64 mVpp
CH2: $V_{RIPPLE(LED)}$, 500 mV / div.
$V_{RIPPLE(LED)}$: 790.51 mVpp
CH3: I_{LED}, 100 mA / div.
CH4: $V_{RIPPLE(CV1)}$, 100 mV / div.
$V_{RIPPLE(CV1)}$: 193.68 mVpp
Time Scale: 300 µs / div. (Zoom)

17.6.2.1.2 Test 2, LED: 0% Load, CV1: 0% Load, CV2: 0% Load

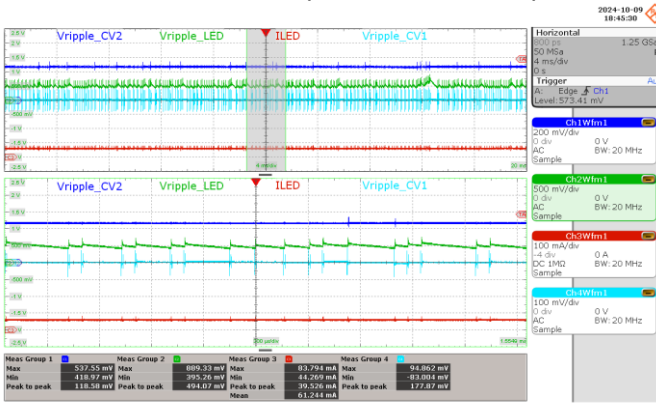


Figure 82 – Output Ripple Voltage
180 VAC, CV1: 0% Load, CV2: 0% Load, LED: 0% Load
CH1: $V_{RIPPLE(CV2)}$, 200 mV / div.
$V_{RIPPLE(CV2)}$: 118.58 mVpp
CH2: $V_{RIPPLE(LED)}$, 500 mV / div.
$V_{RIPPLE(LED)}$: 494.07 mVpp
CH3: I_{LED}, 100 mA / div.
CH4: $V_{RIPPLE(CV1)}$, 100 mV / div.
$V_{RIPPLE(CV1)}$: 177.87 mVpp
Time Scale: 300 µs / div. (Zoom)

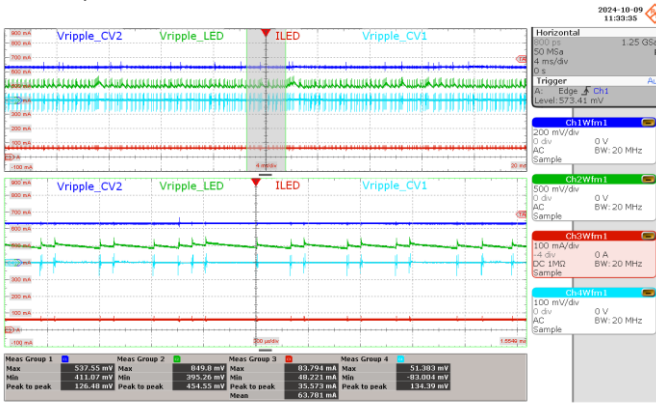


Figure 83 – Output Ripple Voltage
230 VAC, CV1: 0% Load, CV2: 0% Load, LED: 0% Load
CH1: $V_{RIPPLE(CV2)}$, 200 mV / div.
$V_{RIPPLE(CV2)}$: 126.48 mVpp
CH2: $V_{RIPPLE(LED)}$, 500 mV / div.
$V_{RIPPLE(LED)}$: 454.55 mVpp
CH3: I_{LED}, 100 mA / div.
CH4: $V_{RIPPLE(CV1)}$, 100 mV / div.
$V_{RIPPLE(CV1)}$: 134.39 mVpp
Time Scale: 300 µs / div. (Zoom)

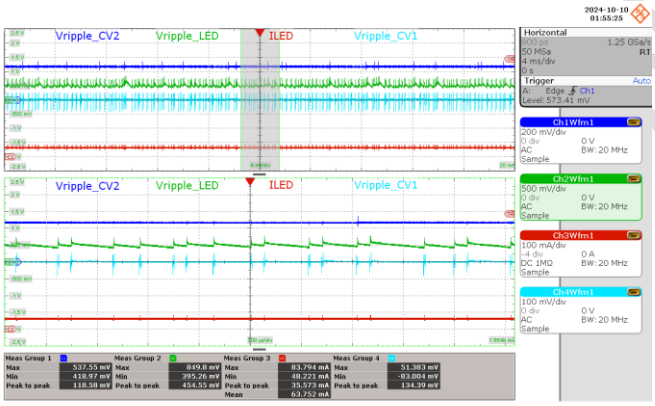


Figure 84 – Output Ripple Voltage
265 VAC, CV1: 0% Load, CV2: 0% Load, LED: 0% Load
CH1: $V_{RIPPLE(CV2)}$, 200 mV / div.
$V_{RIPPLE(CV2)}$: 118.58 mVpp
CH2: $V_{RIPPLE(LED)}$, 500 mV / div.
$V_{RIPPLE(LED)}$: 454.55 mVpp
CH3: I_{LED}, 100 mA / div.
CH4: $V_{RIPPLE(CV1)}$, 100 mV / div.
$V_{RIPPLE(CV1)}$: 134.39 mVpp
Time Scale: 300 µs / div. (Zoom)

18 EMI

The Unit was placed on top of the LED metal heat sink. Three sets of operating conditions were evaluated.

- SVF Disabled, Full Load (82 W), 230 VAC, LN-PE
  - (LED: 36 V / 0.6 A, CV2: 24 V / 2.4 A, CV1: 5 V / 0.5 A)
- SVF Enabled, LED Only, 230 VAC, LN-PE
  - (LED: 36 V / 0.6 A, CV2: 24 V / 0 A, CV1: 5 V / 0 A)
- SVF Enabled, LED + CV1 Only, 230 VAC, LN-PE
  - (LED: 36 V / 0.6 A, CV2: 24 V / 0 A, CV1: 5 V / 0.5 A)

18.1 Output Grounded

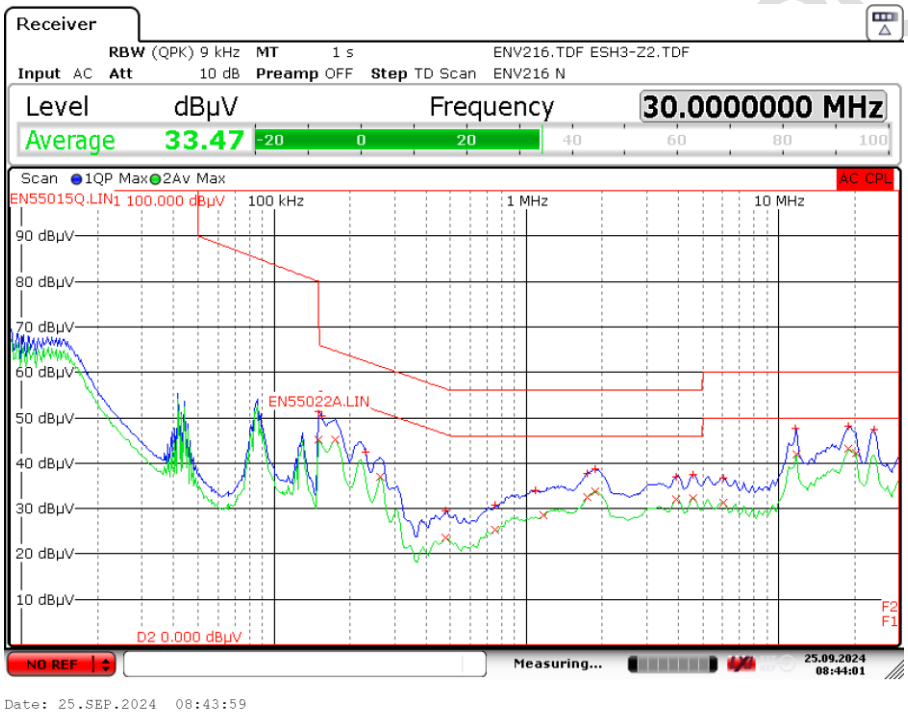


Figure 85 – Conducted EMI with SVF Disabled, Full Load, 230 VAC.

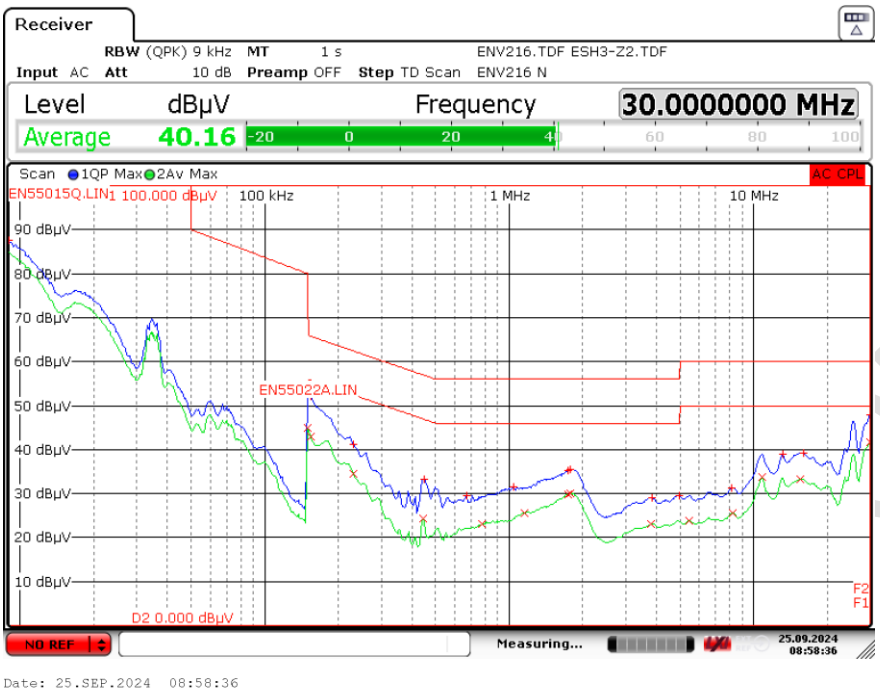


Figure 86 – Conducted EMI with SVF Enabled, LED only, 230 VAC.

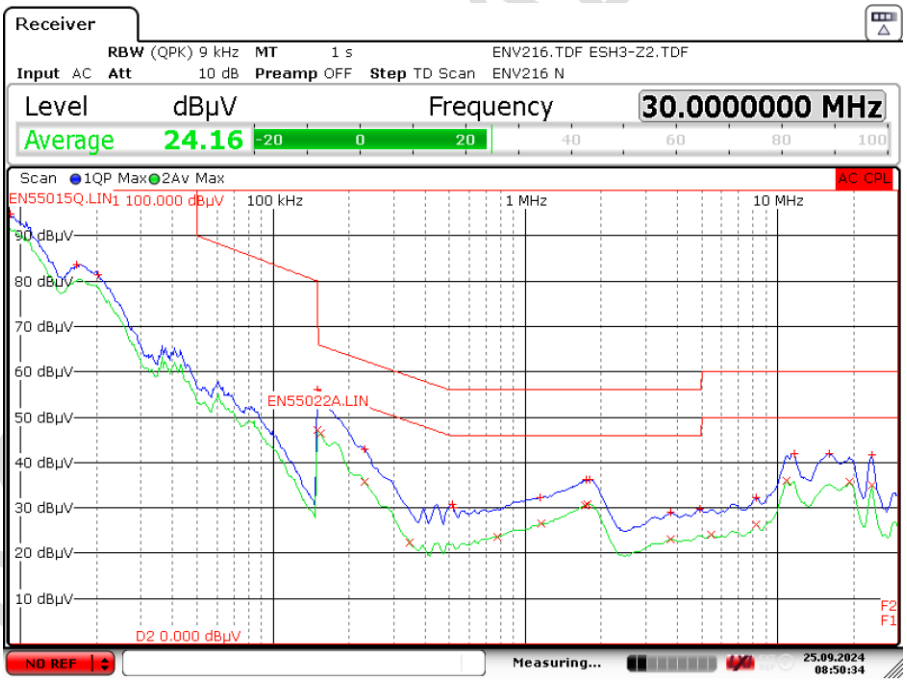


Figure 87 – Conducted EMI with SVF Enabled, LED+CV1 only, 230 VAC.

19 Revision History

Date	Author	Revision	Description & Changes	Reviewed
29-Oct-24	CMC/JKL	A	Initial Release.	Apps & Mktg

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