Design Example Report

Title	**20 W 4 Output Automotive Power Supply for 800V Systems using InnoSwitch™3-AQ INN3947FQ**
Specification	40 VDC – 950 VDC Input; 24.7 V / 240 mA; 3 x 25.5 V/ 550 mA Outputs
Application	Emergency Power Supply for Traction Inverter
Author	Automotive Systems Engineering Department
Document Number	DER-1030Q
Date	March 5, 2025
Revision	A

Summary and Features

- Ultra-compact design for 800 VDC automotive Battery Electric Vehicle (BEV) applications
- Low component count (only 44 electrical components)
- Wide range start-up and operating voltage from 40 VDC to 950 VDC
- >80% full load efficiency across the input voltage range[1]
- Accurate secondary-side regulation without optocouplers
- Ambient operating temperature range:-40° C to 85° C
- Comprehensive fault protection including output current limit and short-circuit
- Uses automotive qualified AEC-Q surface mount (SMD) components[2]
- Low profile - only 20.4 mm high

[1] Applies across 25° C and 85° C ambient. Full load efficiency specification at -40° C ambient is >75%.
[2] AEC-Q200 transformer and input common mode choke qualification belongs to final design.

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1 Introduction

This engineering report describes a 4 output 20 W automotive power supply. The design provides three gate-driver outputs that are decoupled with common mode chokes, and one isolated output to serve as an Emergency Power Supply (EPS) output. It is intended for use in 800 VDC battery powered electric vehicles and supports an ultra-wide input range of 40 VDC to 950 VDC. This design uses the 1700 V rated INN3947FQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

Outputs 1 to 3 provides regulated outputs of 25.5 V which serve as low-side gate driver supplies for the traction inverter. All channels are connected through common-mode chokes to the same supply bus which is galvanically isolated from output 4. Galvanic separation between the outputs as well the use of common mode chokes prevents transient current flow between them. Output 4 provides a 24.7 V output for supplying auxiliary loads during an emergency.

The design provides reinforced isolation between the High Voltage DC (HVDC) input to all outputs by observing required creepage and clearances described in IEC 60664 parts 1 and 4. Basic isolation is provided between the gate driver output set and the EPS output

The report contains the power supply specifications, schematic, printed circuit board (PCB) layout, bill of materials (BOM), specification for the magnetics, and performance data.

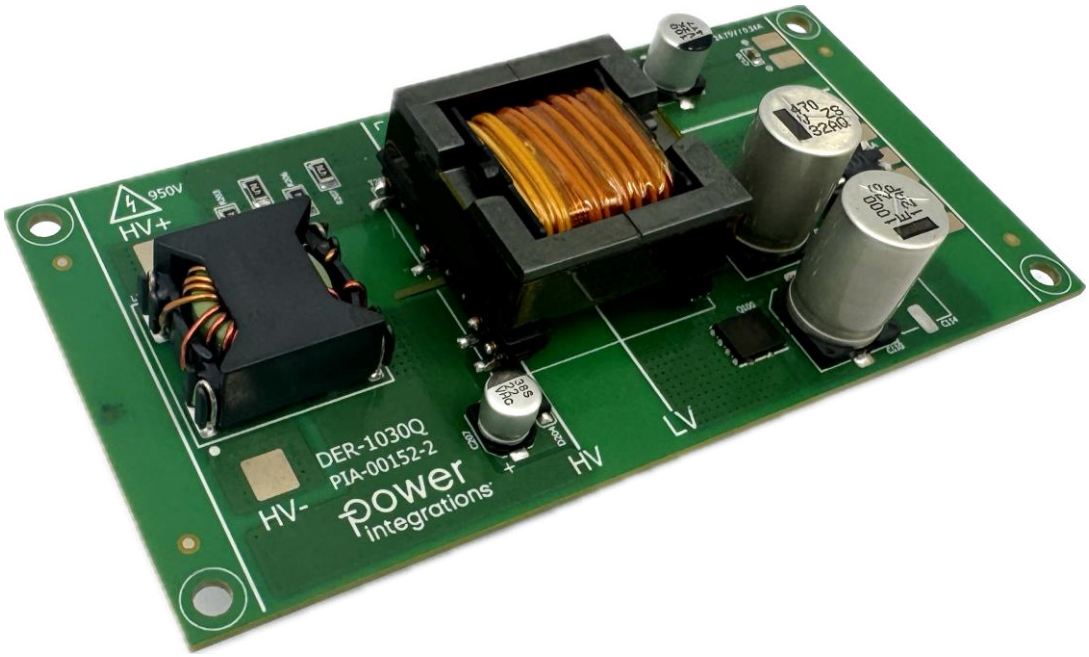


Figure 1 – Populated Circuit Board, Oblique View of Top Side.

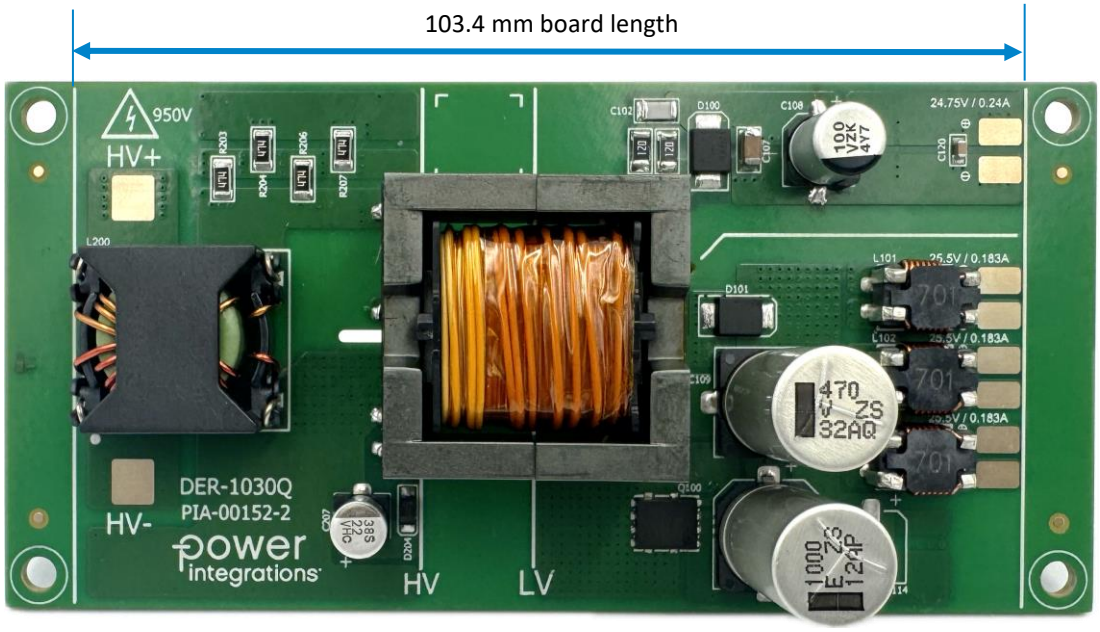


Figure 2 – Populated Circuit Board, Top View.

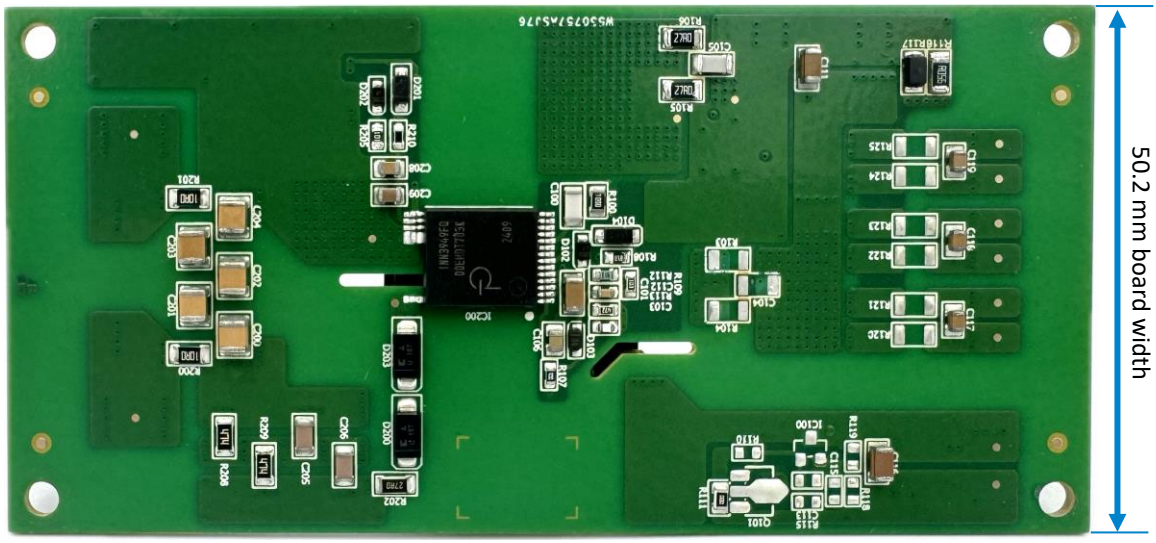


Figure 3 – Populated Circuit Board, Bottom View.

Figure 4 – Populated Circuit Board, Side View.

The three regulated 25.5 V outputs can deliver a combined total of 14 W continuously at an input voltage range of 250 VDC to 950 VDC which can be used to provide gate power for the current generation of SiC MOSFETs.

At 40 VDC input, the power capability of the 25.5 V gate driver outputs is reduced to 4 W. The 24.7 V (EPS) output can deliver 6 W from 40 VDC to 950 VDC input voltage for a total of 10 W output power at 40 VDC. This is sufficient to keep the inverter supply and control circuits operating and allows the vehicle to decelerate (and be in a safe state) in the event of system failure (functional safety requirement).

The InnoSwitch3-AQ IC maintains regulation by directly sensing the 25.5 V output voltage and providing fast, accurate feedback to the primary-side via the safety isolated FluxLink™ magneto-inductive communication link. The secondary-side controller simplifies the implementation of synchronous rectification improving overall conversion efficiency (compared to diode rectification)—saving cost and space and eliminating the need for heat sinks.

2 Design Specifications

The following tables represent the minimum acceptable performance for the design. Actual performance is listed in the Performance Data section.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV+**	40	800	950	VDC
Output Parameters					
25.5 V Output (Total of 3 x Regulated)					
Output Voltage	$\mathbf{V_{OUT\ (25.5\ V)}}$	24.2	25.5	26.8	VDC
Load and Line Regulation	$\mathbf{V_{REG\ (25.5\ V)}}$	-5		+5	%
Output Voltage Ripple Measured on Board	$\mathbf{V_{RIPPLE\ (25.5\ V)}}$		500		mV
Output Overshoot / Output Undershoot	$\mathbf{\Delta V_{OUT\ (25.5\ V)}}$		±5		%
Output Current	$\mathbf{I_{OUT\ (25.5\ V)}}$			555	mA
Continuous Output Power	$\mathbf{P_{OUT(25.5\ V)}}$	1.4		14	W
24.7 V Output (1 x Un-Regulated)					
Output Voltage	$\mathbf{V_{OUT\ (24.7\ V)}}$	23.7	24.7	27.4	VDC
Load and Line Regulation	$\mathbf{V_{REG\ (24.7\ V)}}$	-4		+11	%
Output Voltage Ripple Measured on Board	$\mathbf{V_{RIPPLE\ (24.7\ V)}}$		900		mV
Output Overshoot / Output Undershoot	$\mathbf{\Delta V_{OUT\ (24.7\ V)}}$		±6		%
Output Current	$\mathbf{I_{OUT\ (24.7\ V)}}$			242	mA
Continuous Output Power	$\mathbf{P_{OUT(24.7\ V)}}$	1.8		6	W
Total Output Power Derating					
Continuous Output Power at 40 VDC Input	$\mathbf{P_{OUT}}$			10	W
Continuous Output Power at 250 VDC to 950 VDC Input				20	W
Operating Parameters					
Operating Switching Frequency	$\mathbf{f_{SW}}$			58	kHz

Table 1 – Electrical Requirements.

2.2 Isolation

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3947FQ	BV_{DSS}			1700	V
System Voltage	V_{SYSTEM}			1200	V
Working Voltage	$V_{WORKING}$			950	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175			
Rated Impulse Voltage	$V_{IMPULSE}$			2.5	kV
Altitude Correction Factor for h_a	C_{ha}			1.59	
Basic Clearance Distance Requirement	CLR_{BASIC}	2.4			mm
Reinforced Clearance Distance Requirement	$CLR_{REINFORCED}$	4.8			mm
Basic Creepage Distance Requirement for PCB	$CPG_{BASIC(PCB)}$	5.0			mm
Reinforced Creepage Distance Requirement for PCB	$CPG_{REINFORCED(PCB)}$	10.0			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	V_{ISO}	5000			V_{PK}
Partial Discharge Test Voltage	V_{PD_TEST}	1800			V_{PK}

Table 2 – Isolation Requirements[3].

2.3 Environmental Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	T_a	-40		85	°C
Altitude of Operation	h_a			5500	m
Relative Humidity	**RH**			85.0	%

Table 3 – Environmental Requirements.

[3] Clearance and creepage distances were derived from IEC 60664-1 and IEC 60664-4.

3 Schematic

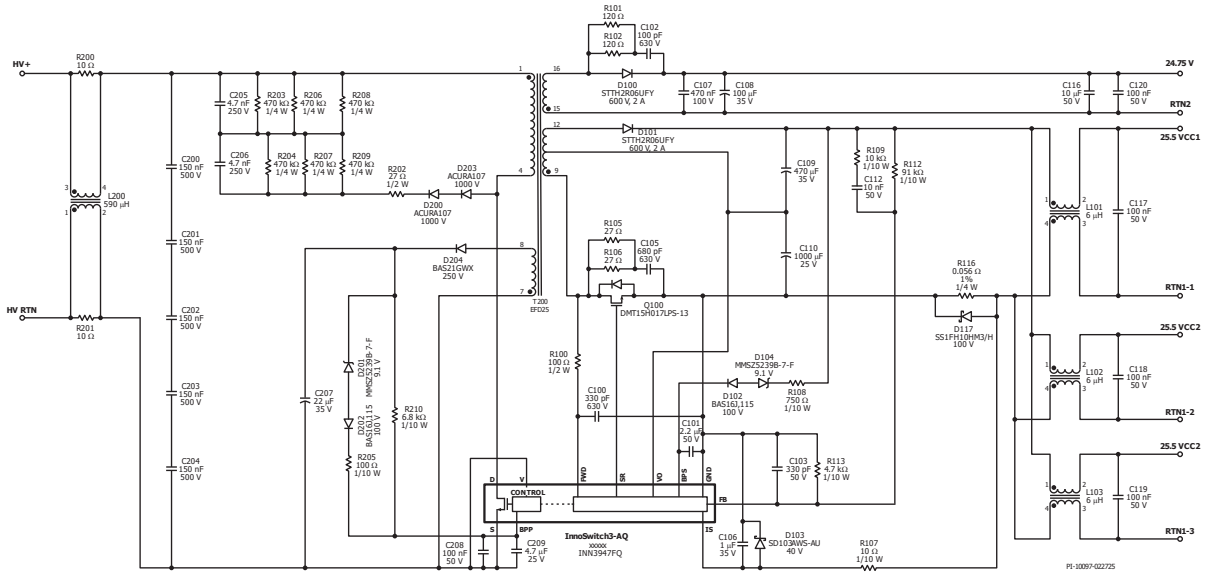


Figure 5 – DER-1030Q Schematic.

4 Circuit Description

4.1 Input Filter

The automotive inverter environment is harsh, characterized by high dv/dt and di/dt from the switching action of the power modules. Large common-mode currents are generated across the isolation barrier of the power supply which can interfere with both its operation and that of other inverter blocks, compromising the integrity of signal measurement. The input common-mode choke L200 together with the bypass capacitors C200 to C204 help filter unwanted noise to prevent it from affecting the overall performance of the design.

Common-mode inductor L200 was selected to enable the reference board to withstand the Power Integrations internal Resistance-to-ripple-on-high-voltage-network test. The test injects high frequency ripple onto the high-voltage input to simulate the actual DC-link capacitor ripple seen in a traction inverter. The final value of L200 will depend on the application requirement - higher noise will require an increased inductance value. Consideration should be given to the DC resistance (DCR) of the inductor which increases with higher inductance and will impact the overall efficiency of the design.

Bypass capacitors C200 to C204 were selected so as not to exceed 65% of their voltage rating as well as to maintain enough pad separation to ensure that the design meets creepage and clearance requirements.

4.2 High-Voltage Circuit

The power supply uses a flyback converter topology that provides isolated low-voltage outputs from the high-voltage input. The primary winding of the flyback transformer T200 is connected between the high-voltage DC input and the drain terminal of the 1700 V SiC power switch which is internal to the InnoSwitch3-AQ IC.

An R2CD-type (Resistor-Resistor-Capacitor-Diode) snubber circuit was placed across the primary winding, to limit the drain-source voltage peak during turn-off. Two super-fast diodes (D200 and D203) were placed in series to meet creepage and clearance requirements and ensure that the reverse voltage across the diodes would not exceed 70% of their maximum rating. Capacitors C205 and C206 capture energy from the leakage inductance of transformer T200. The capacitor values were selected to minimize the voltage ripple across the snubber resistor network and maintain nearly constant power dissipation across the switching period. Resistors R203, R204, R206, R207, R208 and R209 dissipate the energy stored in the snubber capacitors. The resistor values were selected such that the average voltage across each does not exceed 80% of their maximum rating and in power dissipation that was below 50% of maximum rating.

During normal operation, the primary side is powered by an auxiliary winding on transformer T200. This improves efficiency and reduces the heating of the InnoSwitch3-AQ IC. The auxiliary winding output is rectified, and DC filtered using diode D204 and capacitor C207. The InnoSwitch3-AQ is self-starting, using an internal high-voltage current source to charge the Bias Power Pin (BPP) capacitors, C208 and C209. Current is injected into the BPP capacitors through resistor R210. Diodes D201, D202, and resistor R205 serve as a primary-sensed

output overvoltage protection (primary OVP) circuit, which injects current to the BPP pin of InnoSwitch3-AQ IC during output overvoltage events, driving the IC to enter auto-restart (AR) if the fault is present.

4.3 Low Voltage Circuit

The secondary-side of the InnoSwitch3-AQ IC provides output voltage sensing, output current sensing, and gate drive for the secondary MOSFET providing synchronous rectification (SR).

Transformer T200 was designed such that at 950 VDC input, inductance is high enough so as to not mis-trigger SOA protection while being capable of delivering the required power at 40 VDC. At 40 VDC, the design was made to operate at CCM to maximize available power. This was done by minimizing the turns ratio. This resulted in an increase to the voltage on the FWD pin. In order to mitigate this and ensure that the FWD pin and VOUT pin rating would not be exceeded, the 25.5 V output winding was split into two and configured as stacked winding.

The voltage across the upper stack winding of 25.5 V output is rectified by the freewheeling diode D101 and is filtered by the capacitors C109 and C110. The voltage across the lower stack of the 25.5 V winding is rectified by SR FET Q100, then filtered by output capacitor C110. An RCD (Resistor-Capacitor-Diode) snubber formed by resistors R105, R106 and capacitor C105 damps the high-frequency ringing across the Drain-Source nodes of the SR FET. Values of C109 and C110 were selected to properly shape the currents of the secondary winding and minimize current imbalance between the upper and lower stacked windings.

The secondary-side controller of the InnoSwitch3-AQ IC also manages the switching of the SR FETs and the primary switch. Timing for the SR circuit is based on the negative edge voltage transition sensed by the Forward (FWD) pin via resistor R100. Capacitor C100 and resistor R100 form a low-pass filter that reduces voltage spikes seen by the FWD pin and ensures that the maximum rating of 150 V is not exceeded.

In continuous conduction mode (CCM) operation, the SR MOSFET is turned off just before the secondary-side controller requests a new switching cycle from the primary. In discontinuous conduction mode (DCM), the SR MOSFET is turned off when the voltage across it exceeds $V_{SR(TH)}$ (~-3.3 mV). Secondary-side control of the primary-side switch prevents cross-conduction, ensuring reliable circuit operation.

The secondary-side of the InnoSwitch3-AQ IC is self-powered from either the secondary winding forward voltage (through R100 and the FWD pin) or by the output voltage (through the VOUT pin). The Bias Power Supply (BPS) capacitor C101 is charged via an internal regulator in both cases. The VOUT pin is supplied by the lower stack of the 25.5 V winding to keep the maximum voltage below the VOUT pin limit of 27 V.

Diodes D102, D104, and resistor R108 form the secondary-side output overvoltage protection circuit. During output overvoltage events, the diodes conduct, and current is injected into the BPS pin of InnoSwitch3-AQ IC, triggering AR. This network protects against faults on the secondary side when the secondary controller is functioning. When the secondary controller is not functional, the use of a primary side BPP pin-based output overvoltage (OV) function is recommended.

The InnoSwitch3-AQ IC has an internally generated precision reference of 1.265 V that is presented on the FB pin. Resistor R112 and R113 form a voltage divider network that provides an analog of the output voltage to the FB pin. Capacitor C103 provides decoupling of high frequency noise. C110 and R109 increase the ripple content of the signal provided to the FB pin for improved transient response and lower output ripple.

The output current sense resistor R116 sets the output current limit. The voltage across R116 is compared to an internal threshold of around 35 mV. Once reached, secondary requests will be inhibited, causing output voltage to drop. The IC will enter auto-restart (AR) operation when the output voltage falls 10% below regulation during Constant Current (CC) mode and recovers when the load current is reduced below the CC limit. Capacitor C106 and resistor R107 form a low-pass filter that reduces the high-frequency noise seen by the IS pin. During output short circuit events, diodes D117 and D103 provide protection to R116 and the IS pin of the InnoSwitch3-AQ IC, respectively by allowing a large amount of current to pass to ground through themselves.

The voltage across the 24.7 V winding of transformer T200 is rectified by the freewheeling diode D100 and is filtered by the capacitors C107, C108, C116 and C120. An RCD snubber formed by resistors R101, R102 and capacitor C102 damps the high-frequency ringing across the diode. Regulation of the 24.7 V output depends on good coupling (low leakage inductance) of its winding to the 25.5 V outputs. This is addressed in the section on transformer design.

5 PCB Layout

Layers: Six (6) (typical for traction inverter control board)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 1 oz

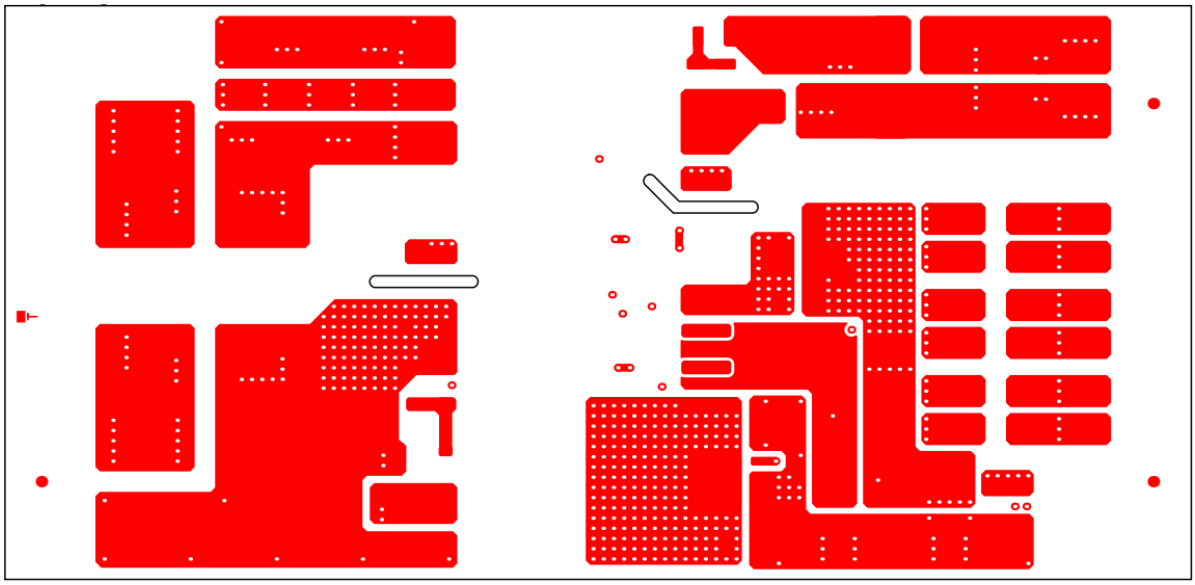


Figure 6 – DER-1030Q Top Layer PCB Layout.

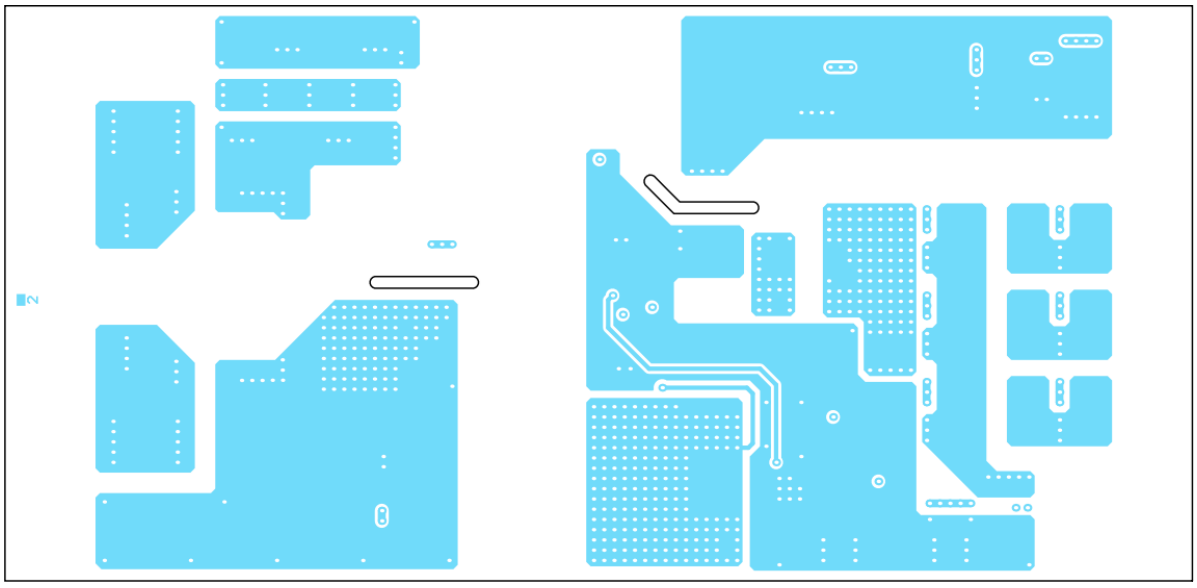


Figure 7 – DER-1030Q Mid-Layer 1 PCB Layout.

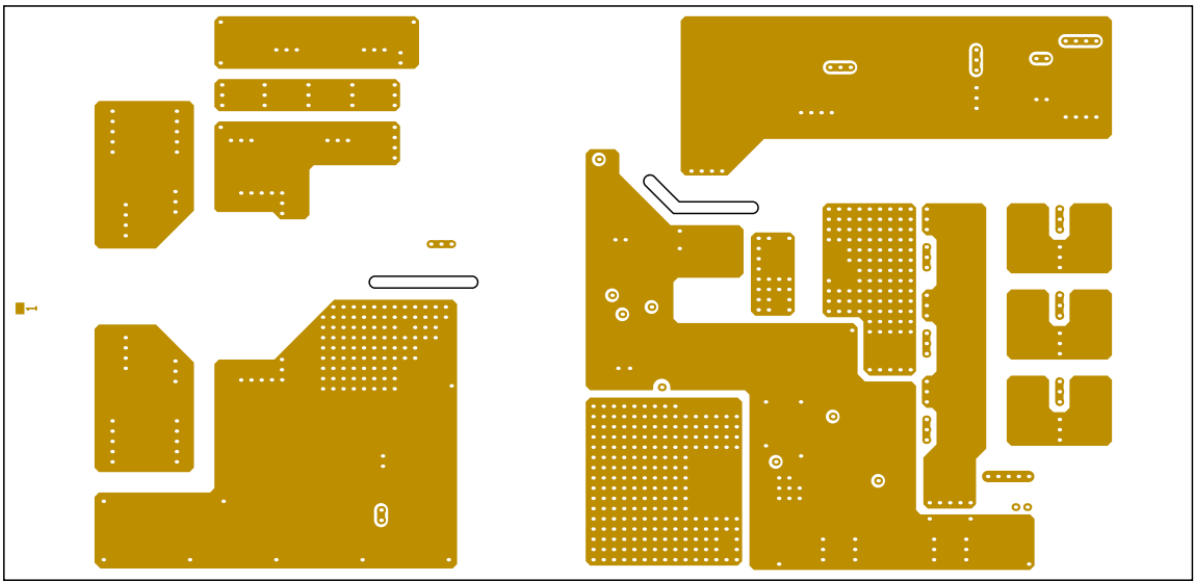


Figure 8 – DER-1030Q Mid-Layer 2 PCB Layout.

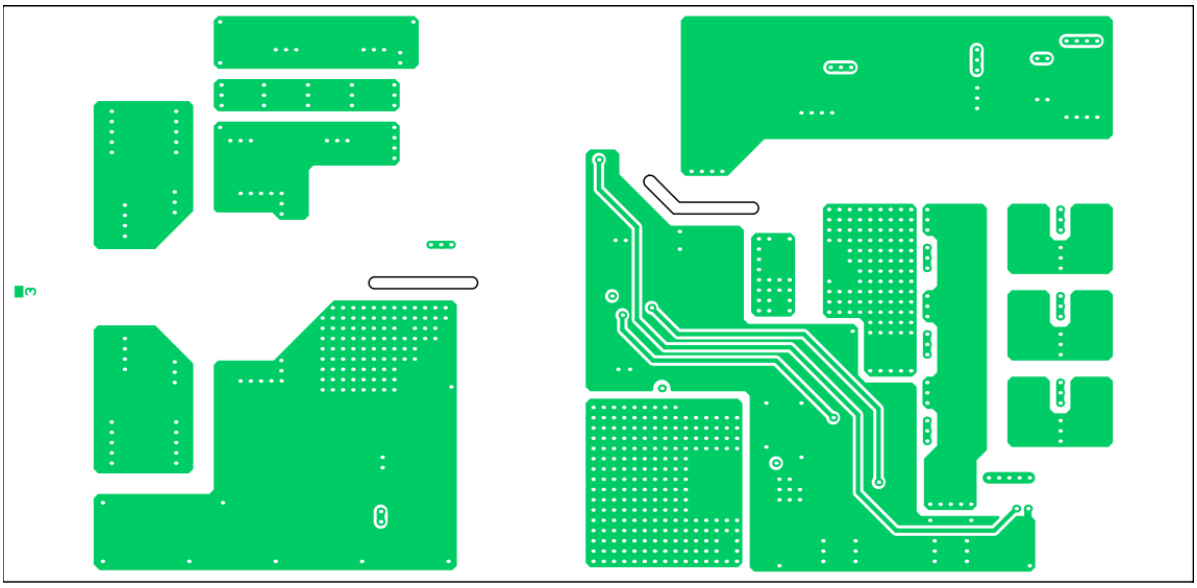


Figure 9 – DER-1030Q Mid-Layer 3 PCB Layout.

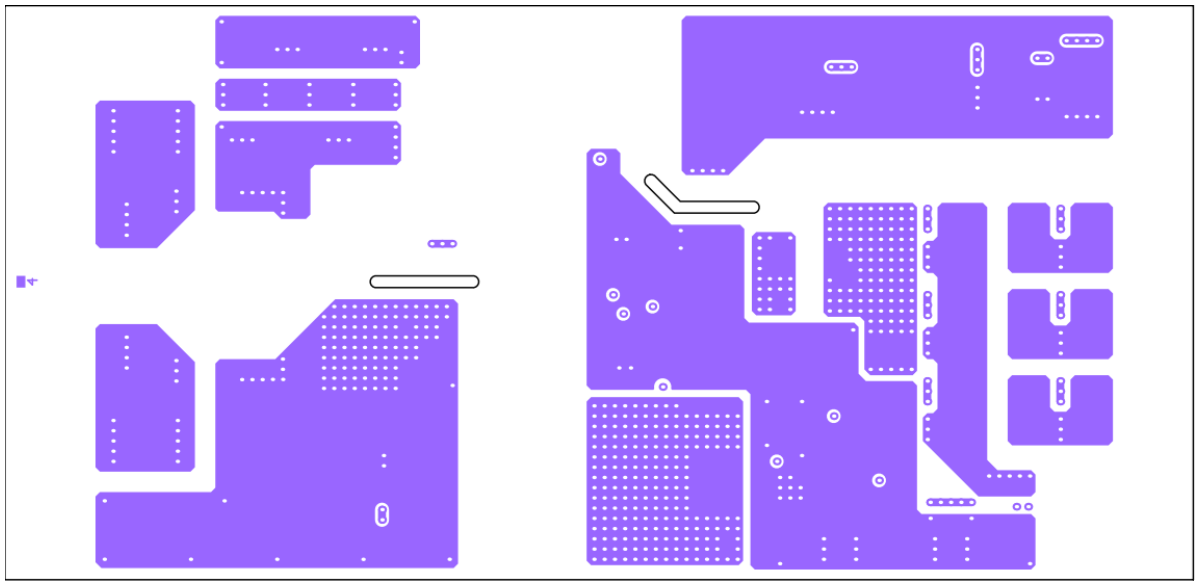


Figure 10 – DER-1030Q Mid-Layer 4 PCB Layout.

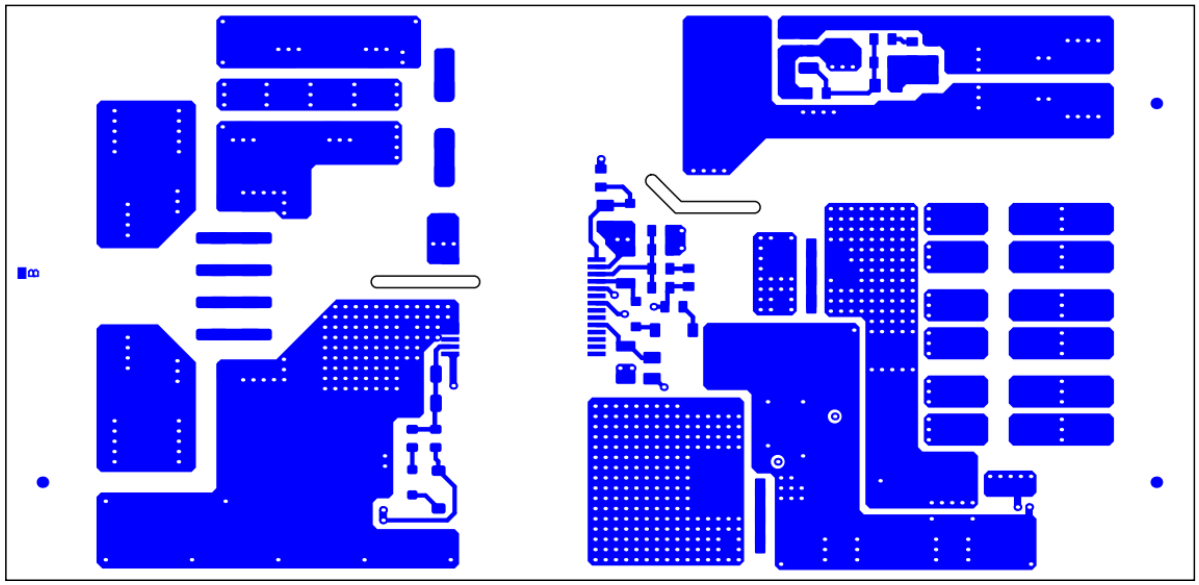


Figure 11 – DER-1030Q Bottom Layer PCB Layout.

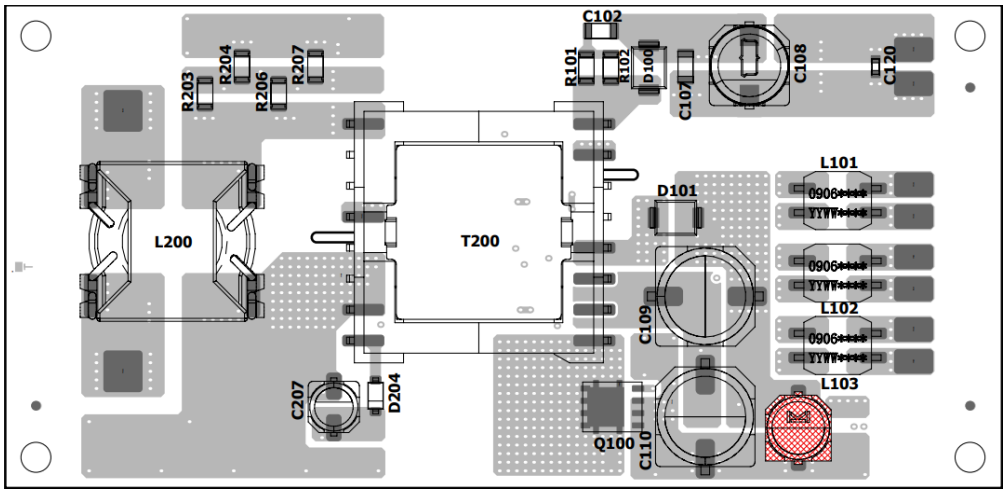


Figure 12 – DER-1030Q Board Assembly (Top).[4]

Figure 13 – DER-1030Q Board Assembly (Bottom).[5]

[4, 5] The components marked in red are components that are not populated in the assembly and excluded from the Bill of Materials (BOM) count.

6 Bill of Materials

Item	Qty.	Designator	Description	MFR Part Number	Manufacturer
1	1	C100	330 pF ±5% 630 V Ceramic Capacitor C0G, NP0 1206 (3216 Metric)	CGA5C4C0G2J331J060AA	TDK
2	1	C101	2.2 µF ±10% 50 V Ceramic Capacitor X7R 1206 (3216 Metric)	GCM31CR71H225KA55K	Murata Electronics
3	1	C102	100 pF ±5% 630 V Ceramic Capacitor C0G, NP0 1206 (3216 Metric)	CGA5C4C0G2J101J060AA	TDK
4	1	C103	330 pF ±5% 50 V Ceramic Capacitor C0G, NP0 0603 (1608 Metric)	C0603C331J5GACAUTO	KEMET
5	1	C105	680 pF ±5% 630 V Ceramic Capacitor C0G, NP0 1206 (3216 Metric)	CGA5F4C0G2J681J085AA	TDK
6	1	C106	1 µF ±10% 35 V Ceramic Capacitor X7R 0805 (2012 Metric)	GMK212B7105KGHT	TAIYO YUDEN
7	2	C107, C111	0.47 µF ±10% 100 V Ceramic Capacitor X7R 1206 (3216 Metric)	HMK316B7474KLHT	Taiyo Yuden
8	1	C108	100 µF 35 V Aluminum - Polymer Capacitors Radial, Can - SMD 35mOhm 4000 Hrs @ 125°C	EEH-ZK1V101XP	Panasonic
9	1	C109	470 µF 35 V Aluminum - Polymer Capacitors Radial, Can - SMD 11mOhm 4000 Hrs @ 125°C	EEH-ZS1V471P	Panasonic
10	1	C110	1000 µF 25 V Aluminum - Polymer Capacitors Radial, Can - SMD 11mOhm 4000 Hrs @ 125°C	EEH-ZS1E102UP	Panasonic
11	1	C112	10000 pF ±10% 50 V Ceramic Capacitor X7R 0603 (1608 Metric)	GCM188R71H103KA37J	Murata Electronics
12	1	C116	10 µF ±10% 50 V Ceramic Capacitor X7R 1206 (3216 Metric)	CGA5L1X7R1H106K160AE	TDK
13	4	C117, C118, C119, C208	0.1 µF ±10% 50 V Ceramic Capacitor X7R 0805 (2012 Metric)	CGA4J2X7R1H104K125AE	TDK
14	1	C120	0.1 µF ±10% 50 V Ceramic Capacitor X7R 0603 (1608 Metric)	AC0603KRX7R9BB104	YAGEO
15	5	C200, C201, C202, C203, C204	0.15 µF ±10% 500 V Ceramic Capacitor X7R 1210 (3225 Metric)	C1210X154KCRACAUTO	KEMET
16	2	C205, C206	4700 pF ±20% 250 V Ceramic Capacitor C0G, NP0 1206 (3216 Metric)	C1206C472MAGECAUTO	KEMET
17	1	C207	22 µF 35 V Aluminum - Polymer Capacitors Radial, Can - SMD 100mOhm 4000 Hrs @ 125°C	HHXC350ARA220ME61G	United Chemi-Con
18	1	C209	4.7 µF ±10% 25 V Ceramic Capacitor X7R 0805 (2012 Metric)	C0805C475K3RACAUTO	KEMET
19	2	D100, D101	Diode 600 V 2 A Surface Mount SMBflat	STTH2R06UFY	STMicroelectronics
20	2	D102, D202	Diode 100 V 250 mA Surface Mount SOD-323F	BAS16J,115	Nexperia
21	1	D103	Diode 40 V 350 mA Surface Mount SOD-323	SD103AWS-AU_R1_000A1	Panjit International Inc.
22	2	D104, D201	Zener Diode 9.1 V 500 mW ±5% Surface Mount SOD-123	MMSZ5239B-7-F	Diodes
23	1	D117	Diode 100 V 1 A Surface Mount DO-219AB (SMF)	SS1FH10HM3/H	Vishay
24	2	D200, D203	Diode 1000 V 1 A Surface Mount DO-214AC (SMA)	ACURA107-HF	Comchip Technology
25	1	D204	Diode 200 V 225 mA Surface Mount SOD-123	BAS21GWX	Nexperia
26	1	IC200	CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3947FQ	Power Integrations
27	3	L101, L102, L103	6 uH Common-Mode Choke 7.00mm x 6.00mm	ACSR0906S060NT	SunLord

28	1	L200	590 uH Common-Mode Choke 19.6 mm x 17.00 mm x 9.9 mm	PM0353NL	Pulse
29	1	Q100	N-Channel 150 V 9.4 A (Ta), 58A (Tc) 1.3 W (Ta) Surface Mount PowerDI5060-8	DMT15H017LPS-13	Diodes
30	1	R100	100 Ohms ±1% 0.5 W, ½ W Chip Resistor 0805 (2012 Metric) Anti-Sulfur, Automotive AEC-Q200, Moisture Resistant, Pulse Withstanding Thick Film	CHP0805AFX-1000ELF	Bourns
31	2	R101, R102	120 Ohms ±5% 0.25 W, ¼ W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200 Thick Film	RMCF1206JT120R	Stackpole Electronics Inc
32	3	R105, R106, R202	27 Ohms ±1% 0.75 W, ¾ W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Pulse Withstanding Thick Film	ESR18EZPF27R0	ROHM Semiconductor
33	1	R107	10 Ohms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RMCF0603JT10R0	Stackpole Electronics Inc
34	1	R108	750 Ohms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RMCF0603JT750R	Stackpole Electronics Inc
35	1	R109	10 kOhms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	ERJ-3GEYJ103V	Panasonic
36	1	R111	0 Ohms Jumper Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200 Thick Film	ERJ-6GEY0R00V	Panasonic
37	1	R112	91 kOhms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	RK73H1JTTD9102F	KOA Speer
38	1	R113	4.7 kOhms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	ERJ-3GEYJ472V	Panasonic
39	1	R116	56 mOhms ±1% 0.25 W, ¼ W Chip Resistor 1206 (3216 Metric) Current Sense Thick Film	RL1206FR-070R056L	YAGEO
40	2	R200, R201	10 Ohms ±1% 0.25 W, ¼ W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC1206FR-0710RL	YAGEO
41	6	R203, R204, R206, R207, R208, R209	470 kOhms ±5% 0.25 W, ¼ W Chip Resistor 1206 (3216 Metric) Automotive AEC-Q200 Thick Film	RMCF1206JT470K	Stackpole Electronics Inc
42	1	R205	100 Ohms ±5% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200, Moisture Resistant Thick Film	AC0603JR-07100RL	YAGEO
43	1	R210	6.8 kOhms ±1% 0.1 W, 1/10 W Chip Resistor 0603 (1608 Metric) Automotive AEC-Q200 Thick Film	ERJ-3EKF6801V	Panasonic
44	1	T200	20 W Power Transformer		Power Integrations

Table 4 – DER-1030Q Bill of Materials[6].

[6] All components are AEC-Q qualified except for Q100 DMT15H017LPS-13, common-mode chokes and transformer.

7 Transformer Specification

7.1 Electrical Diagram

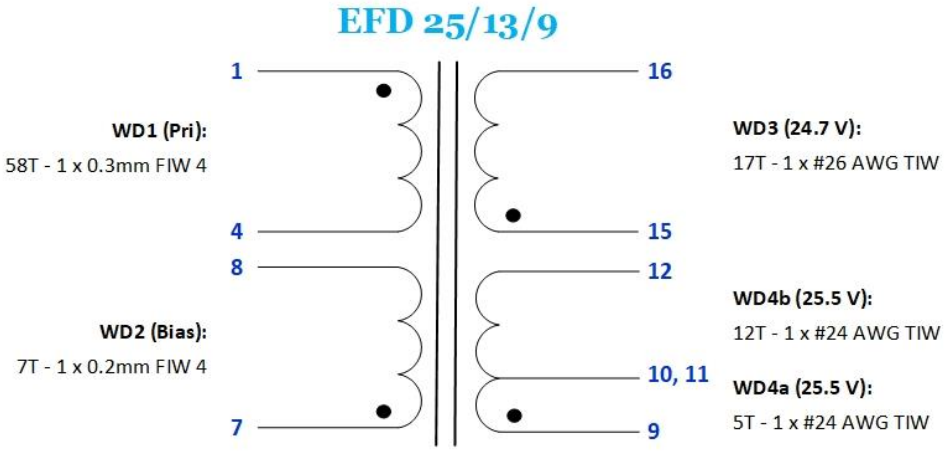


Figure 14 – Transformer Electrical Diagram.

7.2 Electrical Specification

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			20	W
Input Voltage VDC	Flyback topology	40	800	950	V
Switching Frequency	Flyback topology			58	kHz
Duty Cycle	Flyback topology			12.6	%
Np:Ns			3.4		
Rdc	WD1 (Pri)		650		mΩ
	WD2 (Bias)		190		
	WD3 (24.7 V)		115		
	WD4a (25.5 V)		27		
	WD4b (25.5 V)		55		
Coupling Capacitance	Primary side to bias side, Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 7, with pins 1 & 4 shorted and pins 7 & 8 shorted at 25 °C		33		pF
	Primary side to 25.5 V side Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 9, with pins 1 & 4 shorted, pins 10 & 11 shorted, and pins 9 & 12 shorted at 25 °C		85		
	Primary side to 24.7 V side Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 15, with pins 1 & 4 shorted and pins 15 & 16 shorted at 25 °C		74		
Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 4, with all other windings open at 25 °C		618		µH
Part to Part Tolerance	Tolerance of Primary Inductance	-5.0		5.0	%
Primary Leakage Inductance	Measured at 1 V pk-pk, 100 kHz frequency between pin 1 to pin 4, with all other Windings shorted.			6.5	µH

Table 5 – Transformer electrical specification.

7.3 Transformer Build Diagram

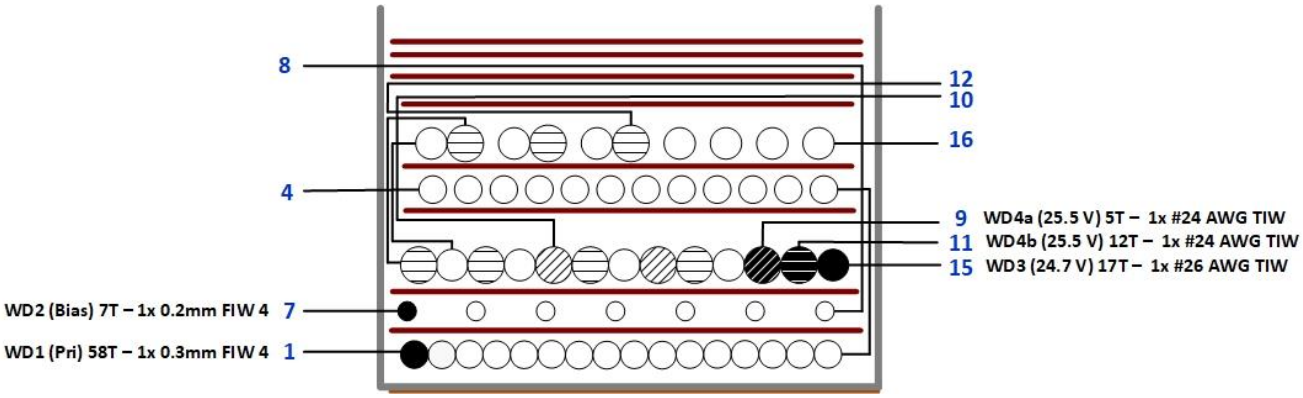


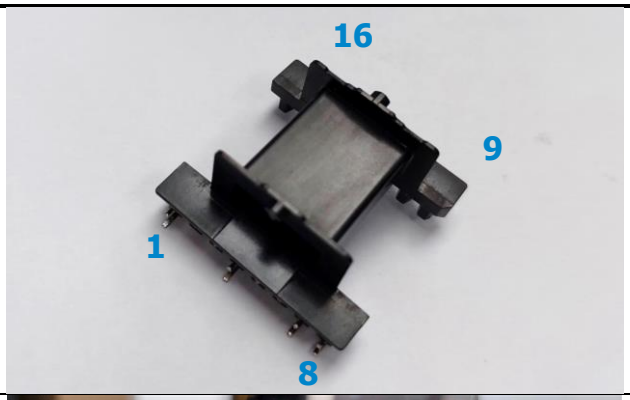
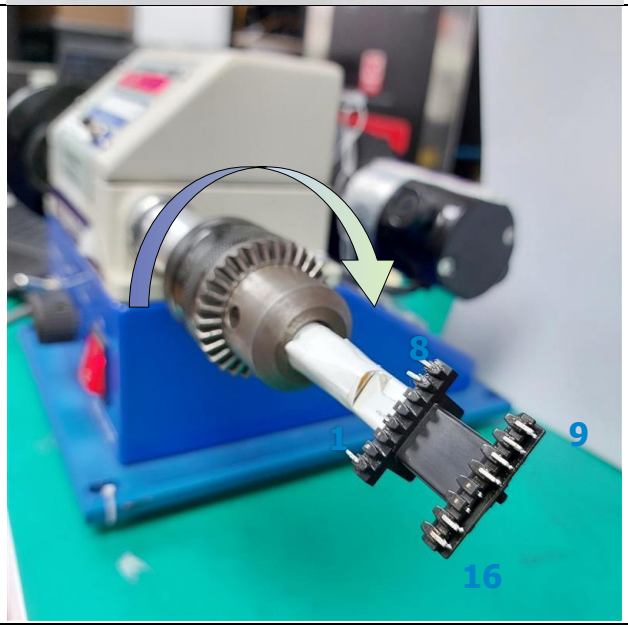
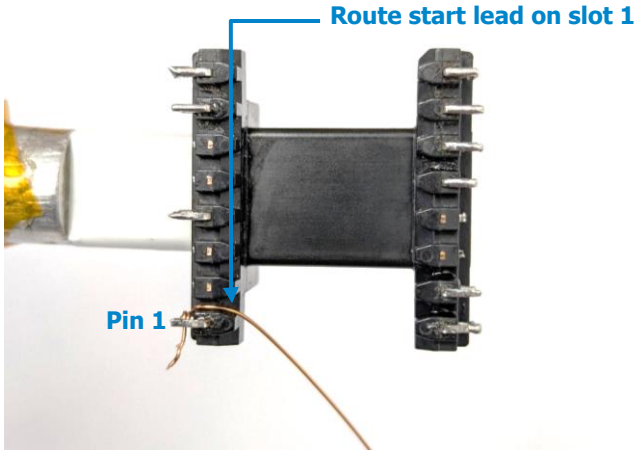
Figure 15 – Transformer Build Diagram.

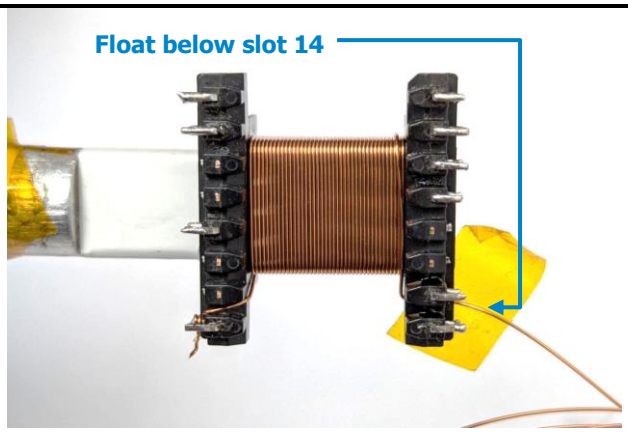
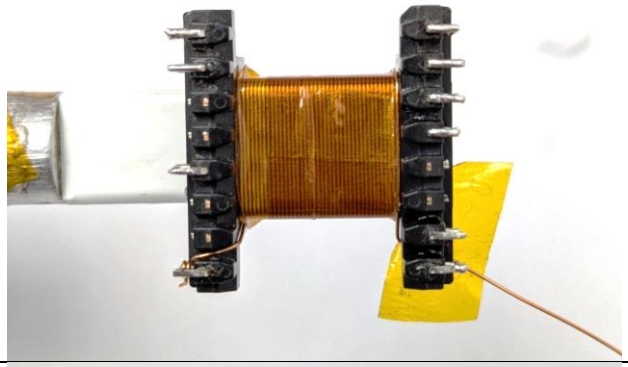
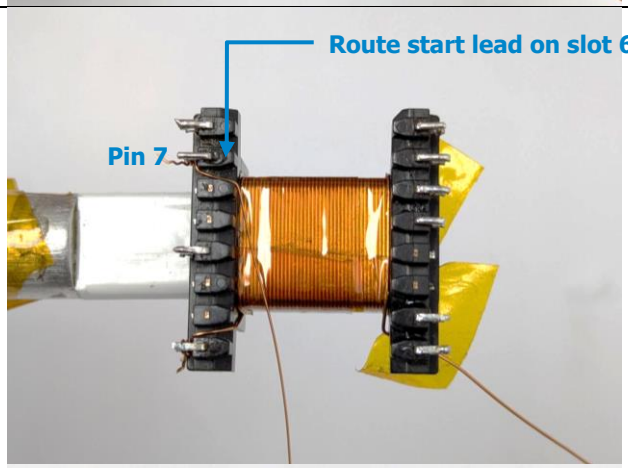
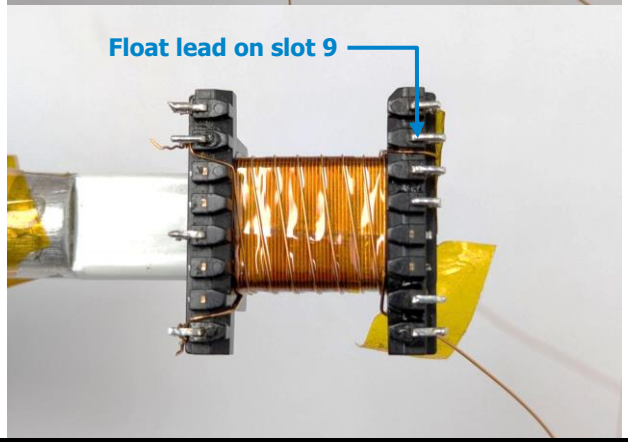
7.4 Material List

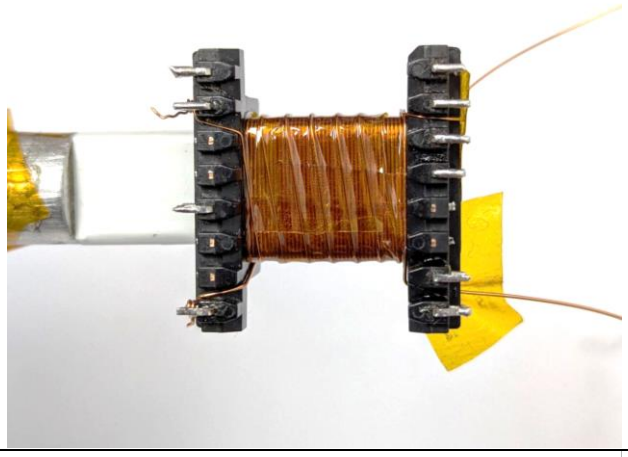
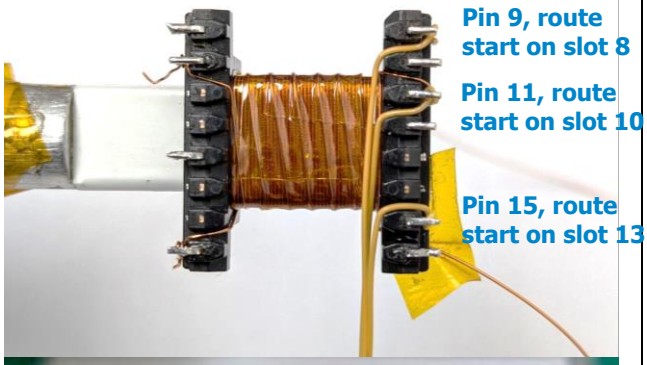
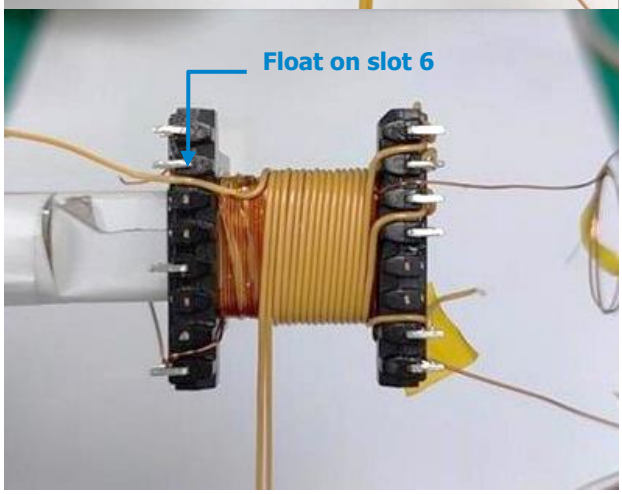
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: ATWPEF252815B303T	1	PC	CTI ≥ 600	SunLord
[2]	Core: EFD 25/13/9	2	PCS	3C96 (or equivalent)	Ferroxcube
[3]	WD1 (Pri): 0.3 mm FIW 4, Class F	2500	mm	Copper Wire	Elektrisola
[4]	WD2 (Bias): 0.2 mm FIW 4, Class F	350	mm		Elektrisola
[5]	WD3 (24.7 V): 0.4 mm (AWG 26) Triple Insulated Wire	850	mm		Furukawa Electric Co., Ltd.
[6]	WD4a (25.5 V): 0.5 mm (AWG 24) Triple Insulated Wire	300	mm		Furukawa Electric Co., Ltd.
[7]	WD4b (25.5 V): 0.5 mm (AWG 24) Triple Insulated Wire	600	mm		Furukawa Electric Co., Ltd.
[8]	3M Polyimide 5413 Amber, width: 0.625in (15.9mm)	400	mm	3M157181 (or equivalent)	3M

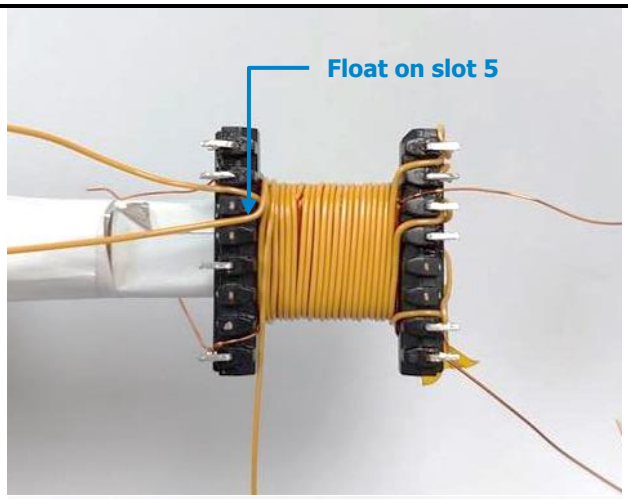
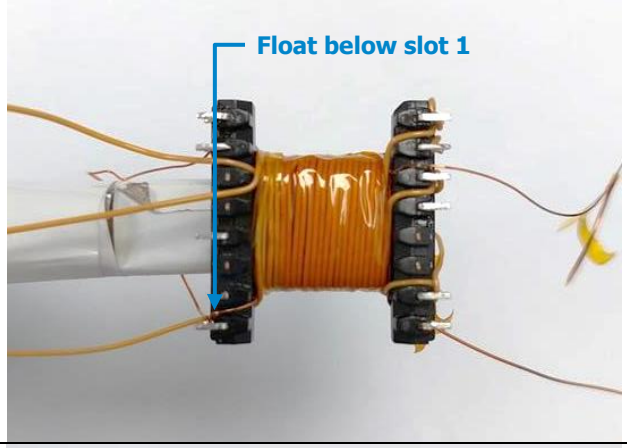
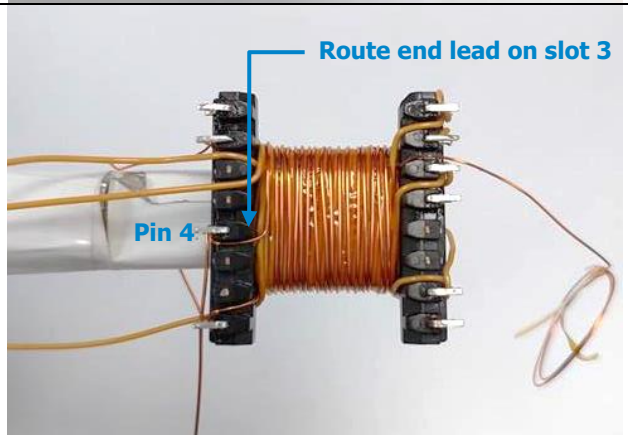
Table 6 – Transformer Bill of Materials.

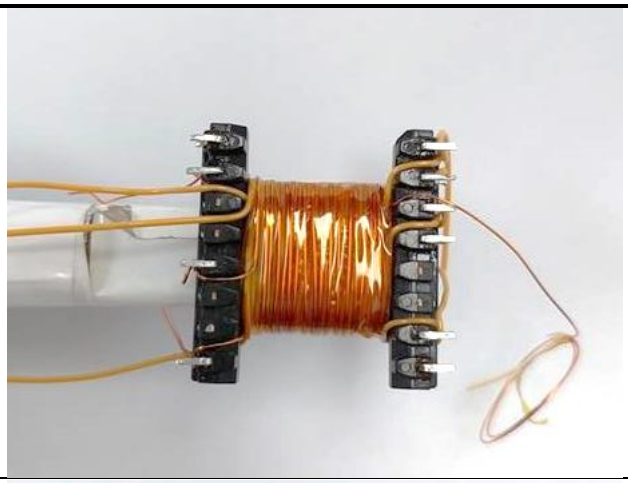
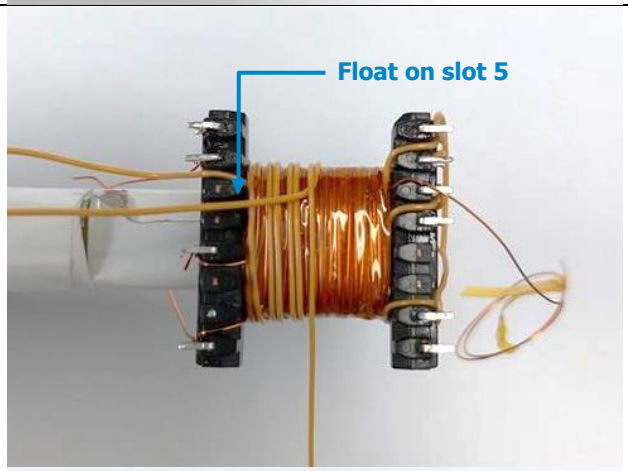
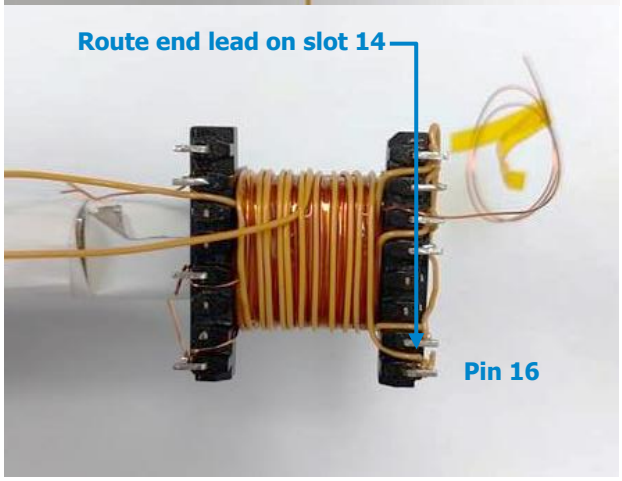
7.5 Winding Illustrations

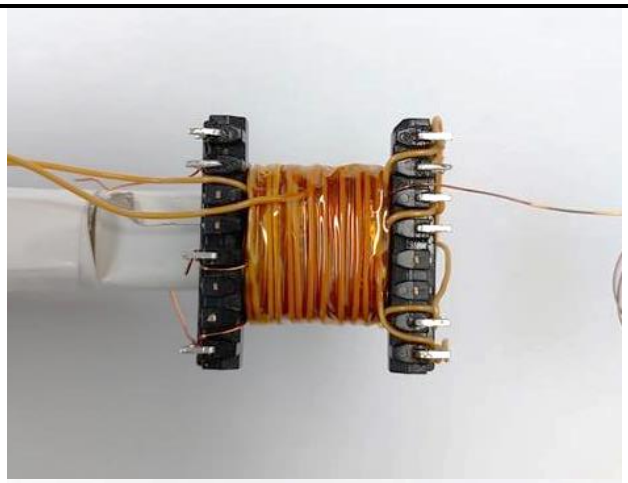
Winding Preparation		Start by removing the unused pins 2, 3, 5, 6, 13, and 14 of the bobbin (Item **[1]**)
		Position the bobbin on the mandrel such that the primary side (pins 1-8) of the bobbin is on the left side. Winding direction is clockwise direction.
WD1: Primary		Route the start lead of WDG1 from pin 1 through slot 1 and then wind 41 turns of wire Item **[3]** with tight tension, from left to right. Spread the winding evenly along the bobbin's width.

	 	Do not terminate yet. Float the lead under slot 14. Secure the winding using 1 layer of tape (Item **[8]**) .
WD2: Bias	 	Route the start lead of WDG2 from pin 7 through slot 6 and then wind 7 turns of wire Item **[4]** with tight tension, from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet. Float the lead on slot 9.

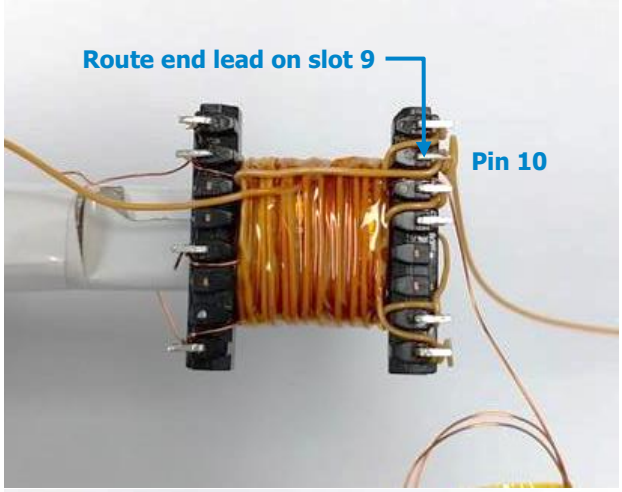
		Secure the winding using 1 layer of tape (Item **[8]**) .
WD3: **24.7 V** **WDG4a,** **WDG4b:** **25.5 V**	 	Use Item **[5]** for WDG3. Start on pin 15 and route start lead on slot 13. Use Item **[6]** for WDG4a. Start on pin 9 and route start lead on slot 8. Use Item **[7]** for WDG4b. Start on pin 11 and route start lead on slot 10. Place WDG4a on the leftmost side and WDG3 on the rightmost side. Wind all three wires together with tight tension from right to left. After 5 turns, fold the end of WDG4a to the left, then float on slot 6. Do not terminate yet.

		Continue to wind WDG3 and WDG4b for 4 more additional turns. Do not terminate yet. Float WDG3 below slot 1 and WDG4a on slot 5.
		Secure winding using 1 layer of tape (item **[8]**).
WD1: Primary		Continue to wind WDG1 from right to left for 17 more additional turns. Spread the winding evenly along the bobbin's width. Terminate the end lead to pin 4 through slot 3.

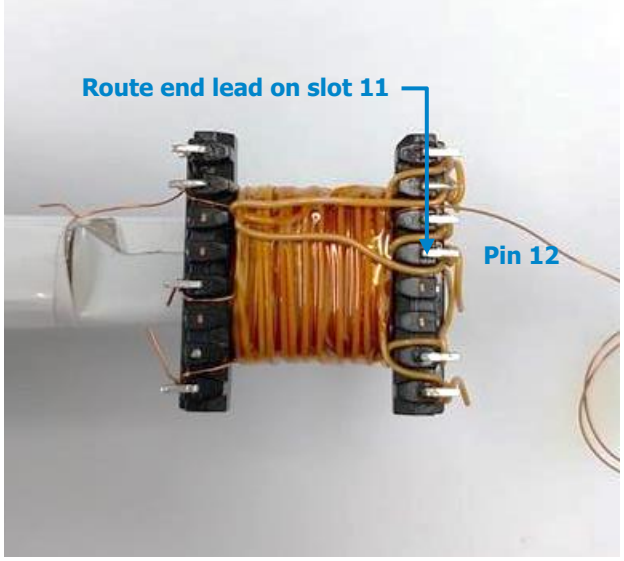
		Secure winding using 1 layer of tape (item **[8]**).
WD3: **24.7 V** **WDG4b:** **25.5 V**	 	Continue to wind WDG3 and WD4b with WD3 on the left side and WDG4b on the right side. After the 3 turns, fold WDG4b to the left and float on slot 5. Continue to wind WDG3 for 5 more additional turns and finally terminating on pin 16 routed through slot 14.



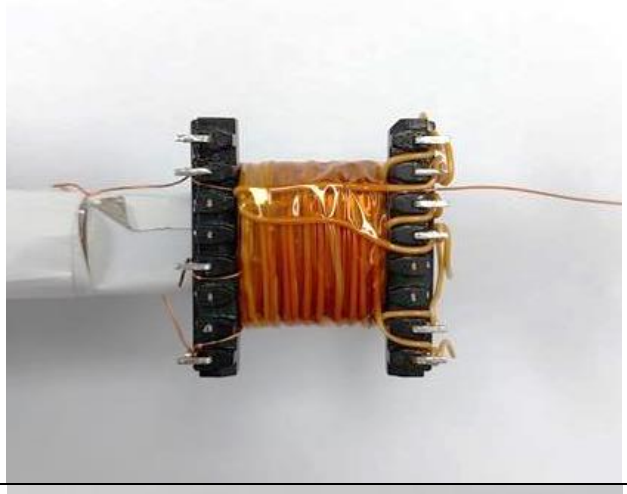
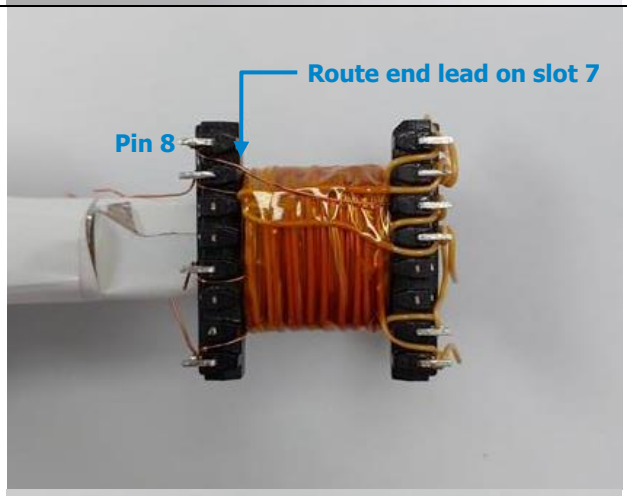
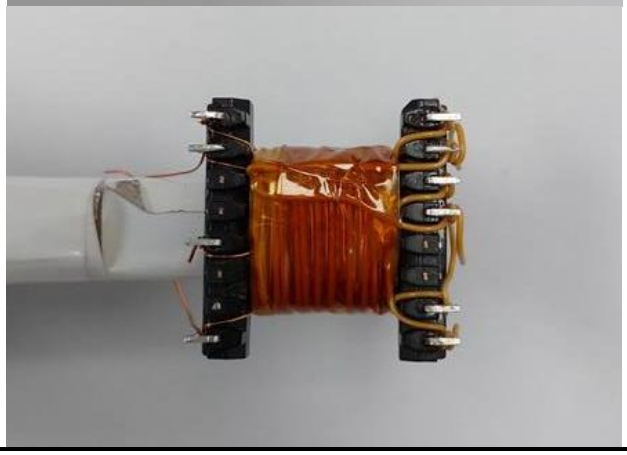
Secure winding using 1 layer of tape (item **[8]**).

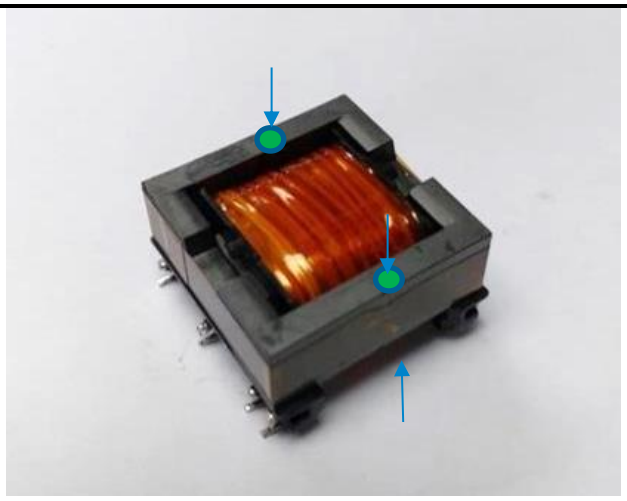


Terminate WDG4a to pin 10 with end lead routed through slot 9.



Terminate WDG4b to pin 12 with end lead routed through slot 11.

		Secure winding using 1 layer of tape (item **[8]**).
WD2: Bias		Terminate WDG2 to pin 8 with end lead routed through slot 7.
		Finish up by covering the winding with 2 layers of tape (item **[8]**).

Finishing		Solder all terminated pins (pins 1, 4, 7, 8, 9, 10, 11, 12, 15, and 16). Gap one of the core halves (item **[2]**) and fasten the core tightly to get 618 µH ± 5% of inductance between pins 1 and 4. In fastening the core, it is preferred to use glue instead of tape that is used in the illustration (see blue arrows for the preferred gluing points – 2 points on top and 2 points on the bottom.)

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_092324; Rev.4.0; Copyright Power Integrations 2024	*INPUT*	*INFO*	*OUTPUT*	*UNITS*	*InnoSwitch3-AQ Flyback Design Spreadsheet*
2	**APPLICATION VARIABLES**					
3	VOUT	25.5		25.5	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	950.00		950.00	V	Input DC voltage 1
6	IOUT1	0.785		0.785	A	Output current 1
7	POUT1			20.02	W	Output power 1
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	800.00		800.00	V	Input DC voltage 2
13	IOUT2	0.785		0.785	A	Output current 2
14	POUT2			20.02	W	Output power 2
15	EFFICIENCY2			0.85		Converter efficiency for output 2
16	Z_FACTOR2			0.50		Z-factor for output 2
18	**OPERATING CONDITION 3**					
19	VINDC3	250.00		250.00	V	Input DC voltage 3
20	IOUT3	0.785		0.785	A	Output current 3
21	POUT3			20.02	W	Output power 3
22	EFFICIENCY3			0.85		Converter efficiency for output 3
23	Z_FACTOR3			0.50		Z-factor for output 3
67	TEMPERATURE_AMBIENT			40.0	°C	System ambient temperature
71	**PRIMARY CONTROLLER SELECTION**					
72	ILIMIT_MODE	INCREASED		INCREASED		INCREASED Device current limit mode
73	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
74	DEVICE_GENERIC			INN39X7		Device selection
75	DEVICE_CODE	INN3947FQ		INN3947FQ		Device code
76	PDEVICE_MAX			50	W	Device maximum power capability
77	RDSON_25DEG			1.53	Ω	Primary switch on-time resistance at 25°C
78	RDSON_125DEG			3.12	Ω	Primary switch on-time resistance at 125°C
79	ILIMIT_MIN			1.674	A	Primary switch minimum current limit
80	ILIMIT_TYP			1.800	A	Primary switch typical current limit
81	ILIMIT_MAX			1.926	A	Primary switch maximum current limit
82	VDRAIN_ON_PRSW			0.27	V	Primary switch on-time voltage drop
83	VDRAIN_OFF_PRSW			1066	V	Peak drain voltage on the primary switch during turn-off at maximum input DC voltage and allowable leakage ring
84	VCLAMP			116.0	V	Voltage across clamp circuit
85	CU_AREA_INNO			1.00	in2	Primary switch copper cooling area
86	TEMP_INNO_MIN			50.55	°C	Device minimum operating temperature with respect to ambient, observed at 800V VINDC
87	TEMP_INNO_MAX			58.90	°C	Device maximum operating temperature with respect to ambient, observed at 250V VINDC
91	**WORST CASE ELECTRICAL PARAMETERS**					
92	FSWITCHING_MAX	37485		37485	Hz	Maximum switching frequency at full load and minimum DC input voltage
93	VOR	86.0		86.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
94	KP			2.381		Measure of continuous/discontinuous mode of operation
95	MODE_OPERATION			DCM		Mode of operation

96	DUTYCYCLE			0.126		Primary switch duty cycle
97	TIME_ON_MIN			0.869	us	Minimum primary switch on-time
98	TIME_ON_MAX			3.89	us	Maximum primary switch on-time
99	TIME_OFF			23.37	us	Primary switch off-time
100	LPRIMARY_MIN			586.7	uH	Minimum primary magnetizing inductance
101	LPRIMARY_TYP			617.6	uH	Typical primary magnetizing inductance
102	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
103	LPRIMARY_MAX			648.5	uH	Maximum primary magnetizing inductance
105	**PRIMARY CURRENT**					
106	IAVG_PRIMARY			0.087	A	Primary switch average current
107	IPEAK_PRIMARY			1.530	A	Primary switch peak current
108	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
109	IRIPPLE_PRIMARY			1.530	A	Primary switch ripple current
110	IRMS_PRIMARY			0.298	A	Primary switch RMS current
114	**TRANSFORMER CONSTRUCTION PARAMETERS**					
115	**CORE SELECTION**					
116	CORE	EFD25		EFD25		Core selection
117	CORE NAME			EFD25/13/9 -3C96		Core code
118	AE			58.0	mm^2	Core cross sectional area
119	LE			57.0	mm	Core magnetic path length
120	AL			2000	nH	Ungapped core effective inductance per turns squared
121	VE			3300	mm^3	Core volume
122	BOBBIN NAME			EFD25/13/9 - 2 (P5-S5)		Bobbin name
123	AW			40.2	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
124	BW			16.40	mm	Bobbin width
125	BH			3.11	mm	Bobbin height
126	MARGIN			0.0	mm	Bobbin safety margin
128	**PRIMARY WINDING**					
129	NPRIMARY			58		Primary winding number of turns
130	BPEAK			3800	Gauss	Peak flux density
131	BMAX			2885	Gauss	Maximum flux density
132	BAC			1443	Gauss	AC flux density (0.5 x Peak to Peak)
133	ALG			184	nH	Typical gapped core effective inductance per turns squared
134	LG			0.361	mm	Core gap length
136	**SECONDARY WINDING**					
137	NSECONDARY	17		17		Secondary winding number of turns
139	**BIAS WINDING**					
140	NBIAS			7		Bias winding number of turns
144	**PRIMARY COMPONENTS SELECTION**					
145	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
146	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
147	**UNDERVOLTAGE PARAMETERS**					
148	BROWN-IN REQUIRED	40.00		40.00	V	Required DC bus brown-in voltage threshold
149	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
150	VZ			9.10	V	Zener diode reverse voltage
151	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
152	ILKG			2.00	uA	Zener diode maximum reverse leakage current (at high ambient temperatures, typically 125 degC)

153	ILKG_MIN			0.10	uA	Zener diode minimum reverse leakage current (at low ambient temperatures, typically 25 degC)
154	BROWN-IN ACTUAL			26.91 - 39.47	V	Actual brown-in voltage range using standard resistors considering tolerances due to part and temperature variations
155	BROWN-OUT ACTUAL			24.13 - 35.46	V	Actual brown-out voltage range using standard resistors considering tolerances due to part and temperature variations
156	**OVERVOLTAGE PARAMETERS**					
157	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
158	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
159	VF				V	OV diode forward voltage
160	VRRM				V	OV diode reverse voltage
161	PIV				V	OV diode peak inverse voltage
162	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
163	**DC BUS SENSE RESISTORS**					
164	RLS_H			1.04	MΩ	Connect six 174 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold
165	RLS_L			124.00	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
168	**BIAS WINDING**					
169	VBIAS	9.00		9.00	V	Rectified bias voltage
170	VF_BIAS			0.70	V	Bias winding diode forward drop
171	VREVERSE_BIASDIODE			123.66	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
172	CBIAS			22	uF	Bias winding rectification capacitor
173	CBPP			4.70	uF	BPP pin capacitor
177	**SECONDARY COMPONENTS SELECTION**					
178	**FEEDBACK COMPONENTS**					
179	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
180	RFB_LOWER			5.23	kΩ	Lower feedback resistor
181	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
185	**MULTIPLE OUTPUT PARAMETERS**					
186	**OUTPUT 1**					
187	VOUT1			25.5	V	Output 1 voltage
188	IOUT1	0.549		0.549	A	Output 1 current
189	POUT1			14.00	W	Output 1 power
190	IRMS_SECONDARY1			1.213	A	Root mean squared value of the secondary current for output 1
191	IRIPPLE_CAP_OUTPUT1			1.081	A	Current ripple on the secondary waveform for output 1
192	NSECONDARY1			17		Number of turns for output 1
193	VREVERSE_RECTIFIER1		Warning[7]	303.95	V	Assuming this output is connected to the FWD pin, then the voltage stress may exceed the FWD pin voltage rating of 150V. Increase the VOR to reduce voltage stress and allow for sufficient margin
194	SRFET1	DMT15H017LPS-13	Warning	DMT15H017LPS-13		Expected voltage stress (including the parasitic ring) on the secondary MOSFET selected exceeds the device

[7] The warnings on lines 193 and 194 are disregarded since actual SR FET and FWD pin voltage should be 5/17 of the value shown in line 193 (based on the number of turns of the lower stack winding).

						BVDSS: pick a MOSFET with a higher BVDSS
195	NUM_SRFET1	1		1		Number of SRFETs in parallel for output 1
196	VF_SRFET1			0.80	V	SRFET typical on-time drain voltage for output 1
197	VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
198	RDSON_SRFET1			37.0	mΩ	SRFET estimated on-time drain resistance at 100°C and VGS=4.4V for output 1
199	RTHJA_SRFET1			53.00	°C/W	SRFET max. thermal impedance for output 1
200	TEMP_SRFET1_MIN			58.3	°C	SRFET minimum operating temperature for output 1 (for each SRFET in parallel) with respect to ambient, observed at 800V VINDC
201	TEMP_SRFET1_MAX			62.0	°C	SRFET maximum operating temperature for output 1 (for each SRFET in parallel) with respect to ambient, observed at 950V VINDC
203	**OUTPUT 2**					
204	VOUT2	24.7		24.7	V	Output 2 voltage
205	IOUT2	0.243		0.243	A	Output 2 current
206	POUT2			6.01	W	Output 2 power
207	IRMS_SECONDARY2			0.537	A	Root mean squared value of the secondary current for output 2
208	IRIPPLE_CAP_OUTPUT2			0.479	A	Current ripple on the secondary waveform for output 2
209	NSECONDARY2			17		Number of turns for output 2
210	VREVERSE_RECTIFIER2		Warning[8]	303.20	V	Taking into consideration the parasitic voltage ring and assuming this output is connected to the Vo/FWD pin, then the actual stress across the SRFET/FWD pin would be 397.95V. Given that the absolute maximum FWD pin voltage rating is 150V, increase the VO
211	SRFET2	DMT15H017LPS-13	Warning	DMT15H017LPS-13		The voltage stress (including the parasitic ring) on the secondary MOSFET selected may exceed the device BVDSS: pick a MOSFET with a higher BVDSS
212	NUM_SRFET2	1		1		Number of SRFETS in parallel for output 2
213	VF_SRFET2			0.80	V	SRFET typical on-time drain voltage for output 2
214	VBREAKDOWN_SRFET2			150	V	SRFET breakdown voltage for output 2
215	RDSON_SRFET2			37.0	mΩ	SRFET on-time drain resistance at 100°C and VGS=4.4V for output 2
216	RTHJA_SRFET2			53.00	°C/W	SRFET max. thermal impedance for output 2
217	TEMP_SRFET2_MIN			56.0	°C	SRFET minimum operating temperature for output 2 (for each SRFET in parallel) with respect to ambient, observed at 800V VINDC
218	TEMP_SRFET2_MAX			59.8	°C	SRFET maximum operating temperature for output 2 (for each

[8] The warnings on lines 209 and 210 are disregarded since Output 2 uses a separate secondary winding with a 600 V-rated freewheeling diode.

						SRFET in parallel) with respect to ambient, observed at 950V VINDC
237	PO_TOTAL			20.01	W	Total power of all outputs
238	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
242	**INPUT VOLTAGE SET-POINTS ANALYSIS**					
243	**TOLERANCE CORNER**					
244	USER_VINDC	40		40	V	Input DC voltage corner to be evaluated
245	USER_ILIMIT	MAX		1.926	A	Current limit corner to be evaluated
246	USER_LPRIMARY	MIN		586.7	uH	Primary inductance corner to be evaluated
248	**OPERATING CONDITION SELECTION**					
249	POUT	13.00		13.00	W	Output power to be evaluated
250	EFFICIENCY			0.85		Converter efficiency to be evaluated
251	Z FACTOR			0.50		Z-factor to be evaluated
252	FSWITCHING			58617	Hz	Maximum switching frequency at the output power to be evaluated.
253	KP			0.848		Measure of continuous/discontinuous mode of operation
254	MODE_OPERATION			CCM		Mode of operation
255	DUTYCYCLE			0.689		Primary switch duty cycle
256	TIME_ON		Info	11.750	us	Primary switch on-time has been capped at 11.75us and the controller switching frequency has increased as a result
257	TIME_OFF			5.310	us	Primary switch off-time
259	**PRIMARY CURRENT**					
260	IAVG_PRIMARY			0.364	A	Primary switch average current
261	IPEAK_PRIMARY			0.918	A	Primary switch peak current
262	IPEDESTAL_PRIMARY			0.139	A	Primary switch current pedestal
263	IRIPPLE_PRIMARY			0.778	A	Primary switch ripple current
264	IRMS_PRIMARY			0.477	A	Primary switch RMS current
266	**MAGNETIC FLUX DENSITY**					
267	BPEAK			3438	Gauss	Peak flux density
268	BMAX			1601	Gauss	Maximum flux density
269	BAC			679	Gauss	AC flux density (0.5 x Peak to Peak)
271	**DEVICE TEMPERATURE**					
272	TEMP_INNO			86.0	°C	Device operating temperature with respect to ambient
273	TEMP_SRFET1			123.6	°C	Operating temperature per SRFET of output 1 with respect to ambient
274	TEMP_SRFET2			122.3	°C	Operating temperature per SRFET of output 2 with respect to ambient
275	TEMP_SRFET3			N/A	°C	Operating temperature per SRFET of output 3 with respect to ambient

Table 7 – DER-1030Q PIXls Spreadsheet.

9 Hi-Pot Testing

Hi-Pot testing measures the dielectric breakdown of the primary-to-secondary isolation used in the transformer. This test is performed to assess the ability of the insulation to withstand steady state voltage stress.

Figure 16 shows the test profile used to evaluate the transformer of DER-1030Q.

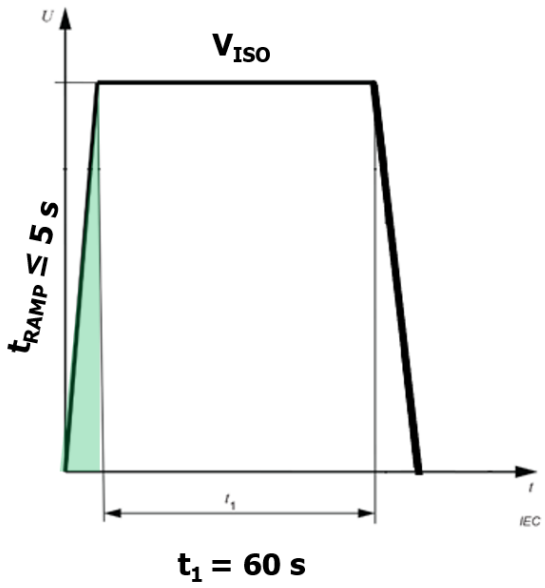


Figure 16 – Hi-Pot Test Profile of DER-1030Q.

The transformer was soaked in varnish and vacuum impregnated to ensure that the varnish fully penetrated the windings. The transformer was then baked in an oven for 2 hours at 85°C. The transformer was isolation-tested at an isolation voltage of 4000 VAC to 5000 VAC with a 5-second ramp-up and 60-second dwell time. The isolation test was made between nodes 1 to 9 at 24 °C ambient, with nodes 1-8 and 9-16 shorted. Refer to Figure 14 for the transformer electrical diagram for more information.

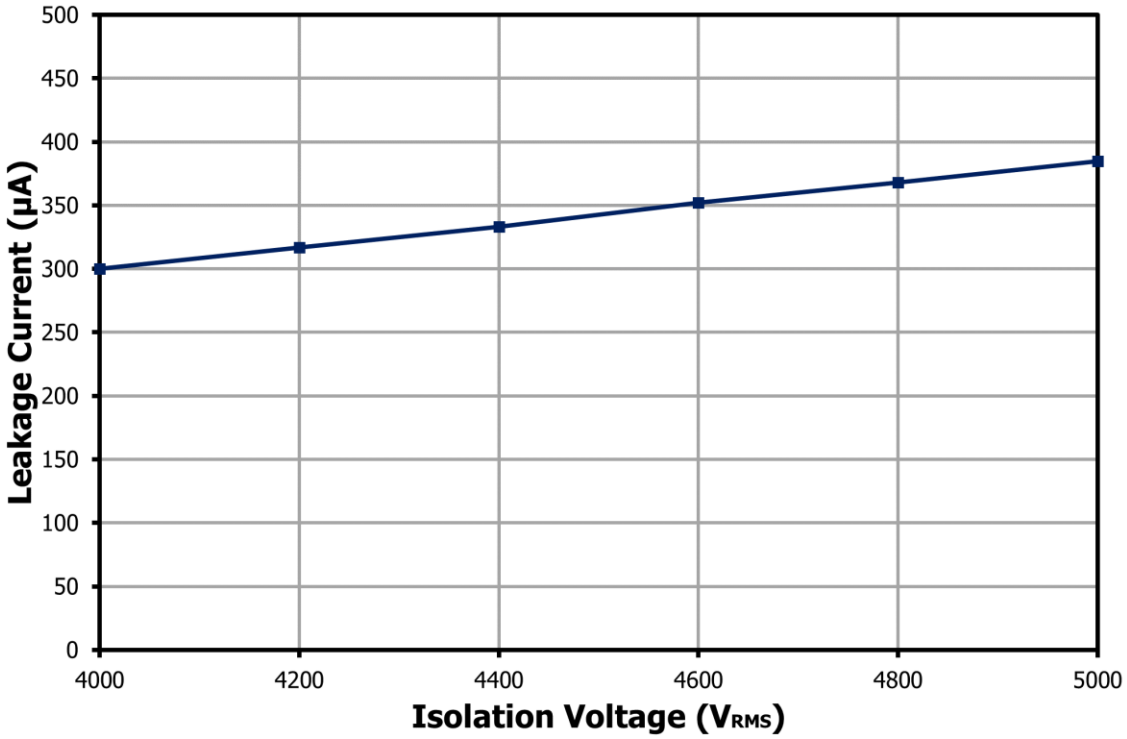


Figure 17 – Isolation Voltage vs. Leakage Current (25 °C Ambient).

Note: The leakage current across the isolation barrier is due to the primary to secondary coupling capacitance. When the high voltage 60 Hz AC test voltage is applied, current flows through this capacitance. Under DC voltage conditions, this leakage current is not present (measured at less than 3 µA).

10 Performance Data

Notes:

1. Measurements were taken with the unit-under-test positioned inside a thermal chamber.
2. The DER-1030Q board was also placed inside a box (within the thermal chamber) to eliminate the effects of any airflow.

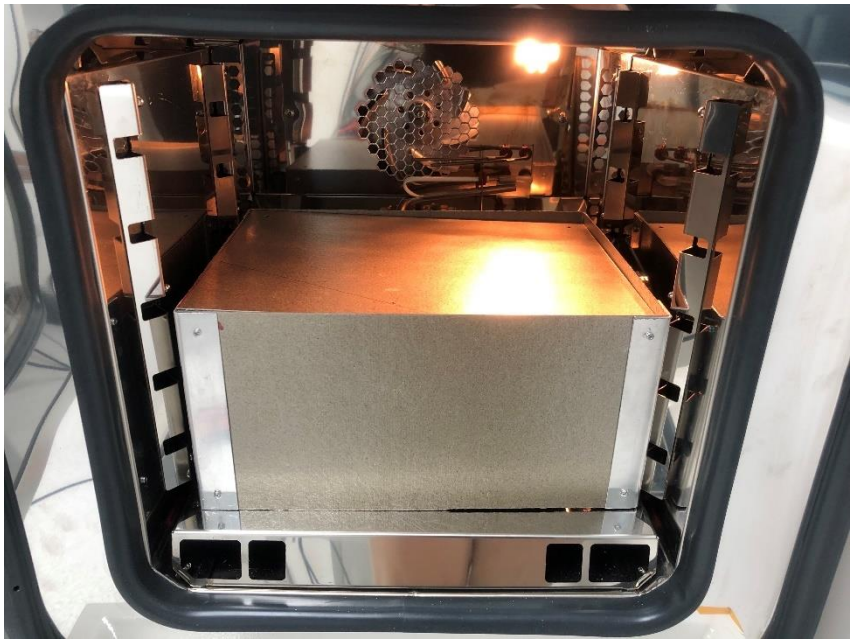


Figure 18 – Unit under test placed inside a box to eliminate the effect of airflow.

3. The DER board was allowed to stabilize for 5 minutes at full load at the start of every test. For each loading condition, the DER-1030Q test board was allowed to stabilize for 1 minute before measurements were taken.

Equipment Type	Model Number	Specifications	Manufacturer
Power Supply	HP20 757 152	2 kV/250 mA/1.5 kW	Iseg
Power Supply	IT6333B	0-60 V/3 A x2 Channels, 0-5 V/ 3 A	ITECH
Electronic Load	PEL-2020A	80 V/20 A/100 W DC Electronic Load	GW Instek
Power Meter	66205	600 V/30 A Digital Power Meter	Chroma
Power Meter	WT310E	600 V/20 A Digital Power Meter	Yokogawa
High-Voltage Measurement	TT-SI 9101	70 MHz 700 V Differential Probe	Testec
High-Voltage Measurement	TT-SI 9110	100 MHz 1400 V Differential Probe	Testec
Low-Voltage Measurement	PHT 312	400 V Passive Probe Extended Temperature	PMK
Low-Voltage Measurement	701937	500 MHz 600 V Passive Probe	Yokogawa
Current Measurement	701928	100 MHz 30 A_{rms} Current Probe	Yokogawa
Current Measurement	CWTUM/06/R	30 MHz 120 A_{peak} Rogowski Coil	CWT
Current Measurement	CWTUM/1/R	30 MHz 300 A_{peak} Rogowski Coil	CWT
Thermocouple Measurement	GL840	20-Channel Data Logger	Graphtec
Thermal Image	TiX580	1000°C Thermal Imaging Camera	Fluke
Thermal Chamber	SH-242	Temperature & Humidity Chamber	Espec
Oscilloscope	DLM5058	2.5 GS/s 500 MHz Mixed Signal	Yokogawa

Table 8 – List of Equipment Used for Testing.

10.1 No-Load Input Power

Figure 19 shows the test circuit used for the no-load input power measurement. The voltmeter was placed before the ammeter. This was done to prevent the voltmeter bias current from affecting the input current measurements. A Chroma Digital Power Meter 66205 was used to measure the current and voltage.

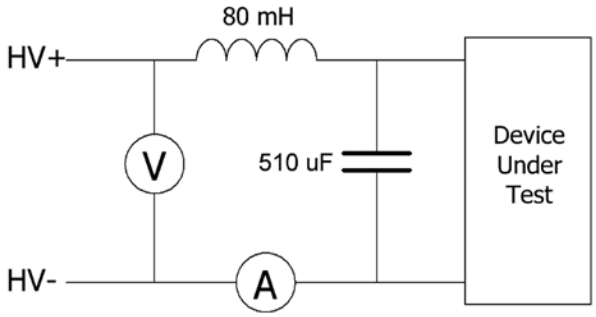


Figure 19 - No-Load Input Power Measurement Circuit Configuration.

For each input voltage, the unit was soaked for ten minutes before measurements were made. The leakage current through the DC-Link capacitor was also measured before testing and was subtracted from the measured no-load input current. The voltage across the input inductor was assumed to be negligible due to its very low DCR (40 mΩ) and low input current. AC losses in the inductor were also assumed to be negligible.

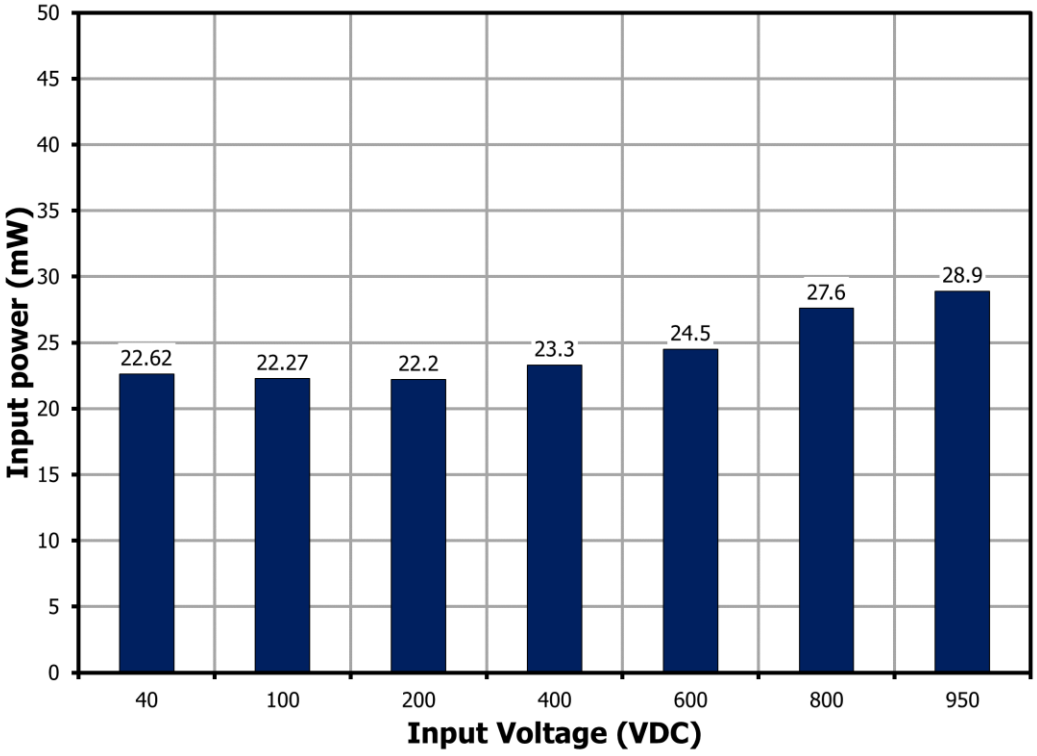


Figure 20 – No-load Input Power vs. Input Line Voltage.

10.2 Efficiency

10.2.1 Efficiency Across Line

Efficiency across line describes how the change in input voltage affects the overall efficiency of the unit. The points in the graph were taken at 100% load (10 W at 40 VDC input and 20 W at 250 VDC – 950 VDC input).

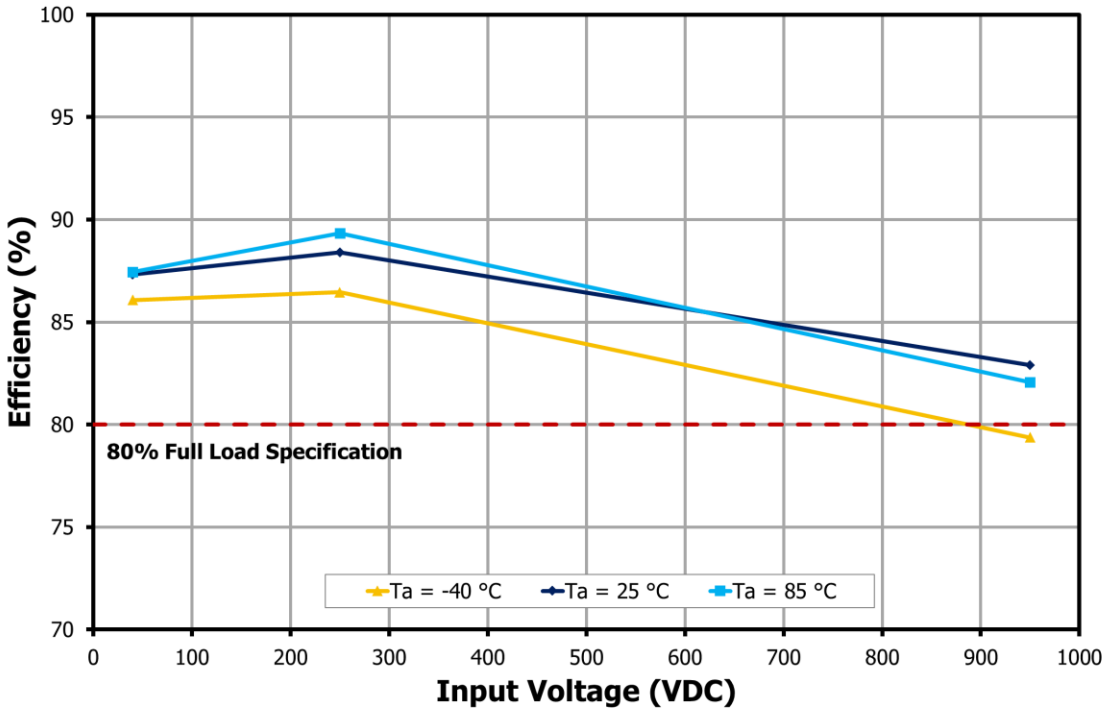


Figure 21 – Full Load Efficiency vs. Input Line Voltage.[9]

[9] >80% full load efficiency specification applies across 25° C and 85° C ambient. Full load efficiency specification at -40° C ambient is >75%.

10.2.2 Efficiency Across Load

Efficiency across load describes how output loading affects the overall efficiency of the power supply. Each line on the graphs represents the efficiency vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 Voutput load is increased from its minimum to maximum loading condition.

10.2.2.1 40 VDC Input

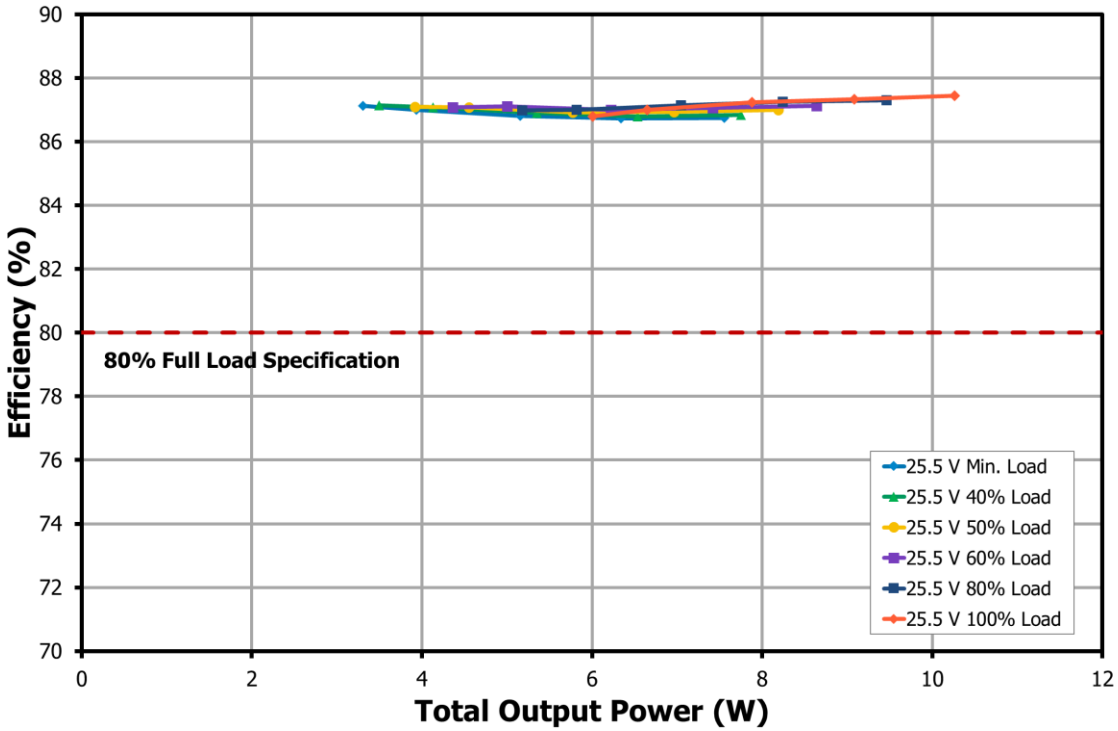


Figure 22 – Efficiency vs. Total Output Power at 40 VDC Input and 85 °C Ambient.[10]

[10] >80% full load efficiency specification applies across 25° C and 85° C ambient. Full load efficiency specification at -40° C ambient is >75%.

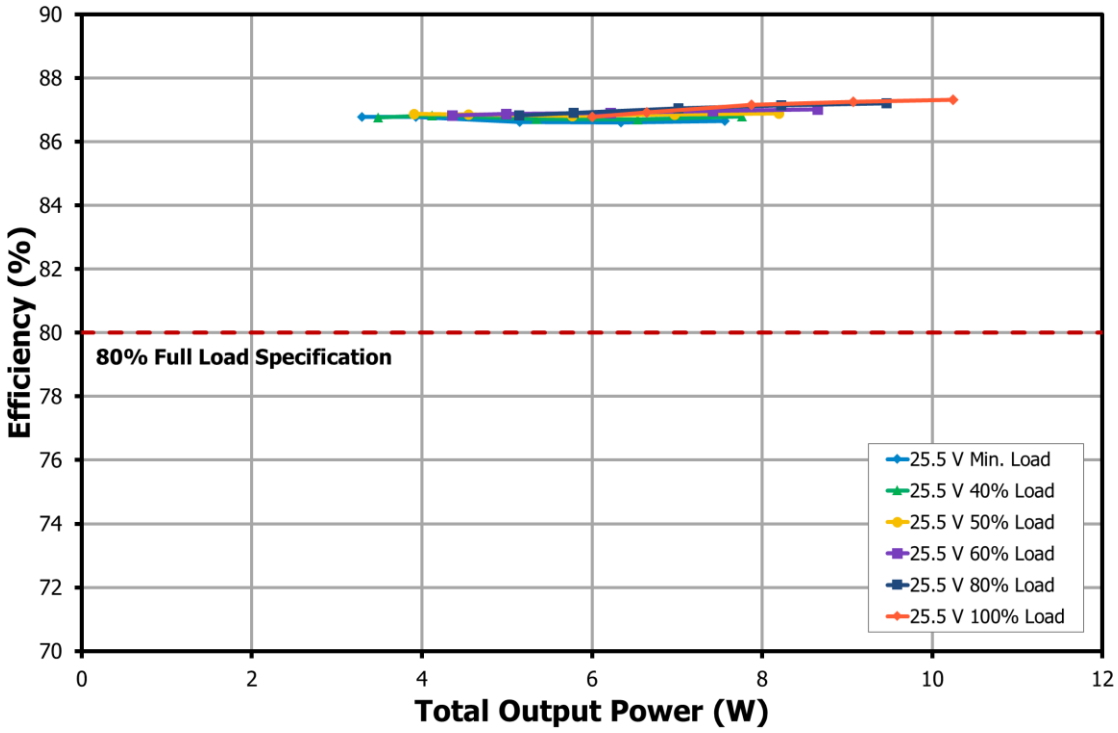


Figure 23 – Efficiency vs. Total Output Power at 40 VDC Input and 25 °C Ambient.[11]

[11] >80% full load efficiency specification applies across 25° C and 85° C ambient. Full load efficiency specification at -40° C ambient is >75%.

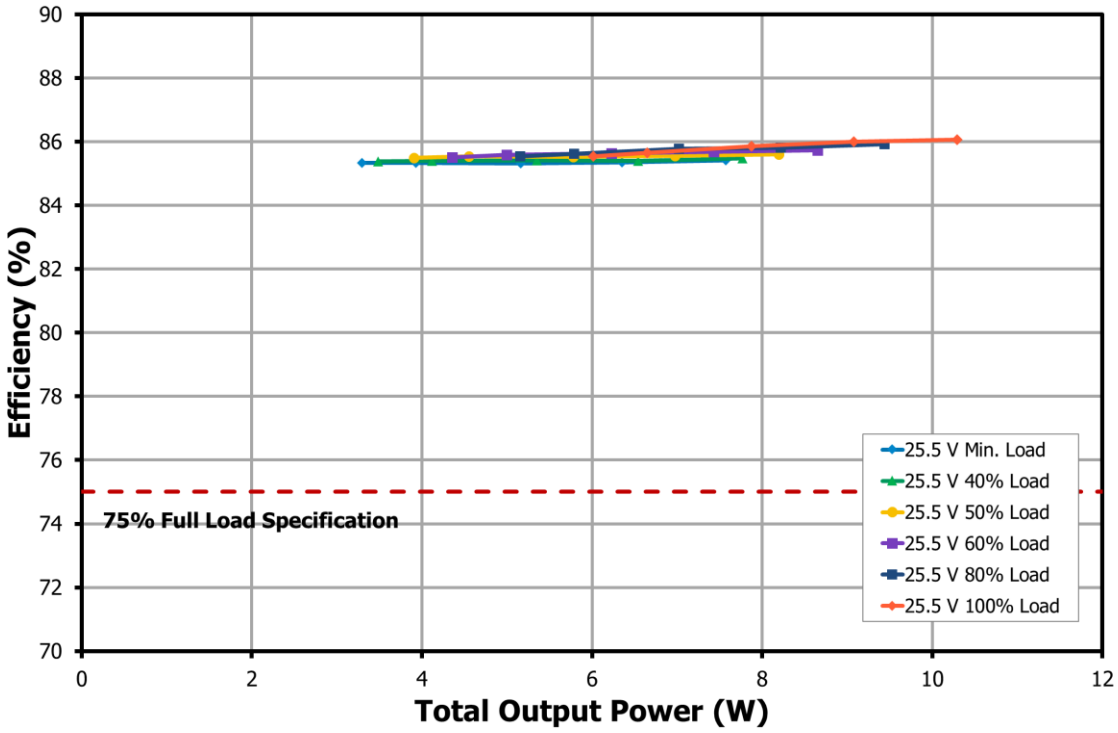


Figure 24 – Efficiency vs. Total Output Power at 40 VDC Input and -40 °C Ambient.[12]

[12] >75% full load efficiency specification applies at -40° C ambient. Full load efficiency specification across 25° C and 85° C ambient is >80%.

10.2.2.2 250 VDC Input

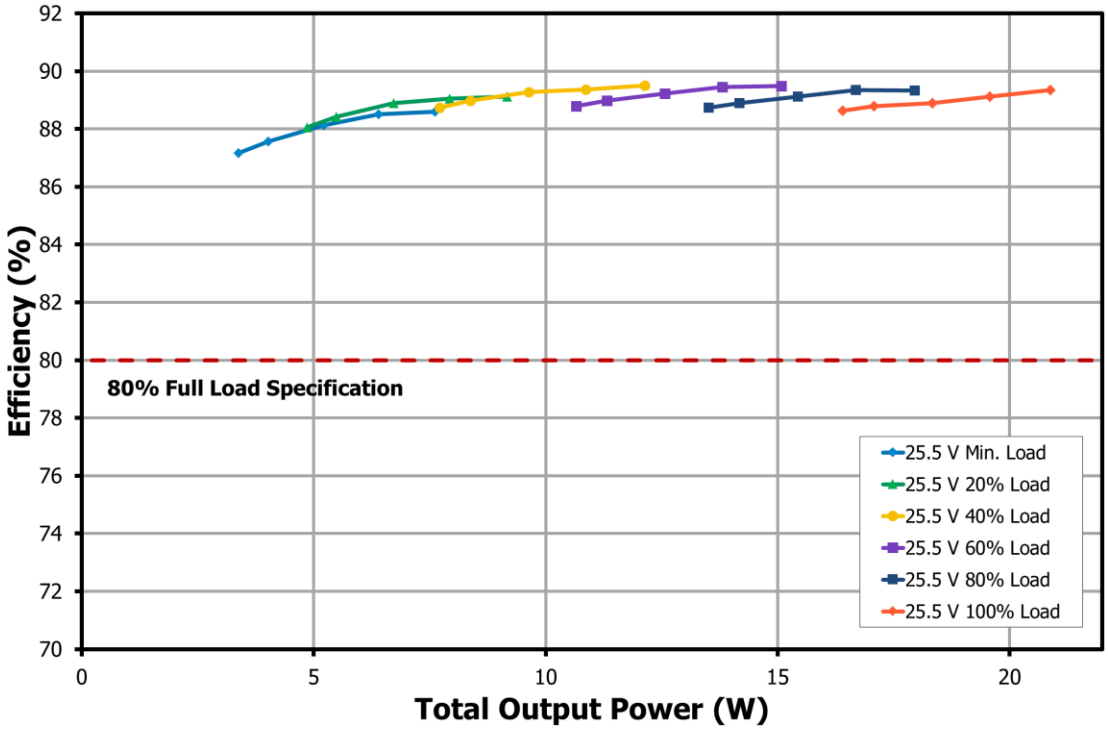


Figure 25 – Efficiency vs. Total Output Power at 250 VDC Input and 85 °C Ambient.[13]

[13] >80% full load efficiency specification applies across 25° C and 85° C ambient. Full load efficiency specification at -40° C ambient is >75%.

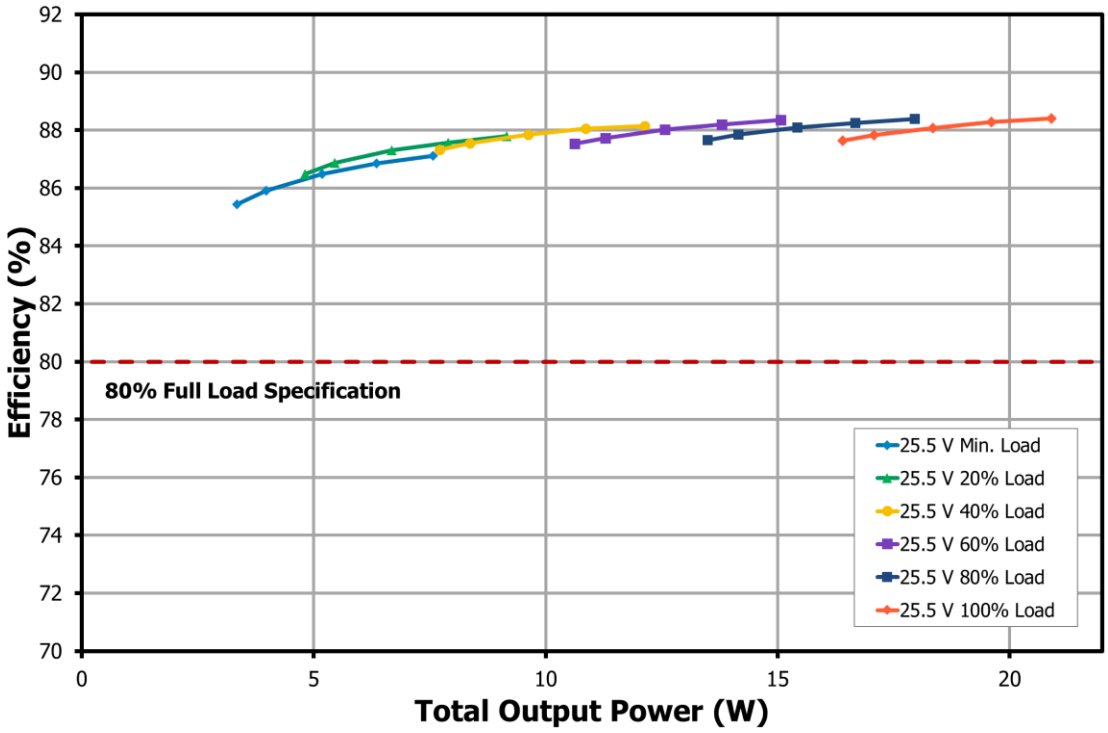


Figure 26 – Efficiency vs. Total Output Power at 250 VDC Input and 25 °C Ambient.[14]

[14] >80% full load efficiency specification applies across 25° C and 85° C ambient. Full load efficiency specification at -40° C ambient is >75%.

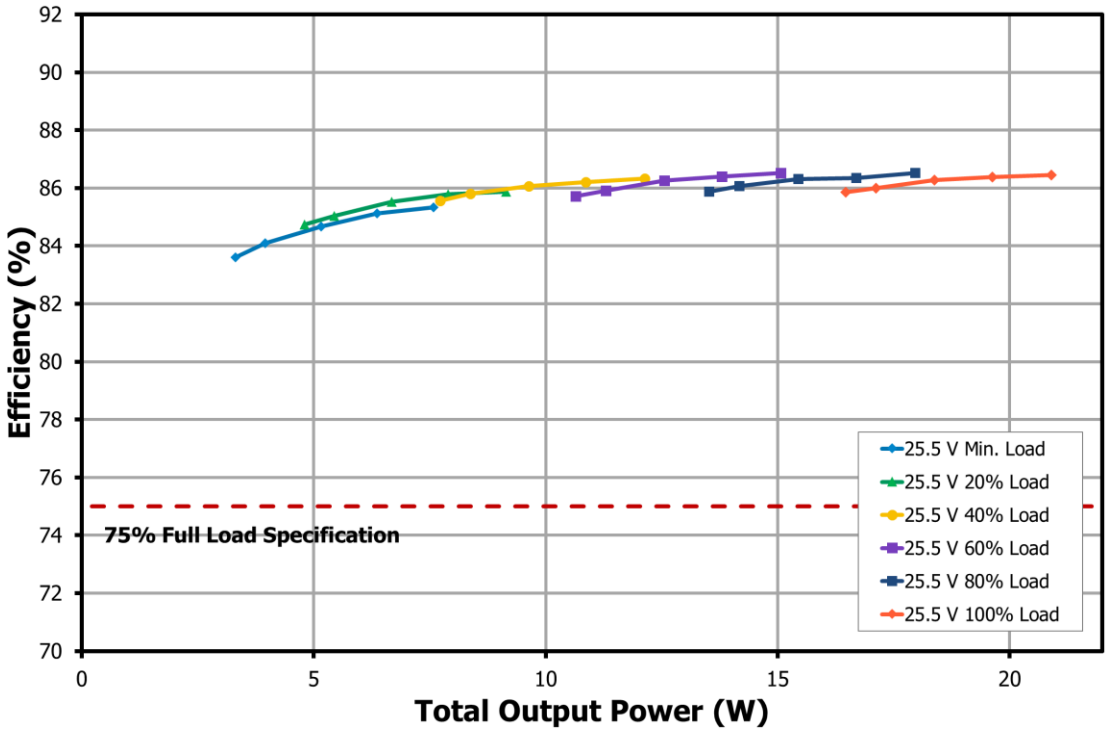


Figure 27 – Efficiency vs. Total Output Power at 250 VDC Input and -40 °C Ambient.[15]

[15] >75% full load efficiency specification applies at -40° C ambient. Full load efficiency specification across 25° C and 85° C ambient is >80%.

10.2.2.3 950 VDC Input

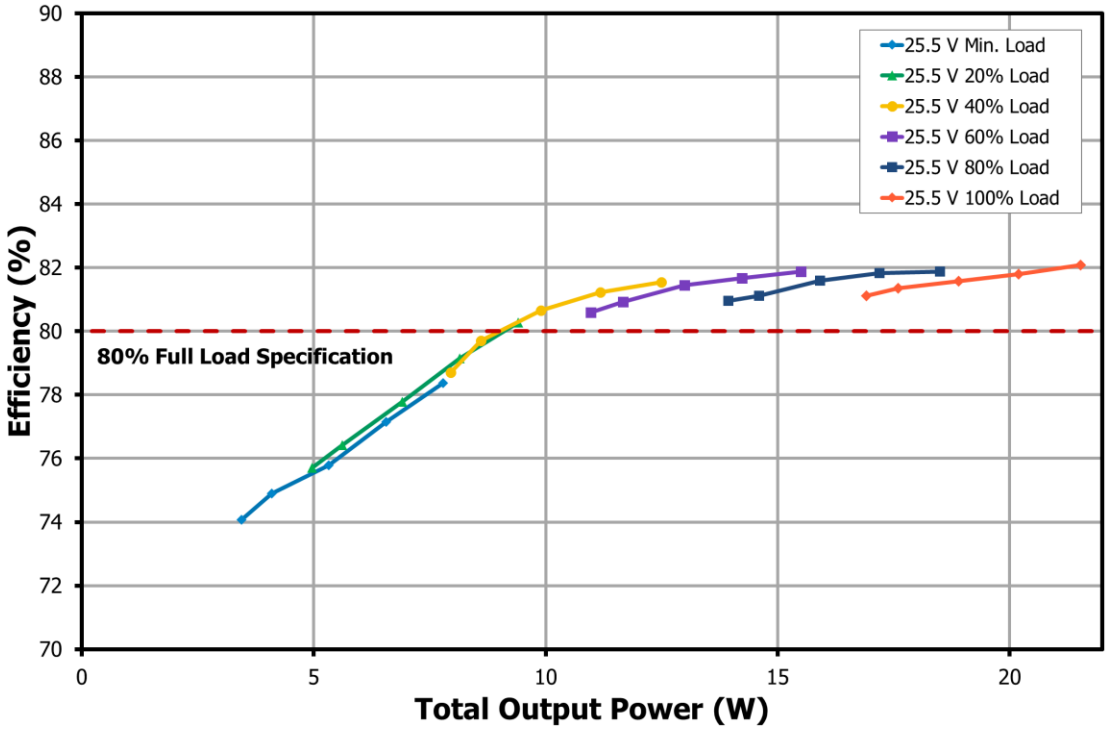


Figure 28 – Efficiency vs. Total Output Power at 950 VDC Input and 85 °C Ambient.[16]

[16] >80% full load efficiency specification applies across 25° C and 85° C ambient. Full load efficiency specification at -40° C ambient is >75%.

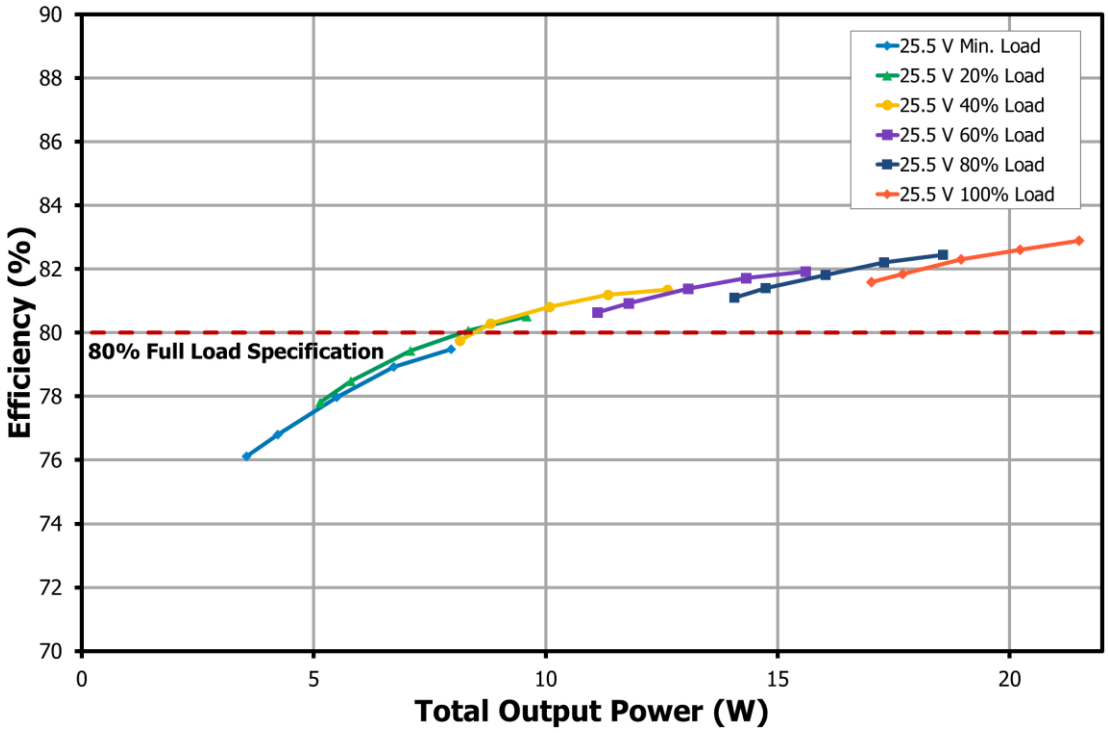


Figure 29 – Efficiency vs. Total Output Power at 950 VDC Input and 25 °C Ambient.[17]

[17] >80% full load efficiency specification applies across 25° C and 85° C ambient. Full load efficiency specification at -40° C ambient is >75%.

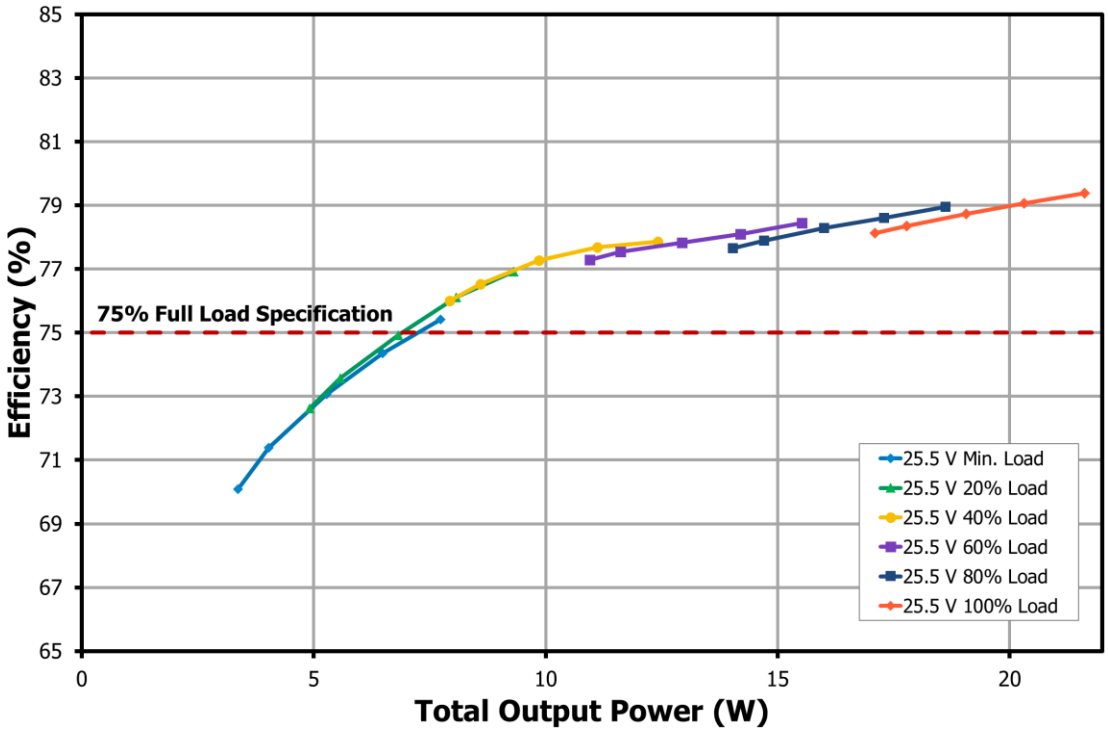


Figure 30 – Efficiency vs. Total Output Power at 950 VDC Input and -40 °C Ambient.[18]

[18] >75% full load efficiency specification applies at -40° C ambient. Full load efficiency specification across 25° C and 85° C ambient is >80%.

10.3 Load Regulation

Load regulation describes how a change in load affects output voltage.

10.3.1 40 VDC Input

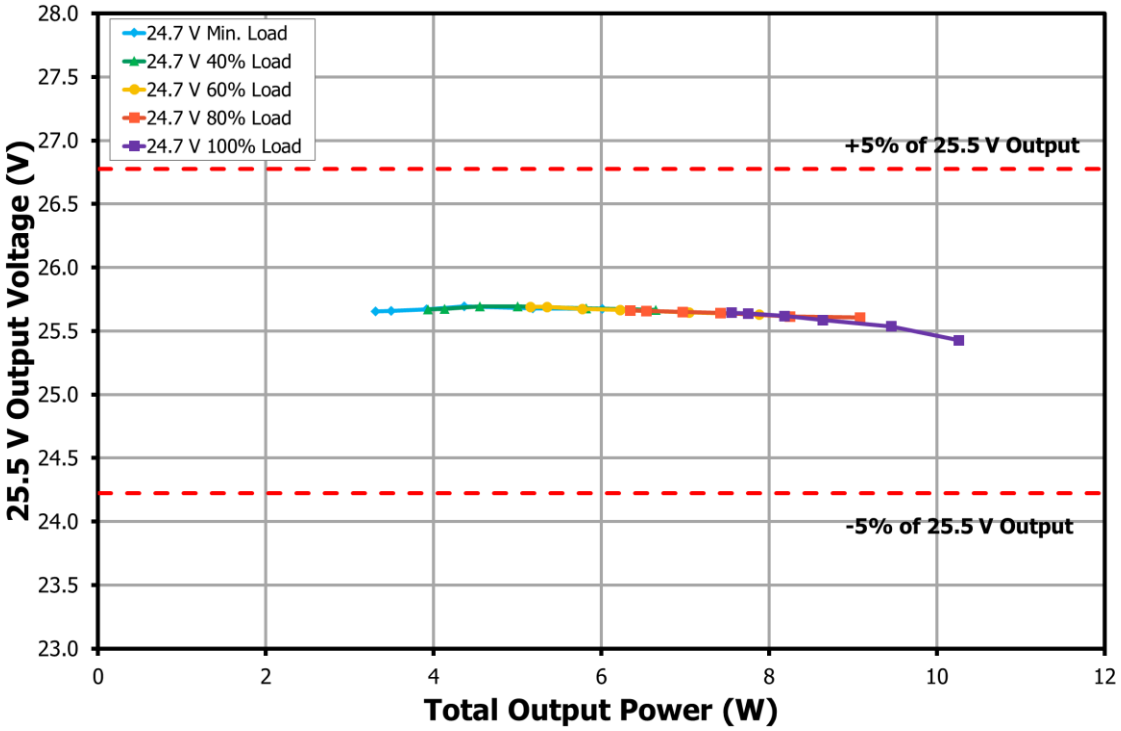


Figure 31 – 25.5 V Output Voltage vs. Total Output Power at 40 VDC Input and 85 °C Ambient.[19]

[19] Each line represents the 25.5 output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

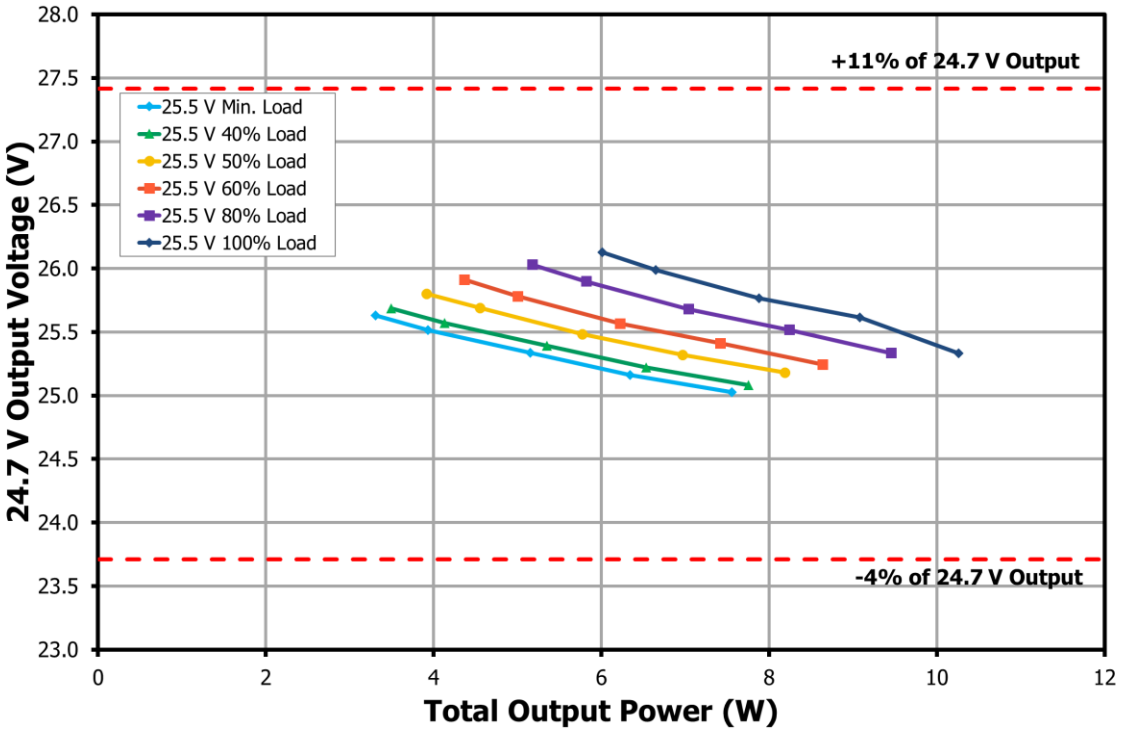


Figure 32 – 24.7 V Output Voltage vs. Total Output Power at 40 VDC Input and 85 °C Ambient.[20]

[20] Each line represents the 24.7 V output regulation vs. total output power of the unit under test when the 25.5 V output load is maintained at a set percentage while the 24.7 Voutput load is increased from its minimum to maximum loading condition.

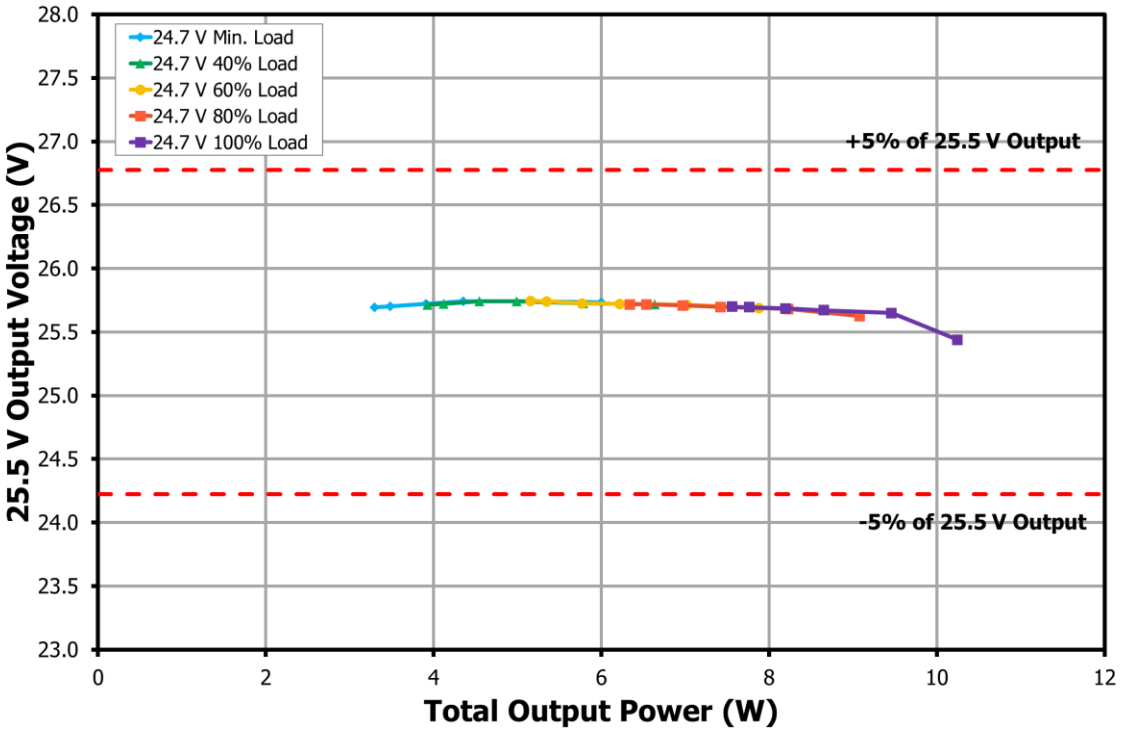


Figure 33 – 25.5 V Output Voltage vs. Total Output Power at 40 VDC Input and 25 °C Ambient.[21]

[21] Each line represents the 25.5 V output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a set percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

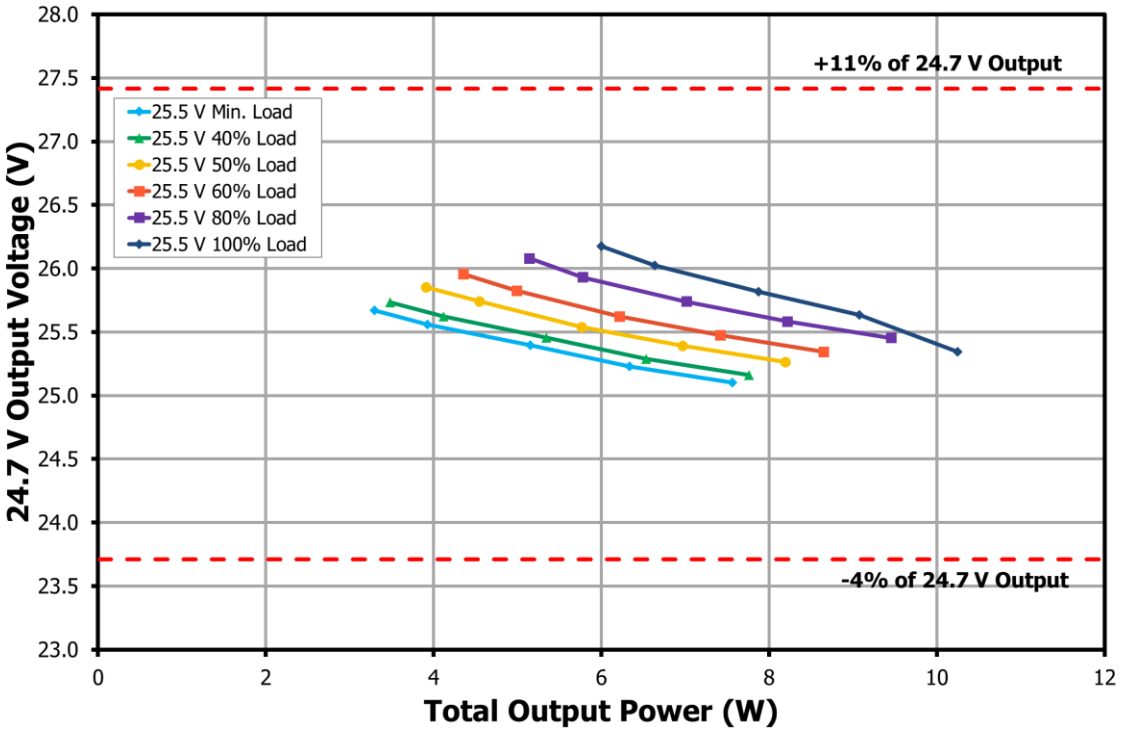


Figure 34 – 24.7 V Output Voltage vs. Total Output Power at 40 VDC Input and 25 °C Ambient.[22]

[22] Each line represents the 24.7 Voutput regulation vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

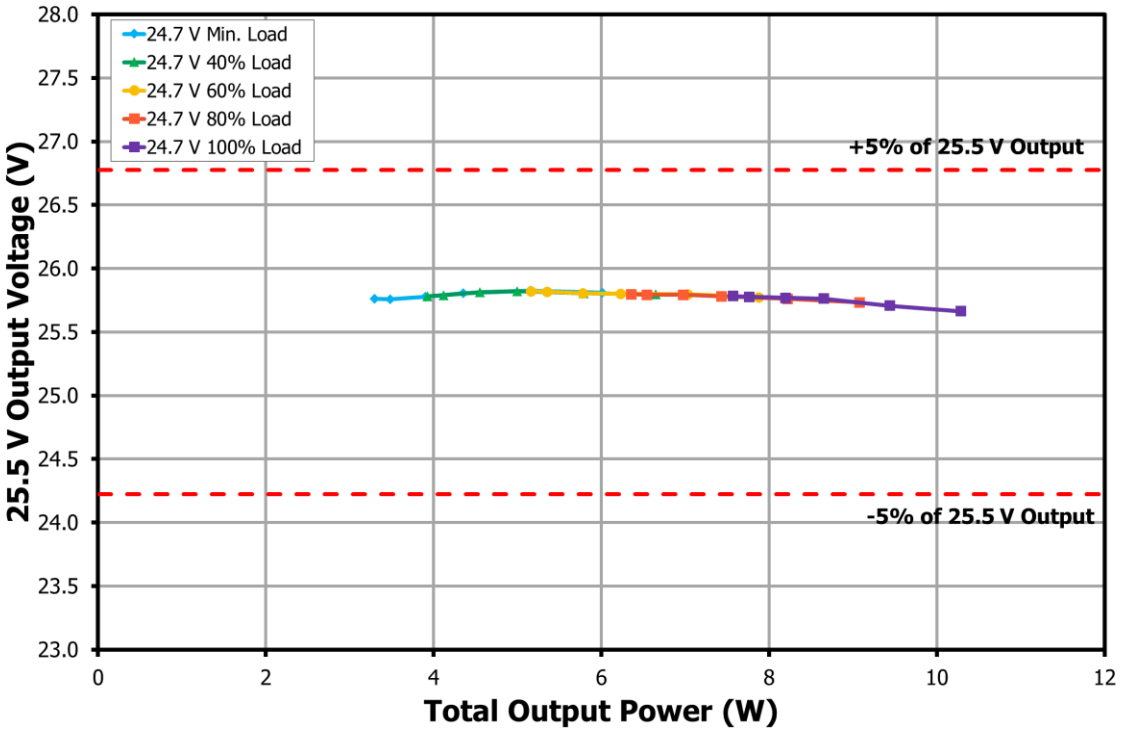


Figure 35 - 25.5 V Output Voltage vs. Total Output Power at 40 VDC Input and -40 °C Ambient.[23]

[23] Each line represents the 25.5 V output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a set percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

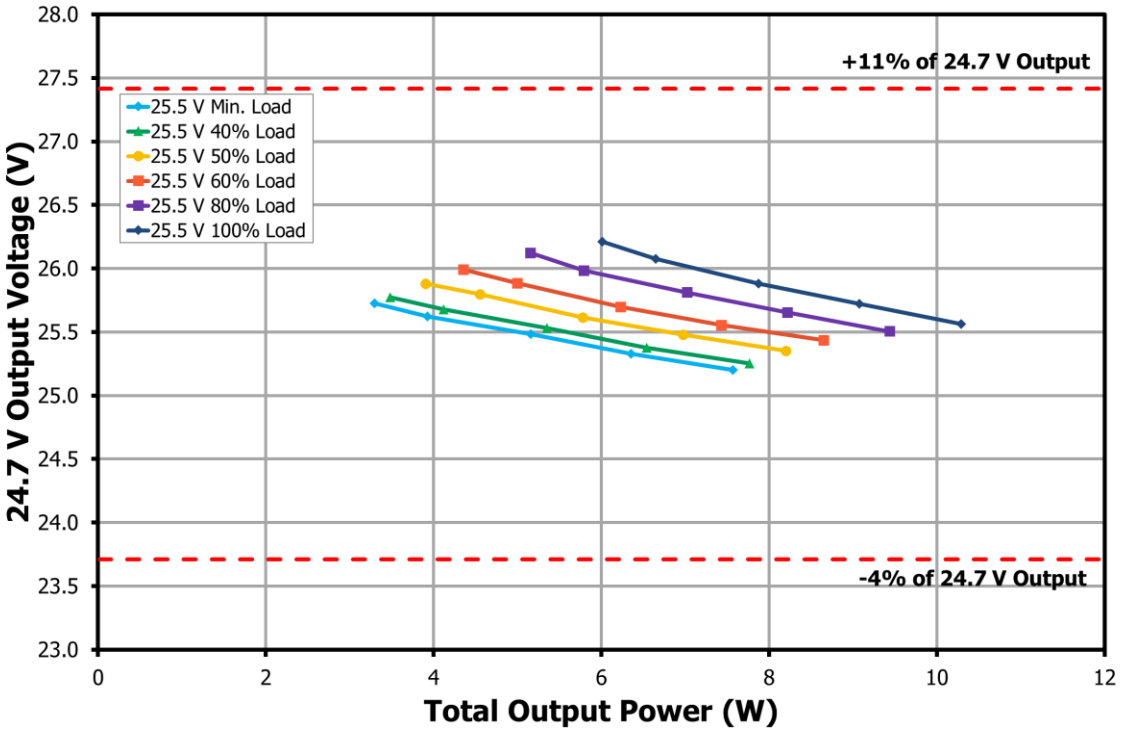


Figure 36 – 24.7 V Output Voltage vs. Total Output Power at 40 VDC Input and -40 °C Ambient.[24]

[24] Each line represents the 24.7 V output regulation vs. total output power of the unit under test when the 25.5 V output load is maintained at a set percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

10.3.2 250 VDC Input

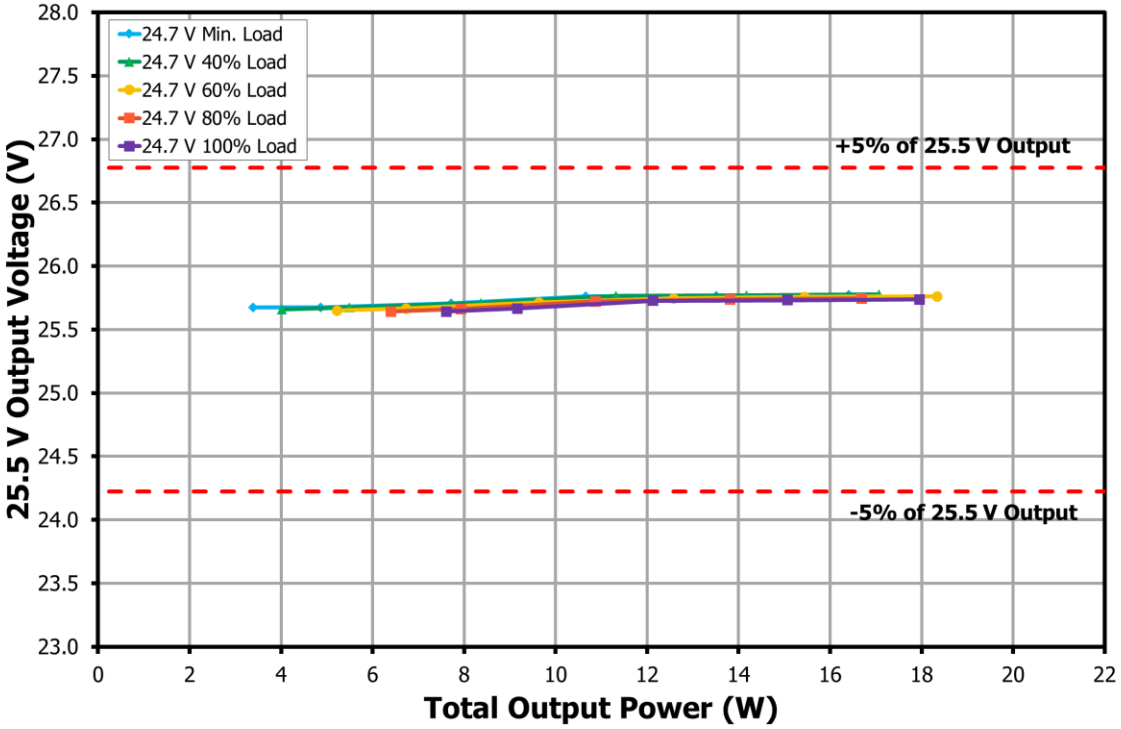


Figure 37 – 25.5 V Output Voltage vs. Total Output Power at 250 VDC Input and 85 °C Ambient.[25]

[25] Each line represents the 25.5 V output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a set percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

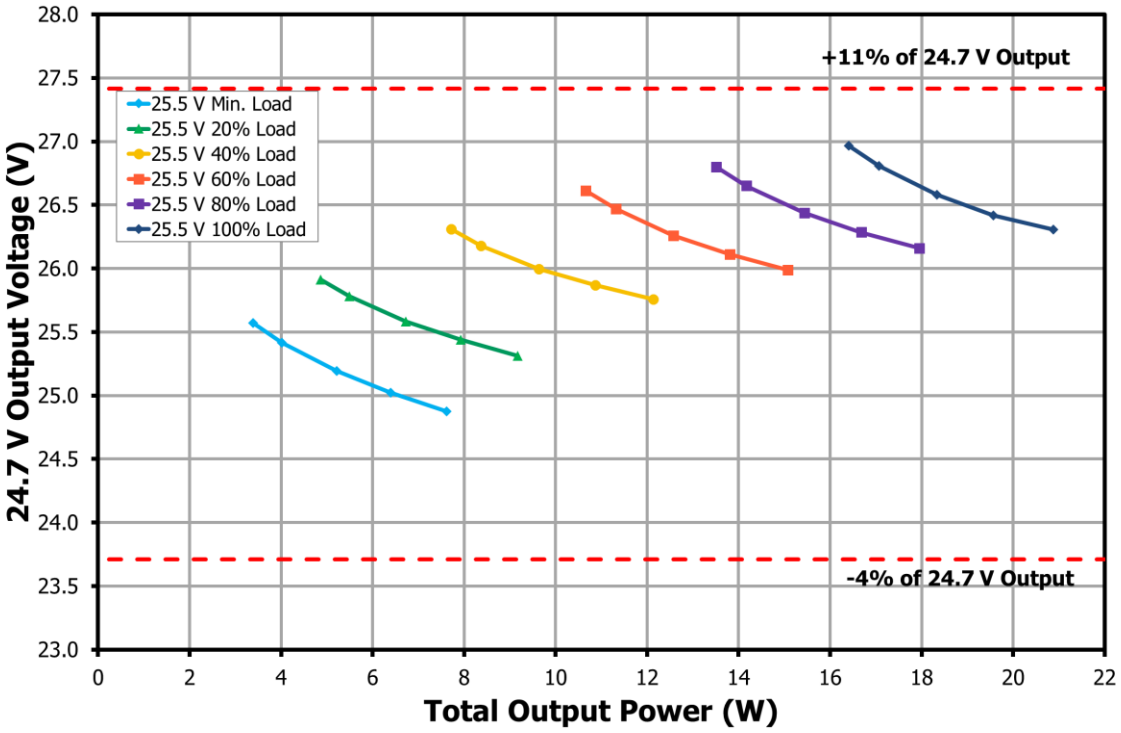


Figure 38 – 24.7 V Output Voltage vs. Total Output Power at 250 VDC Input and 85 °C Ambient.[26]

[26] Each line represents the 24.7 V output regulation vs. total output power of the unit under test when the 25.5 V output load is maintained at a set percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

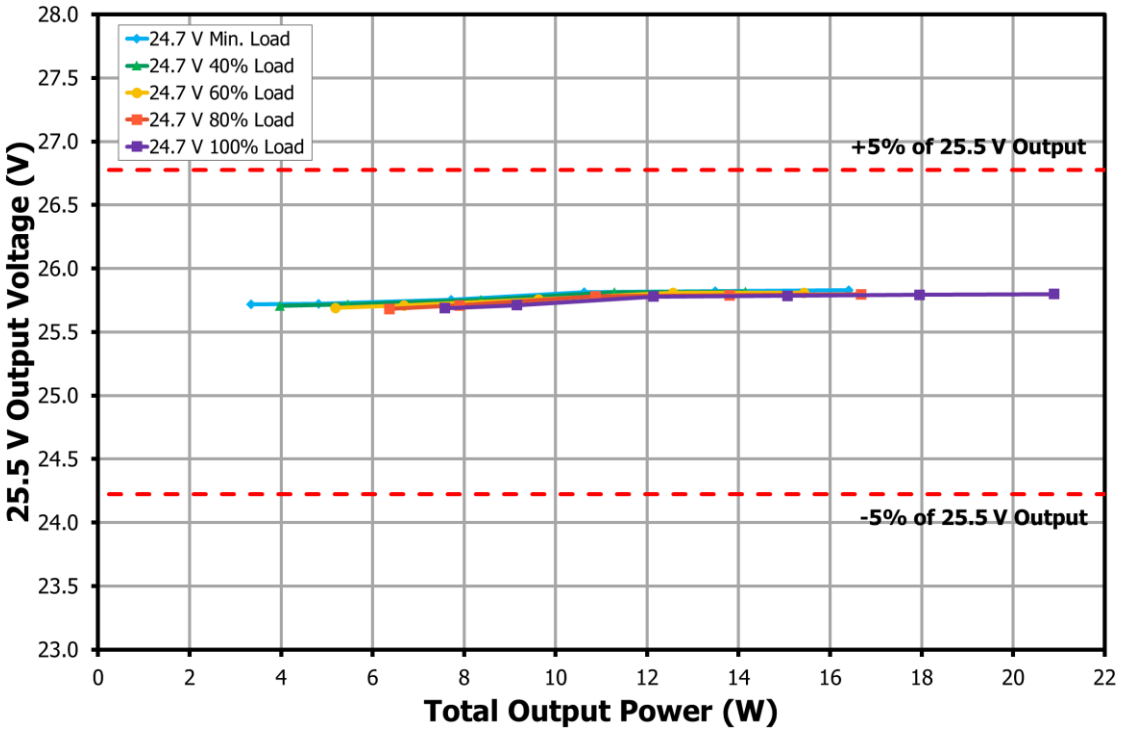


Figure 39– 25.5 V Output Voltage vs. Total Output Power at 250 VDC Input and 25 °C Ambient.[27]

[27] Each line represents the 25.5 V output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

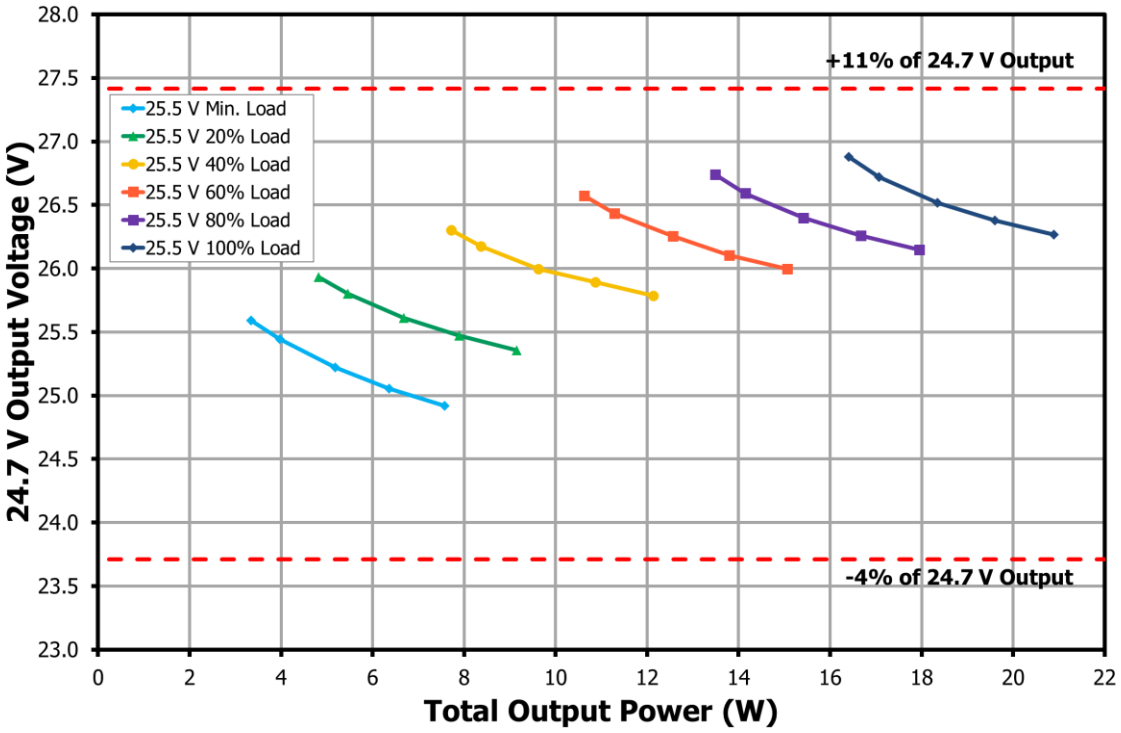


Figure 40– 24.7 V Output Voltage vs. Total Output Power at 250 VDC Input and 25 °C Ambient.[28]

[28] Each line represents the 24.7 V output regulation vs. total output power of the unit under test when the 25.5 V output load is maintained at a set percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

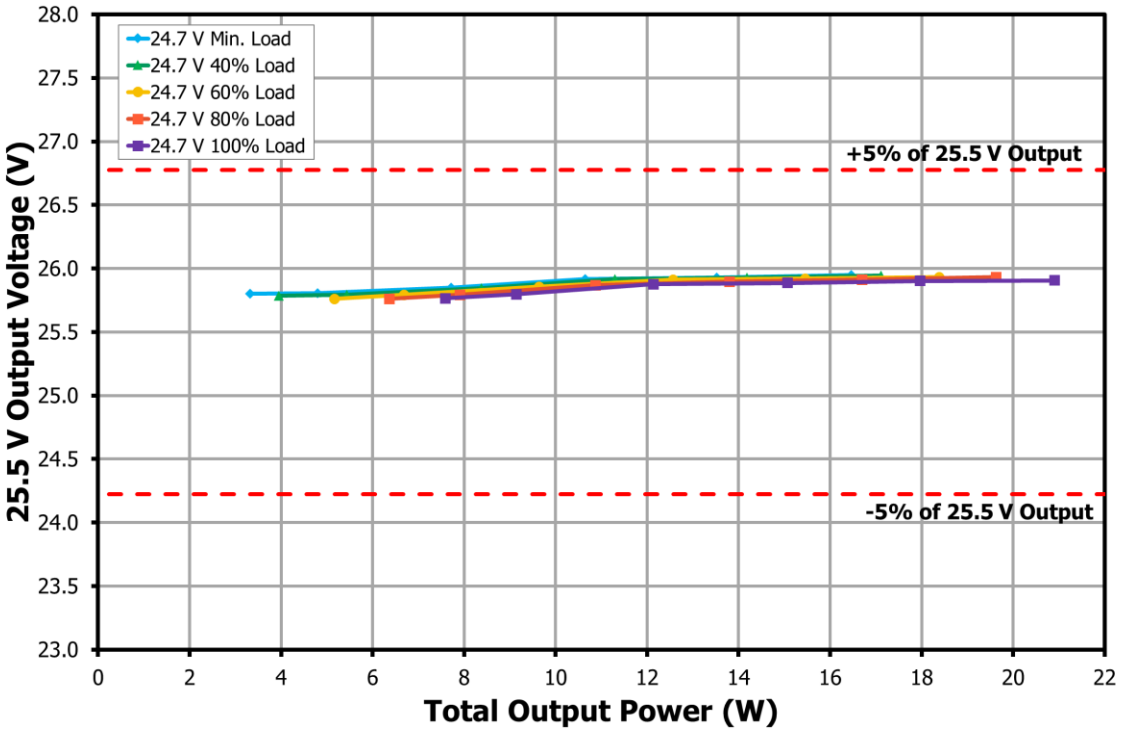


Figure 41 – 25.5 V Output Voltage vs. Total Output Power at 250 VDC Input and -40 °C Ambient.[29]

[29] Each line represents the 25.5 V output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a set percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

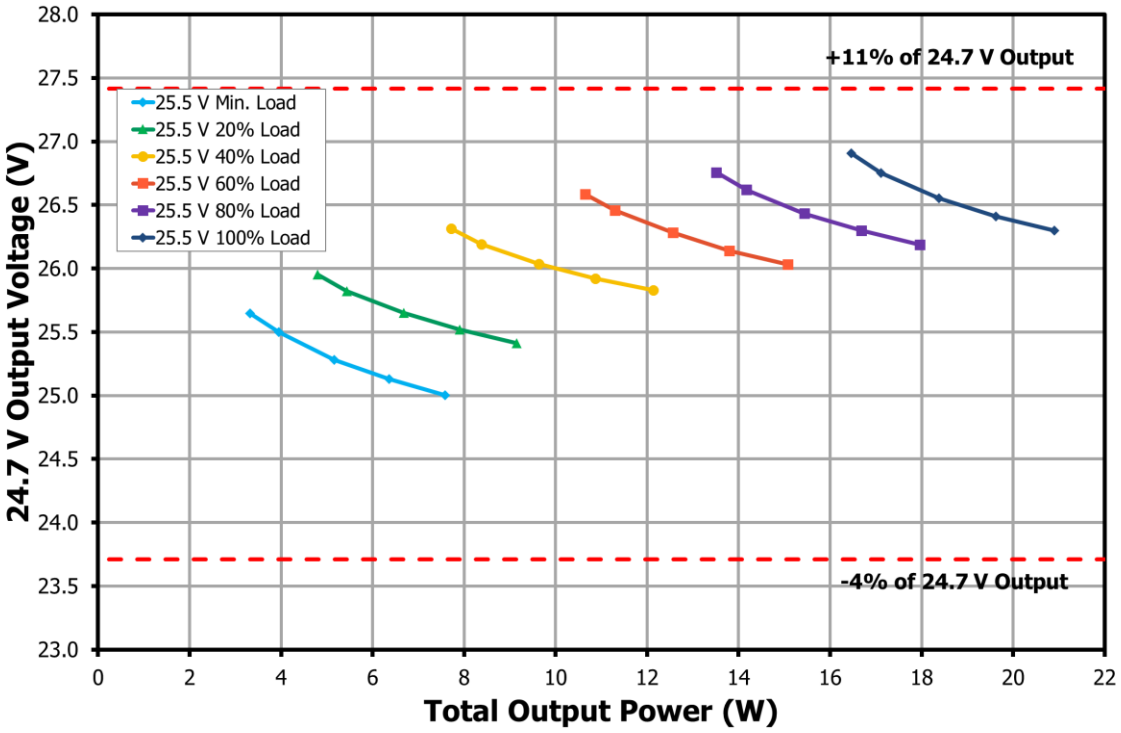


Figure 42 – 24.7 V Output Voltage vs. Total Output Power at 250 VDC Input and -40 °C Ambient.[30]

[30] Each line represents the 24.7 V output regulation vs. total output power of the unit under test when the 25.5 V output load is maintained at a set percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

10.3.3 950 VDC Input

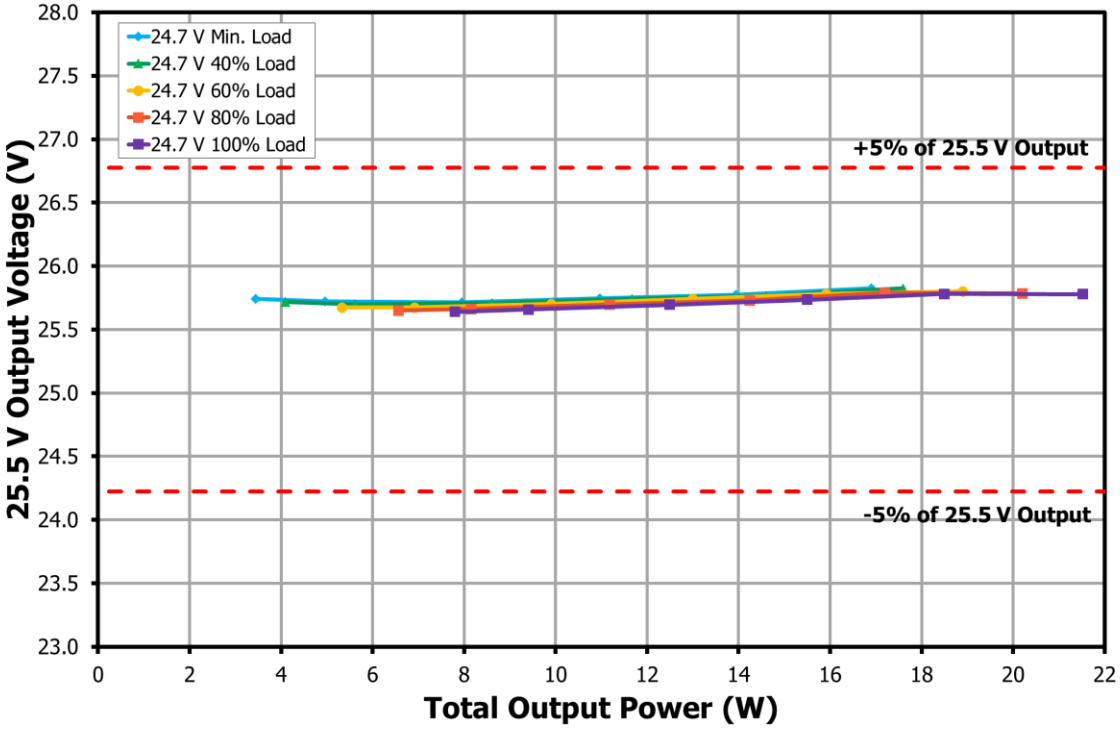


Figure 43 – 25.5 V Output Voltage vs. Total Output Power at 950 VDC Input and 85 °C Ambient.[31]

[31] Each line represents the 25.5 V output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

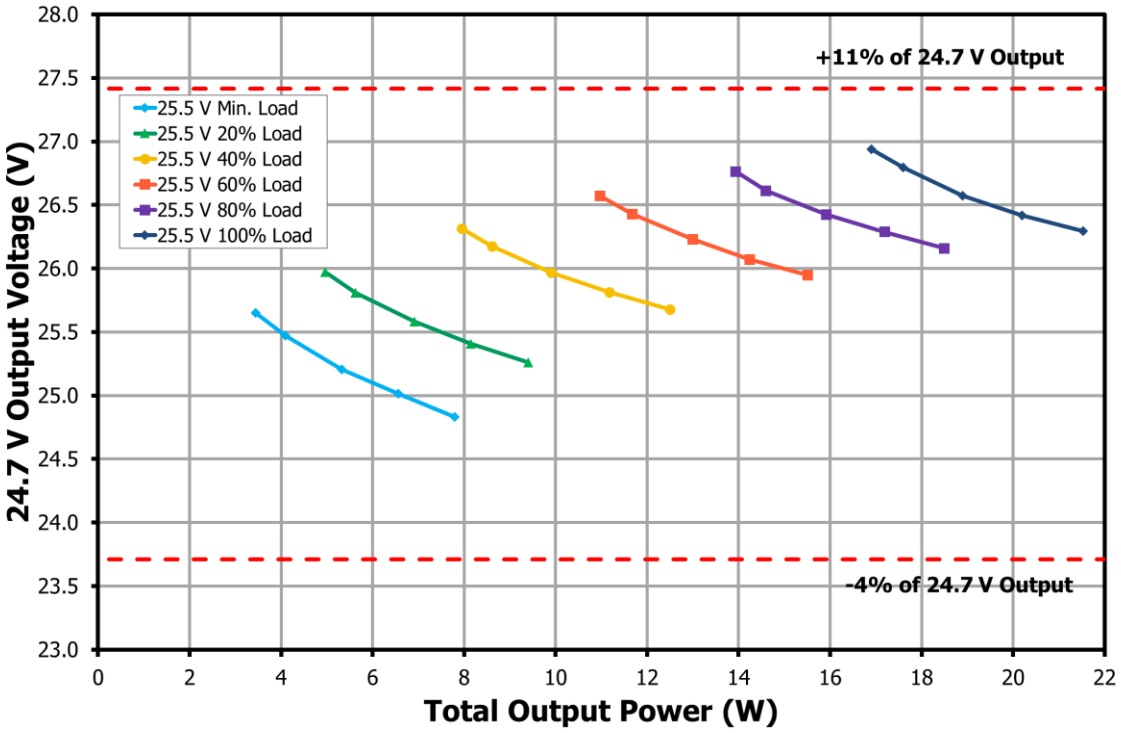


Figure 44 – 24.7 V Output Voltage vs. Total Output Power at 950 VDC Input and 85 °C Ambient.[32]

[32] Each line represents the 24.7 V output regulation vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 Voutput load is increased from its minimum to maximum loading condition.

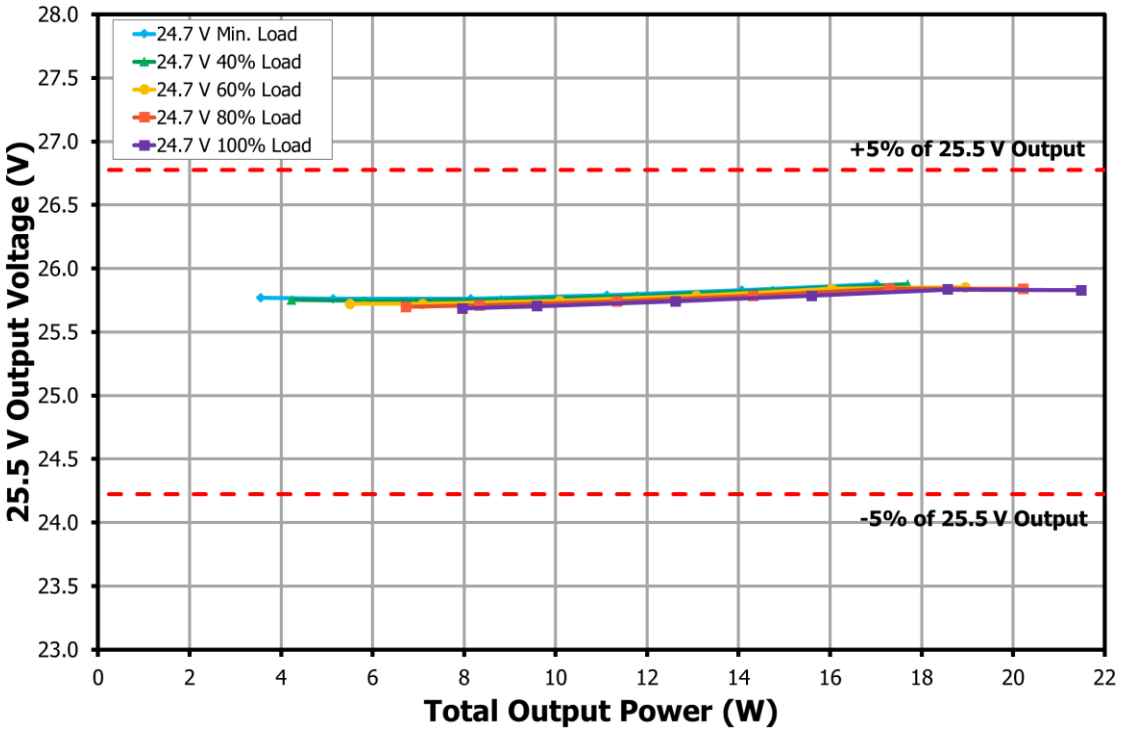


Figure 45 – 25.5 V Output Voltage vs. Total Output Power at 950 VDC Input and 25 °C Ambient.[33]

[33] Each line represents the 25.5 V output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

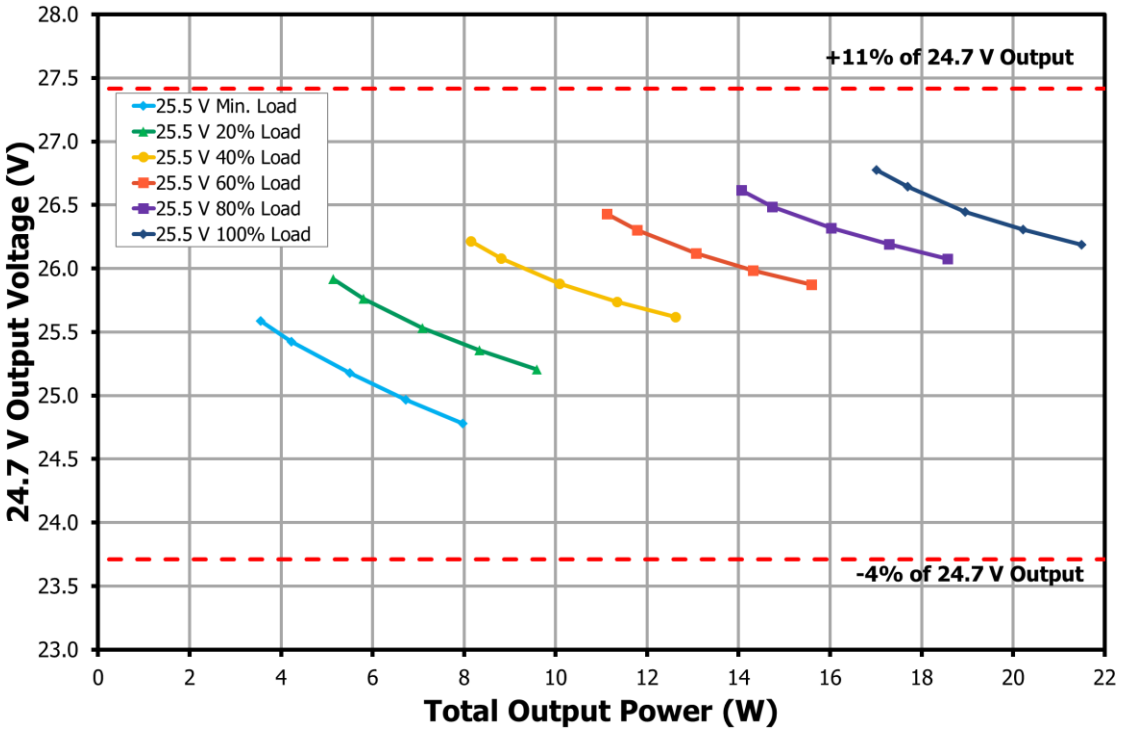


Figure 46 – 24.7 V Output Voltage vs. Total Output Power at 950 VDC Input and 25 °C Ambient.[34]

[34] Each line represents the 24.7 V output regulation vs. total output power of the unit under test when the 25.5 V output load is maintained at a set percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

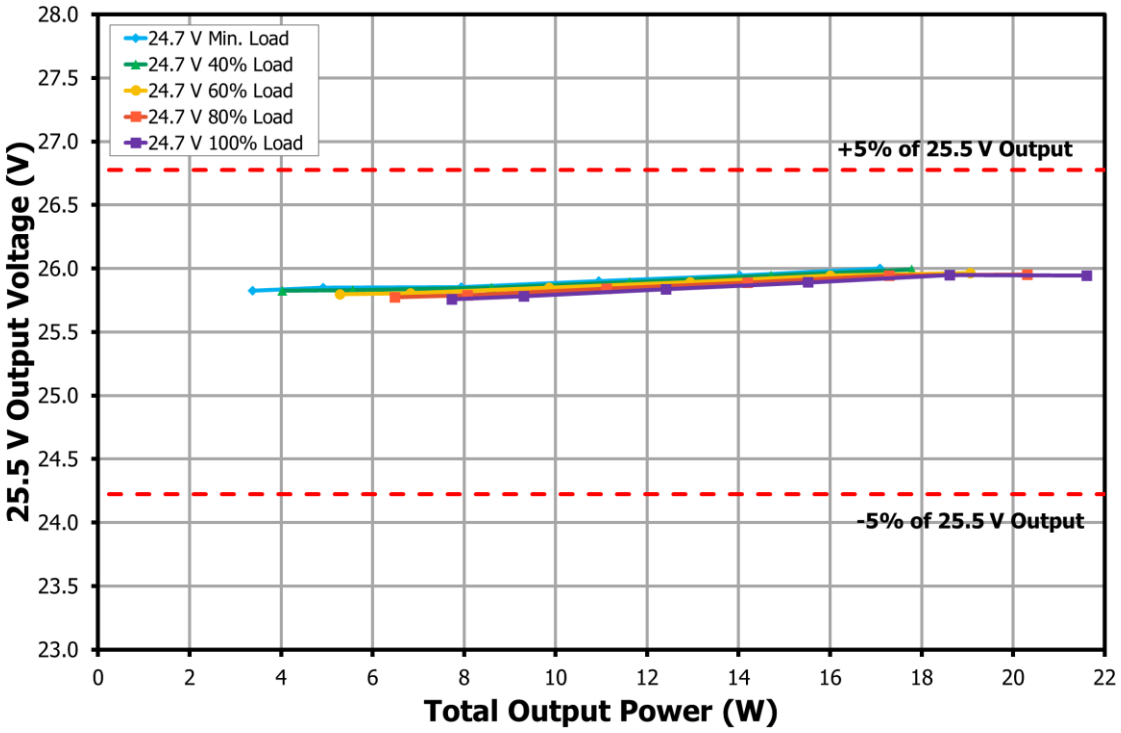


Figure 47 – 25.5 V Output Voltage vs. Total Output Power at 950 VDC Input and -40 °C Ambient.[35]

[35] Each line represents the 25.5 V output regulation vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

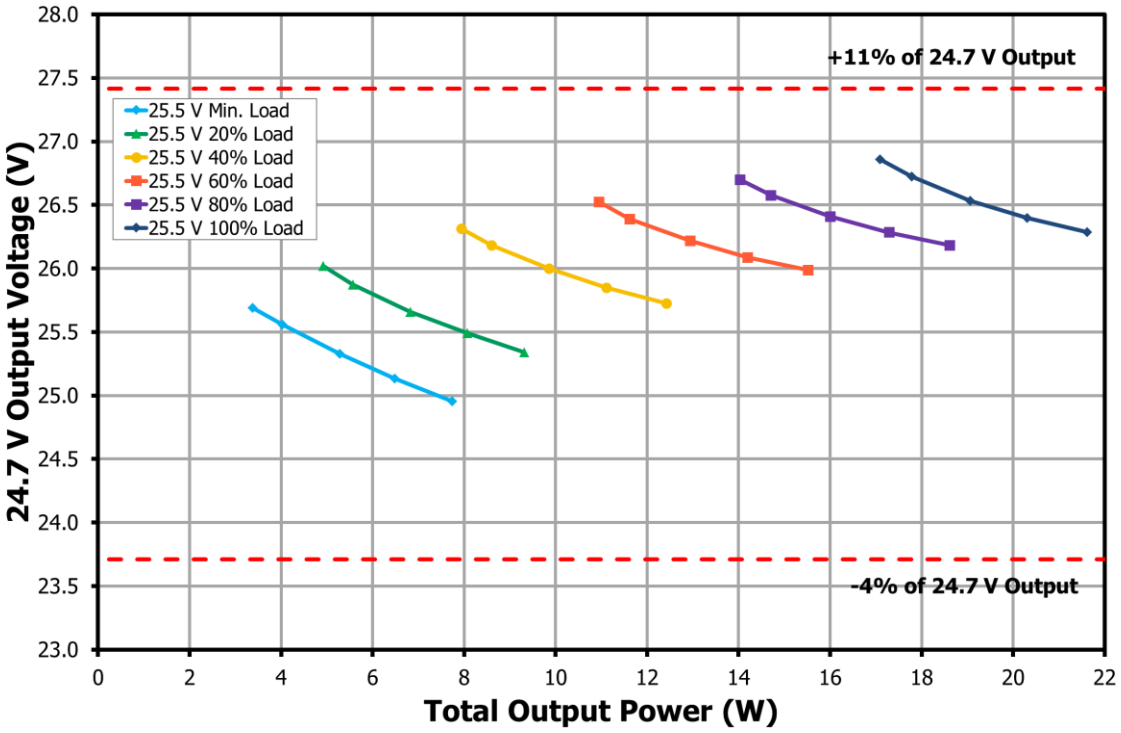


Figure 48 – 24.7 V Output Voltage vs. Total Output Power at 950 VDC Input and -40 °C Ambient.[36]

[36] Each line represents the 24.7 V output regulation vs. total output power of the unit under test when the 25.5V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

10.4 Line Regulation

Line regulation describes how the change in input voltage affects the output voltage.

10.4.1 Loading Condition: 25.5 V = Max. / 24.7 V = Max.

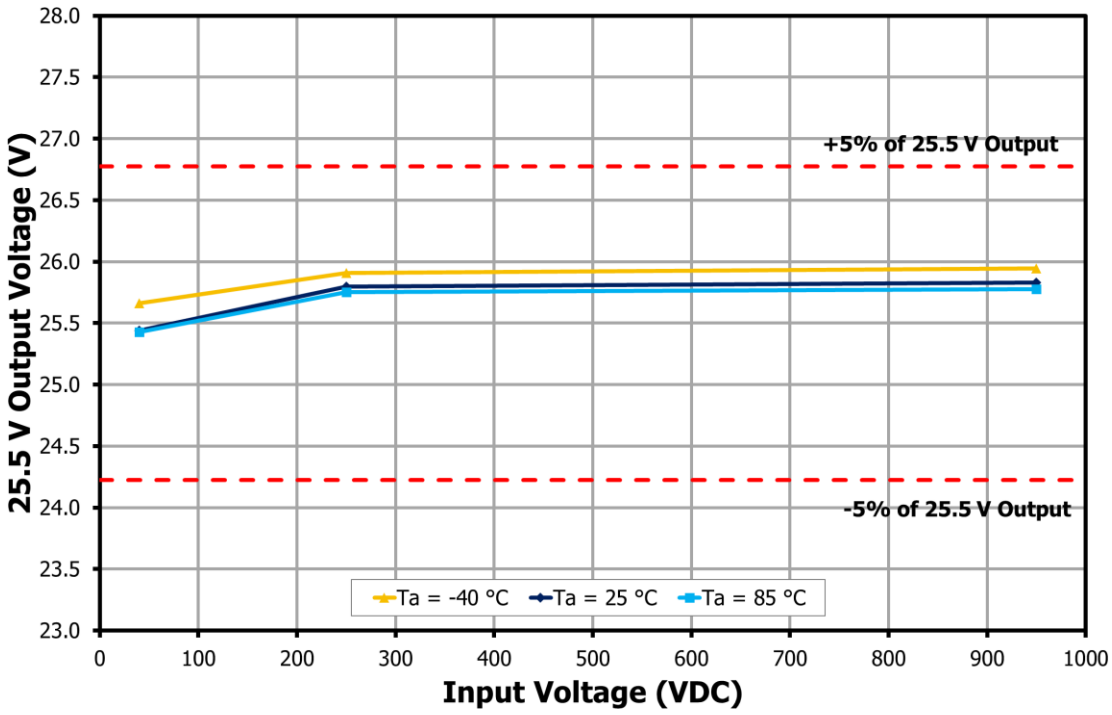


Figure 49 – 25.5 V Output Voltage vs. Input Line Voltage.

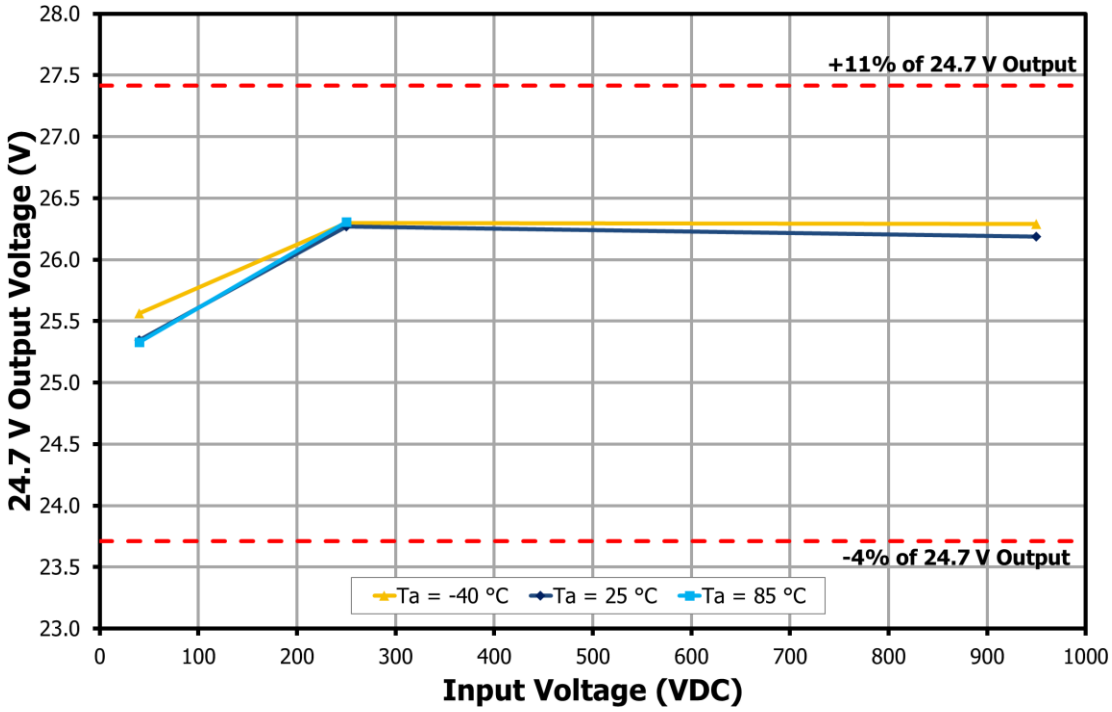


Figure 50 – 24.7 V Output Voltage vs. Input Line Voltage.

10.4.2 Loading Condition: 25.5 V = Max. / 24.7 V = Min.

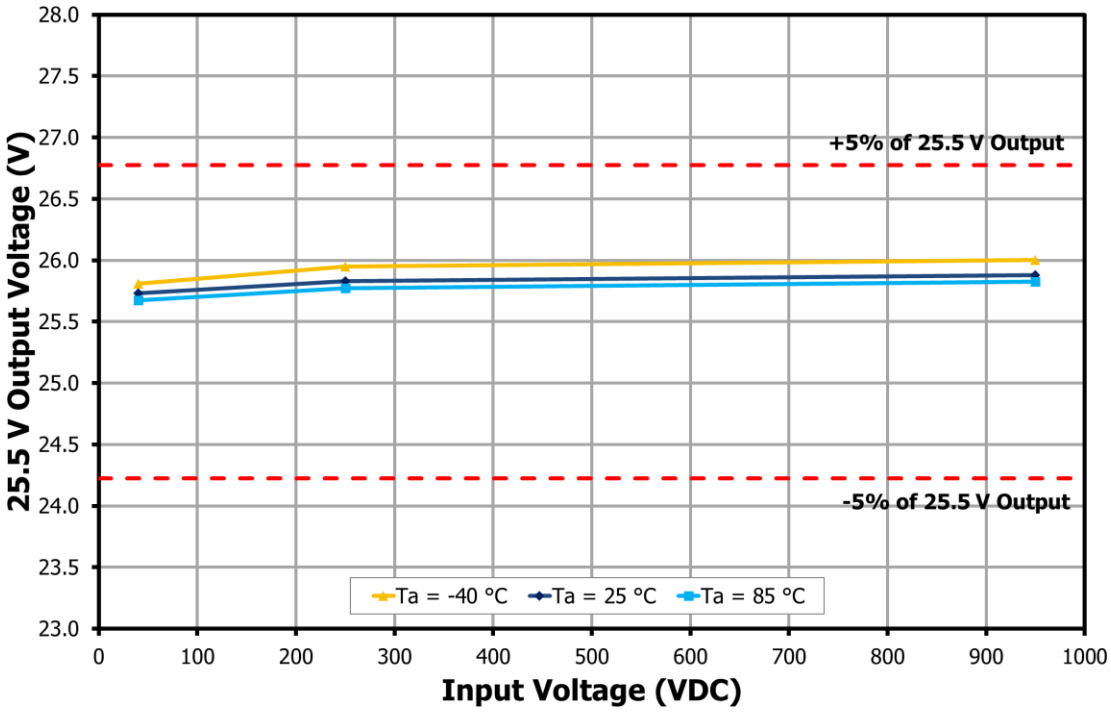


Figure 51 – 25.5 V Output Voltage vs. Input Line Voltage.

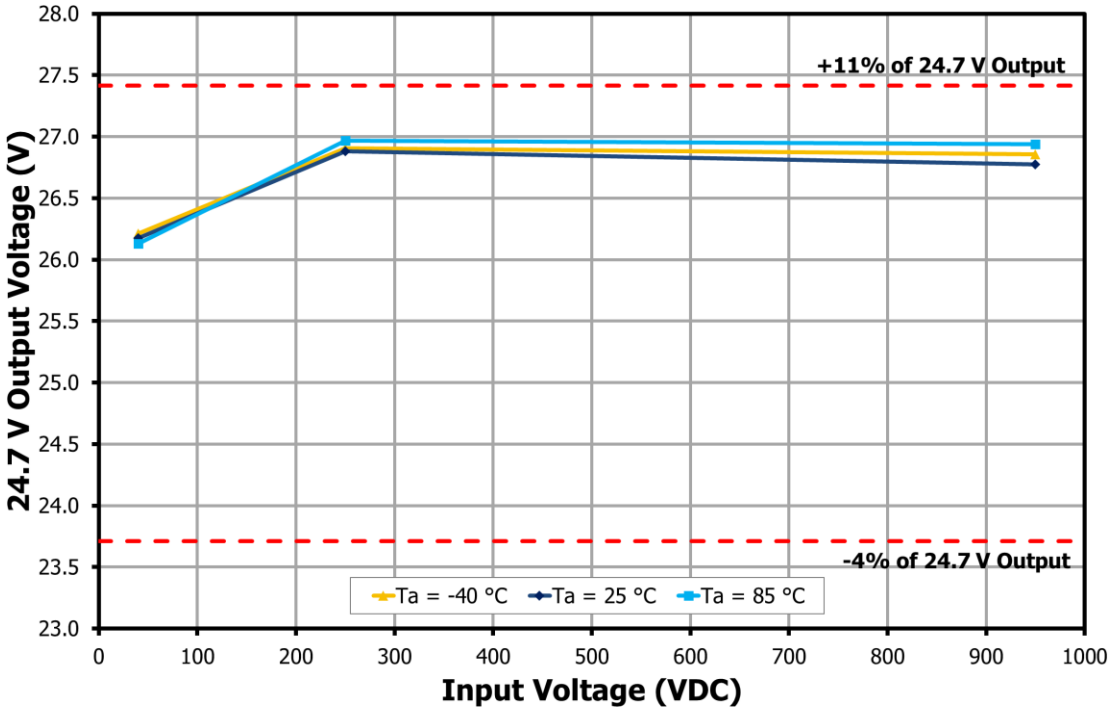


Figure 52 – 24.7 V Output Voltage vs. Input Line Voltage.

10.4.3 Loading Condition: 25.5 V = Min. / 24.7 V = Max.

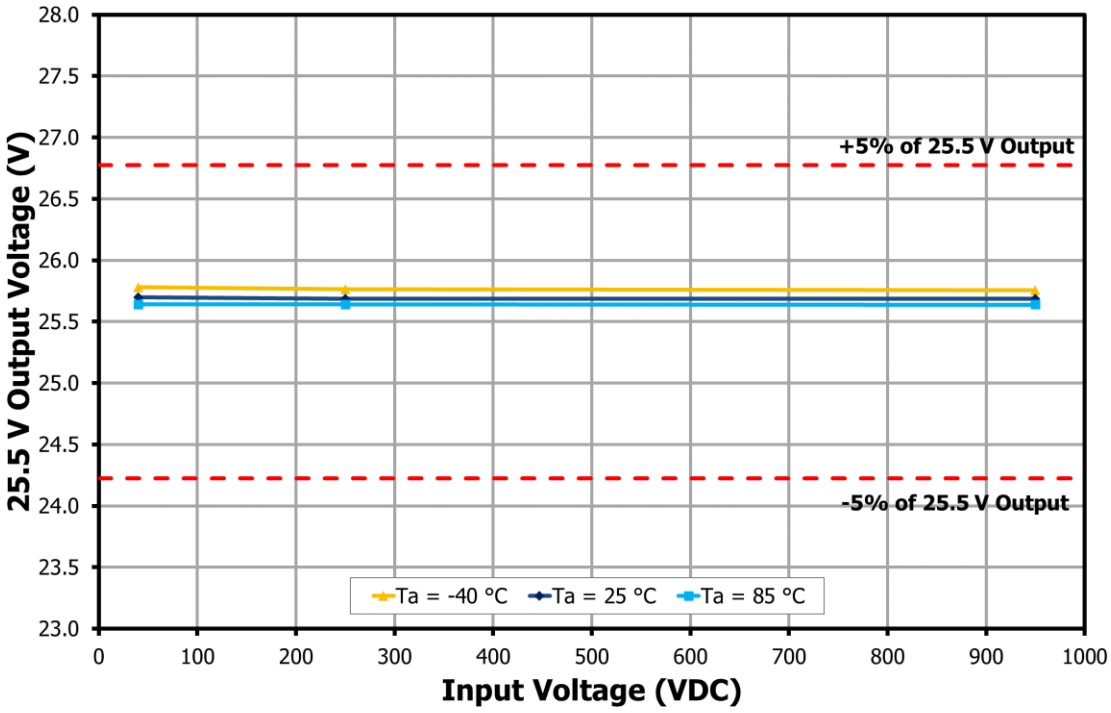


Figure 53 – 25.5 V Output Voltage vs. Input Line Voltage.

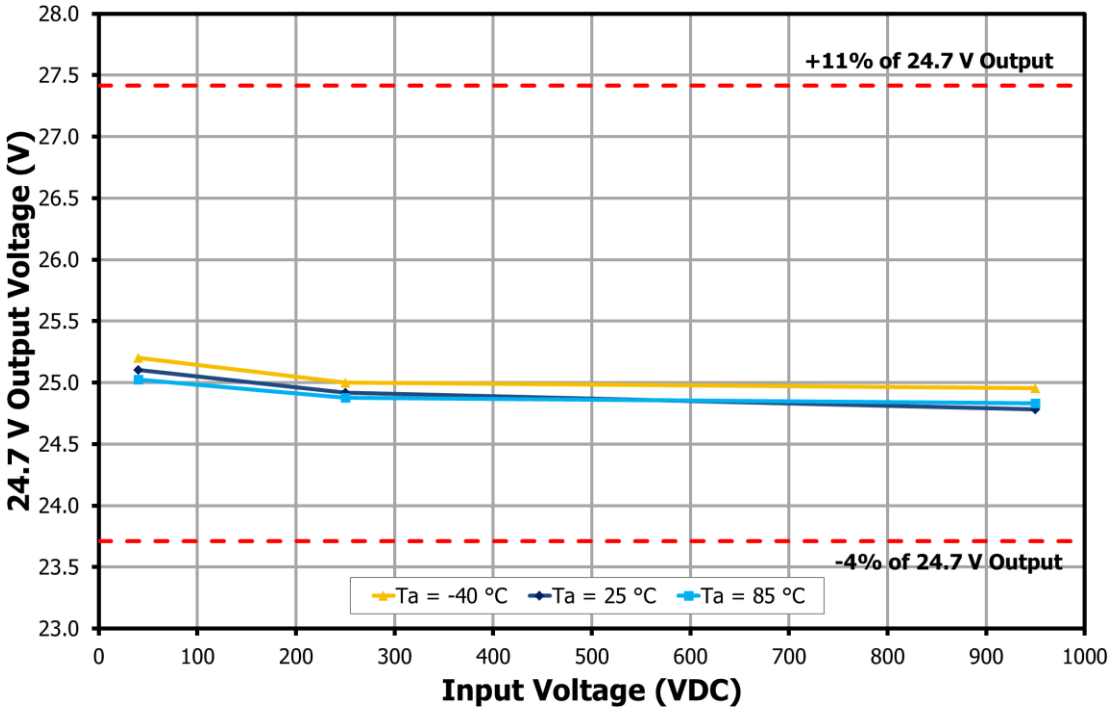


Figure 54 – 24.7 V Output Voltage vs. Input Line Voltage.

11 Thermal Performance

11.1 Thermal Data at 85 °C Ambient

The unit was placed inside a thermal chamber. The chamber was pre-heated to 85 °C for 30 minutes before turning on the unit-under-test. The following measurements were taken after soaking the unit for 1 hour to allow component temperatures to stabilize.

Critical Components	Temperature (°C)		
	40 VDC 10 W	250 VDC 20 W	950 VDC 20 W
InnoSwitch3 (IC200)	96	95	113
Primary Snubber Diode (D203)	92	93	98
Primary Snubber Resistor (R209)	90	91	93
Transformer Core (T200)	93	96	102
Transformer Winding (T200)	94	97	103
Synchronous Rectifier (SR) MOSFET (Q100)	90	93	97
SR MOSFET Snubber Resistor (R105)	91	94	99
25.5 V Stack Diode (D101)	97	107	110
24.7 V Freewheeling Diode (D100)	95	96	97
24.7 V Snubber Resistor (R101)	93	94	95
Output Current Sense Resistor (R116)	89	92	94
Ambient	86	86	86

Table 9 – Summary of DER-1030Q Critical Component Temperatures at 85 °C Ambient.

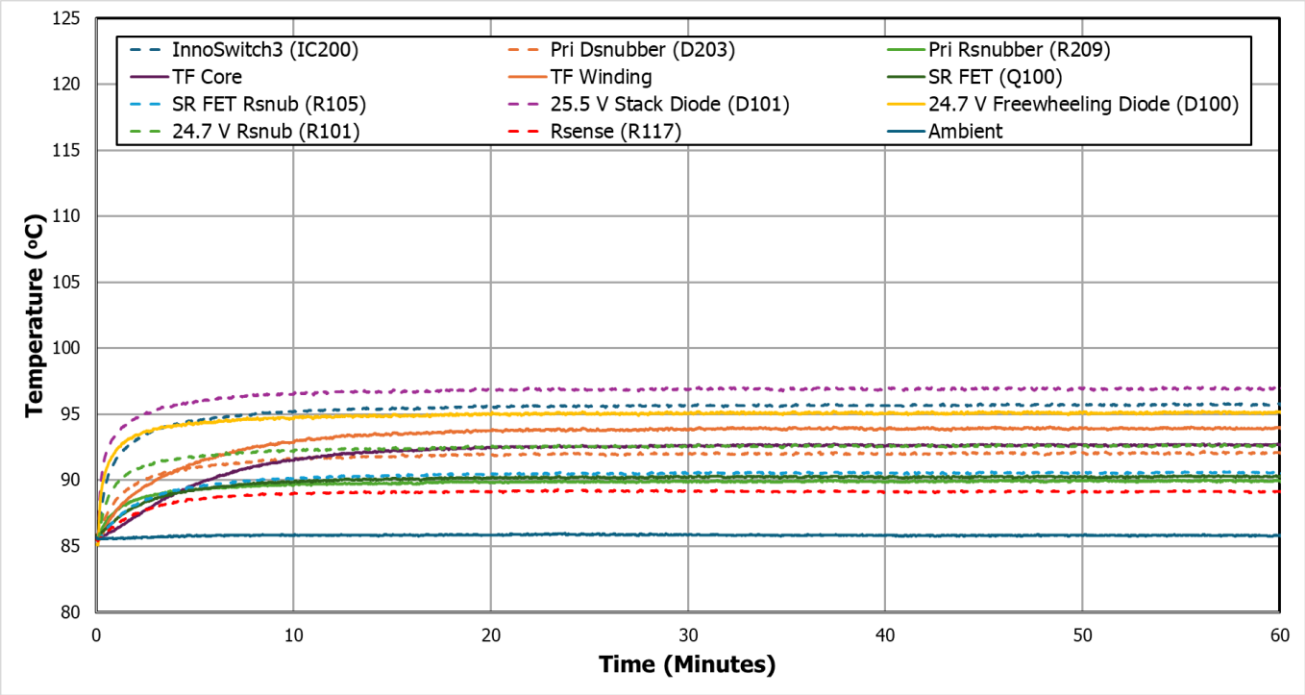


Figure 55 – Operating Temperature of DER-1030Q Critical Components (40 VDC Input, 10 W Output).

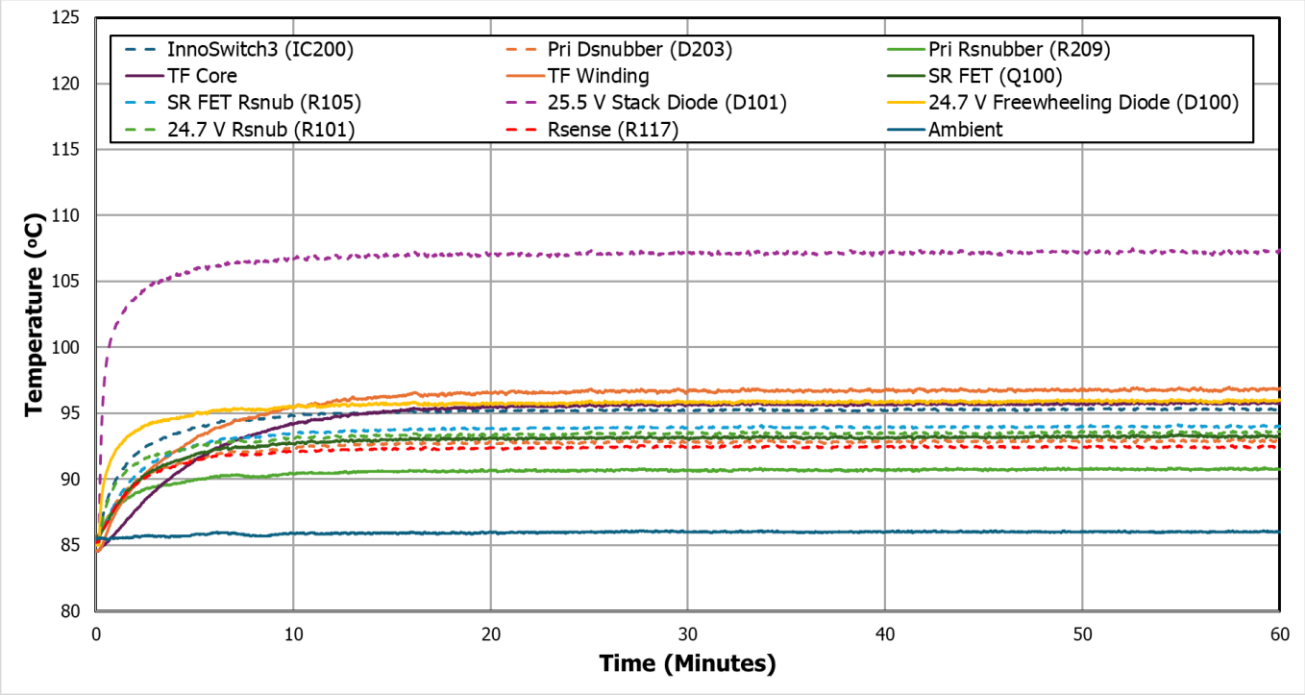


Figure 56 – Operating Temperature of DER-1030Q Critical Components (250 VDC Input, 20 W Output).

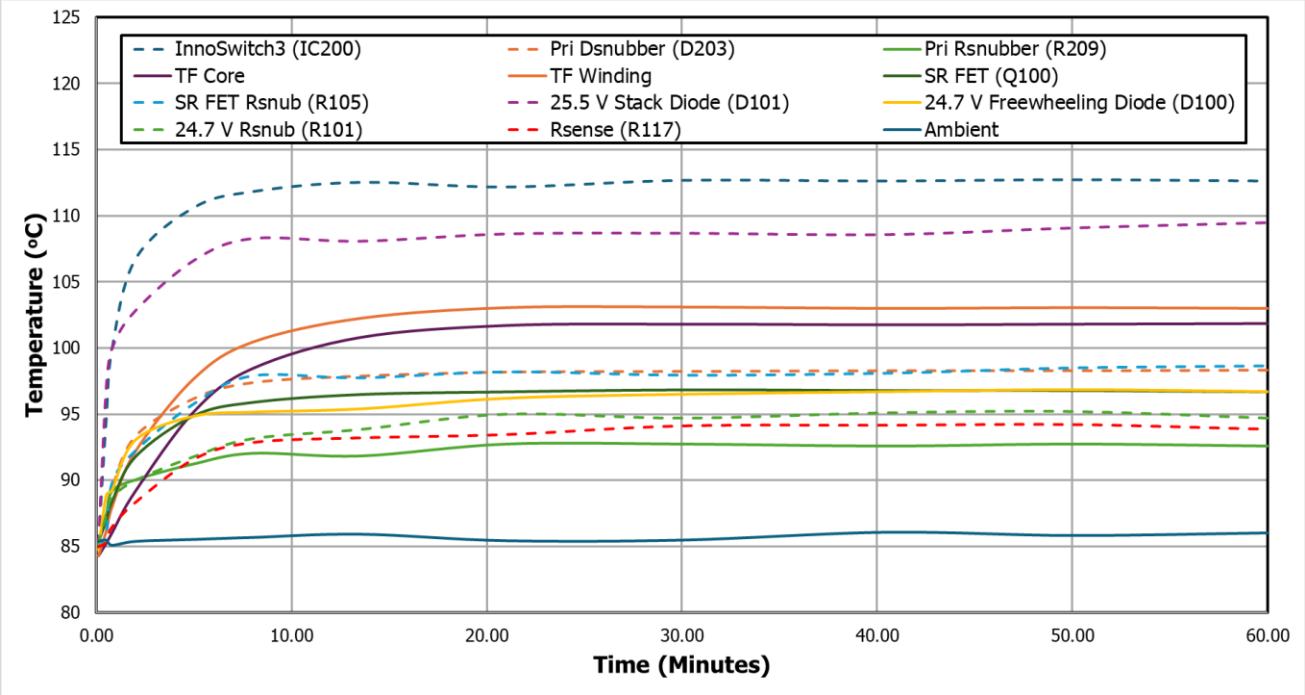


Figure 57 – Operating Temperature of DER-1030Q Critical Components (950 VDC Input, 20 W Output).

11.2 Thermal Data at 25 °C Ambient

The following thermal scans were captured using a Fluke thermal imager after soaking the power supply in an enclosure to minimize the effect of airflow for 1 hour.

Critical Components	Temperature (°C)		
	40 VDC 10 W	250 VDC 20 W	950 VDC 20 W
InnoSwitch3 (IC200)	54	45	70
Primary Snubber	43	41	53
Transformer	46	51	64
Synchronous Rectifier (SR) MOSFET (Q100)	37	40	47
SR MOSFET Snubber	38	43	56
25.5 V Stack Diode (D101)	48	63	70
24.7 V Freewheeling Diode (D100)	47	48	51
24.7 V Snubber	43	45	50
Output Current Sense Resistor (R116)	36	41	48

Table 10 – Summary of DER-1030Q Critical Components at 25 °C ambient.

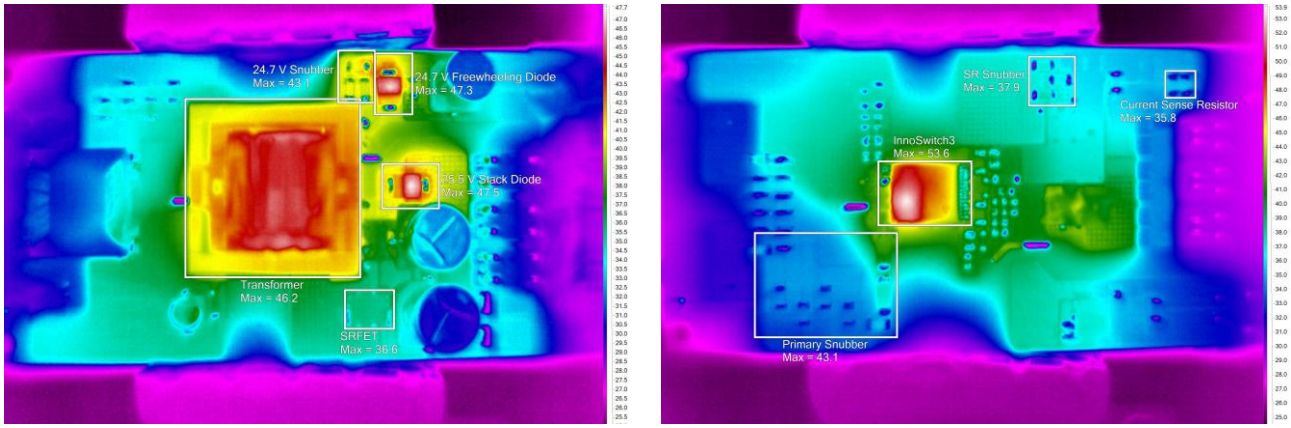


Figure 58 –Thermal Scans, Top PCB (Left) and Bottom PCB (Right). 40 VDC Input, 10 W Output

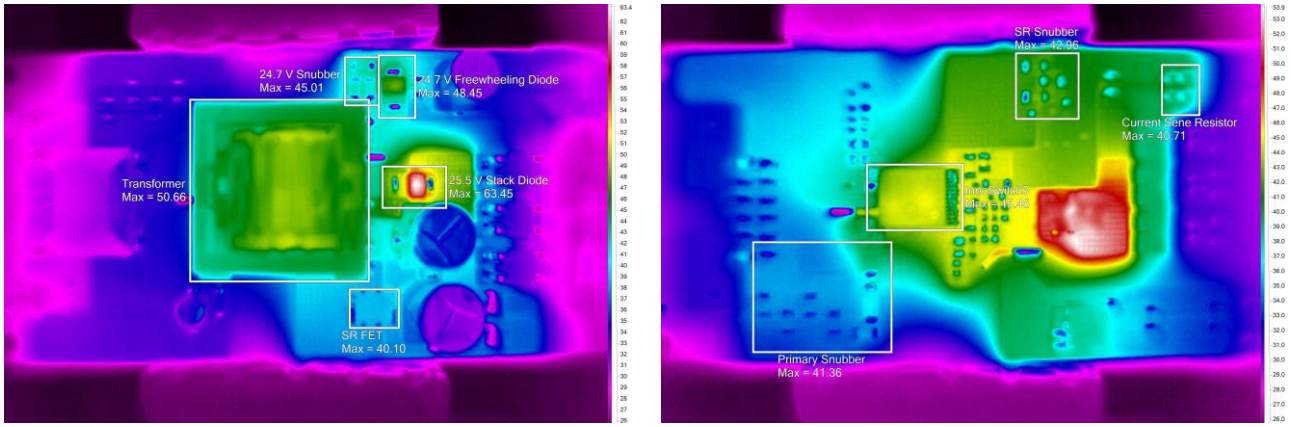


Figure 59 –Thermal Scans, Top PCB (Left) and Bottom PCB (Right). 250 VDC Input, 20 W Output

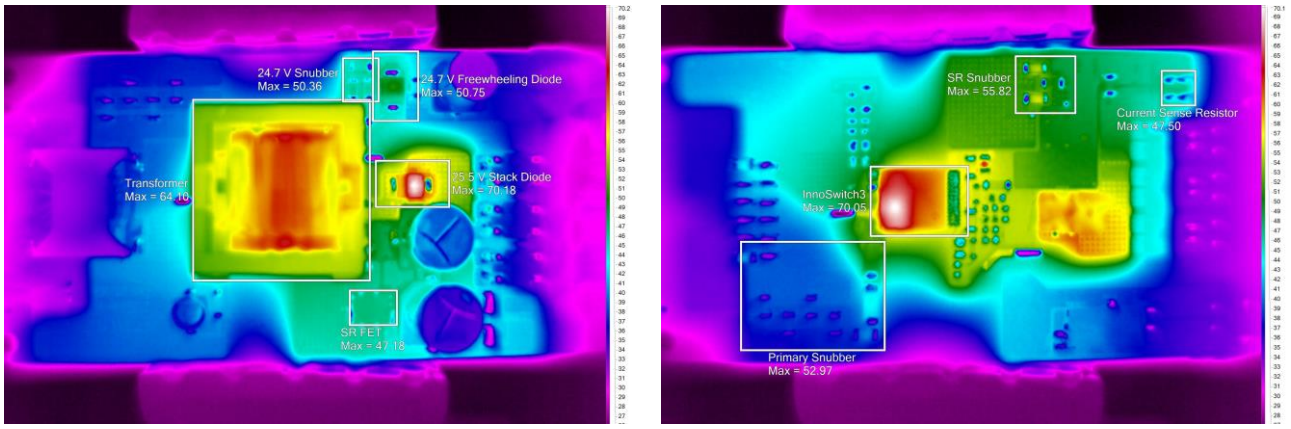


Figure 60 –Thermal Scans, Top PCB (Left) and Bottom PCB (Right). 950 VDC Input, 20 W Output

12 Waveforms

12.1 Start-up Waveforms

The following measurements were taken by connecting the unit to a fully charged DC-link capacitor[37] at different input voltages. A constant resistance load configuration was used for all start-up tests.

12.1.1 85 °C Ambient

12.1.1.1 Output Voltage and Current[38]

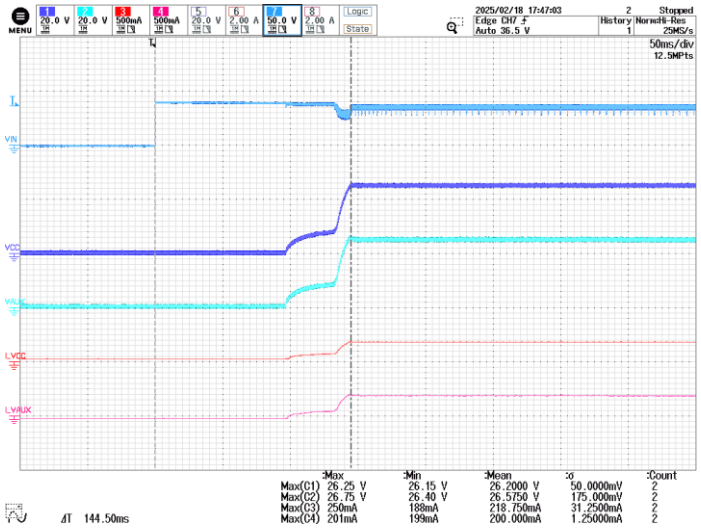


Figure 61 – Output Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W, 85 °C Ambient.
CH1: $V_{OUT\ (25.5\ V)}$, 20 V / div.
CH2: $V_{OUT\ (24.7\ V)}$, 20 V / div.
CH3: $I_{OUT\ (25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT\ (24.7\ V)}$, 500 mA / div.
CH7: V_{IN}, 50 V / div.
Time: 50 ms / div.

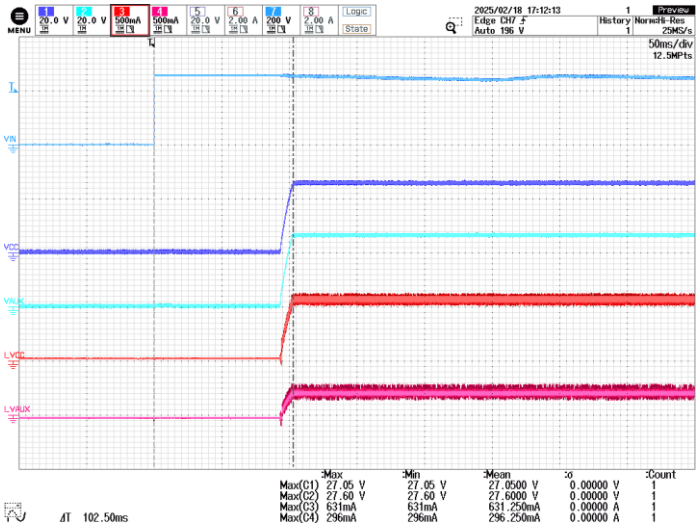


Figure 62 – Output Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W, 85 °C Ambient.
CH1: $V_{OUT\ (25.5\ V)}$, 20 V / div.
CH2: $V_{OUT\ (24.7\ V)}$, 20 V / div.
CH3: $I_{OUT\ (25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT\ (24.7\ V)}$, 500 mA / div.
CH7: V_{IN}, 200 V / div.
Time: 50 ms / div.

[37] Inrush current was limited by adding a 10 Ω series resistor between the DC-link capacitor and the unit under test.
[38] Voltage dip on the HV+ waveform was due to the line impedance between the DC link capacitor and the unit under test.

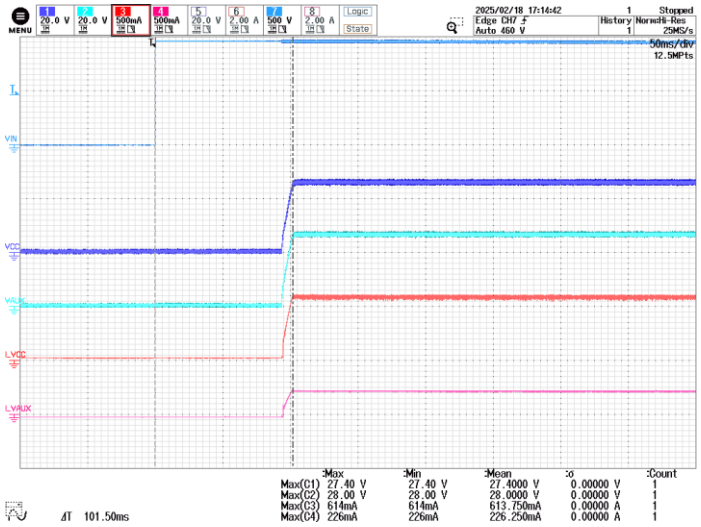


Figure 63 – Output Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH1: $V_{OUT\ (25.5\ V)}$, 20 V / div.
CH2: $V_{OUT\ (24.7\ V)}$, 20 V / div.
CH3: $I_{OUT\ (25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT\ (24.7\ V)}$, 500 mA / div.
CH7: V_{IN}, 500 V / div.
Time: 50 ms / div.

12.1.1.2 Primary Drain Voltage and Current[3940]

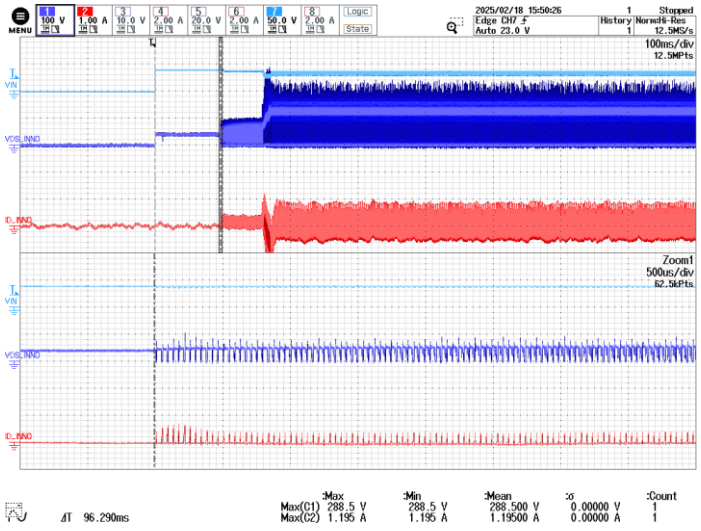


Figure 64 – INN3947FQ Drain Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 100 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
CH7: V_{IN}, 50 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

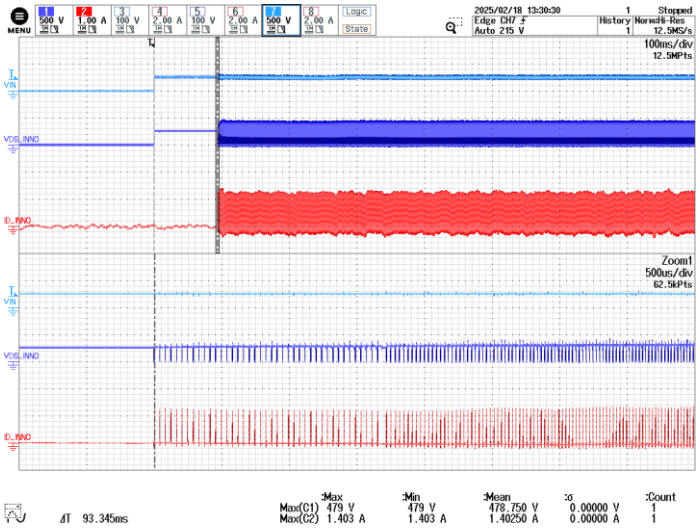


Figure 65 – INN3947FQ Drain Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

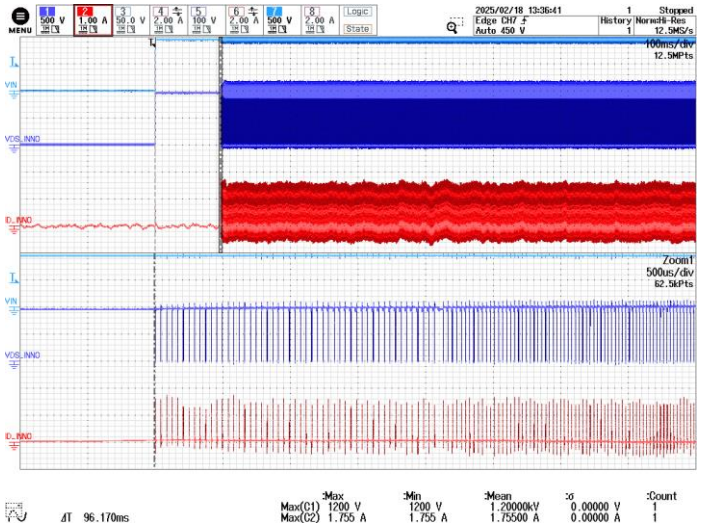


Figure 66 – INN3947FQ Drain Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

[39] The time between when HV+ turned on to when the InnoSwitch3 IC started switching was due to the "Wait and Listen" period of the InnoSwitch3 IC.
[40] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

12.1.1.3 SR FET Drain Voltage and Current[41]

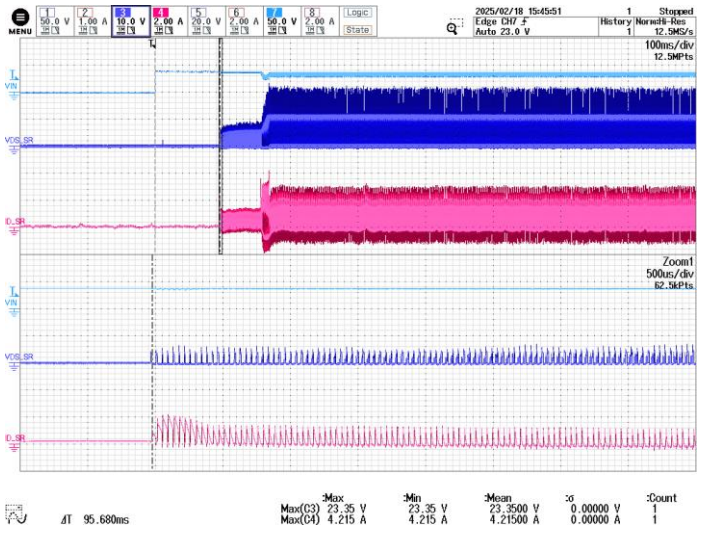


Figure 67 – SR FET Drain Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
85 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 10 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
CH7: V_{IN}, 50 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

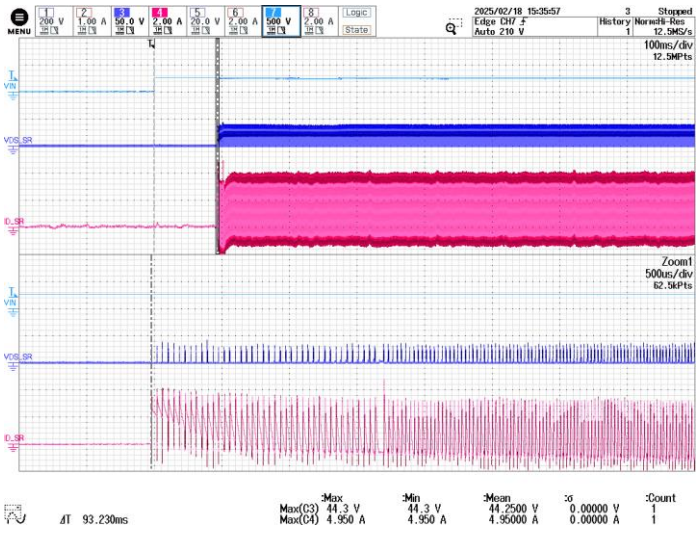


Figure 68 – SR FET Drain Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

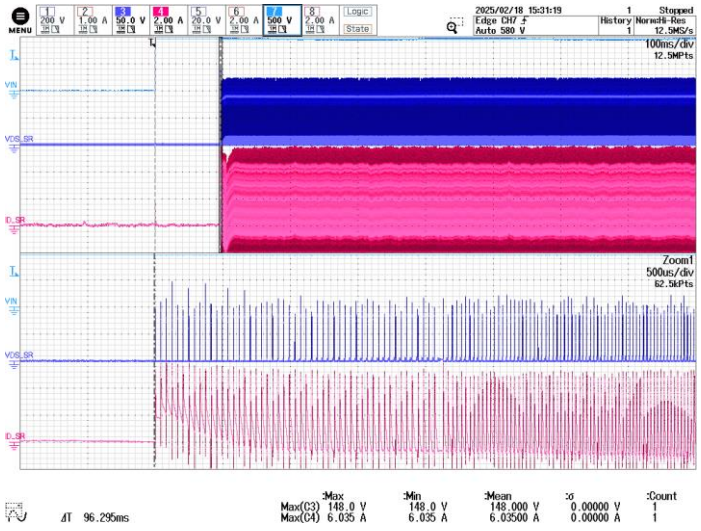


Figure 69 – SR FET Drain Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

[41] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

12.1.1.4 25.5 V Stack Diode Voltage and Current[42]

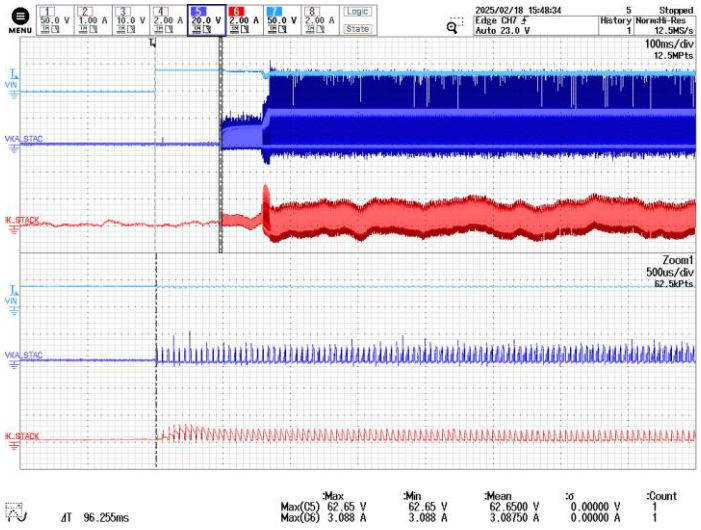


Figure 70 – 25.5 V Stack Diode Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
85 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 20 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 50 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

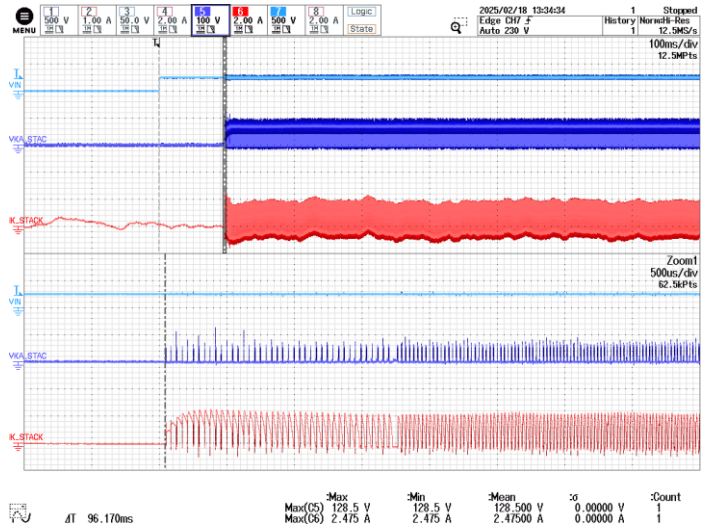


Figure 71 – 25.5 V Stack Diode Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

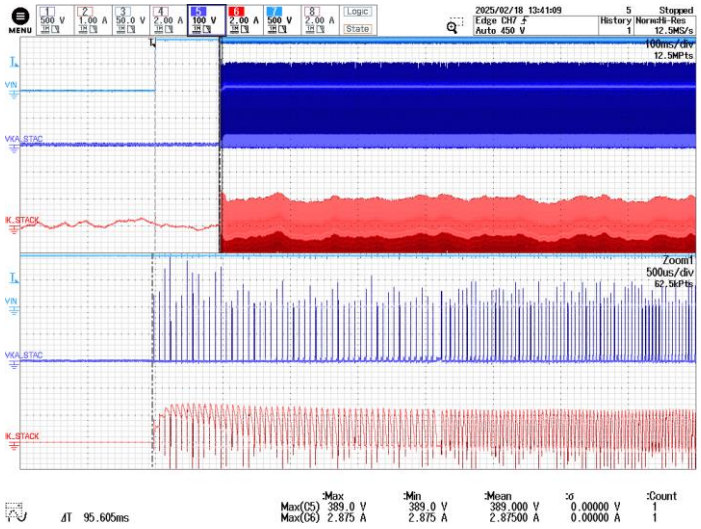


Figure 72 – 25.5 V Output Stack Diode Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

[42] The current waveforms were measured using a 300 A_{peak} Rogowski coil.

12.1.1.5 24.7 V Output Freewheeling Diode Voltage and Current[43]

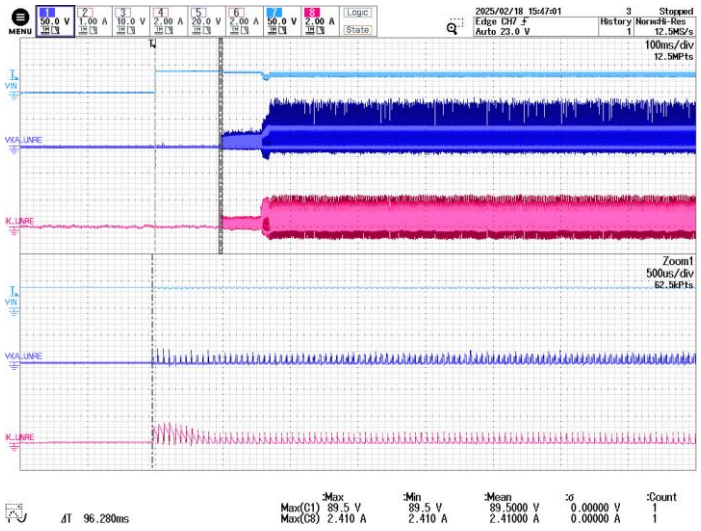


Figure 73 – 24.7 V Output Freewheeling Diode Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
85 °C Ambient.
CH1: $V_{KA\ (24.7\ V\ Diode)}$, 50 V / div.
CH8: $I_{K\ (24.7\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 50 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

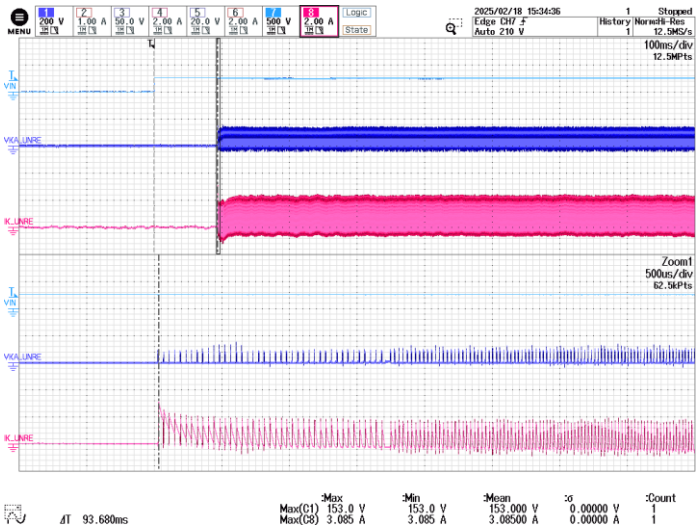


Figure 74 – 24.7 V Output Freewheeling Diode Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH1: $V_{KA\ (24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K\ (24.7\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

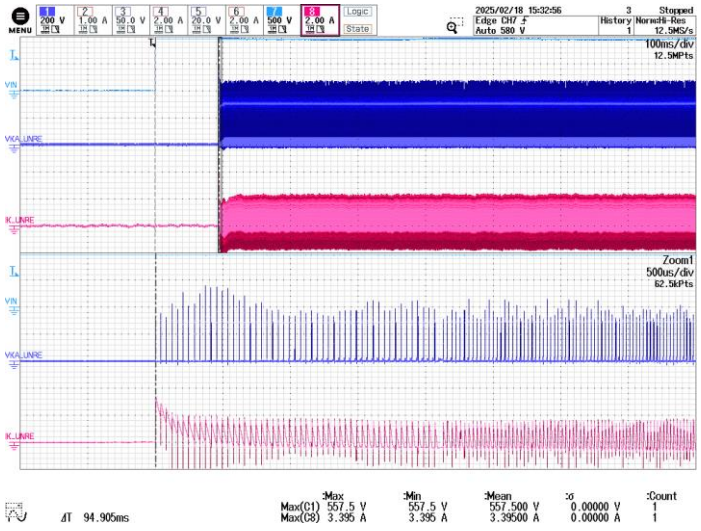


Figure 75 – 24.7 V Freewheeling Diode Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
85 °C Ambient.
CH1: $V_{KA\ (24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K\ (24.7\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

[43] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

12.1.2 -40 °C Ambient

12.1.2.1 Output Voltage and Current[44]

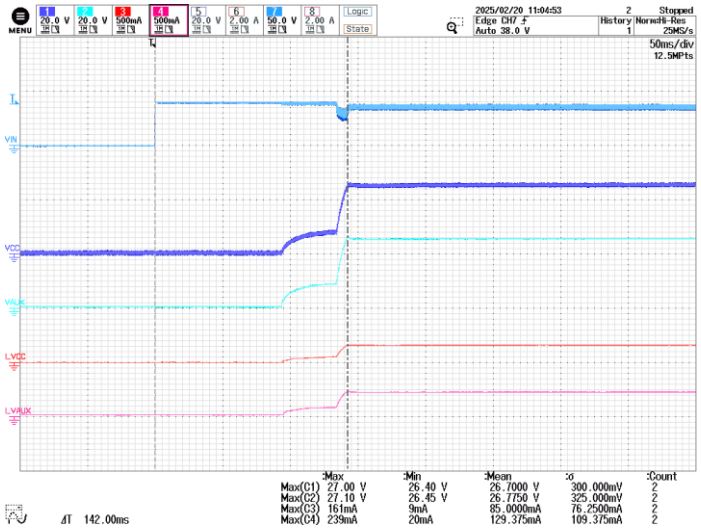


Figure 76 – Output Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
-40 °C Ambient.
CH1: $V_{OUT\ (25.5\ V)}$, 20 V / div.
CH2: $V_{OUT\ (24.7\ V)}$, 20 V / div.
CH3: $I_{OUT\ (25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT\ (24.7\ V)}$, 500 mA / div.
CH7: V_{IN}, 50 V / div.
Time: 50 ms / div.

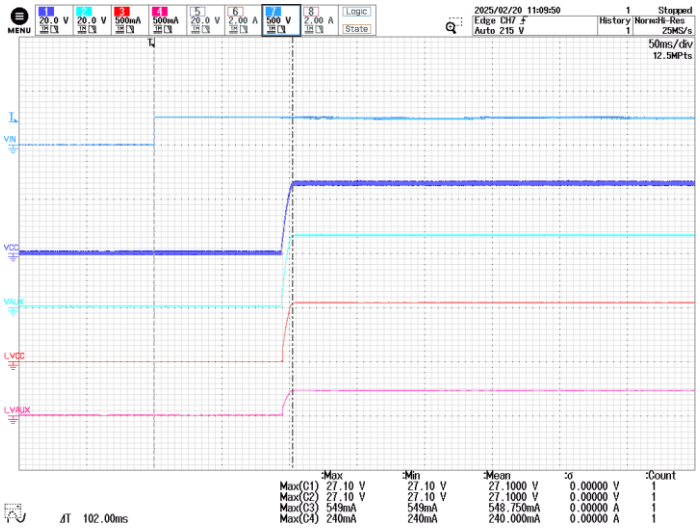


Figure 77 – Output Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH1: $V_{OUT\ (25.5\ V)}$, 20 V / div.
CH2: $V_{OUT\ (24.7\ V)}$, 20 V / div.
CH3: $I_{OUT\ (25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT\ (24.7\ V)}$, 500 mA / div.
CH7: V_{IN}, 500 V / div.
Time: 50 ms / div.

[44] Voltage dip on the HV+ waveform was due to the effective line impedance from the DC link capacitor to the unit under test.

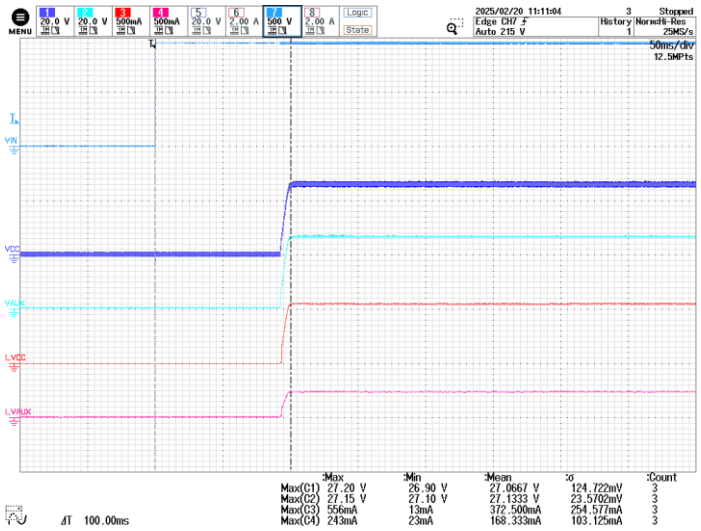


Figure 78 – Output Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH1: $V_{OUT\ (25.5\ V)}$, 20 V / div.
CH2: $V_{OUT\ (24.7\ V)}$, 20 V / div.
CH3: $I_{OUT\ (25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT\ (24.7\ V)}$, 500 mA / div.
CH7: V_{IN}, 500 V / div.
Time: 50 ms / div.

12.1.2.2 Primary Drain Voltage and Current[45, 46]

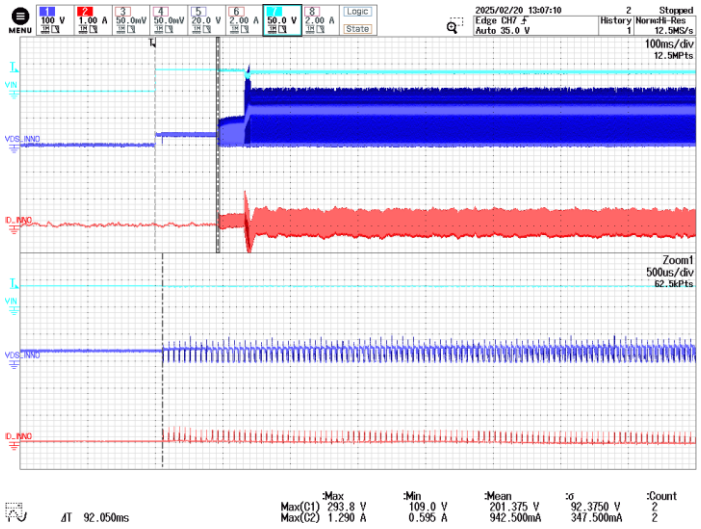


Figure 79 – INN3947FQ Drain Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
-40 °C Ambient.
CH1: $V_{DS(INNO)}$, 100 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
CH7: V_{IN}, 50 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

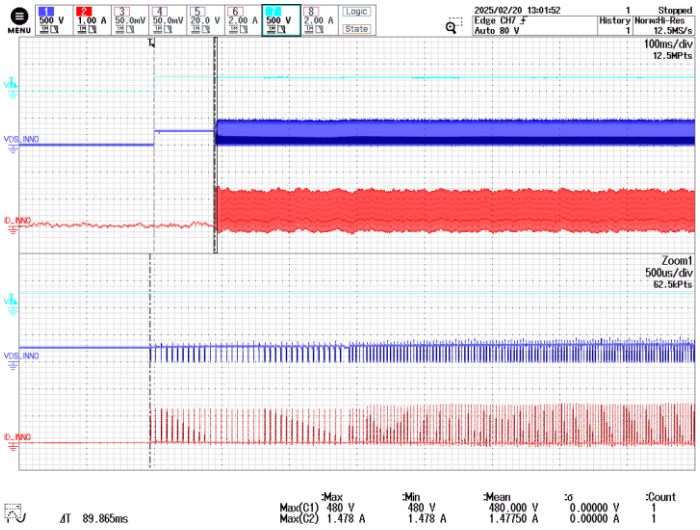


Figure 80 – INN3947FQ Drain Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

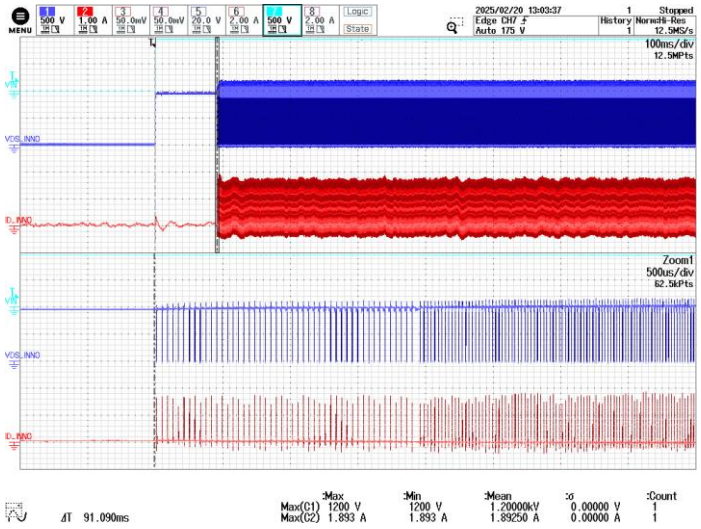


Figure 81 – INN3947FQ Drain Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

[45] The time between when HV+ turned on and the InnoSwitch3 IC starts switching was due to the "Wait and Listen" period of the InnoSwitch3 IC.
[46] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

12.1.2.3 SR FET Drain Voltage and Current[47]

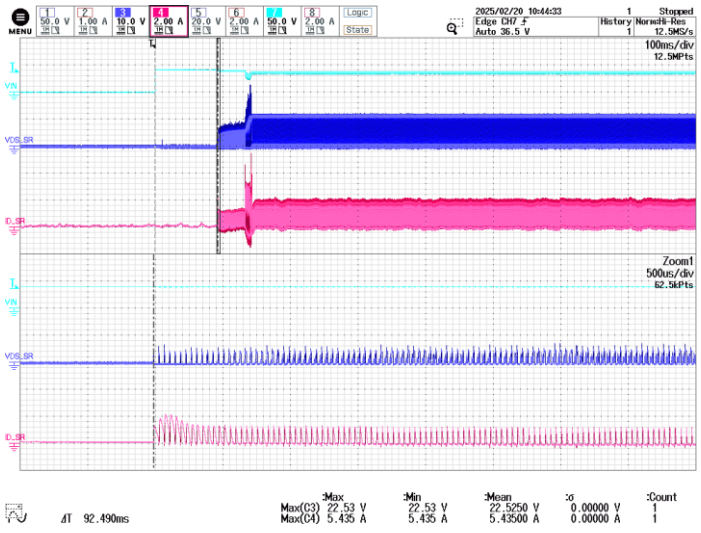


Figure 82 – SR FET Drain Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
-40 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 10 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
CH7: V_{IN}, 50 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

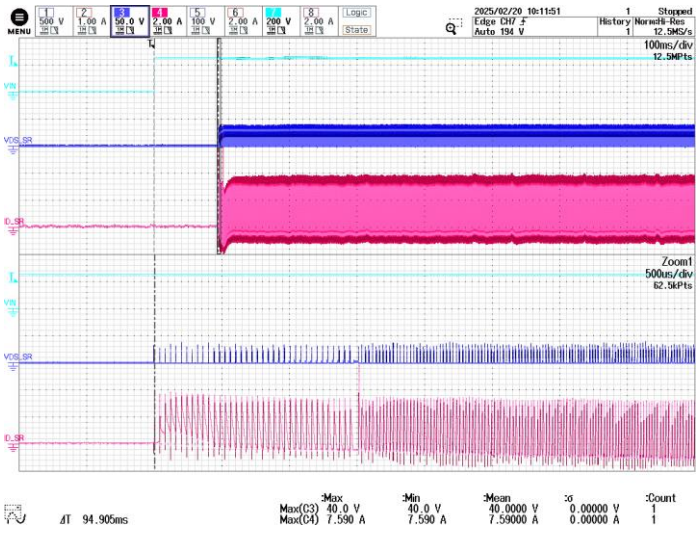


Figure 83 – SR FET Drain Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
CH7: V_{IN}, 200 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

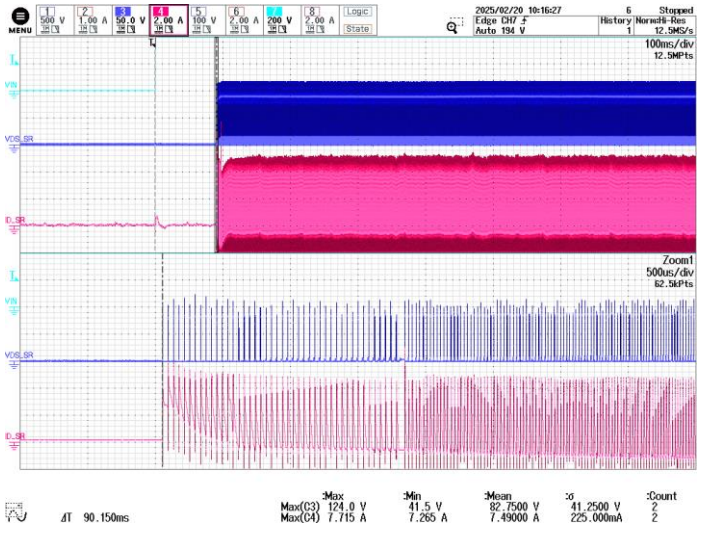


Figure 84 – SR FET Drain Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

[47] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

12.1.2.4 25.5 V Stack Diode Voltage and Current[48]

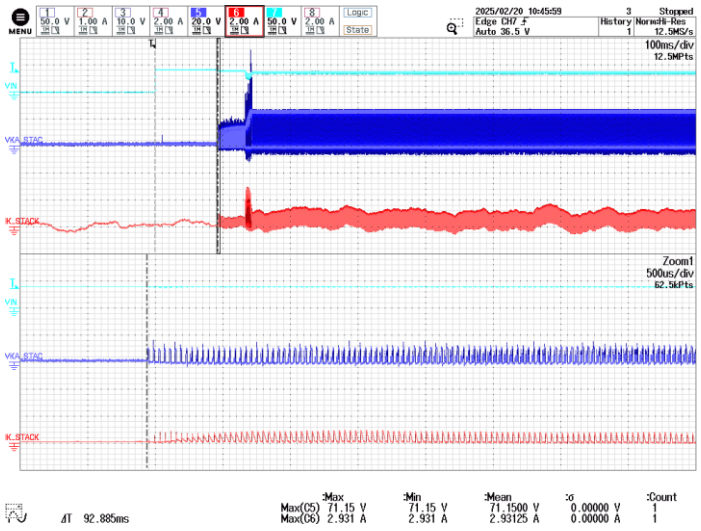


Figure 85 – 25.5 V Stack Diode Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
-40 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 20 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 50 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

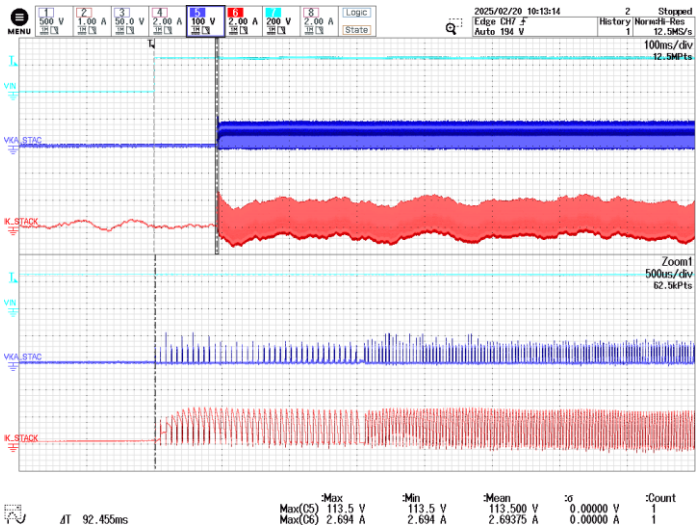


Figure 86 – 25.5 V Stack Diode Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 200 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

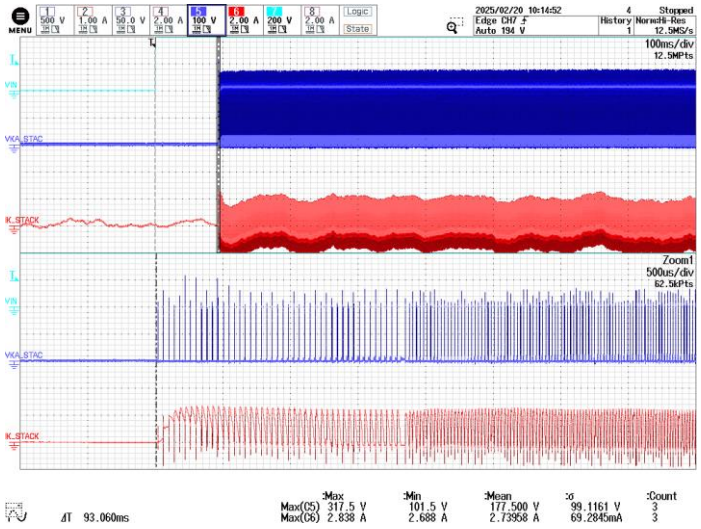


Figure 87 – 25.5 V Stack Diode Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 100 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

[48] The current waveforms were measured using a 300 A_{peak} Rogowski coil.

12.1.2.5 24.7 V output Freewheeling Diode Voltage and Current[49]

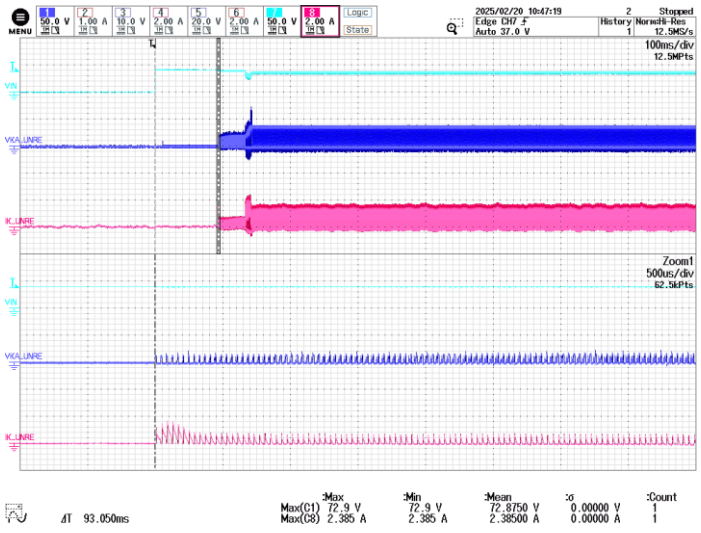


Figure 88 – 24.7 V Output Freewheeling Diode Voltage and Current.
40 VDC, 25.5 V / 162 Ω, 24.7 V / 102 Ω, 10 W,
-40 °C Ambient.
CH1: $V_{KA\ (24.7\ V\ Diode)}$, 50 V / div.
CH8: $I_{K\ (24.7\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 50 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

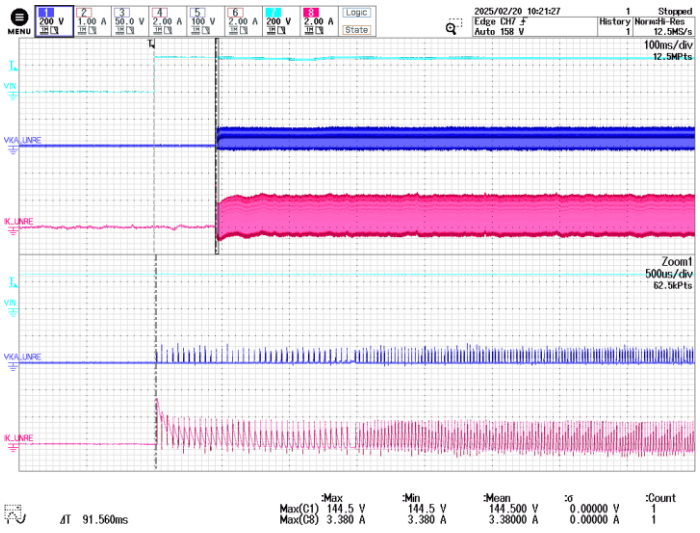


Figure 89 – 24.7 V Freewheeling Diode Voltage and Current.
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH1: $V_{KA\ (24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K\ (24.7\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 200 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

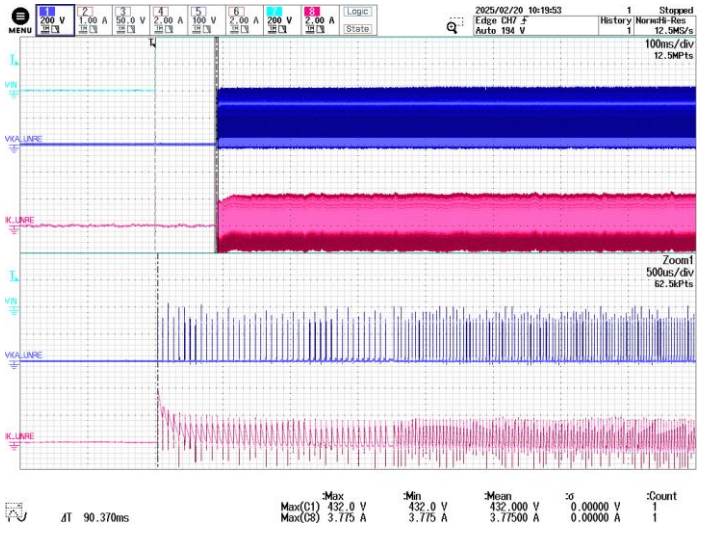


Figure 90 – 24.7 V Freewheeling Diode Voltage and Current.
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω, 20 W,
-40 °C Ambient.
CH1: $V_{KA\ (24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K\ (24.7\ V\ Diode)}$, 2 A / div.
CH7: V_{IN}, 500 V / div.
Time: 100 ms / div. (500 µs / div. Zoom)

[49] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

12.2 Steady-State Stress Waveforms

12.2.1 Switching Waveforms at 25 °C Ambient

Steady-State Switching Waveforms 25 °C Ambient										
Input	**25.5 V Output**	**24.7 V Output**	**INN3947FQ**		**SR FET**		**25.5 V Output Stack Diode**		**24.7 V Output Freewheeling Diode**	
V_{IN} (V)	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**IC200 V_{DS} (V)**	**V_{STRESS} (%)**	**Q100 V_{DS} (V)**	**V_{STRESS} (%)**	**D101 (V_{KA})**	**V_{STRESS} (%)**	**D100 (V_{KA})**	**V_{STRESS} (%)**
40	275	242	273	16	23	15	64	11	89	15
	0	0	158	9	14	9	33	5	47	8
250	550	242	460	27	41	28	99	17	148	25
	0	0	383	23	42	28	101	17	151	25
950	550	242	1198	70	128	85	302	50	464	77
	0	0	1098	65	128	85	296	49	460	77

Table 11 - Summary of Voltage Stress Analysis at 25 °C Ambient.

12.2.1.1 Primary Drain Voltage and Current

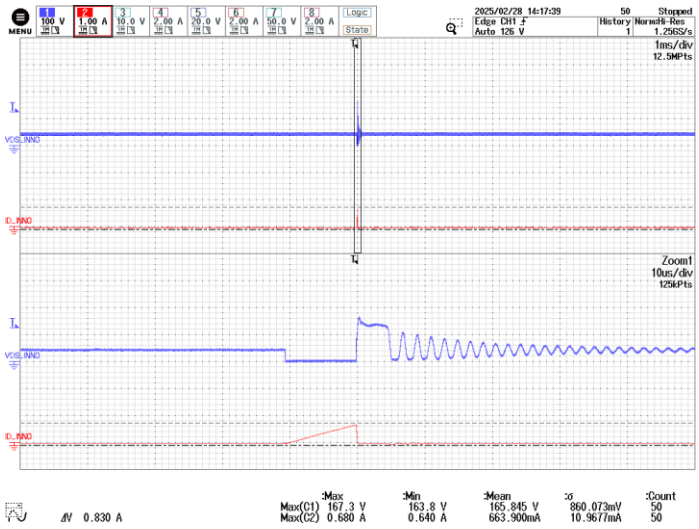


Figure 91 – INN3947FQ Drain Voltage and Current.
40 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH1: $V_{DS(INNO)}$, 100 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 92 – INN3947FQ Drain Voltage and Current.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH1: $V_{DS(INNO)}$, 100 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 10 µs / div.

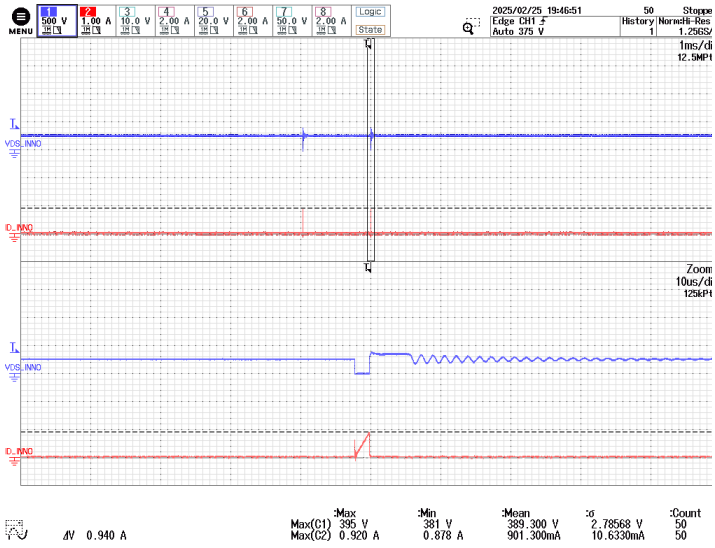


Figure 93 – INN3947FQ Drain Voltage and Current.
250 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

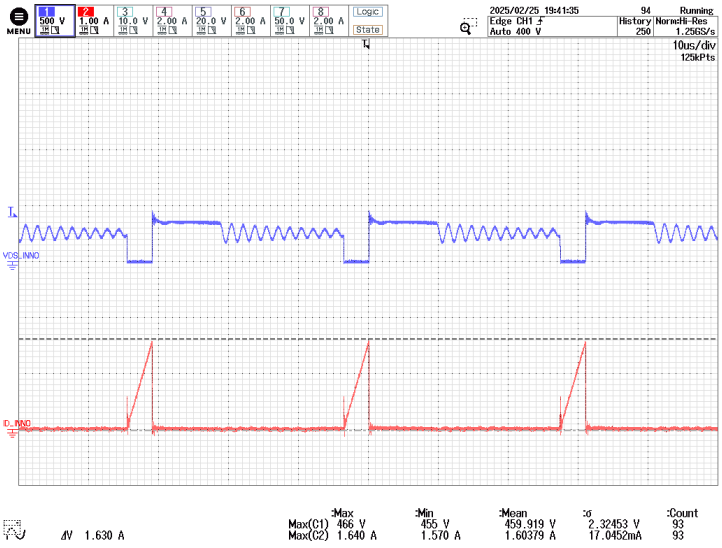


Figure 94 – INN3947FQ Drain Voltage and Current.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 10 µs / div.

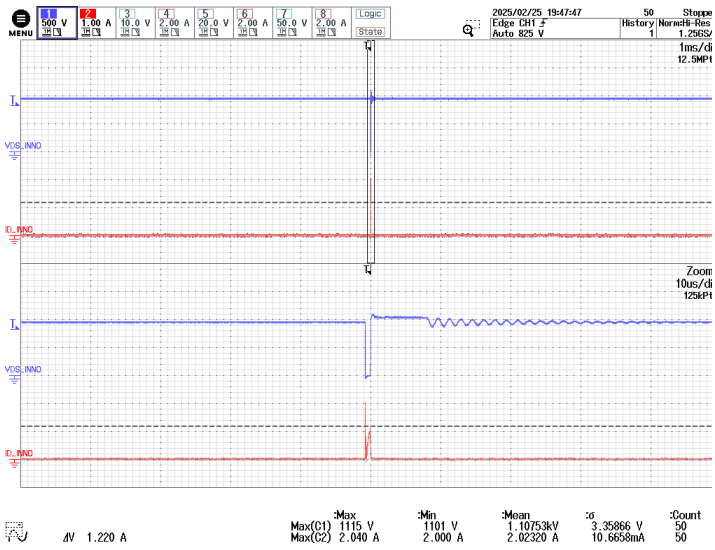


Figure 95 – INN3947FQ Drain Voltage and Current.
950 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

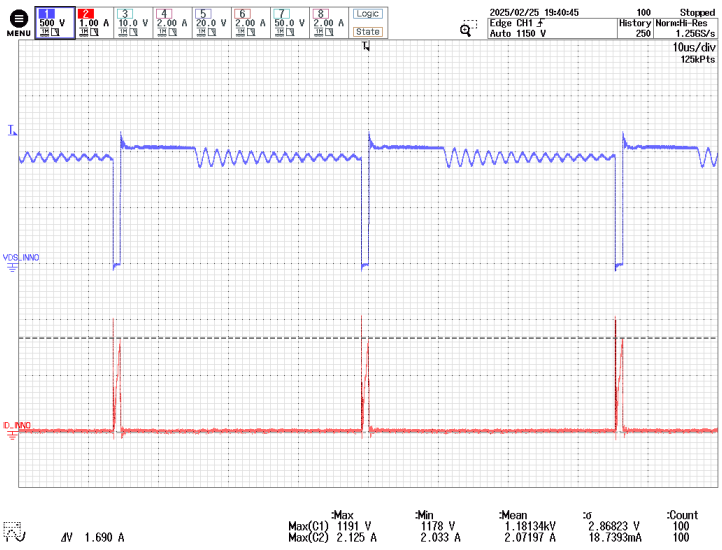


Figure 96 – INN3947FQ Drain Voltage and Current.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 10 µs / div.

12.2.1.2 SR FET Drain Voltage and Current[50]

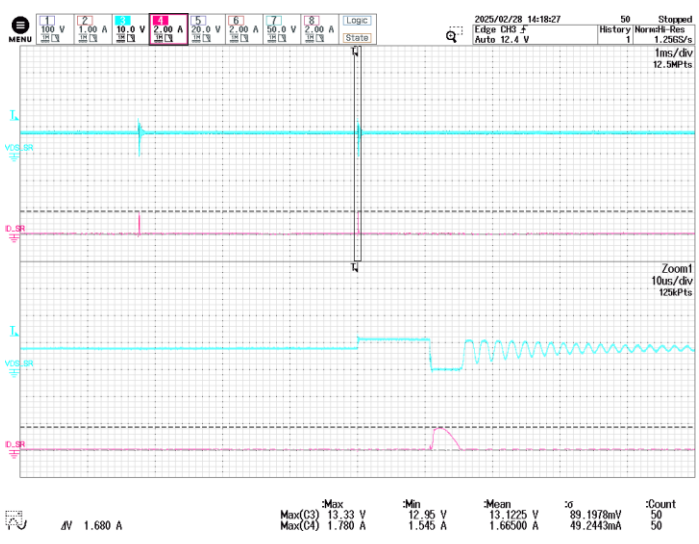


Figure 97 – SR FET Drain Voltage and Current.
40 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 10 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

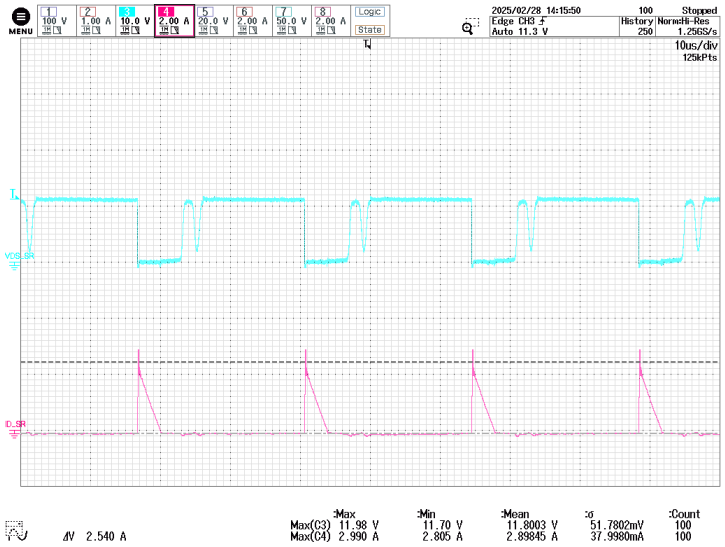


Figure 98 – SR FET Drain Voltage and Current.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
Time: 10 µs / div.

Figure 99 – SR FET Drain Voltage and Current.
250 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 100 – SR FET Drain Voltage and Current.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
Time: 10 µs / div.

[50] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

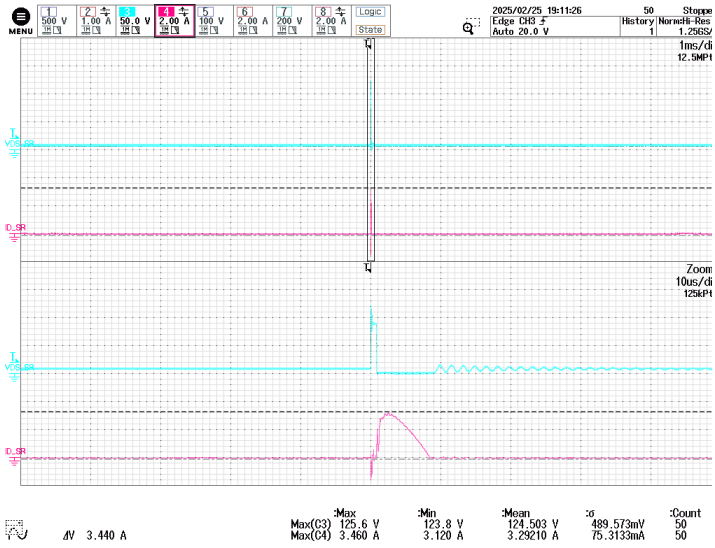


Figure 101 – SR FET Drain Voltage and Current.
950 VDC, 25.5 V/ No Load, 24.7 V / No Load,
25 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

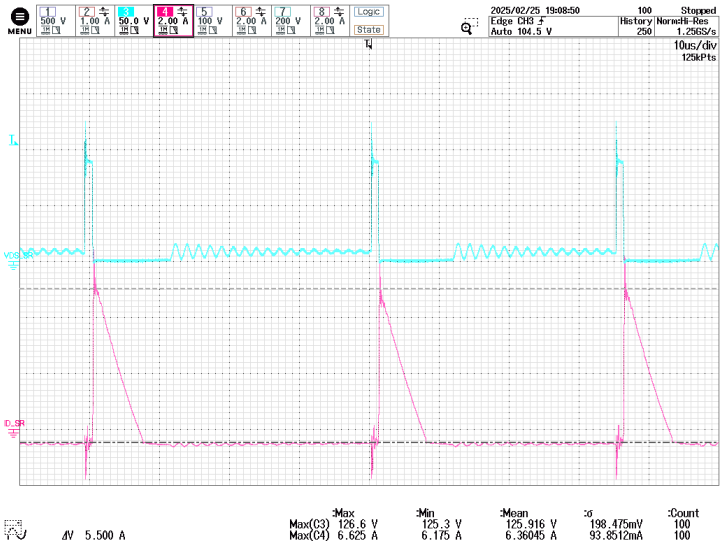


Figure 102 – SR FET Drain Voltage and Current.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH3: $V_{DS\ (SR\ FET)}$, 50 V / div.
CH4: $I_{D\ (SR\ FET)}$, 2 A / div.
Time: 10 µs / div.

12.2.1.3 25.5 V Output Stack Diode Voltage and Current[51]

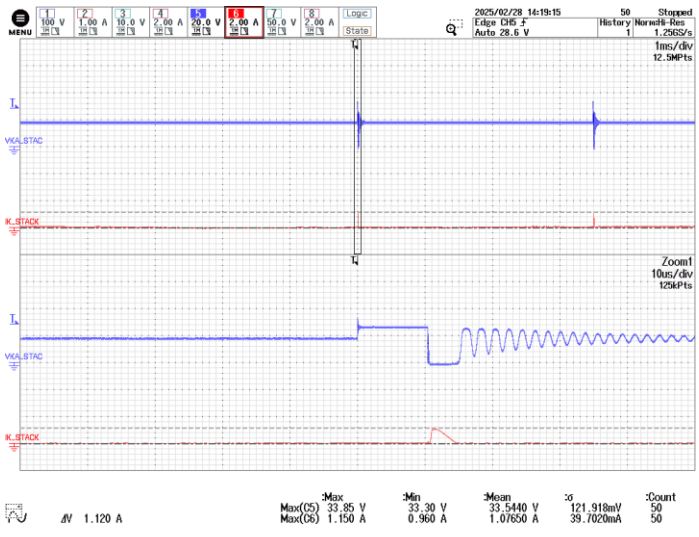


Figure 103 – 25.5 V Output Stack Diode Voltage and Current.
40 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 20 V / div.
CH6: $I_{K(25.5\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 104 – 25.5 V Stack Diode Voltage and Current.
40 VDC, 25.5 V / Full Load, 24.7 V/ Full Load,
25 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

Figure 105 – 25.5 V Stack Diode Voltage and Current.
250 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 20 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

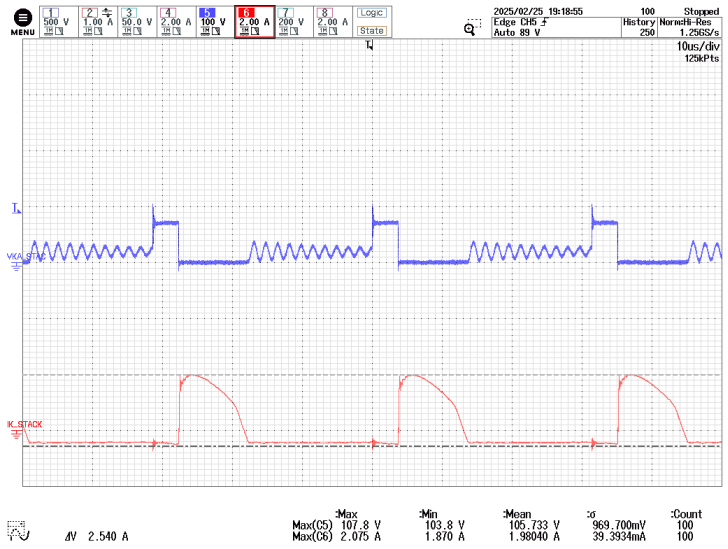


Figure 106 – 25.5 V Stack Diode Voltage and Current.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

[51] The current waveforms were measured using a 300 A_{peak} Rogowski coil.

Figure 107 – 25.5 V Stack Diode Voltage and Current.
950 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 20 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 108 – 25.5 V Stack Diode Voltage and Current.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH5: $V_{KA\ (25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K\ (25.5\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

12.2.1.4 24.7 V Output Freewheeling Diode Voltage and Current[52]

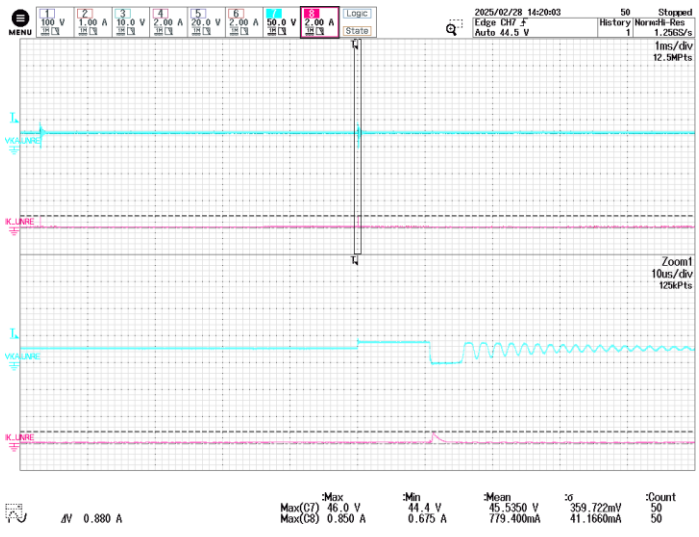


Figure 109 – 24.7 V Freewheeling Diode Voltage and Current.
40 VDC, 25.5 V / No Load, 24.7 V/ No Load,
25 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 50 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

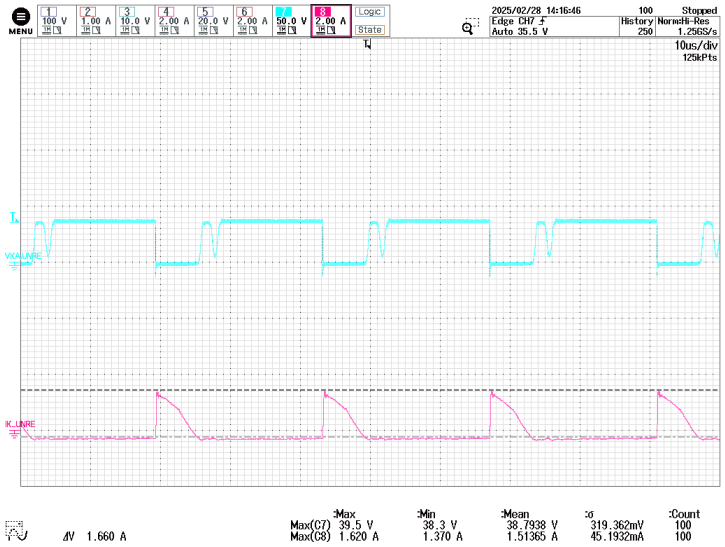


Figure 110 – 24.7 V Freewheeling Diode Voltage and Current.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

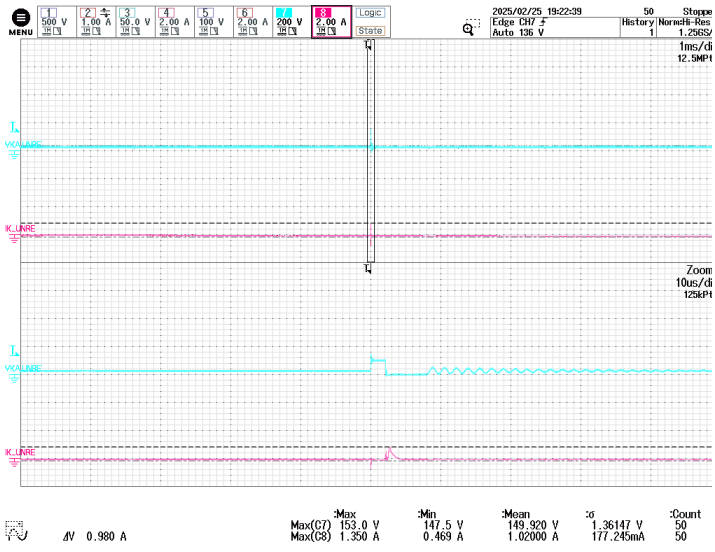


Figure 111 – 24.7 V Freewheeling Diode Voltage and Current.
250 VDC, 25.5 V / No Load, 24.7 V / No Load,
25 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 50 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 112 – 24.7 V Freewheeling Diode Voltage and Current.
250 VDC, 25.5 V / Full Load, 24.7 V/ Full Load,
25 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

[52] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

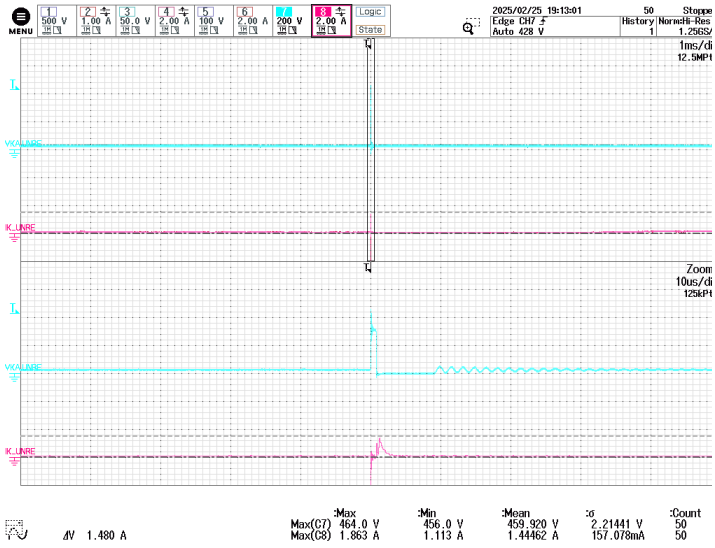


Figure 113 – 24.7 V Freewheeling Diode Voltage and Current.
950 VDC, 25.5 V/ No Load, 24.7 V / No Load,
25 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 50 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 114 – 24.7 V Freewheeling Diode Voltage and Current.
950 VDC, 25.5 V / Full Load, 24.7 V/ Full Load,
25 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

12.2.2 Switching Waveforms at 85 °C Ambient

Steady-State Switching Waveforms 85 °C Ambient										
Input	**25.5 V Output**	**24.7 V Output**	**INN3947FQ**		**SR FET**		**25.5 V Stack Diode**		**24.7 V Freewheeling Diode**	
V_{IN} (V)	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**IC200 V_{DS} (V)**	**V_{STRESS} (%)**	**Q100 V_{DS} (V)**	**V_{STRESS} (%)**	**D101 (V_{KA})**	**V_{STRESS} (%)**	**D100 (V_{KA})**	**V_{STRESS} (%)**
40	275	242	265	16	25	17	60	10	92	15
	0	0	158	9	13	9	32	5	45	8
250	550	242	460	27	40	27	101	17	144	24
	0	0	389	23	42	28	104	17	151	25
950	550	242	1186	70	126	84	312	52	479	80
	0	0	1103	65	125	83	312	52	482	80

Table 12 – Summary of Voltage Stress Analysis at 85 °C Ambient.

12.2.2.1 Primary Drain Voltage and Current[53]

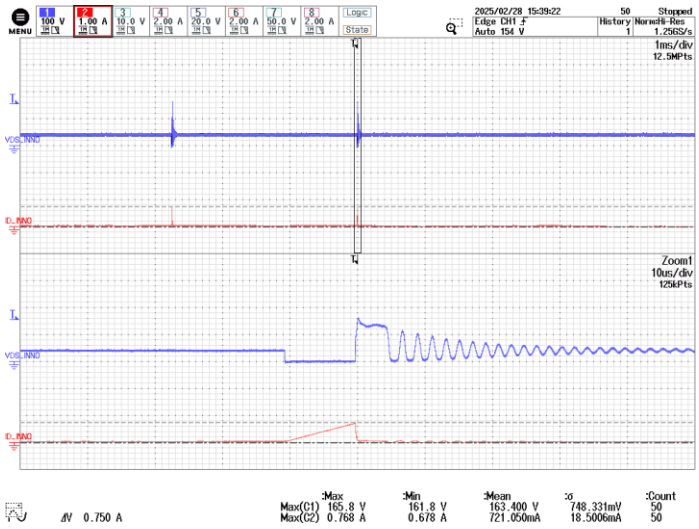


Figure 115 – INN3947FQ Drain Voltage and Current.
40 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 100 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 116 – INN3947FQ Drain Voltage and Current.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 10 µs / div.

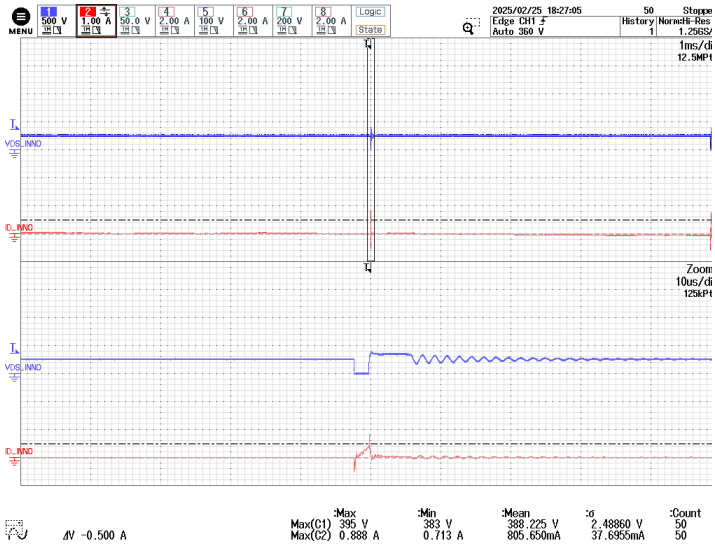


Figure 117 – INN3947FQ Drain Voltage and Current.
250 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

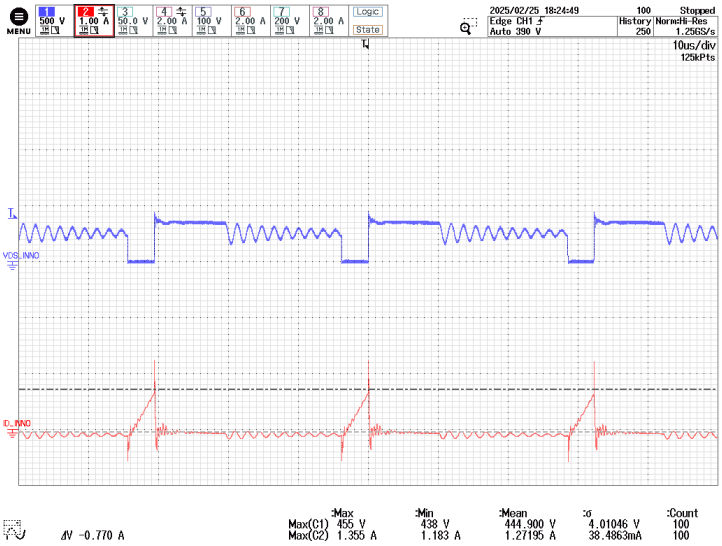


Figure 118 – INN3947FQ Drain Voltage and Current.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 10 µs / div.

[53] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

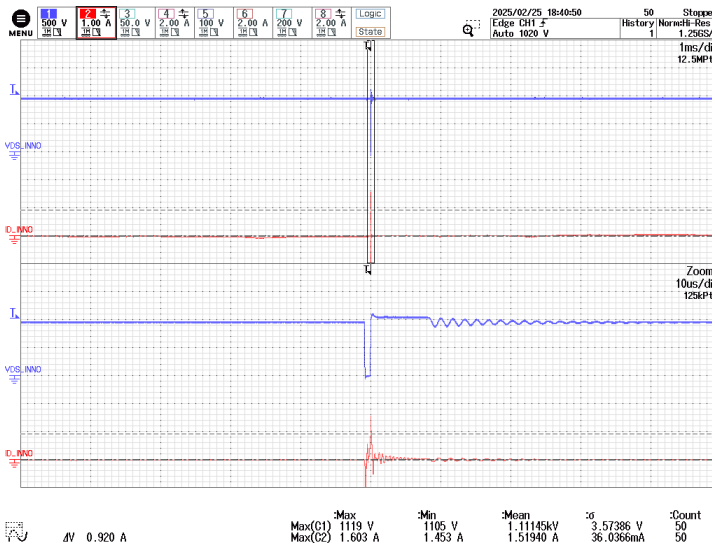


Figure 119 – INN3947FQ Drain Voltage and Current.
950 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 120 – INN3947FQ Drain Voltage and Current.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH2: $I_{D(INNO)}$, 1 A / div.
Time: 10 µs / div.

12.2.2.2 SR FET Drain Voltage and Current[54]

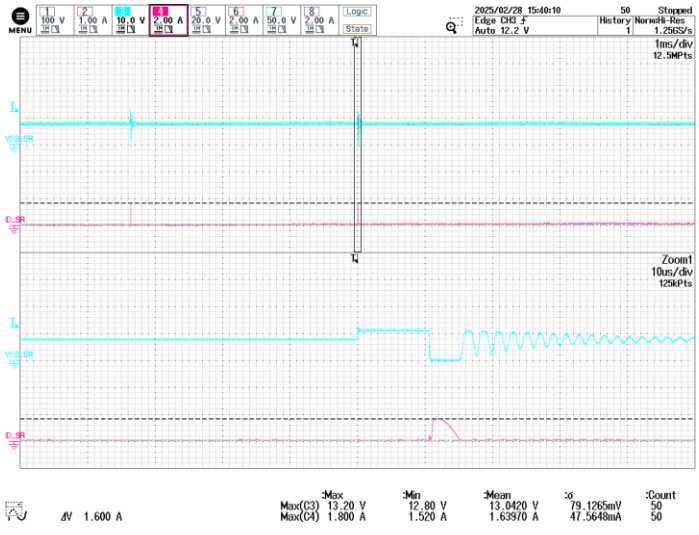


Figure 121 – SR FET Drain Voltage and Current.
40 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH3: $V_{DS(SR\ FET)}$, 10 V / div.
CH4: $I_{D(SR\ FET)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

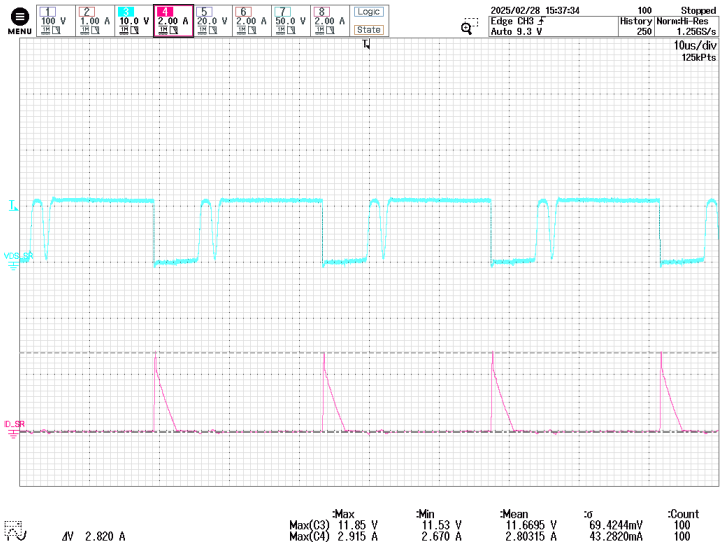


Figure 122 – SR FET Drain Voltage and Current.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH3: $V_{DS(SR\ FET)}$, 50 V / div.
CH4: $I_{D(SR\ FET)}$, 2 A / div.
Time: 10 µs / div.

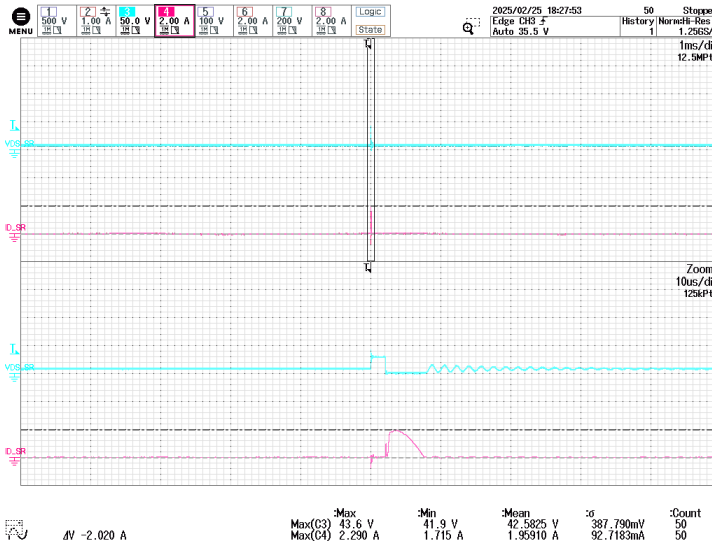


Figure 123 – SR FET Drain Voltage and Current.
250 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH3: $V_{DS(SR\ FET)}$, 50 V / div.
CH4: $I_{D(SR\ FET)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 124 – SR FET Drain Voltage and Current.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH3: $V_{DS(SR\ FET)}$, 50 V / div.
CH4: $I_{D(SR\ FET)}$, 2 A / div.
Time: 10 µs / div.

[54] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

Figure 125 – SR FET Drain Voltage and Current.
950 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH3: $V_{DS(SR\ FET)}$, 50 V / div.
CH4: $I_{D(SR\ FET)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

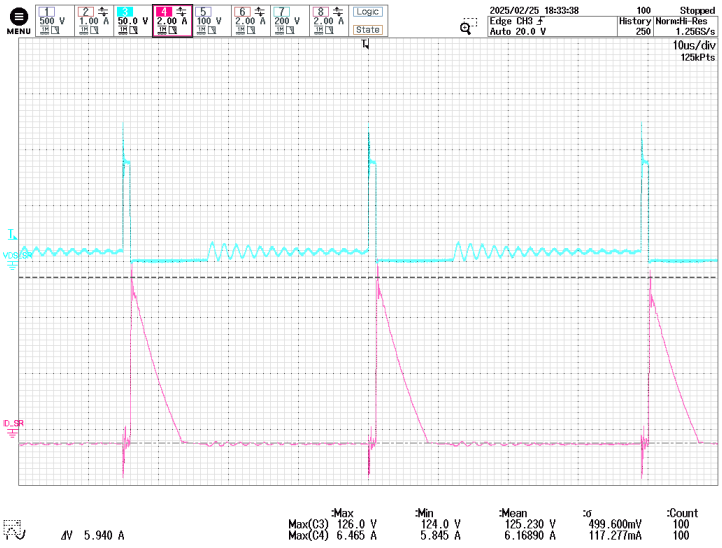


Figure 126 – SR FET Drain Voltage and Current.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH3: $V_{DS(SR\ FET)}$, 50 V / div.
CH4: $I_{D(SR\ FET)}$, 2 A / div.
Time: 10 µs / div.

12.2.2.3 25.5 V Stack Diode Voltage and Current[55]

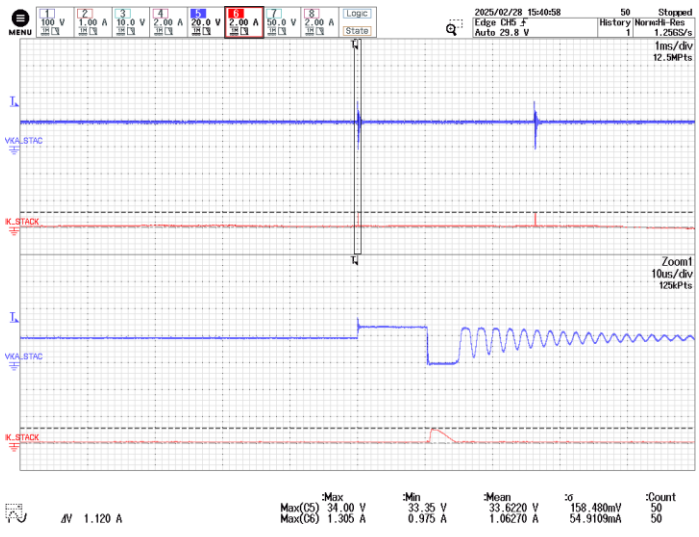


Figure 127 – 25.5 V Stack Diode Voltage and Current.
40 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 20 V / div.
CH6: $I_{K(25.5\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 128 – 25.5 V Stack Diode Voltage and Current.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K(25.5\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

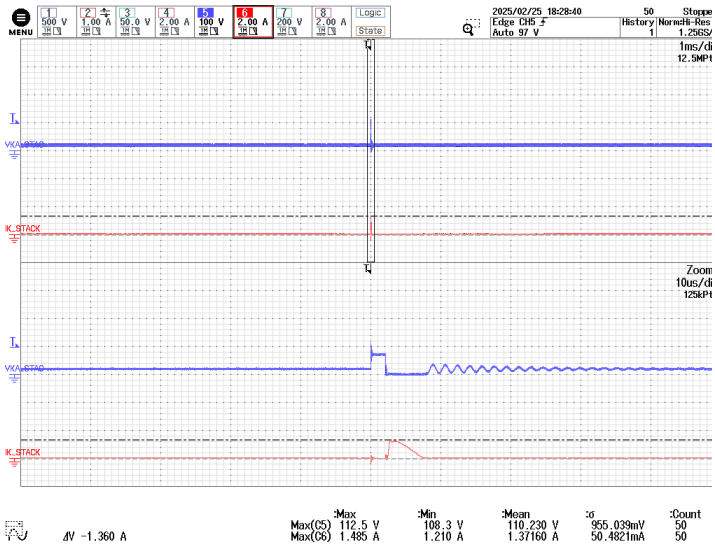


Figure 129 – 25.5 V Stack Diode Voltage and Current.
250 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 20 V / div.
CH6: $I_{K(25.5\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

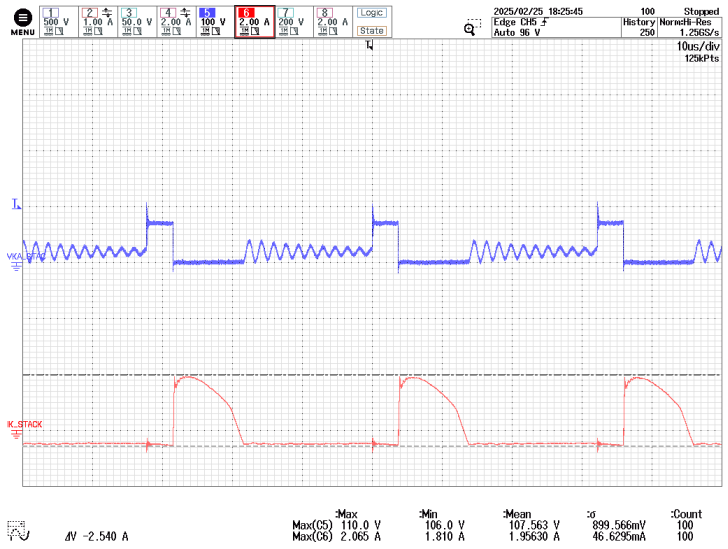


Figure 130 – 25.5 V Stack Diode Voltage and Current.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K(25.5\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

[55] The current waveforms were measured using a 300 A_{peak} Rogowski coil.

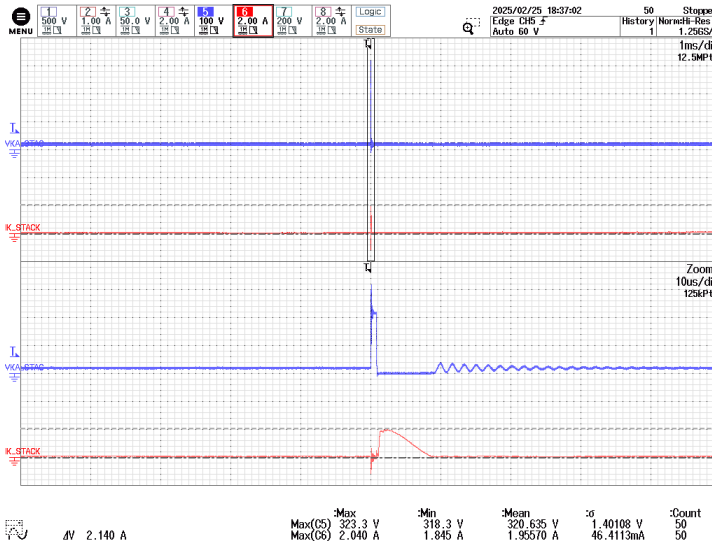


Figure 131 – 25.5 V Stack Diode Voltage and Current.
950 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 20 V / div.
CH6: $I_{K(25.5\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 132 – 25.5 V Stack Diode Voltage and Current.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 100 V / div.
CH6: $I_{K(25.5\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

12.2.2.4 24.7 V Freewheeling Diode Voltage and Current[56]

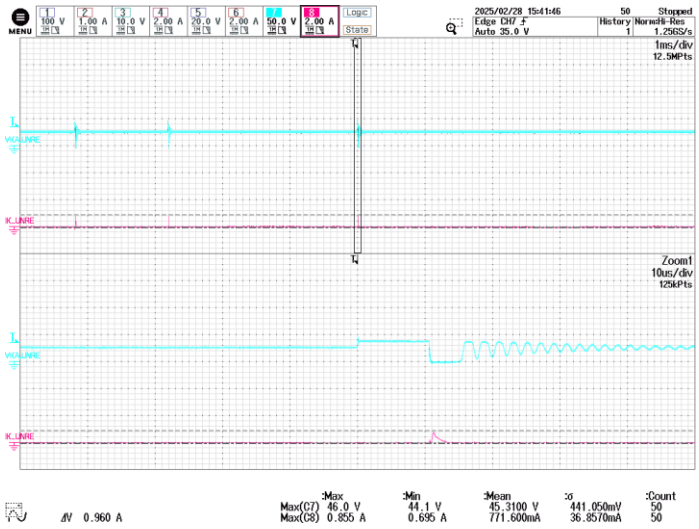


Figure 133 – 24.7 V Freewheeling Diode Voltage and Current.
40 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 50 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

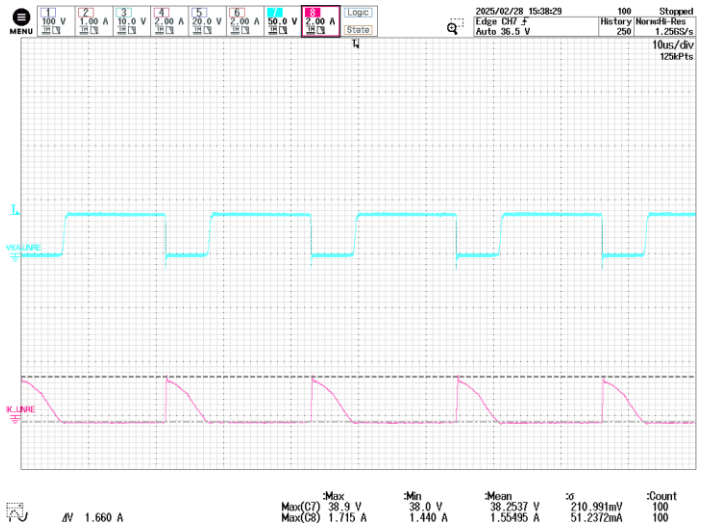


Figure 134 – 24.7 V Freewheeling Diode Voltage and Current.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

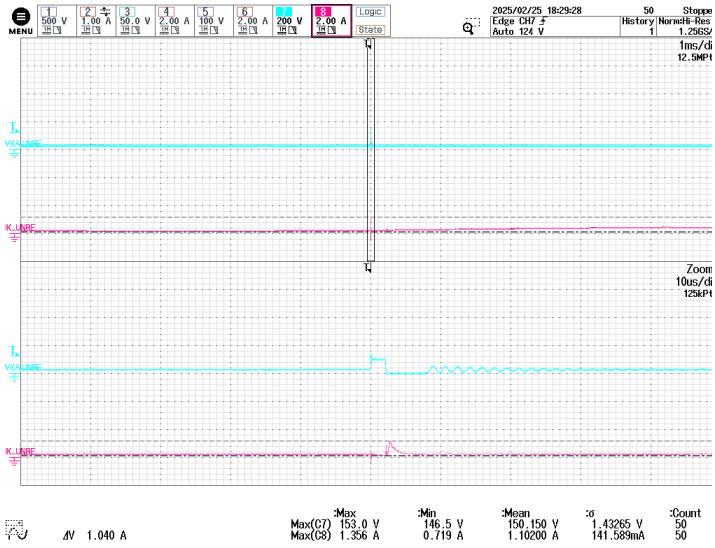


Figure 135 – 24.7 V Freewheeling Diode Voltage and Current.
250 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 50 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

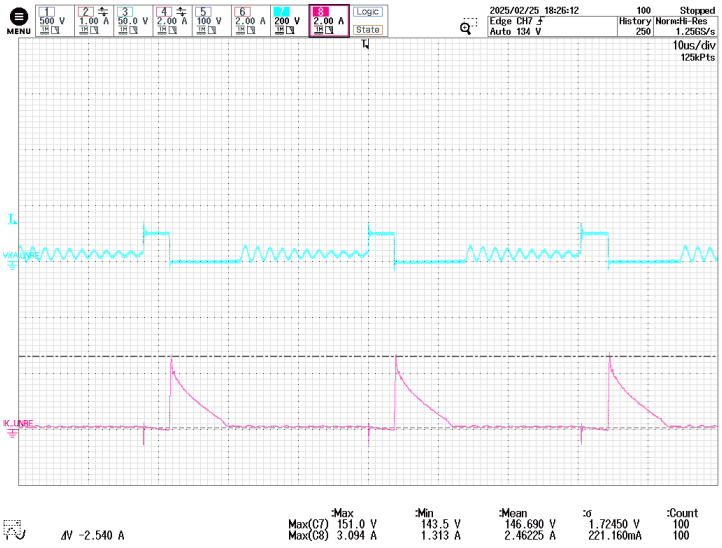


Figure 136 – 24.7 V Freewheeling Diode Voltage and Current.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

[56] The current waveforms were measured using a 120 A_{peak} Rogowski coil.

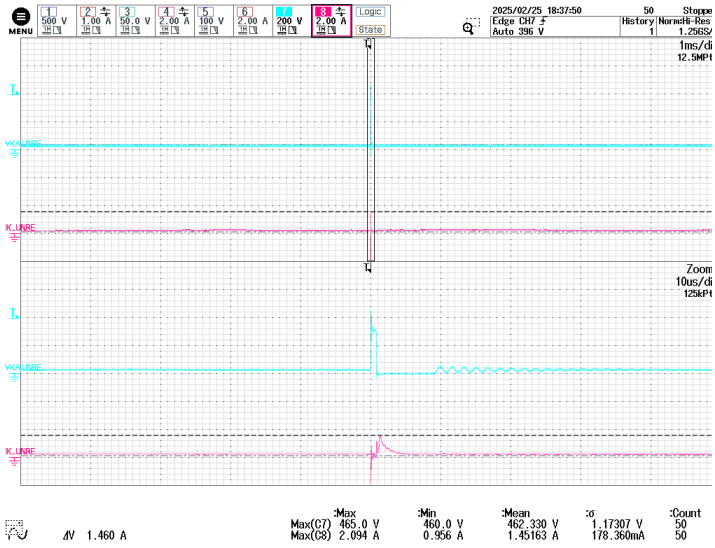


Figure 137 – 24.7 V Freewheeling Diode Voltage and Current.
950 VDC, 25.5 V / No Load, 24.7 V / No Load,
85 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 50 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 1 ms / div. (10 µs / div. Zoom)

Figure 138 – 24.7 V Freewheeling Diode Voltage and Current.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
85 °C Ambient.
CH7: $V_{KA(24.7\ V\ Diode)}$, 200 V / div.
CH8: $I_{K(24.7\ V\ Diode)}$, 2 A / div.
Time: 10 µs / div.

12.3 Short-Circuit Response at 85 ºC Ambient

The unit was tested by applying an output short-circuit at the 25.5 V output during normal working conditions and then removing the short-circuit to determine whether the unit would recover and operate normally. During a short-circuit, the expected response is for the unit to enter auto-restart (AR) mode and attempt to recover every 1.7 to 2.11 seconds. The test is done at full load with constant resistance load for both outputs.

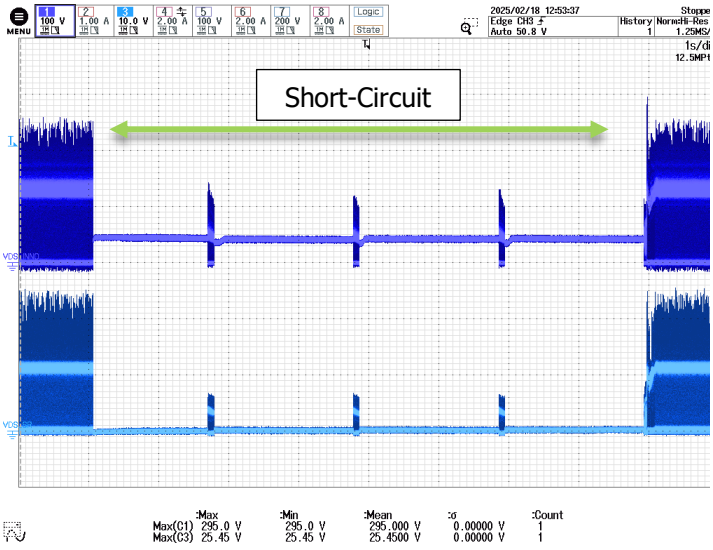


Figure 139 – INN3947FQ and SR FET Drain Voltage
40 VDC, 25.5 V / 91 Ω, 24.7 V / 102 Ω,
25.5 V Shorted, 85 °C Ambient.
CH1: $V_{DS(INNO)}$, 100 V / div.
CH3: $V_{DS(SR)}$, 10 V / div.
Time: 1 s / div.

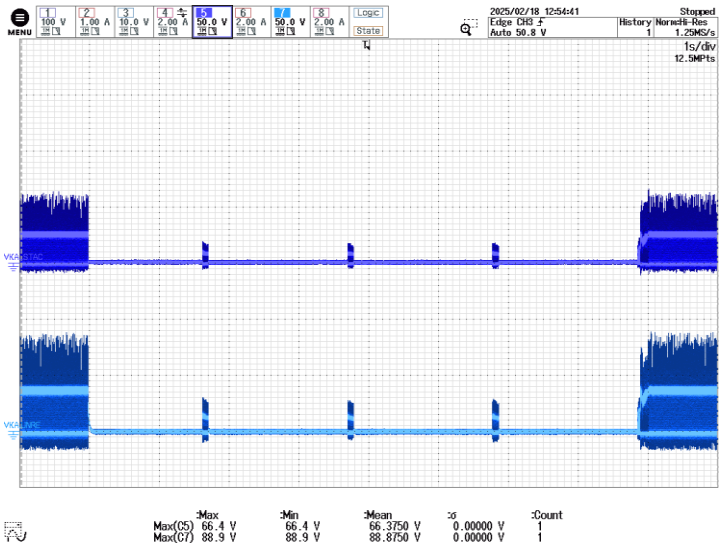


Figure 140 – 25.5 V Stack Diode and 24.7 V Freewheeling Diode Cathode to Anode Voltage
40 VDC, 25.5 V / 91 Ω, 24.7 V / 102 Ω,
25.5 V Shorted, 85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 50 V / div.
CH7: $V_{KA(24.7\ V\ Diode)}$, 50 V / div.
Time: 1 s / div.

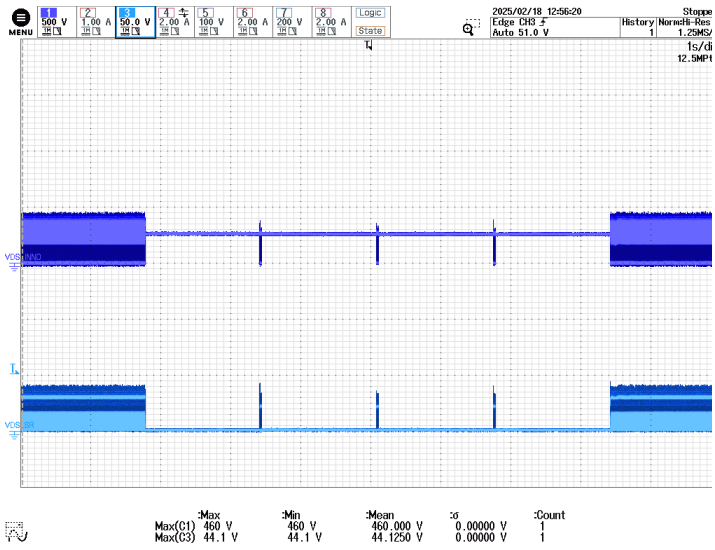


Figure 141 – INN3947FQ and SR FET Drain Voltage
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω,
25.5 V Shorted, 85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH3: $V_{DS(SR)}$, 50 V / div.
Time: 1 s / div.

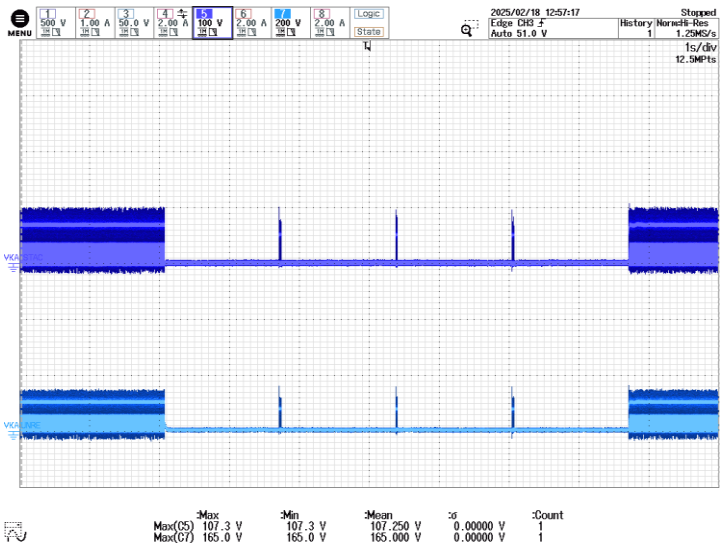


Figure 142 – 25.5 V Stack Diode and 24.7 V Freewheeling Diode Cathode to Anode Voltage
250 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω,
25.5 V Shorted, 85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 100 V / div.
CH7: $V_{KA(24.7\ V\ Diode)}$, 200 V / div.
Time: 1 s / div.

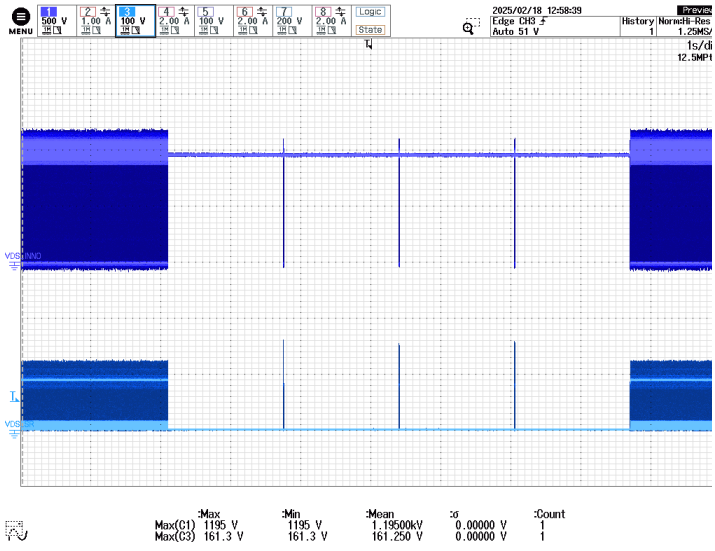


Figure 143 – INN3947FQ and SR FET Drain Voltage
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω,
25.5 V Shorted, 85 °C Ambient.
CH1: $V_{DS(INNO)}$, 500 V / div.
CH3: $V_{DS(SR)}$, 50 V / div.
Time: 1 s / div.

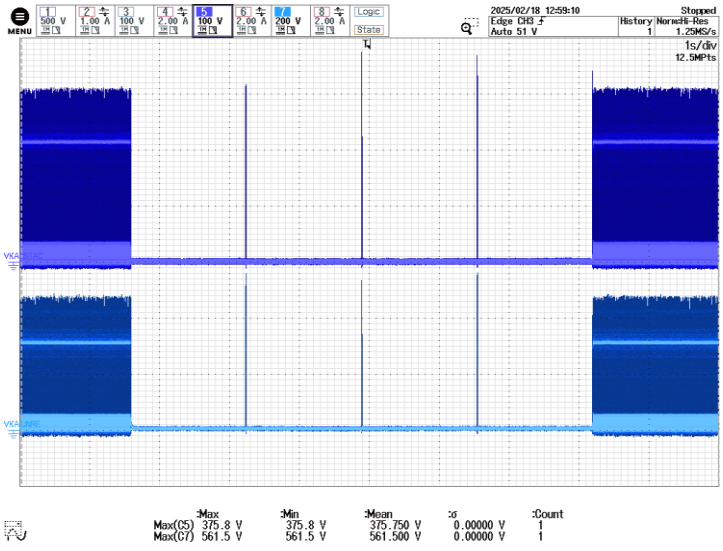


Figure 144 – 25.5 V Stack Diode and 24.7 V Freewheeling Diode Cathode to Anode Voltage
950 VDC, 25.5 V / 47 Ω, 24.7 V / 102 Ω,
25.5 V Shorted, 85 °C Ambient.
CH5: $V_{KA(25.5\ V\ Diode)}$, 100 V / div.
CH7: $V_{KA(24.7\ V\ Diode)}$, 200 V / div.
Time: 1 s / div.

12.4 Load Transient Response at 85 °C Ambient

The load transient response describes the response characteristic of the unit under test to sudden load changes. Output voltage waveforms were captured with switching load transient from minimum to maximum and back to minimum. The time duration for the load at each state was to 100 ms with a slew rate of 100 mA / µs.

Test Conditions (0.1 A / µs Slew Rate, 200 ms Period, Min.-Typ.-Min.)			**Output Overshoot and Undershoot Results**			
Input	**25.5 V Output**	**24.7 V Output**	**25.5 V Output**		**24.7 V Output**	
V_{IN} (V)	**I_{OUT} (mA)**	**I_{OUT} (mA)**	**$mV_{OVERSHOOT}$**	**$mV_{UNDERSHOOT}$**	**$mV_{OVERSHOOT}$**	**$mV_{UNDERSHOOT}$**
40	55 mA – 157 mA – 55 mA	242 mA	219	-256	380	-345
	157 mA	73 mA – 242 mA – 73 mA	246	-276	590	-675
250	55 mA – 550 mA – 55 mA	242 mA	191	-290	990	-1325
	550 mA	73 mA – 242 mA – 73 mA	149	-123	500	-510
950	55 mA – 550 mA – 55 mA	242 mA	253	-458	1045	-1425
	550 mA	73 mA – 242 mA – 73 mA	180	-244	500	-585

Table 13 – Summary of Load Transient Response at 85 °C Ambient.

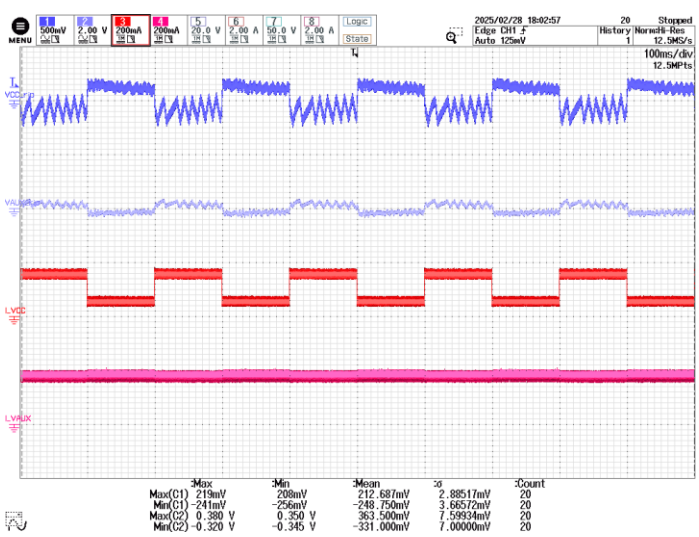


Figure 145 – Output Voltage and Current.
40 VDC, 25.5 V / 55 mA - 157 mA – 55 mA Transient Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 500 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 2 V / div.
CH3: $I_{OUT(25.5\ V)}$, 200 mA / div.
CH4: $I_{OUT(24.7\ V)}$, 200 mA / div.
Time: 100 ms / div.

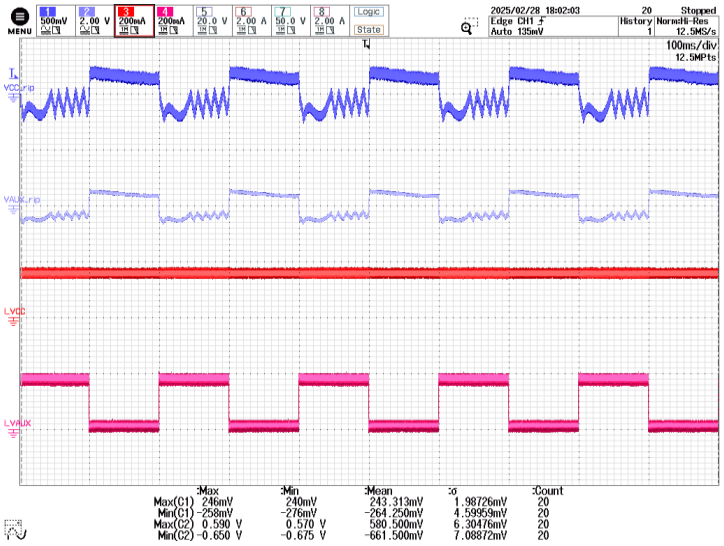


Figure 146 – Output Voltage and Current.
40 VDC, 24.7 V / 73 mA – 242 mA – 73 mA Transient Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 500 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 2 V / div.
CH3: $I_{OUT(25.5\ V)}$, 200 mA / div.
CH4: $I_{OUT(24.7\ V)}$, 200 mA / div.
Time: 100 ms / div.

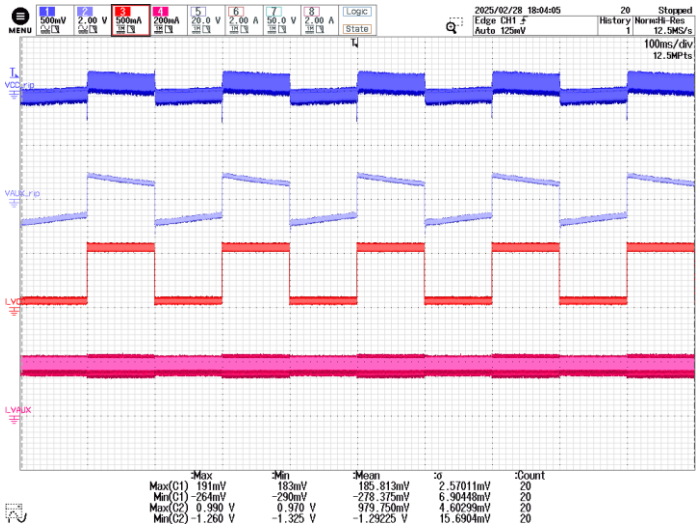


Figure 147 – Output Voltage and Current.
250 VDC, 25.5 V / 55 mA - 550 mA – 55 mA Transient Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 500 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 2 V / div.
CH3: $I_{OUT(25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT(24.7\ V)}$, 200 mA / div.
Time: 100 ms / div.

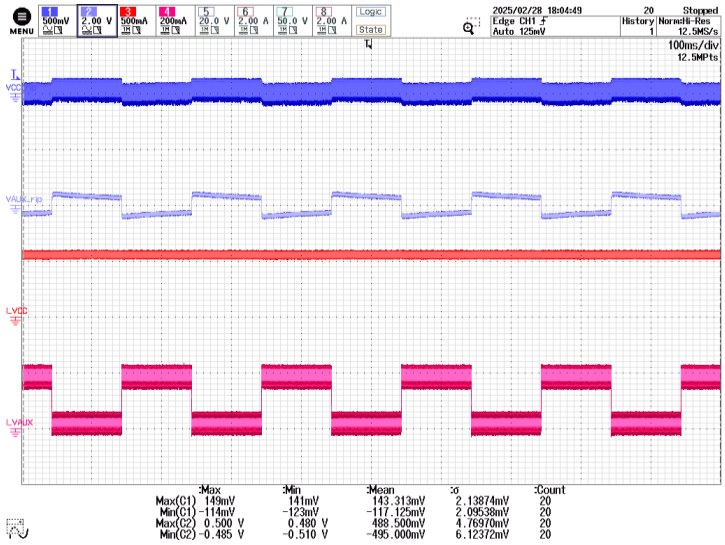


Figure 148 – Output Voltage and Current.
250 VDC, 24.7 V / 73 mA – 242 mA – 73 mA Transient Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 500 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 2 V / div.
CH3: $I_{OUT(25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT(24.7\ V)}$, 200 mA / div.
Time: 100 ms / div.

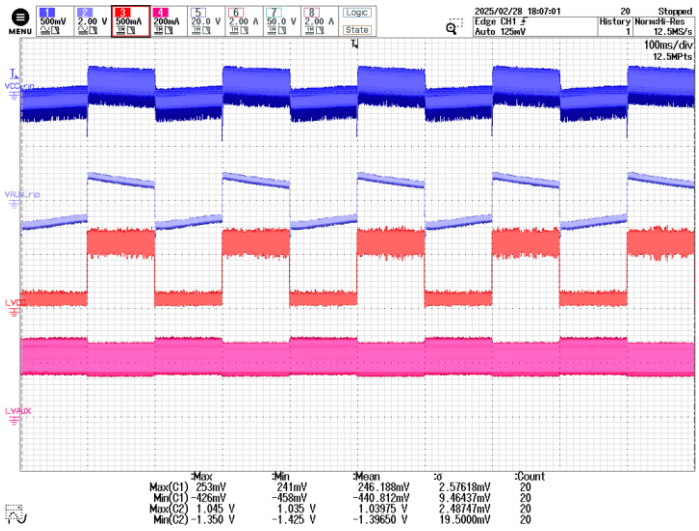


Figure 149 – Output Voltage and Current.
950 VDC, 25.5 V / 55 mA - 550 mA – 55 mA Transient Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 500 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 2 V / div.
CH3: $I_{OUT(25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT(24.7\ V)}$, 200 mA / div.
Time: 100 ms / div.

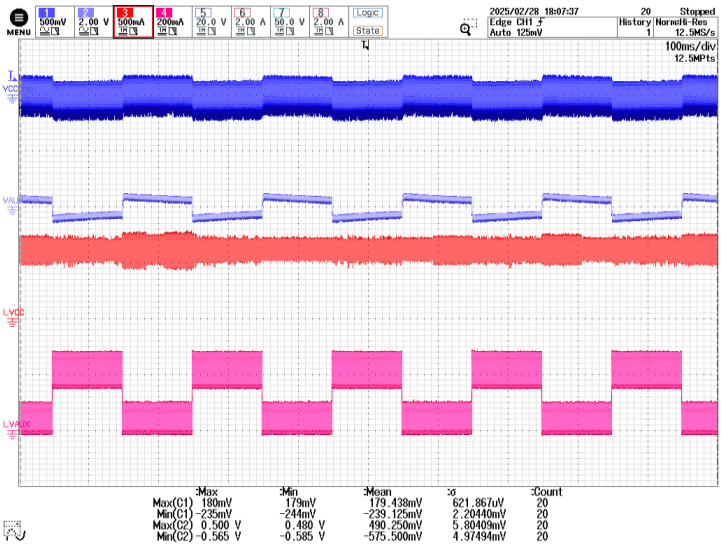


Figure 150 – Output Voltage and Current.
950 VDC, 24.7 V / 73 mA – 242 mA – 73 mA Transient Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 500 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 2 V / div.
CH3: $I_{OUT(25.5\ V)}$, 500 mA / div.
CH4: $I_{OUT(24.7\ V)}$, 200 mA / div.
Time: 100 ms / div.

12.5 Output Voltage Ripple Measurements

12.5.1 Output Voltage Ripple Measurement Technique

A modified oscilloscope test probe was used for output voltage ripple measurements to eliminate spurious signals due to pick-up. Figure 126 and Figure 127 below provide details of the probe modification.

A 1 μF / 50 V ceramic capacitor parallel to the probe tip of a CT2708 probe adapter and GND terminal. A twisted pair of wires, kept as short as possible, were then soldered directly between the probe and the output terminals of the unit under test.

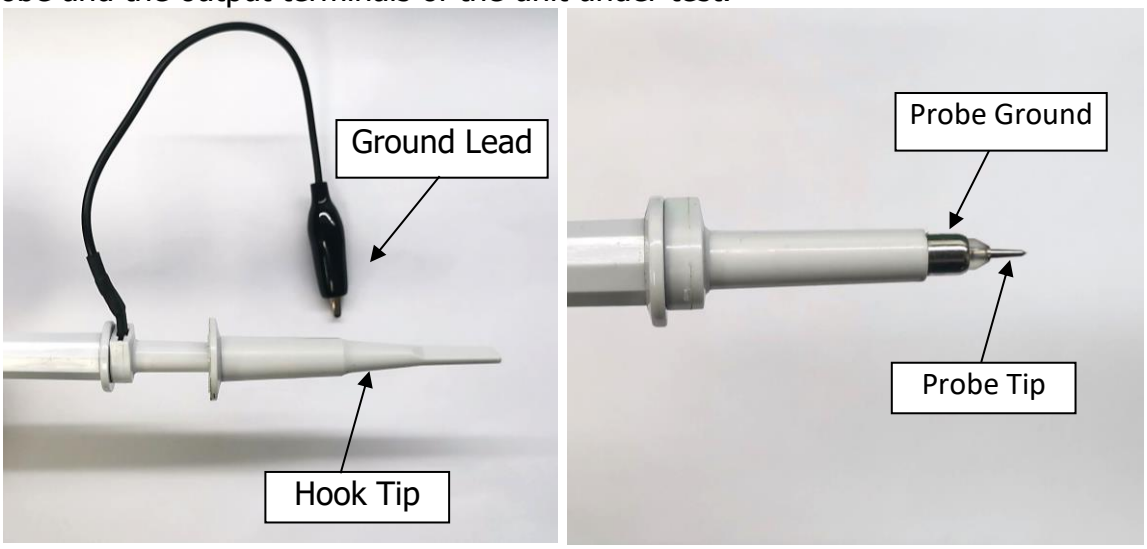


Figure 151 – Oscilloscope Probe Prepared for Ripple Measurement. (Hook Tip and Ground Lead Removed.)

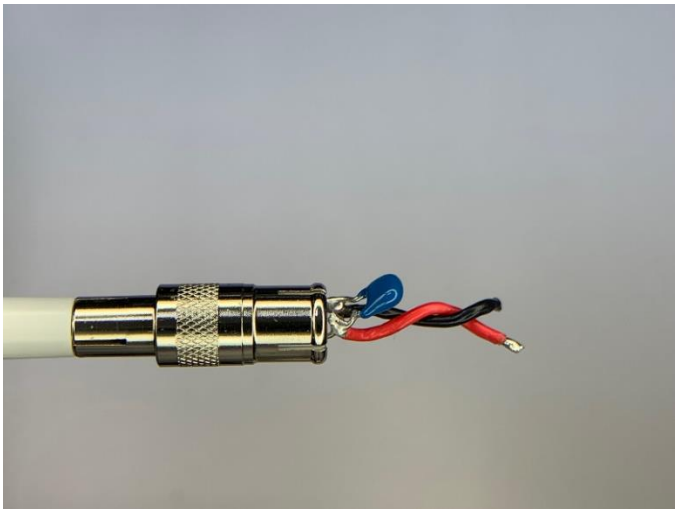


Figure 152 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with wires for ripple measurement, and a parallel decoupling capacitor added.)

12.5.2 Output Voltage Ripple Waveforms

The output voltage ripple waveform was recorded at the output terminals using the ripple measurement probe with decoupling capacitor.

12.5.2.1 Output Voltage Ripple at 85 °C Ambient[57]

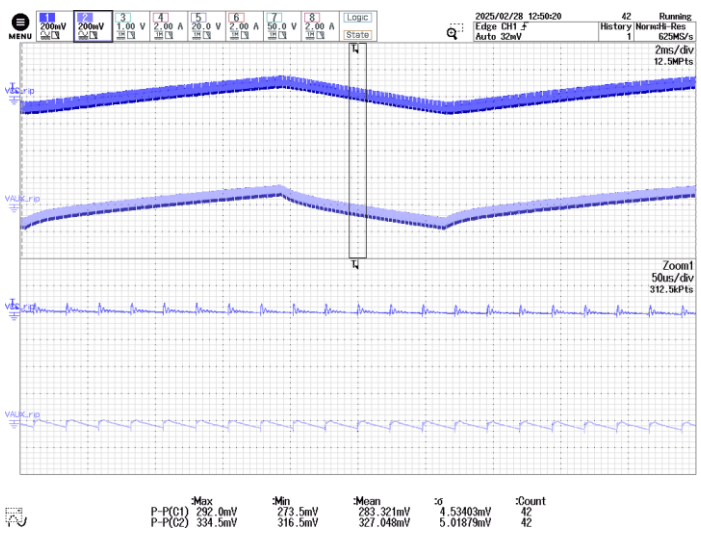


Figure 153 – Output Voltage Ripple.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

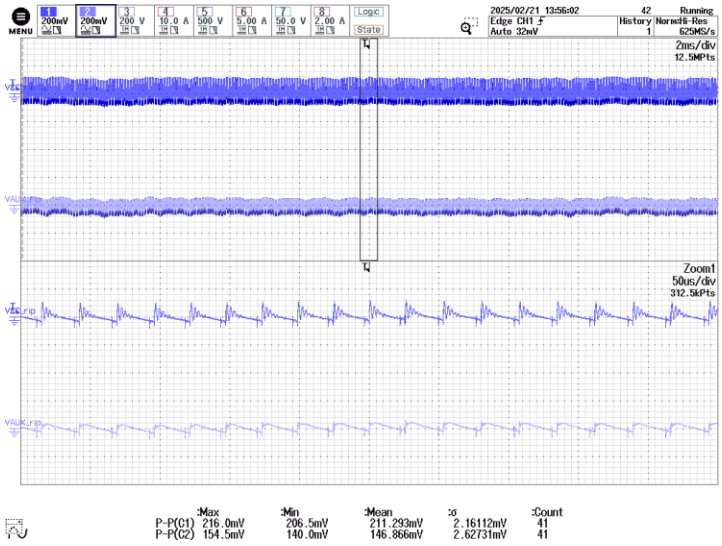


Figure 154 – Output Voltage Ripple.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

[57] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

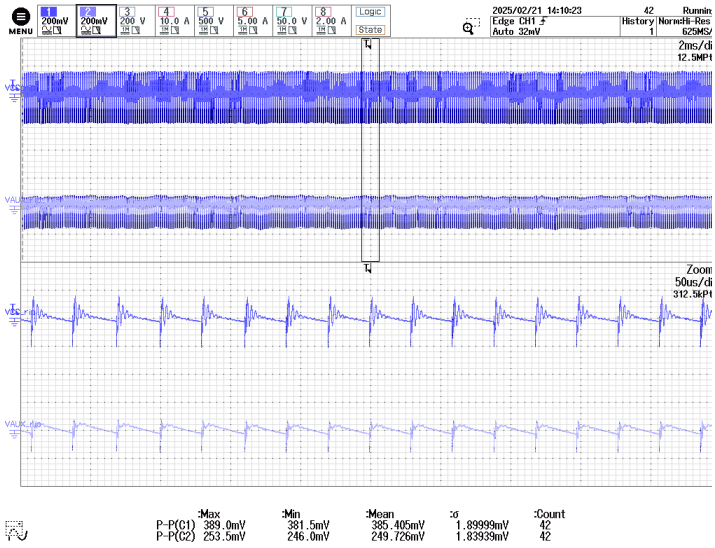


Figure 155 – Output Voltage Ripple.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load, 85 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

12.5.2.2 Output Voltage Ripple at 25 °C Ambient[58]

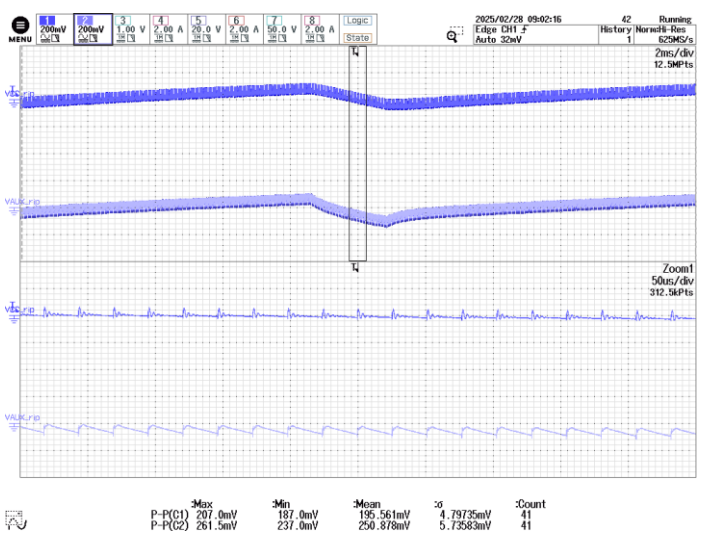


Figure 156 – Output Voltage Ripple.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

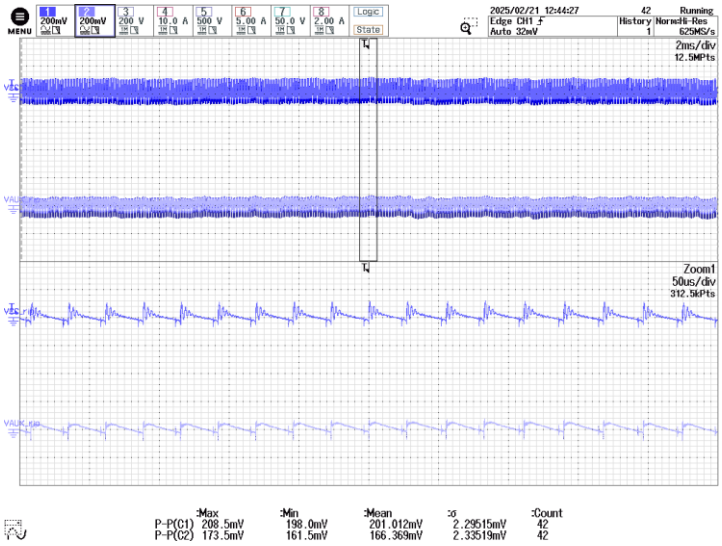


Figure 157 – Output Voltage Ripple.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

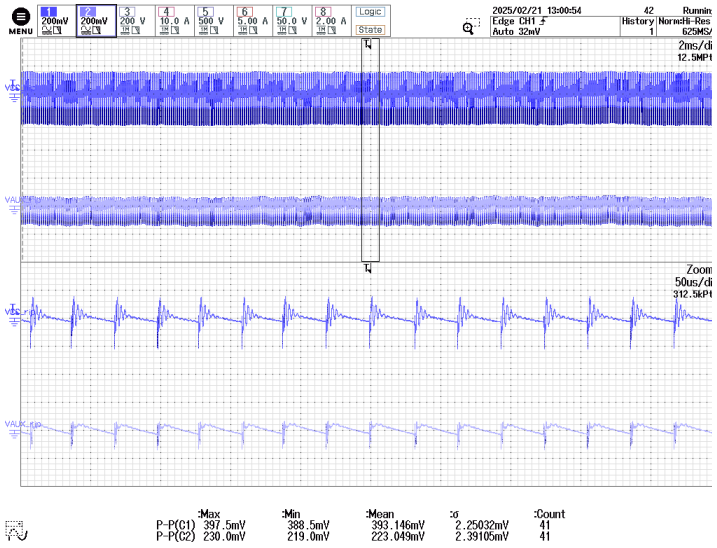


Figure 158 – Output Voltage Ripple.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
25 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

[58] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

12.5.2.3 Output Voltage Ripple at -40 °C Ambient[59]

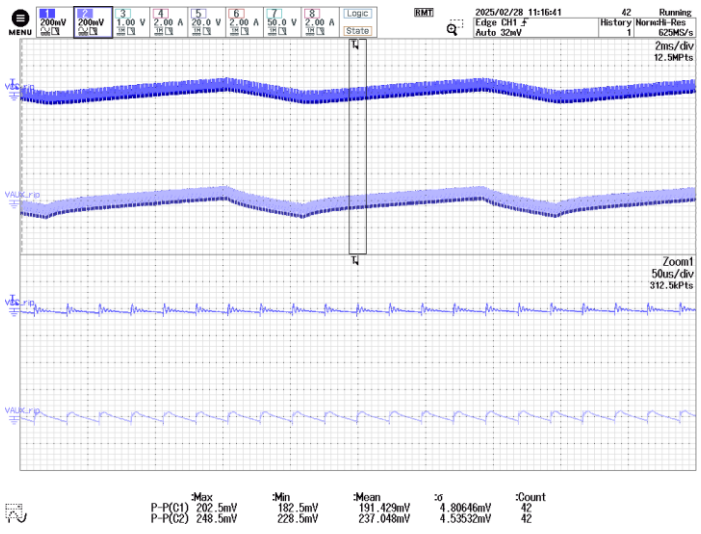


Figure 159 – Output Voltage Ripple.
40 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
-40 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

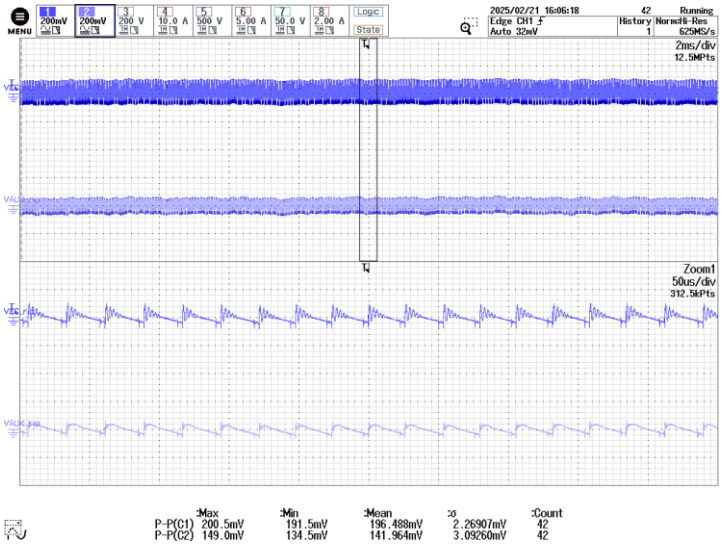


Figure 160 – Output Voltage Ripple.
250 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
-40 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

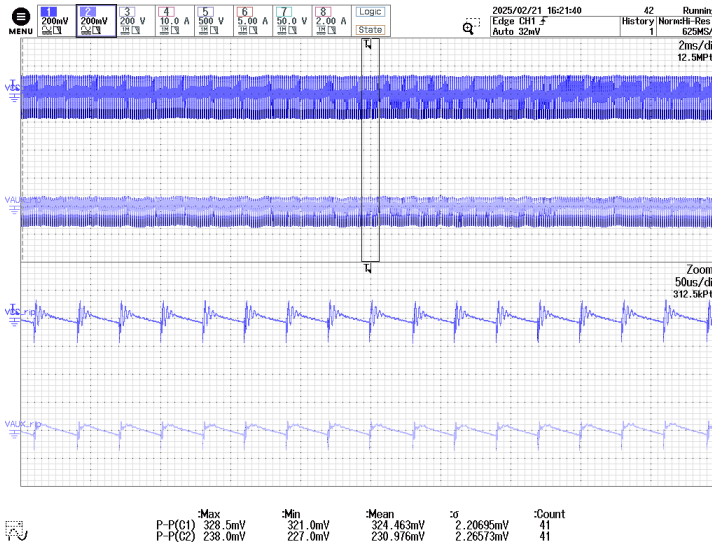


Figure 161 – Output Voltage Ripple.
950 VDC, 25.5 V / Full Load, 24.7 V / Full Load,
-40 °C Ambient.
CH1: $V_{OUT(25.5\ V)}$, 200 mV / div.
CH2: $V_{OUT(24.7\ V)}$, 200 mV / div.
Time: 2 ms / div. (50 µs / div. Zoom).

[59] Peak-to-peak voltage measurement recorded in each oscilloscope capture was the worst-case ripple which included both the low frequency and high frequency switching voltage ripple (top portion of each capture).

12.5.3 Output Voltage Ripple vs. Load

Each line on the graphs represents the output voltage ripple vs. total output power of the unit under test.

12.5.3.1 40 VDC Input

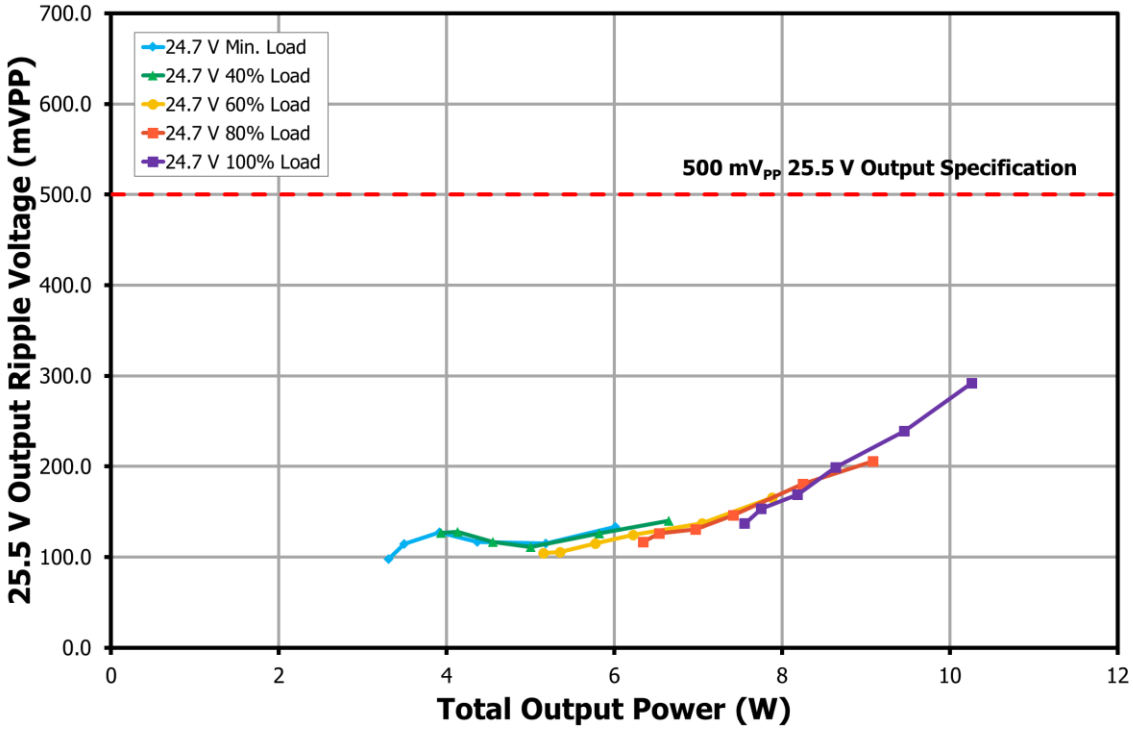


Figure 162 – 25.5 V Output Voltage Ripple vs. Total Output Power at 40 VDC Input and 85 °C Ambient.[60]

[60] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

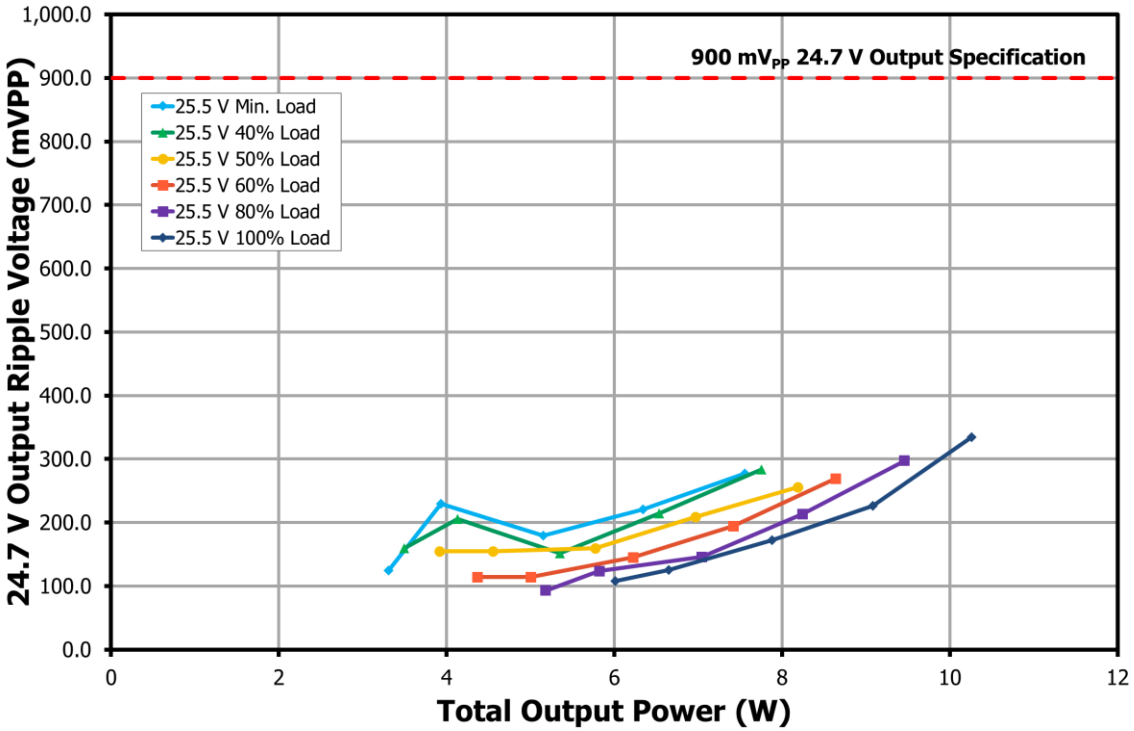


Figure 163 – 24.7 V Output Voltage Ripple vs. Total Output Power at 40 VDC Input and 85 °C Ambient.[61]

[61] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

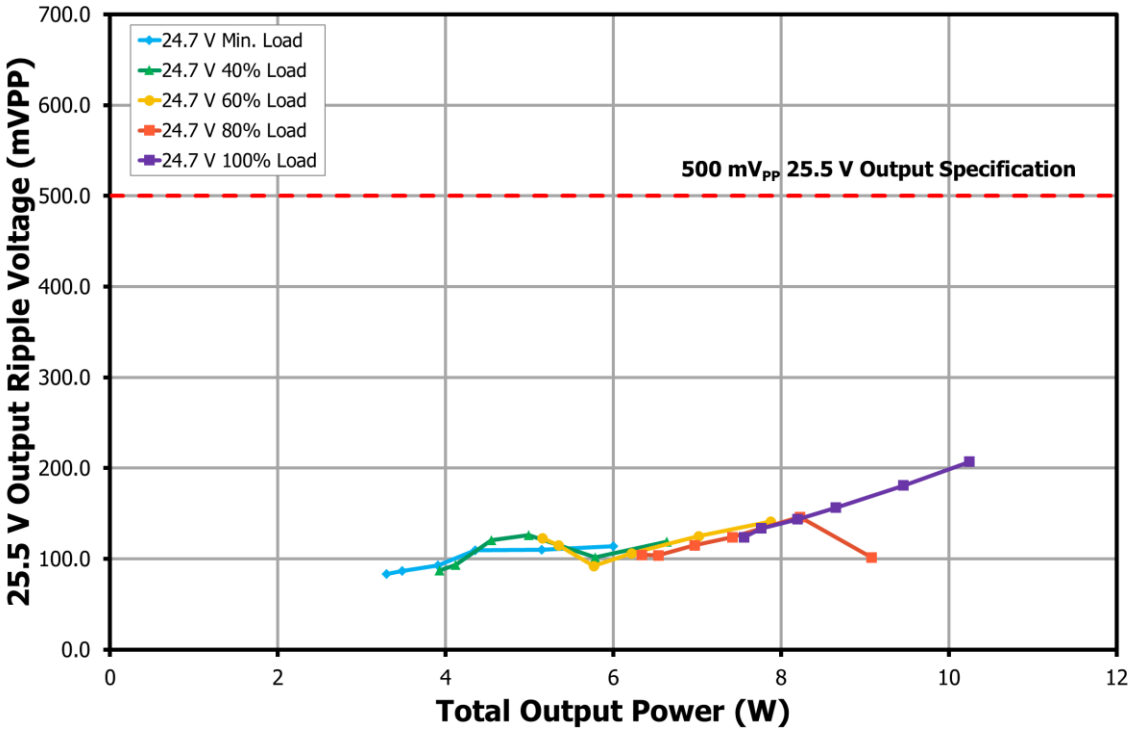


Figure 164 – 25.5 V Output Voltage Ripple vs. Total Output Power at 40 VDC Input and 25 °C Ambient.[62]

[62] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

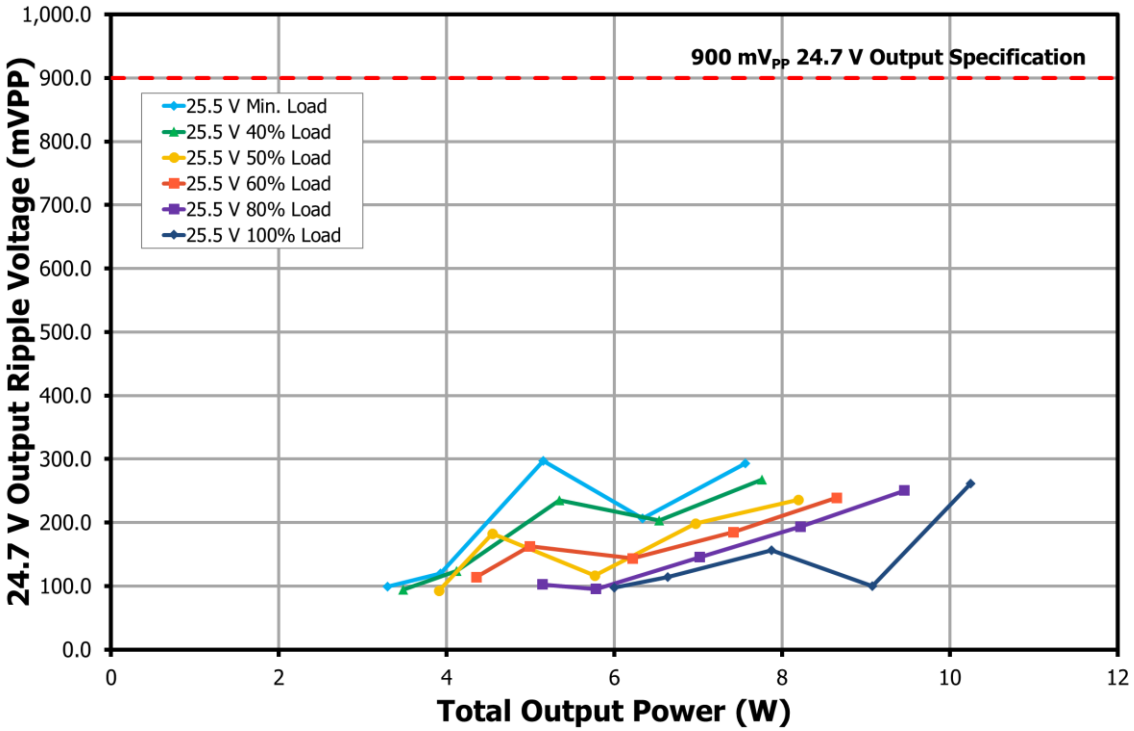


Figure 165 – 24.7 V Output Voltage Ripple vs. Total Output Power at 40 VDC Input and 25 °C Ambient.[63]

[63] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

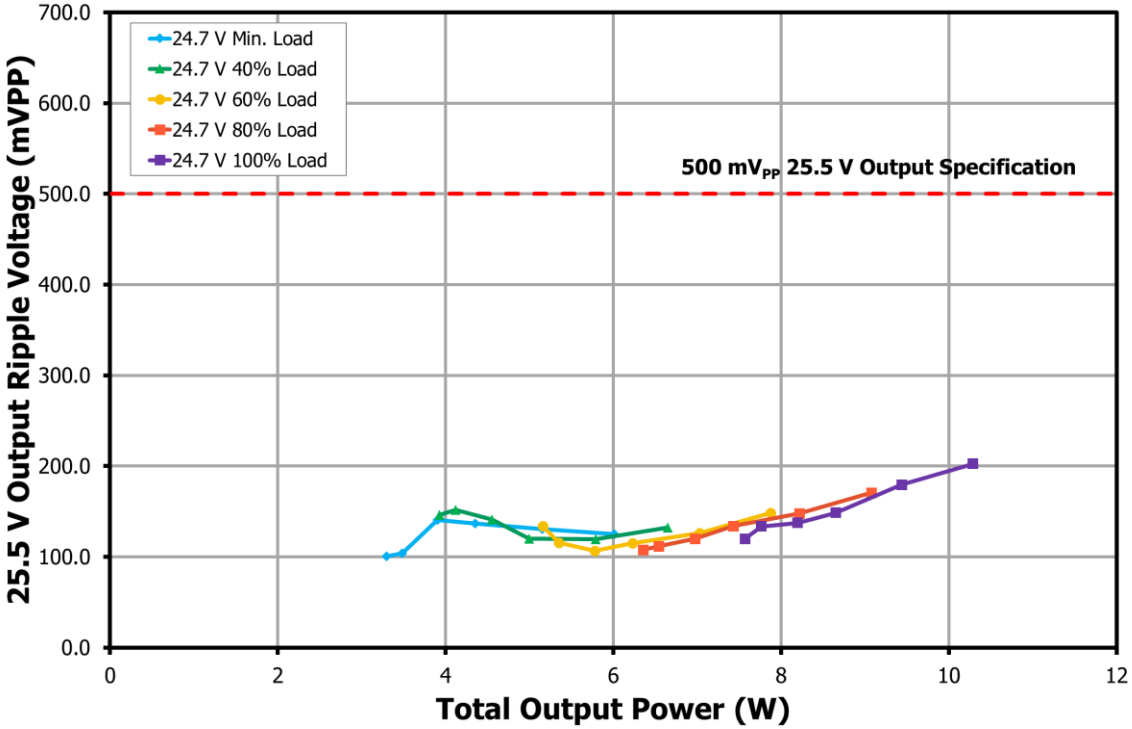


Figure 166 – 25.5 V Output Voltage Ripple vs. Total Output Power at 40 VDC Input and -40 °C Ambient.[64]

[64] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

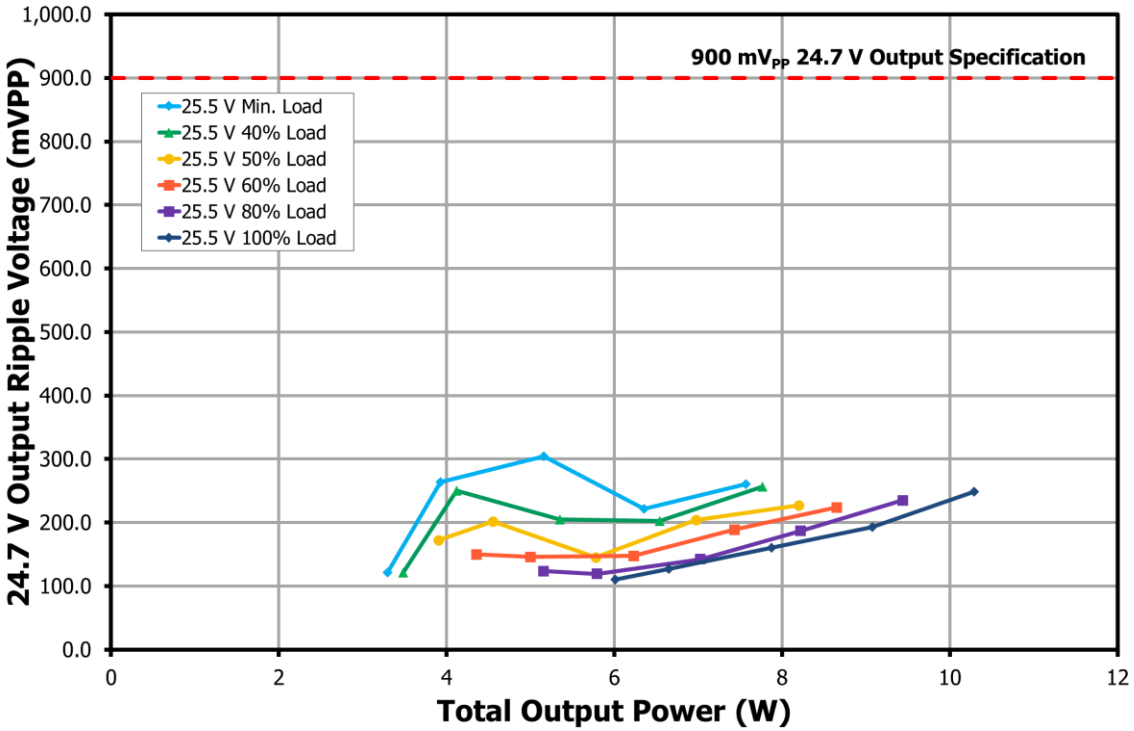


Figure 167 – 24.7 V Output Voltage Ripple vs. Total Output Power at 40 VDC Input and -40 °C Ambient.[65]

[65] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

12.5.3.2 250 VDC Input

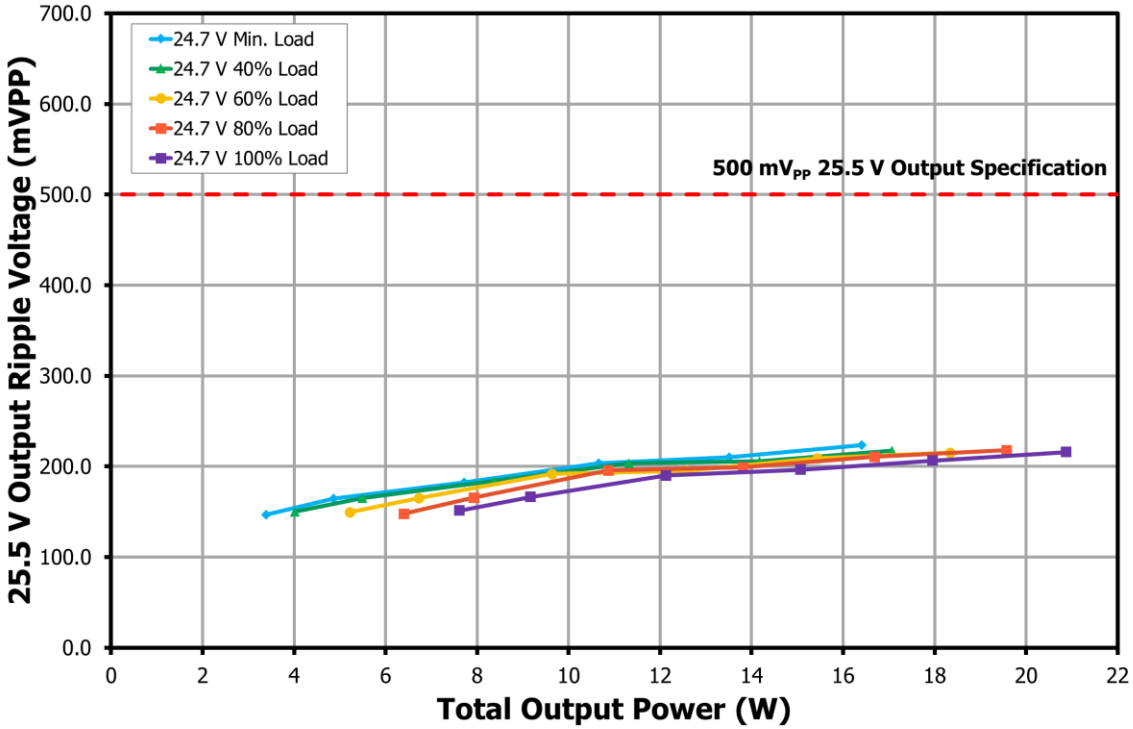


Figure 168 – 25.5 V Output Voltage Ripple vs. Total Output Power at 250 VDC Input and 85 °C Ambient.[66]

[66] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

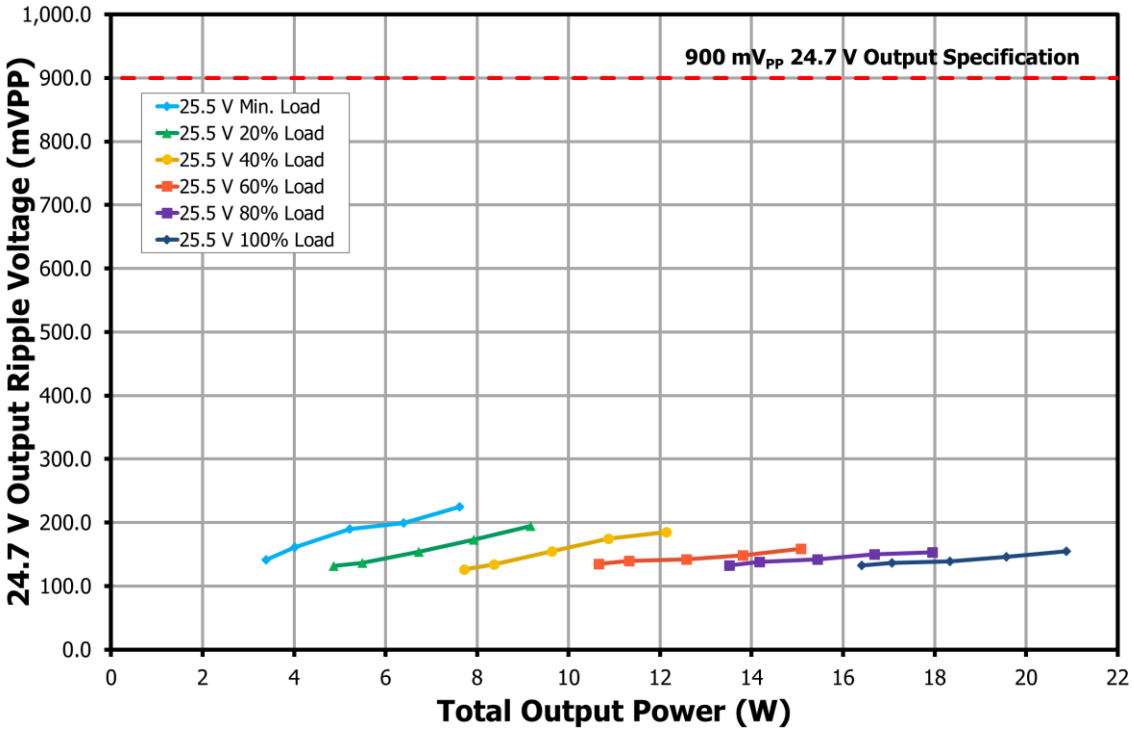


Figure 169 – 24.7 V Output Voltage Ripple vs. Total Output Power at 250 VDC Input and 85 °C Ambient.[67]

[67] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

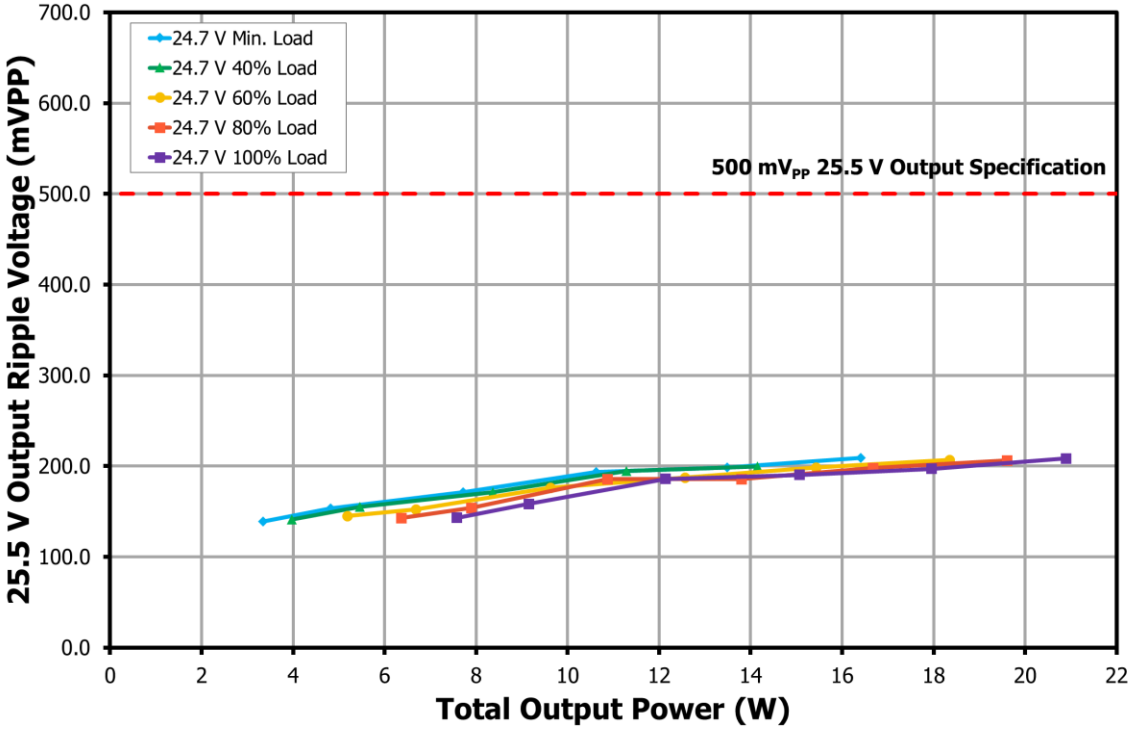


Figure 170– 25.5 V Output Voltage Ripple vs. Total Output Power at 250 VDC Input and 25 °C Ambient.[68]

[68] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

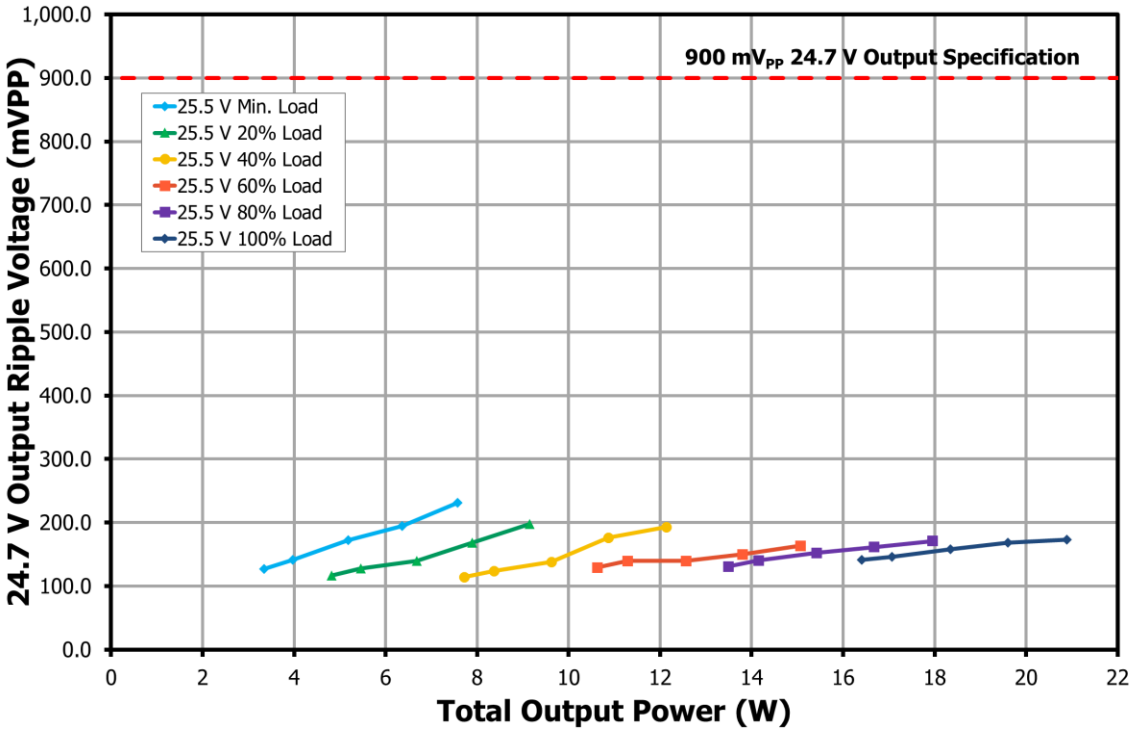


Figure 171– 24.7 V Output Voltage Ripple vs. Total Output Power at 250 VDC Input and 25 °C Ambient.[69]

[69] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

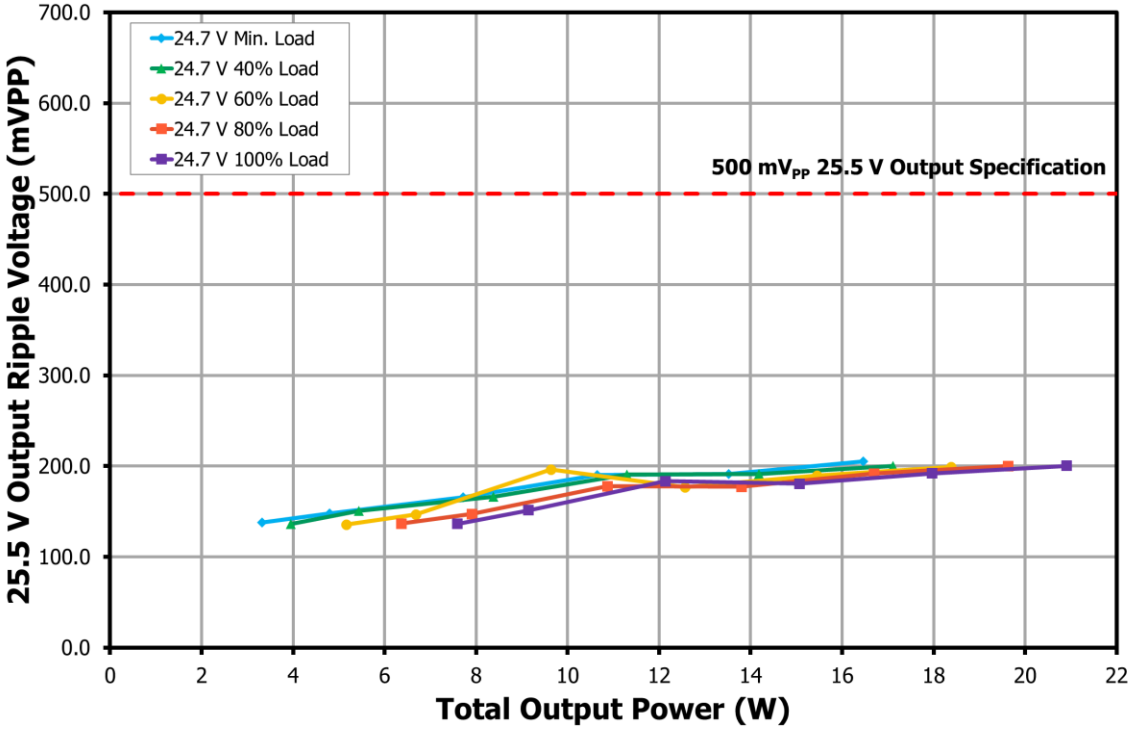


Figure 172 – 25.5 V Output Voltage Ripple vs. Total Output Power at 800 VDC Input and -40 °C Ambient.[70]

[70] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

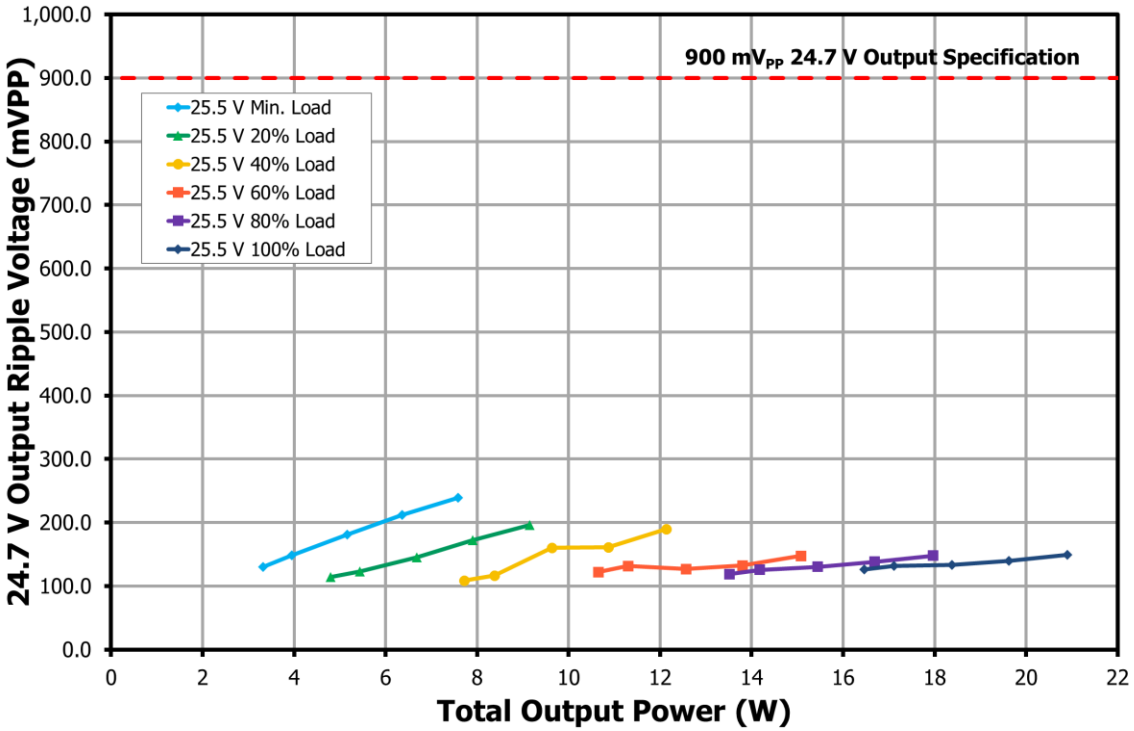


Figure 173 – 24.7 V Output Voltage Ripple vs. Total Output Power at 800 VDC Input and -40 °C Ambient.[71]

[71] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

12.5.3.3 950 VDC Input

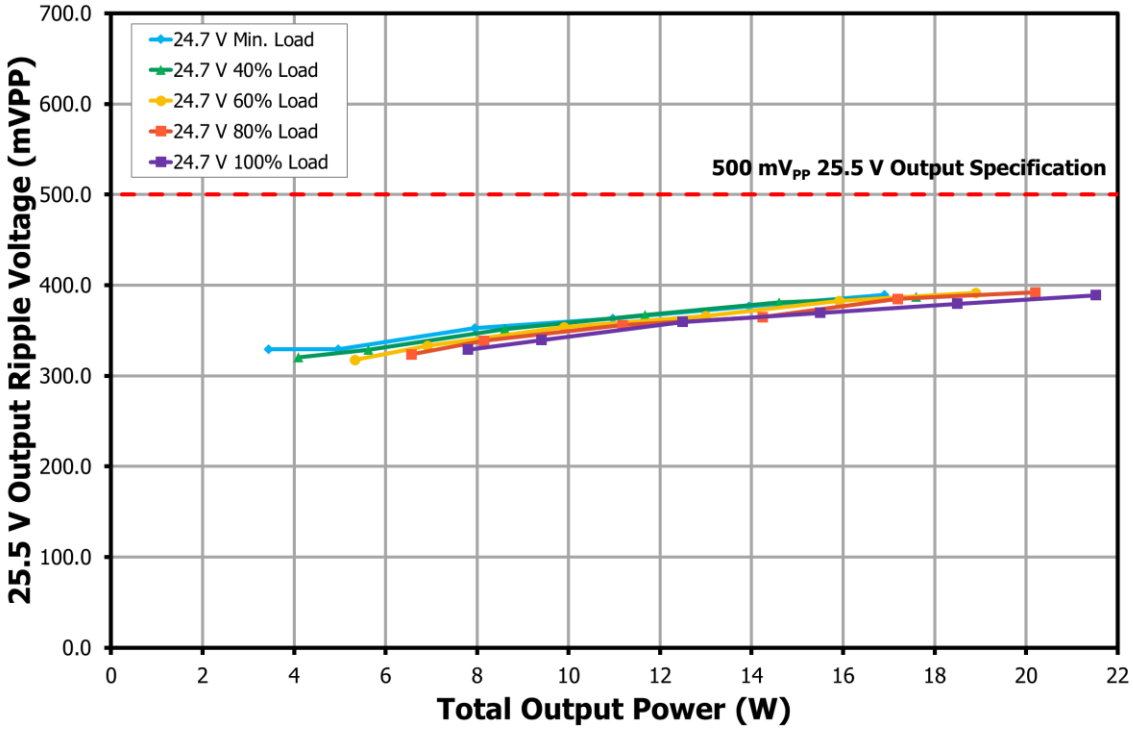


Figure 174 – 25.5 V Output Voltage Ripple vs. Total Output Power at 950 VDC Input and 85 °C Ambient.[72]

[72] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

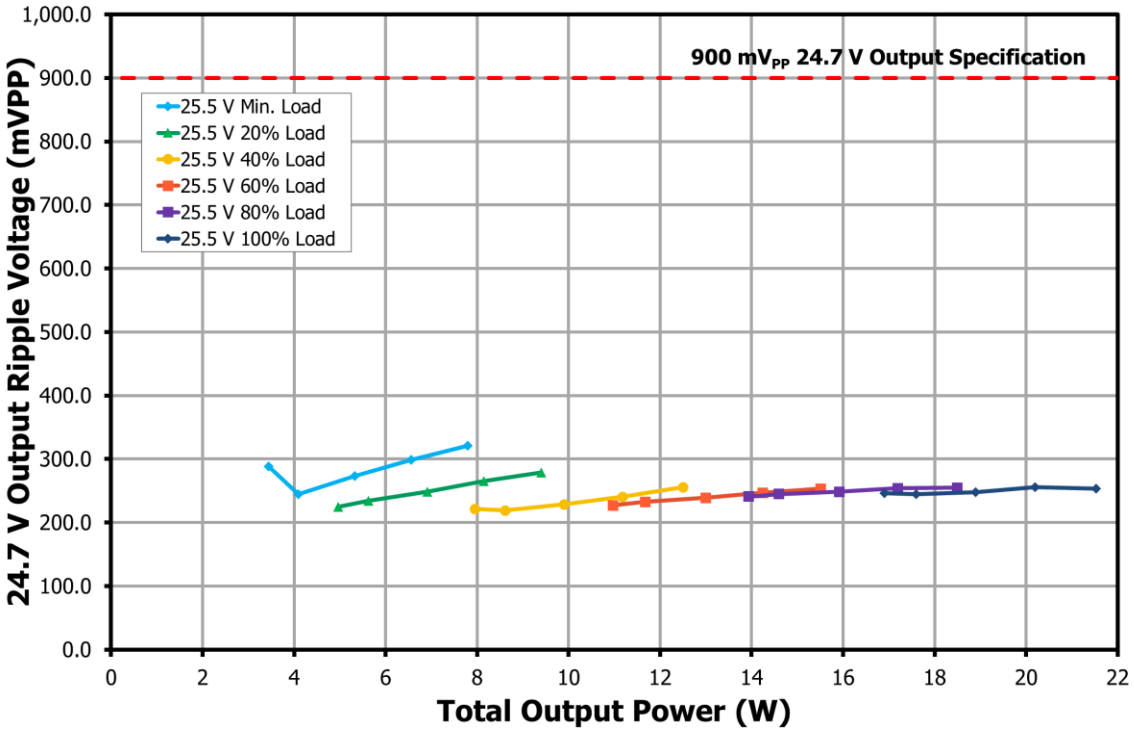


Figure 175 – 24.7 V Output Voltage Ripple vs. Total Output Power at 950 VDC Input and 85 °C Ambient.[73]

[73] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

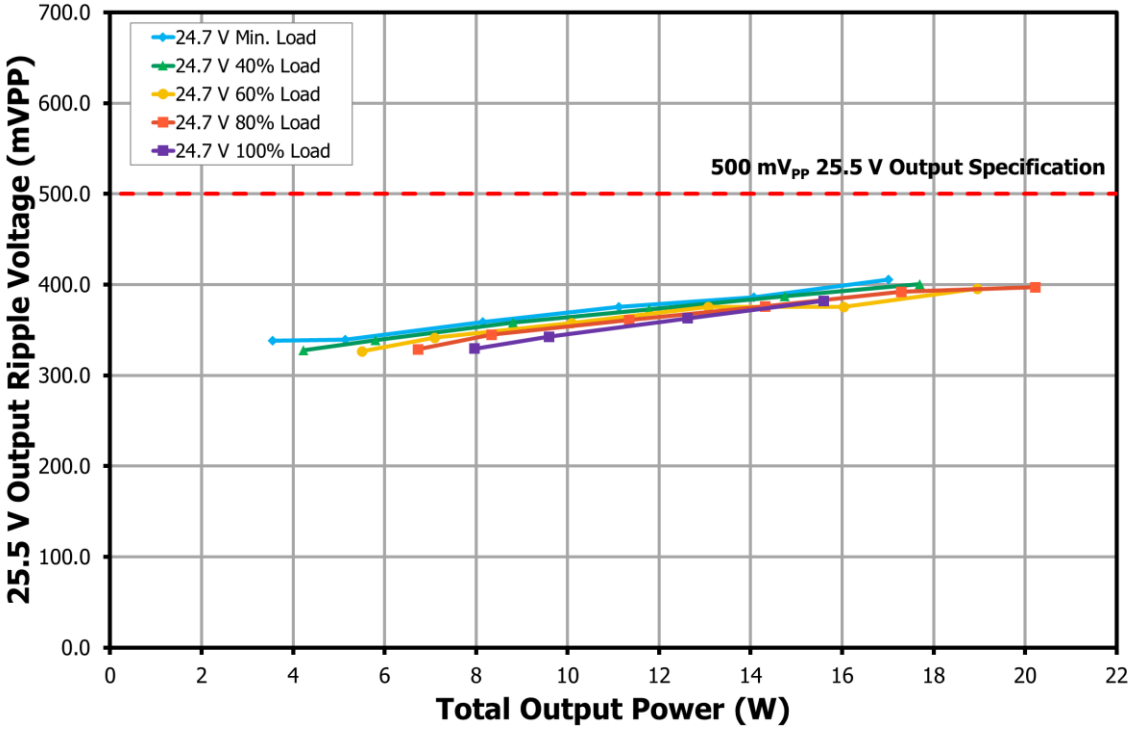


Figure 176– 25.5 V Output Voltage Ripple vs. Total Output Power at 950 VDC Input and 85 °C Ambient.[74]

[74] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

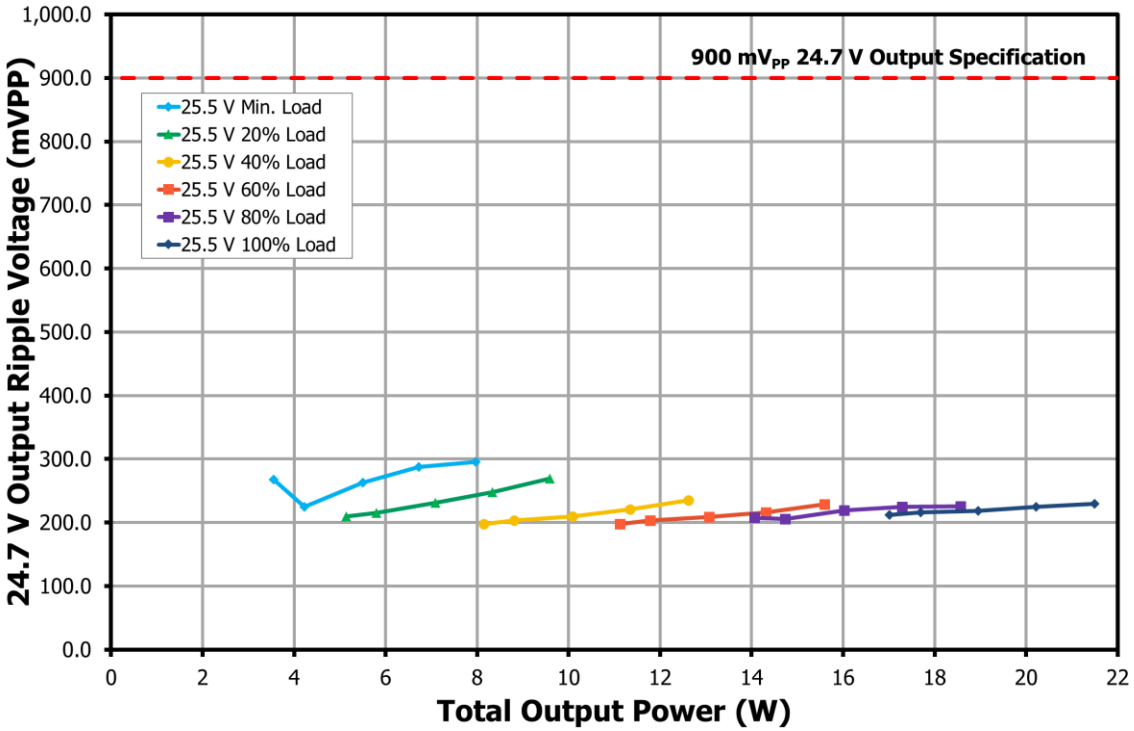


Figure 177– 24.7 V Output Voltage Ripple vs. Total Output Power at 950 VDC Input and 85 °C Ambient.[75]

[75] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

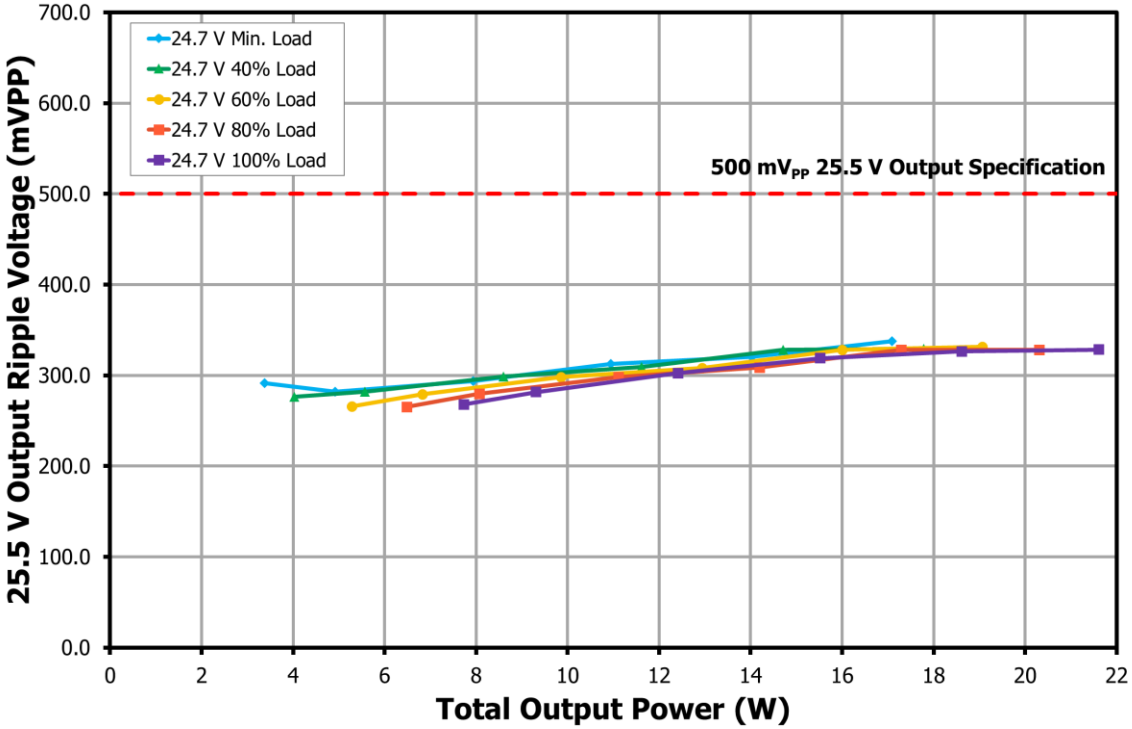


Figure 178 – 25.5 V Output Voltage Ripple vs. Total Output Power at 950 VDC Input and -40 °C Ambient.[76]

[76] Each line represents the 25.5 V output ripple vs. total output power of the unit under test when the 24.7 V output load is maintained at a certain percentage while the 25.5 V output load is increased from its minimum to maximum loading condition.

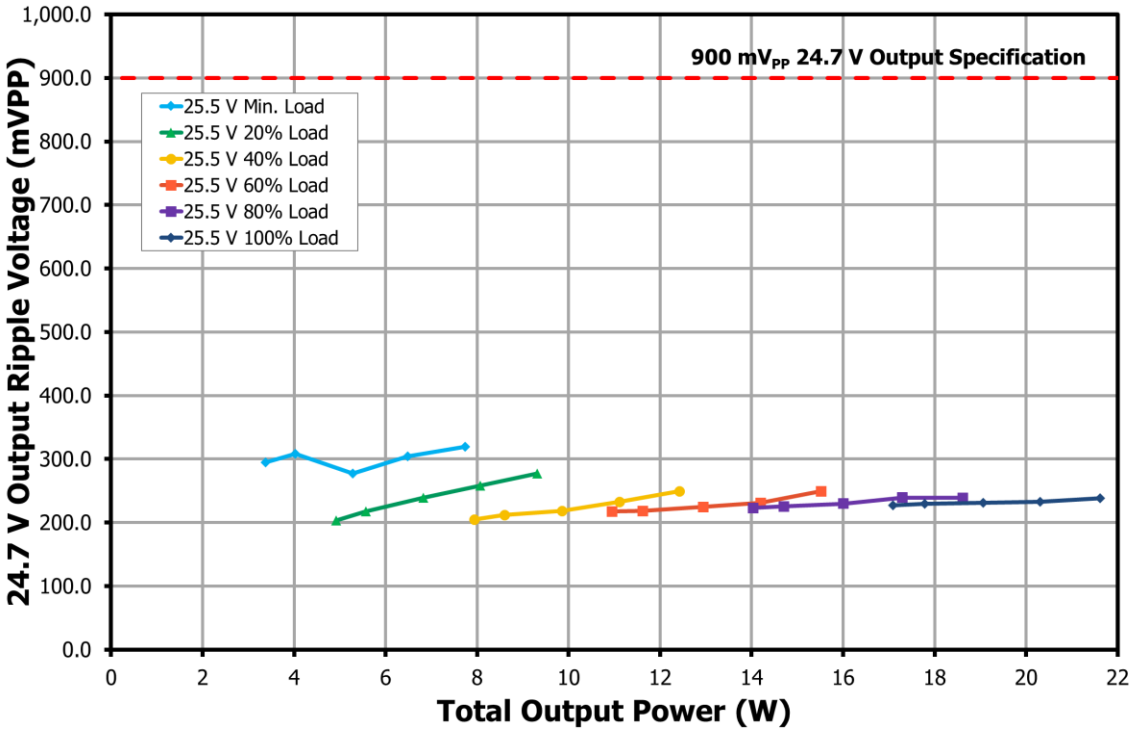


Figure 179 – 24.7 V Output Voltage Ripple vs. Total Output Power at 950 VDC Input and -40 °C Ambient.[77]

[77] Each line represents the 24.70 V output ripple vs. total output power of the unit under test when the 25.5 V output load is maintained at a certain percentage while the 24.7 V output load is increased from its minimum to maximum loading condition.

13 Output Overload

13.1 25.5 V Output Overload Capability

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C and allowed to stabilize for 30 minutes before turning on the unit under test. The unit was also allowed to stabilize for 20 minutes after each change in input voltage. Output voltage and output current measurements were taken 60 seconds after every change in loading condition.

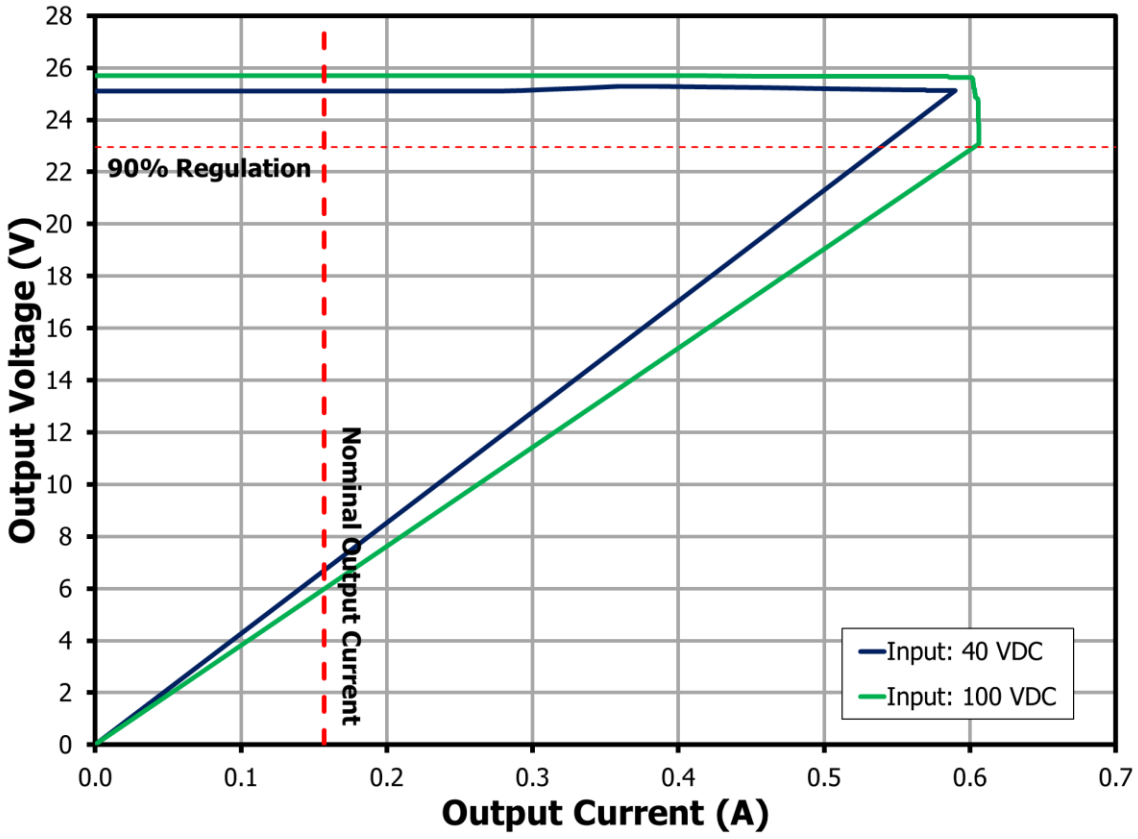


Figure 180 – 25.5 V Output Overload Curve at 40 VDC Input and 100 VDC Input.

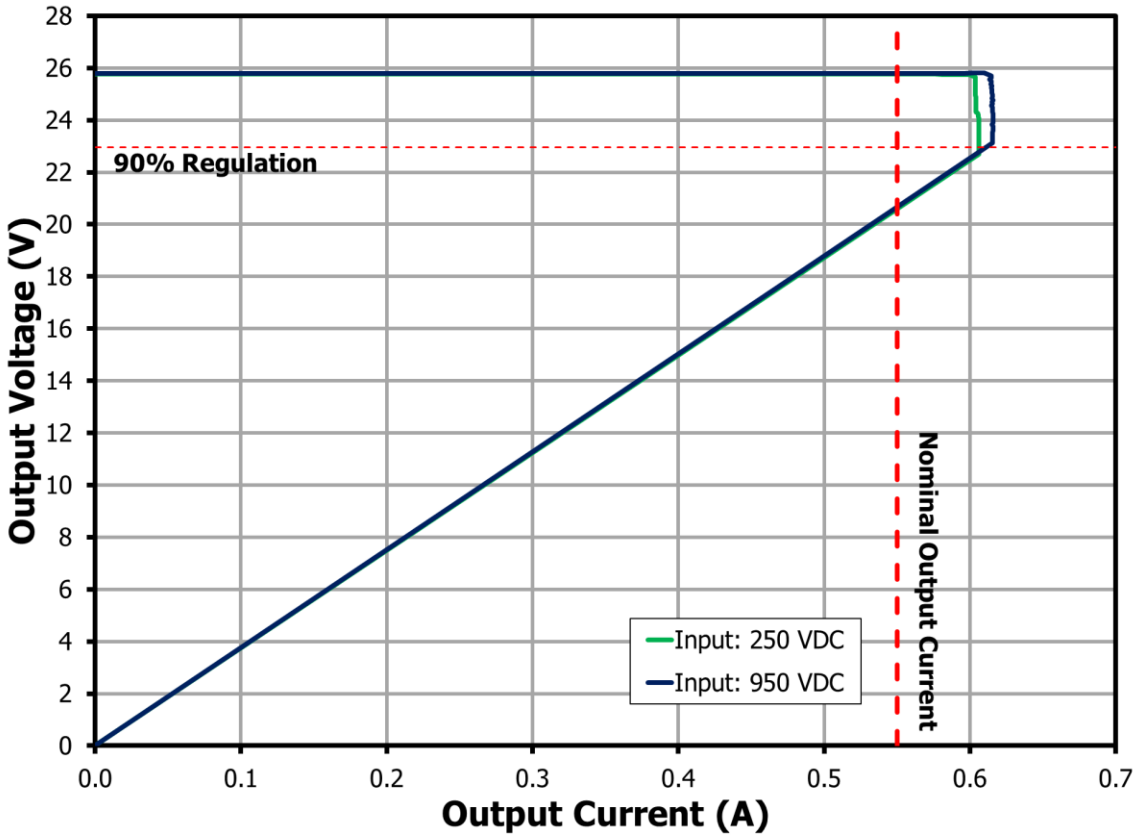


Figure 181 – 25.5 V Output Overload Curve at 250 VDC Input and 950 VDC Input.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
5-Mar-25	CAM	A	Initial Release.	Apps & Mktg

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