2SMLT0220D2C0C SCALE-iFlex LT Family

Module Adapted Gate Driver (MAG) for Driving Half-Bridge Power Modules with NTC Measurement via Electrical Interface

Product Highlights

Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution for LV100 and XHP[™]2 power modules up to 3300 V blocking voltage
- Dual channel gate driver
- To be controlled by IMC 2SILT1200T2A0C-33
- 1.0 W output power per channel at maximum ambient temperature
- ± 20 A maximum gate current
- Operation altitude up to 2000 m
- Optimized for paralleling of up to 4 power modules
- 40 °C to 85 °C operating ambient temperature

Protection / Safety Features

- · Short circuit protection
- Overvoltage protection by Advanced Active Clamping (AAC)
- NTC temperature sensing
- Undervoltage lock-out (UVLO)
- Gate clamping to VISO rail.
- · Applied double sided conformal coating

Full Safety and Regulatory Compliance

- Clearance and creepage distances between both secondary sides meet requirements for functional isolation according to IEC61800-5-1
- **RoHS** compliant

Applications

- Wind and photovoltaic power
- Industrial drives

Description

This datasheet describes the Module Adapted Gate Driver (MAG) of the SCALE-iFlex[™] LT with NTC gate driver family. The 2SMLT0220D2C0C works conjointly with a central Isolated Master Control (IMC) 2SILT1200T2A0C-33 that supports up to four power modules of LV100, HPnC and XHP^{TM} 2 packages, and a cable set.

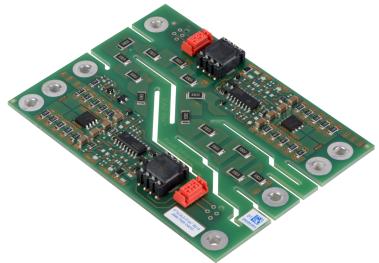
The IMC 2SILT1200T2A0C-33 operates power modules with a rated blocking voltage of up to 3300 V. The MAGs are matched to the specific power modules from a variety of suppliers.

SCALE-iFlex LT with NTC enables easy paralleling of power modules providing high flexibility and system scalability.

Figure 1. Board Photo of 2SMLT0220D2C0C.

XHP[™] is a registered trademark of Infineon Technologies AG





Pin Functional Description

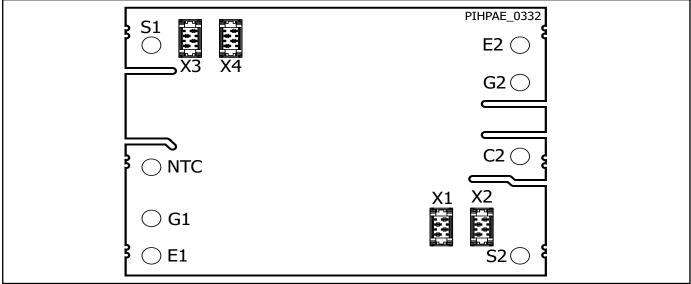


Figure 2. Pin Configuration of 2SMLT0220D2C0C.

Connections to Power Module

2SMLT0220D2C0 MAGs are directly mounted to power modules using screws.

E1

Auxiliary emitter contact of channel 1 switch.

G1

Gate contact of channel 1 switch.

E2

Auxiliary emitter contact of channel 2 switch.

G2

Gate contact of channel 2 switch.

Screw holes S1, S2

Screw holes for mechanical fixation of the board to the power module.

NTC

Contacts to module internal NTC.

C2

Auxiliary collector contact of channel 2 switch.

Connector X1

TE CONNECTIVITY 338068-4 Micro-MaTch Header (or similar); Connection from MAG to IMC or previous MAG for gate driver channel 1.

Connector X2

TE CONNECTIVITY 338068-4 Micro-MaTch Header (or similar); Connection from MAG to next MAG (if any) for gate driver channel 1.

Connector X3

TE CONNECTIVITY 338068-4 Micro-MaTch Header (or similar); Connection from MAG to IMC or previous MAG for gate driver channel 2.

Connector X4

TE CONNECTIVITY 338068-4 Micro-MaTch Header (or similar); Connection from MAG to next MAG (if any) for gate driver channel 2.

Functional Description of 2SMLT0220D2C0C

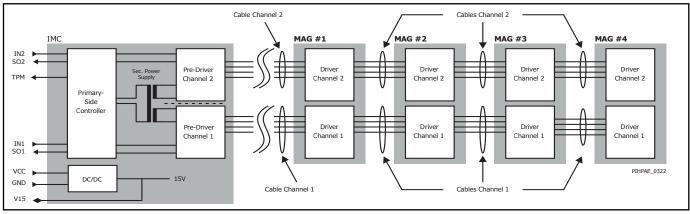


Figure 3. Functional Block Diagram of 2SILT1200T2A0C with 4 2SMLT0220D2C0C MAGs.

The 2SMLT0220D2COC (MAGs) are dual channel plug-and-play gate drivers for XHP2/LV100 power modules. The MAGs are fully mechanically and electrically adapted to the IGBT modules. They work in conjunction with the IMC to drive up to 4 parallel connected power modules (one MAG per power module is necessary).

Cable Terminals (X1, X2, X3, X4)

All MAGs have two connector terminals per channel.

The first MAG needs to be connected to the secondary-side of the IMC. Channel 1 from the IMC needs to be connected to channel 1 of the MAG (X1 or X2). Accordingly, channel 2 of the IMC with channel 2 of the MAG (X3 or X4).

In case more than one MAG is used, the first MAG needs to be connected with the second MAG. Accordingly, the second MAG with the third MAG and so on. Note that X1 and X2 respectively X3 and X4 are fully identical and can be exchanged. However, connections to channel 1 and channel 2 shall not be mixed.

Screw Terminals

The MAG is mounted on top of the power module. It must be screwed to the power semiconductor module. For details please refer to the 'mounting instruction' section in this document.

Cables

SCALE-iFlex LT with NTC gate drivers require a set of cables to establish the electrical connection between the IMC and the first MAG as well as between paralleled MAGs. The usage of cables allows for flexible positioning of the IMC within the application. Furthermore, it allows adapting to various pitches between paralleled power modules. Cables recommendations are given in the data sheet of the IMC.

Power Supplies

The isolated voltages for the gate driver channels of the MAG is generated by the integrated DC/DC converter of the IMC. The positive rail of the gate driver channels has the voltage level $V_{\rm VISO}$ and the negative rail has the voltage level $V_{\rm COM}$. Both are referenced to the emitter potential at terminal E1 or E2 of the driven power semiconductor.

Gate Voltage

SCALE-iFlex LT with NTC possesses a voltage regulator for the positive (turn-on) rail of the gate voltage. Internal current sources are regulating actively the positive gate-emitter voltage $V_{\text{GE(ON)}}$ independently of actual load conditions within the maximum specified ratings. Therefore, the on-state gate-emitter voltage of the power semi-conductor equals

in steady state the positive supply voltage V_{vrso} .

The off-state gate-emitter voltage $V_{\rm _{GE(OFF)}}$ equals in steady-state the voltage $V_{\rm _{COM}}$. This voltage is load dependent. It has its lowest value under no load conditions and is increasing slightly (i.e. getting less negative) with increasing load.

In the event of an under voltage lock-out condition the gate driver changes the control of the positive rail towards control of the negative rail V_{COM} to avoid any unpredictable system behavior.

Short-Circuit Protection

The SCALE-iFlex LT with NTC gate uses the semiconductor desaturation effect to detect short-circuits.

The desaturation is monitored on each MAG by using a resistor sensing network. The collector-emitter voltage is checked after the response time t_{RES} at turn-on to detect a short-circuit. If the voltage is higher than the programmed threshold voltage $V_{CE(SAT)}$, the driver detects a short-circuit condition. The monitored power semi-conductor is switched off after a delay of $t_{PD(SOX)}$ and a fault signal is transmitted to the IMC. Paralleled MAGs detect desaturation conditions with minimum time delays and turn off the corresponding power semiconductor.

It should be noted that the response time t_{RES} is dependent on the DC-link voltage. It remains constant between about 50% to 100% of the maximum DC-link voltage and increases at lower DC-link voltage. Please refer to the relevant data sheet section.

Note: The desaturation function is for short-circuit detection only and cannot provide over-current protection. However, over-current detection has a lower time priority and can be easily provided by the application.

Gate Clamping

In the event of a short-circuit condition, the gate voltage is increased due to the high dv_{ce}/dt between the collector and emitter terminals of the driven power semiconductor. This dv_{ce}/dt drives a current through the Miller-capacitance (capacitance between the gate and collector) and charges the gate capacitance, which eventually leads to a gate-emitter voltage larger than the nominal gate-emitter turn-on voltage. In consequence, the short-circuit current is increased due to the



transconductance of the power semiconductor.

Advanced Active Clamping (AAC)

Active clamping is a technique designed to partially turn on the power semiconductor in case the collector-emitter voltage exceeds a predefined threshold. The power semiconductor is then kept in linear operation. Figure 4 illustrates the general behavior of active clamping and its voltage thresholds. Basic active clamping topologies implement a single feedback path from the power semiconductor collector/drain through transient voltage suppressor (TVS) diodes to the power semiconductor gate. The gate driver contains Power Integrations' Advanced Active Clamping (AAC) based on this principle: When active clamping is activated, the turn-off MOSFET of the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature is mainly integrated in the secondary-side ASIC of the gate driver.

To ensure that the gate-emitter voltage stays close to the nominal turn-on voltage each MAG features a gate-clamping circuitry. The gate clamping provides a voltage similar to $V_{_{VISO}}$ to the gate, i.e. 15 V. As the effective short-circuit current is a function of the gate-emitter voltage the short-circuit current is limited. As consequence, the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits and enables a safe turn-off of the device.

It should be noted that AAC should not be activated during regular operation to avoid excessive heating of the transient voltage suppressor diodes.

Conformal Coating

The electronic components of the gate driver are protected by a layer of acrylic conformal coating with a typical thickness of 50μ m using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments.

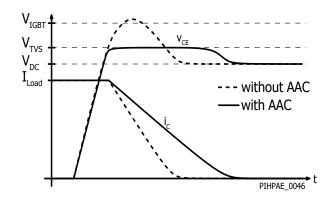


Figure 4. Advanced Active Clamping



Absolute Maximum Ratings

Parameter	Symbol	Conditions T _A = -40 °C to 85 °C	Min	Max	Units
Absolute Maximum Ratings ¹					
Gate Output Power Per channel ²	P _{GX}			1	W
Switching Frequency ³	f _{sw}			25	kHz
	V _{dc(link)}	Transient only (for 2.3 kV versions)		2300	v
		Transient only (for 1.7 kV versions)		1700	V
Operating Voltage Secondary-		Limited to 60 s (for 2.3 kV versions)		1800	V
Secondary Side		Limited to 60 s (for 1.7 kV versions)		1250	V
		Permanently applied (2.3 kV driver versions)		1600	v
		Permanently applied (1.7 kV driver versions)		1250	v
Common-Mode Transient Peak Voltage	V _{AE}	Between parallel connected emitters		50	V_{peak}
Common-Mode Time-Voltage-Area	∫ dv *dt	Between parallel connected emitters		20	μVs
Storage Temperature ⁴	T _{st}		-40	50	°C
Operating Ambient Temperature	T _A		-40	85	°C
Surface Temperature⁵	Т			125	°C
Relative Humidity	H _R	No condensation		93	%
Altitude of Operation ⁶	A _{OP}			2000	m

NOTES:

- 1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
- 2. Actually achievable maximum power depends on several parameters and may be lower than the given value. It has to be validated in the final system. It is mainly limited by the maximum allowed surface temperature.
- 3. This limit applies to the whole product family. The actual achievable switching frequency may be lower for specific gate driver variants and has to be validated in final system as it is additionally limited by maximum gate output power in conjunction with the maximum allowed surface temperature.
- 4. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
- 5. The component surface temperature, which may strongly vary depending on the actual operating conditions, must be limited to the given value to ensure long-term reliability of the product.
- 6. Operation above this level requires a voltage derating to ensure proper isolation coordination.





Characteristics

Parameter	Symbol	$V_{\rm vcc} = 24 V$	Min	Тур	Max	Units	
Device Comple			T _A = 25 °C				
Power Supply	UVLO _{VISO}	Referenced to respective terminal E1 or E2	Clear fault (resume operation)	11.6	12.6	13.6	
			Set fault (suspend operation)	11.0	12.0	13.0	V
Power Supply Monitoring Threshold			Hysteresis	0.35			-
(Secondary-Side)	UVLO _{COM}		Clear fault (resume operation)		-5.15		
			Set fault (suspend operation)		-4.85		v
			Hysteresis		0.3		
Gate Ouput					1		
Gate Turn-On Voltage	V	P _x reference		15		v	
	V _{GE(ON)}	P _x reference		15		•	
Gate Turn-Off Voltage	$V_{GE(OFF)}$	P _x reference		-9.5		v	
		P _x reference	= 5.6 W (IMC), d to terminal E1 or E2		-8.8		, in the second
Short Circuit Protection	1	1			1	I	1
Static V _{ce} -Monitoring Threshold	V _{CE(STAT)}	(With 1.		54		v	
Response Time (10% V _{GE} to 90% V _{GE})	t _{res} -	10% to 90% of V _{GE} (with 2.3 kV)	DC-link voltage= 1800 V		5.7		μs
		10% to 90% of V _{GE} (with 2.3 kV)	DC-link voltage= 1260 V		6.0		μs
		10% to 90% of V _{GE} (with 1.7 kV)	DC-link voltage= 1250 V		6.9		μs
		10% to 90% of V _{GE} (with 1.7 kV)	DC-link voltage= 600 V		7.7		μs
Delay to Turn-Off Power Semiconductor After Short-Circuit Detection	t _{PD(SOx)}				0.1		μs



Characteristics (cont.)

Parameter	Symbol	Conditions $T_A = 25 \text{ °C}$	Min	Тур	Max	Units
Electrical Isolation						
Creepage Distance	CPG _{s-s}	Secondary-side to secondary-side 22				mm
Clearance Distance	CLR _{s-s}	Secondary-side to secondary-side	8.7			mm
Mounting						
Terminal Connection Torque ⁷	M _{MAG}	Screw M3				Nm
Screw header/washer diameter	d _{M3}	Terminals G1,E1, C2, G2, E2, NTC			8	mm
	- с _{мз} –	Terminals S1, S2			8	mm
Bending	I _{BEND}	According to IPC			0.75	%

Mounting Instruction

The MAG is mounted on top of the target power module. 2SMLT0220D2C0C must be screwed to the power semiconductor module with metal screws. The mounting force is given with M_{MAG} . M_{MAG} must not exceed the values given in the respective data sheet of the target power module. Hence, the actual mounting torque may be smaller than M_{MAG} .

It is recommended to follow mounting instructions from the corresponding power semiconductor manufacturer.

Parallel connected modules shall have the same distances between each other to ensure a symmetrical switching behaviour.

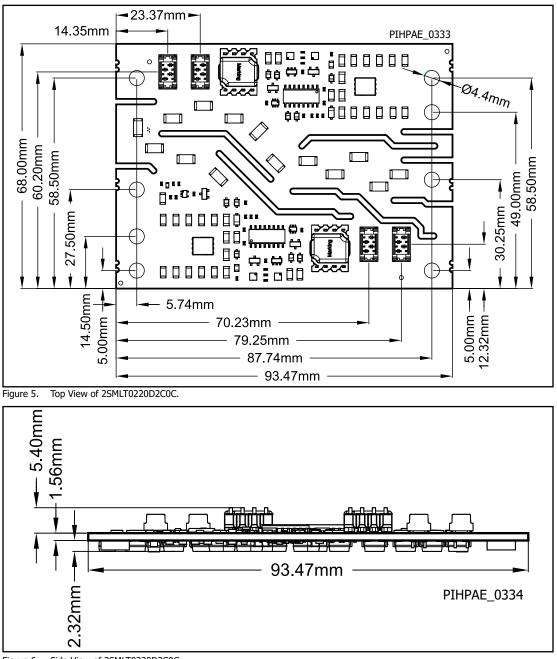
To ensure proper cooling by natural or forced convection minimum clearance of 50 mm of the MAG top side is required. This includes also that the AC and/or DC bus bars are not covering parts or the entire MAG top side.

Minimum distances between paralleled modules shall be considered according to the converter system isolation coordination. Otherwise insulation foils shall be used to isolated adjacent MAGs from each other.





Product Dimensions of 2SMLT0220D2C0C



Side View of 2SMLT0220D2C0C. Figure 6.

Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances according to Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.





Product details

Part Number	Power Module	Voltage Class	Current Class	Package	IGBT Supplier	R _{G(on)}	$R_{G(off)}$
2SMLT0220D2C0C- FF1800XTR17T2P5	FF1800XTR17T2P5	1700 V	1800 A	XHP 2	Infineon	0.54 Ω	4.0 Ω
2SMLT0220D2C0C- 2MBI1200XZF230-50	2MBI1200XZF230-50	2300 V	1200 A	HPnC	Fuji	0.22 Ω	8.6 Ω
2SMLT0220D2C0C- CM1200DW-40T	CM1200DW-40T	2000 V	1200 A	LV100	Mitsubishi	TBD	TBD



Revision	Notes	Date
А	Final Datasheet.	12/24

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