Design Example Report

Title	*86 W Output Automotive Power Supply for 800 V Systems Using InnoSwitch™3-AQ INN3949CQ*
Specification	300 VDC – 900 VDC Input; 13.5 V / 6.37 A Output
Application	Auxiliary Equipment Power Supply
Author	Automotive Systems Engineering Department
Document Number	DER-952Q
Date	May 6, 2024
Revision	1.1

Summary and Features

- Ultra-compact design for 800 V_{DC} BEV automotive applications
- Low component count (only 62 components)[1] design with a single 1700 V power switch
- Wide-range start-up and operating input from 300 V_{DC} to 900 V_{DC}[2]
- Reinforced 900 V isolated transformer (IEC-60664-1 and IEC-60664-4 compliant)
- ≥92% full-load efficiency across the input voltage range
- 1% output voltage line and load regulation
- Secondary-side output regulation
- Ambient operating temperature from -40 °C to 85 °C
- Complete fault protection, including output current limit and short-circuit protection
- Uses automotive-qualified AEC-Q surface mount (SMD) components[3]
- Low profile, 22 mm height

[1] Excluding input and output terminal blocks.
[2] Derated power below 300 V_{DC} input.
[3] AEC-Q200 transformer qualification and AEC-Q qualified SR MOSFET selection belongs to final design.

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Disclaimer:

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No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations, or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

1 Introduction

This engineering report describes an 86 W single-output automotive power supply. It is intended for use in 800 V battery system electric vehicles supporting a wide input range of 300 V_{DC} to 900 V_{DC}. This design uses the 1700 V rated INN3949CQ from the InnoSwitch3-AQ family of ICs in a flyback converter configuration.

The design provides reinforced isolation between the primary (high-voltage input) and secondary (output) sides by complying with creepage and clearance requirements calculated according to IEC-60664 parts 1 and 4.

This document contains the power supply specifications, schematic diagram, printed circuit board (PCB) layout, bill of materials (BOM), magnetics specifications, and performance data.

Figure 1 – Populated Circuit Board, Entire Assembly.

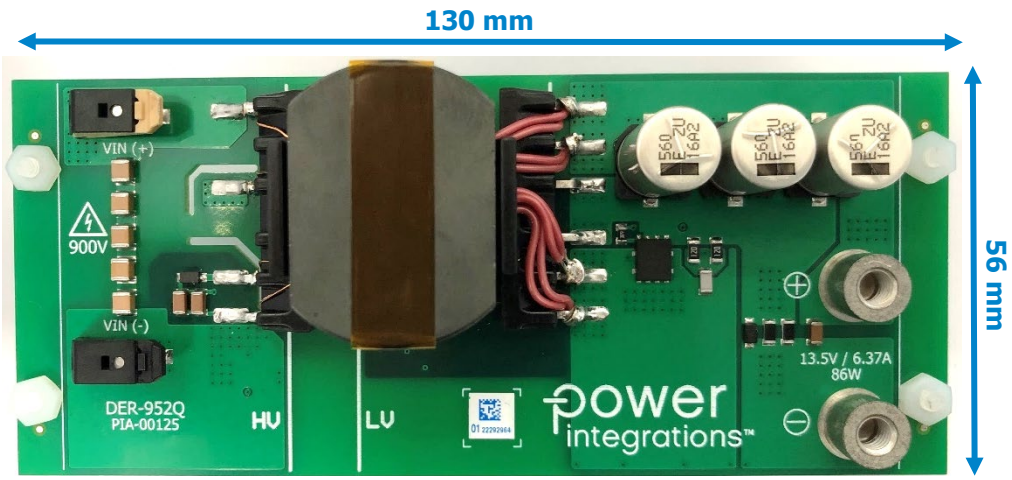


Figure 2 – Populated Circuit Board, Top.

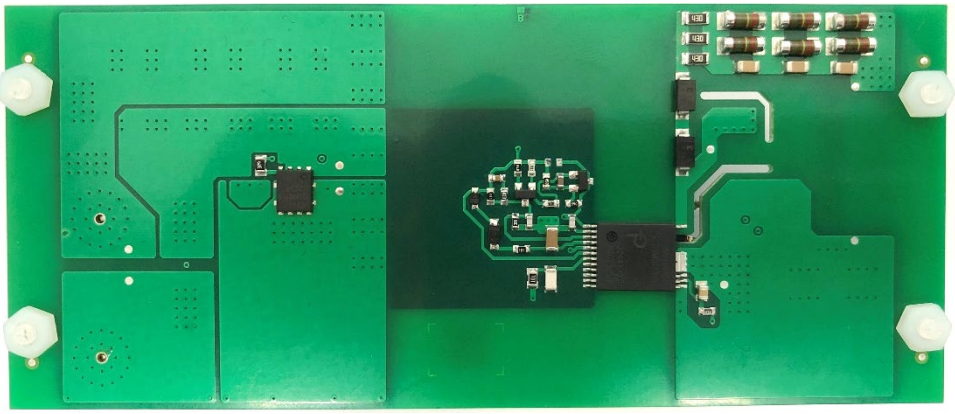


Figure 3 – Populated Circuit Board, Bottom.

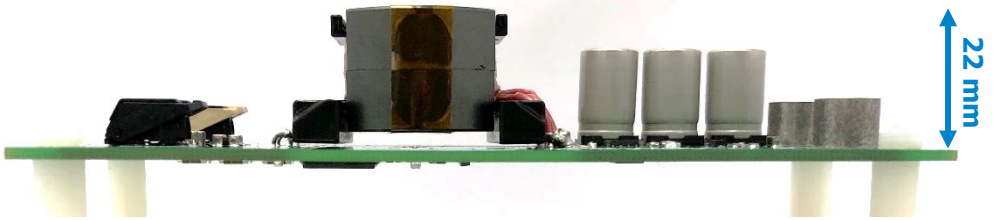


Figure 4 – Populated Circuit Board, Side.

The design described here can deliver the full 86 W output power at 85 °C ambient temperature from 300 V_{DC} to 900 V_{DC} input voltage range. The 13.5 V output configuration allows the design to replace a vehicle's auxiliary battery as a power supply for the vehicle's 12 VDC system.

The InnoSwitch3-AQ IC maintains regulation by directly sensing the output voltage and providing fast, accurate feedback to the primary-side via FluxLink™. Secondary-side control also enables synchronous rectification improving the overall efficiency compared to diode rectification, thus saving cost and space by eliminating the need for a heat sink.

2 Design Specification

The following tables below represent the minimum acceptable performance of the design. Actual performance is listed in the results section.

2.1 Electrical Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Input Parameters					
Positive DC Link Input Voltage Referenced to HV-	**HV**	300	800	900	V_{DC}
Output Parameters					
Output Voltage Parameters					
Regulated Output Voltage	**V_{OUT}**	13.37	13.5	13.64	V_{DC}
Output Voltage Load and Line Regulation	**V_{REG}**	-1		+1	%
Ripple Voltage Measured on Board	**V_{RIPPLE}**			500	mV
Output Current Parameters					
Output Current	**I_{OUT}**		6370		mA
Output Power Parameters					
Continuous Output Power at 300 V_{DC} – 900 V_{DC} Input	**P_{OUT}**		86[4]		W
Output Overshoot and Undershoot During Dynamic Load Condition	**ΔV_{OUT}**	-5		+5	%
Operating Parameters					
Operating Switching Frequency	**f_{SW}**	25		38	kHz

Table 1 – Electrical Specifications.

[4] For maximum output power capability at V_{IN} less than 300 V, see Section 13.

2.2 Isolation Coordination

Description	Symbol	Min.	Typ.	Max.	Units
Maximum Blocking Voltage of INN3949CQ	$\mathbf{BV_{DSS}}$			1700	V
System Voltage	$\mathbf{V_{SYSTEM}}$			1370	V
Working Voltage	$\mathbf{V_{WORKING}}$			900	V
Pollution Degree	**PD**			2	
CTI for FR4	**CTI**	175			
Rated Impulse Voltage	$\mathbf{V_{IMPULSE}}$			2.5	kV
Altitude Correction Factor for h_a	**Cha**	1.59			
Basic Clearance Distance Requirement	$\mathbf{CLR_{BASIC}}$	2.4			mm
Reinforced Clearance Distance Requirement	$\mathbf{CLR_{REINFORCED}}$	4.8			mm
Basic Creepage Distance Requirement for PCB	$\mathbf{CPG_{BASIC(PCB)}}$	5.4			mm
Reinforced Creepage Distance Requirement for PCB	$\mathbf{CPG_{REINFORCED(PCB)}}$	10.8			mm
Isolation Test Voltage Between Primary and Secondary-Side for 60s	$\mathbf{V_{ISO}}$	3536			V_{RMS}
Partial Discharge Test Voltage	$\mathbf{V_{PD\_TEST}}$	1860			V_{PK}

Table 2 – Isolation Coordination[5].

2.3 Environmental Specifications

Description	Symbol	Min.	Typ.	Max.	Units
Ambient Temperature	Ta	-40		85	°C
Altitude of Operation	ha			5500	m
Relative Humidity	Rh			85	%

Table 3 – Environmental Specifications.

[5] Clearance and creepage distances are derived from IEC 60664-1 and IEC 60664-4.

3 Schematic

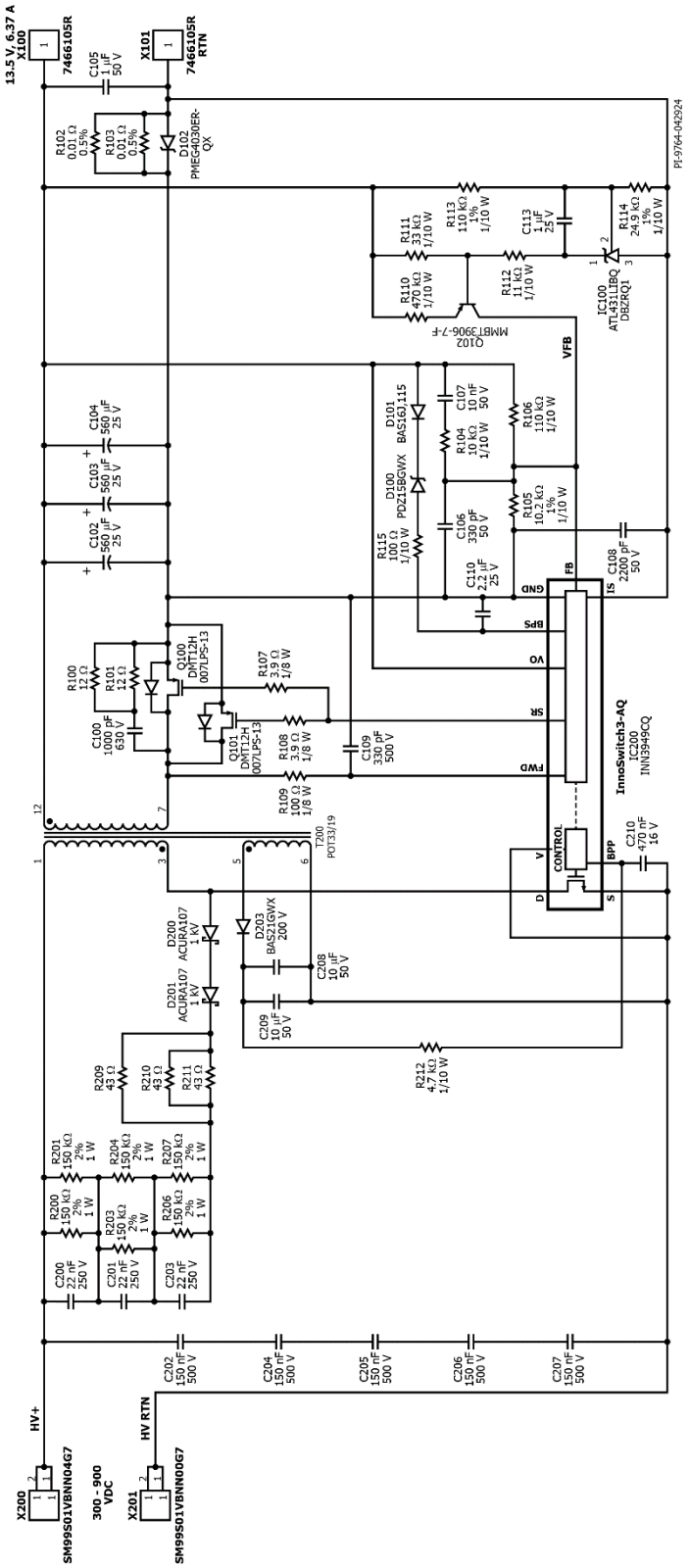


Figure 5 – DER-952Q Schematic.

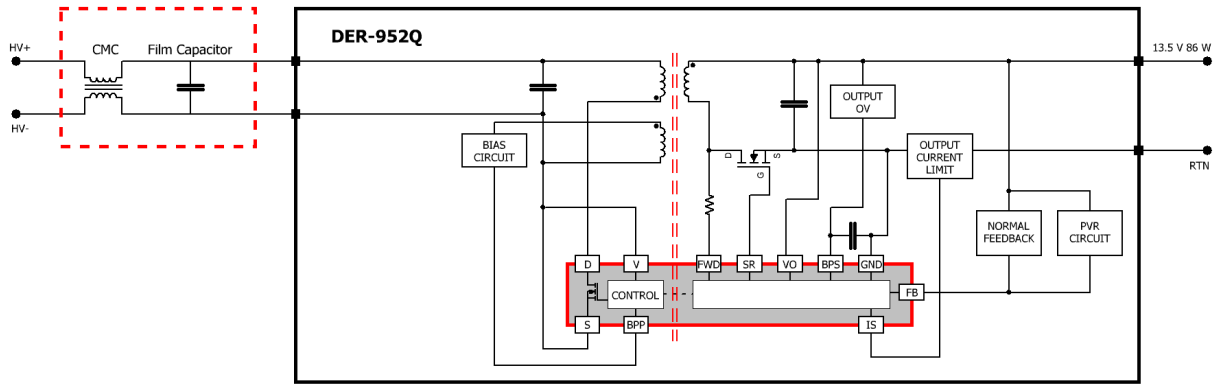


Figure 6 – DER-952Q Application with CMC and Film Capacitor Block Diagram.[6]

[6] Addition of the external CMC and film capacitor is optional. The CMC and film capacitor are only necessary if there is a need to protect the unit from common mode noise. The film capacitor is added with the CMC to reduce CMC ripple current for lower losses and operating temperature. Filter component values should be calculated based on system application requirements.

4 Circuit Description

4.1 Input Filter

Bypass capacitors C202, C204, C205, C206, and C207 help filter input noise and are used to minimize the primary-side current loop. The capacitors are selected not to exceed 65% of their voltage rating and to maintain enough pad-to-pad distance to meet creepage and clearance requirements.

4.2 High-Voltage Side Circuit

The circuit design uses a flyback converter topology to provide an isolated low-voltage output from the high-voltage input. The flyback transformer T200 primary winding is connected to the high-voltage DC input and the drain terminal of the 1700 V SiC power MOSFET switch inside the INN3949CQ (IC200).

An R2CD-type snubber circuit is placed across the primary-side winding to limit the drain-source voltage peaks seen by the internal SiC MOSFET during turn-off. Two super-fast (or better) surface mount, AEC-Q qualified diodes (D200 and D201), are placed in series to meet creepage and clearance requirements. This also ensures that the reverse voltage across the diodes would not exceed 70% of their maximum rating. Capacitors C200, C201, and C203 catch the energy from the leakage inductance of transformer T200. The capacitor values are selected to minimize the voltage ripple across the snubber resistor network and maintain near-constant power dissipation throughout the switching period. Resistors R200, R201, R203, R204, R206, and R207 dissipate the energy stored by the snubber capacitors. The resistor values are selected so that their average voltage will not exceed 80% of their maximum voltage rating and dissipate below 50% of their rated power.

The InnoSwitch3-AQ IC200 is self-starting, using an internal high-voltage current source to charge the BPP capacitor, C210. The INN3949CQ IC is guaranteed to operate at 30 V input but can typically start below this level.

The transformer T200 auxiliary winding provides power to the primary-side during normal operation. This minimizes the power derived from the internal high-voltage current source, improving overall efficiency and reducing heating of the IC200. The auxiliary winding output is rectified and filtered by diode D203 and capacitors C208 and C209. The filtered (DC) voltage is fed to the BPP pin through resistor R212.

In this design, the UV and OV features are disabled by shorting the V pin to the SOURCE pin.

4.3 Low-Voltage Side Circuit

The secondary-side of the INN3949CQ provides output voltage sensing, output current sensing, and gate drive for the synchronous rectification MOSFET (SR FET). SR FETs Q100 and Q101 rectify the voltage across the secondary winding of the transformer T200, then filtered by output capacitors C102, C103, C104, and C105. An RC-type snubber formed by resistors R100, R101 and capacitor C100 dampens the high-frequency ringing in the SR FET Drain-Source nodes.

The secondary-side controller inside IC200 controls the switching of the SR FETs. Timing is based on the negative edge voltage transition sensed from the FWD pin via resistor R109. Capacitor C109 and resistor R109 form a low-pass filter that reduces voltage spikes seen by the FWD pin and ensures that the maximum rating of 150 V will not be exceeded.

In continuous conduction mode operation, the primary-side power MOSFET is turned off just before the secondary-side controller requests a new switching cycle from the primary. In discontinuous mode, the SR MOSFET is turned off when the voltage across it falls below a certain threshold, $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET removes any possibility of cross-conduction between the two switches and ensures reliable SR operation.

The secondary-side of the IC is powered by either the secondary winding forward voltage (thru R109 and the FWD pin) or by the output voltage (thru the VOUT pin). In both cases, energy is used to charge the decoupling capacitor C110 via an internal regulator.

The INN3949CQ IC has an FB pin internal reference of 1.265 V. Resistors R105, and R106 form the basic voltage divider feedback network for InnoSwitch3-AQ designs. However, for this design, the output voltage value set by R105 and R106 is 10 – 15 % higher than the target output voltage as a requirement for implementing the *Precise Voltage Regulation* circuit. Capacitor C106 provides decoupling from high-frequency noise affecting power supply operation. Capacitor C107 and R104 form a feedforward network to speed up the feedback response time and lower the output ripple.

Output current is sensed by monitoring the voltage drop across parallel resistors R102 and R103. The resulting current measurement is filtered with decoupling capacitor C108 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of around 35 mV is used to reduce losses. Once the threshold is exceeded, the INN3949CQ IC200 will adjust the number of pulses to maintain a fixed current output (CC mode). The IC will enter auto-restart (AR) operation when the output voltage is below 90% of regulation and recover when the load current is reduced below the CC limit. Schottky diode D102 limits the voltage across the IS pin to protect it during output short-circuit events.

4.4 Precision Voltage Regulation (PVR) Circuit[7]

The PVR circuit improves output voltage regulation by using an external error amplifier with a high-precision reference voltage (ATL431) to control the FB pin. The PVR injects a DC bias current to the FB pin of INN3949CQ to reduce the DC error at the output. The ATL431 error amplifier network is placed after the current sense resistor to also compensate for the sense resistor voltage drop.

The ATL431LIBQDBZRQ1 is selected for its high precision and stability across temperatures. The output voltage is sensed through voltage dividers R113 and R114. The resistor values are chosen such that at the rated output voltage, the voltage at the REF

[7] Circuit implementation is optional. Application is only necessary if there is a need for output voltage regulation within 1%.

pin of IC100 equals its reference voltage of 2.5 V. Shunt regulator IC100 sinks cathode current proportional to the difference between the scaled output voltage and its internal reference. The amount of cathode current affects the amount of current injected into the InnoSwitch3's FB pin. Capacitor C113 together with resistor R113 forms an integrator to ensure the PVR circuit only corrects for DC error.

Resistor R111 and R112 provide the base current path for Q102 and the bias current for IC100. Together with R110, the values of these resistors are chosen such that IC100 and Q102 are kept away from saturation and provide an adequate allowance for the base and cathode currents to swing during transient load events. While operating in the forward active region, Q102 acts as a variable impedance in parallel to the upper feedback resistor R106.

5 PCB Layout

Layers: Six (6)
Board Material: FR4
Board Thickness: 1.6 mm
Copper Weight: 1 oz

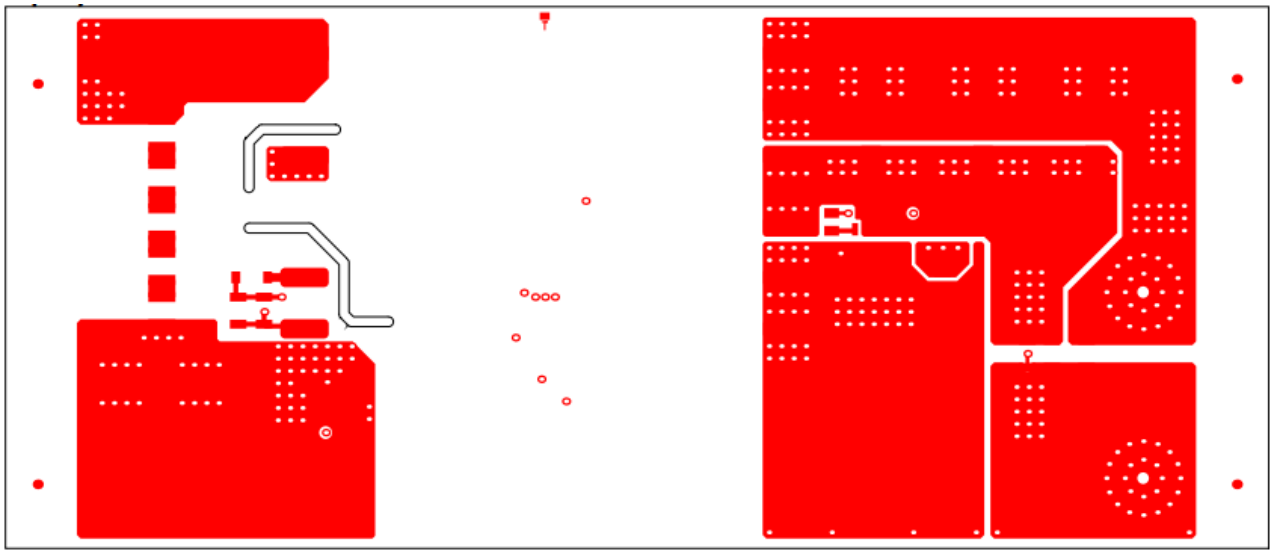


Figure 7 – DER-952Q Top Layer PCB Layout.

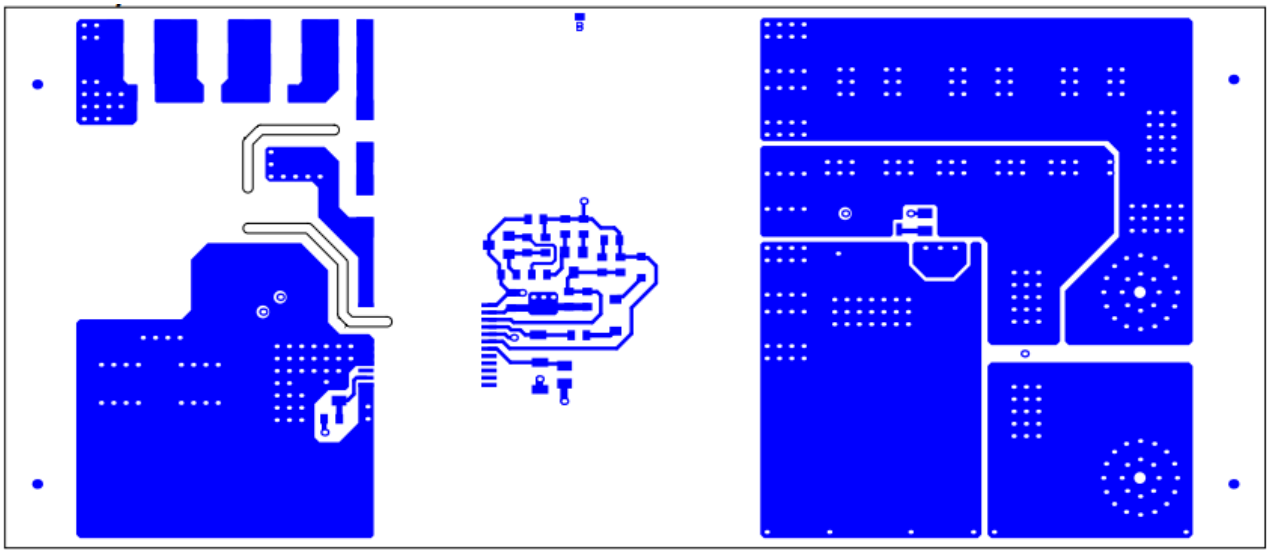


Figure 8 – DER-952Q Bottom Layer PCB Layout.

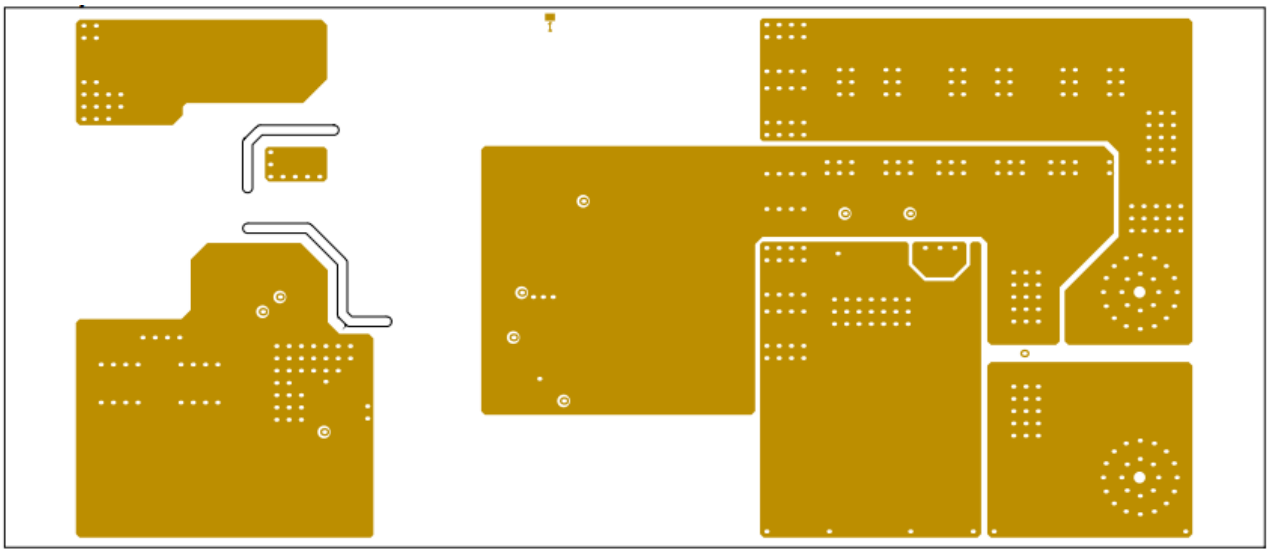


Figure 9 – DER-952Q Mid-Layer 1 PCB Layout

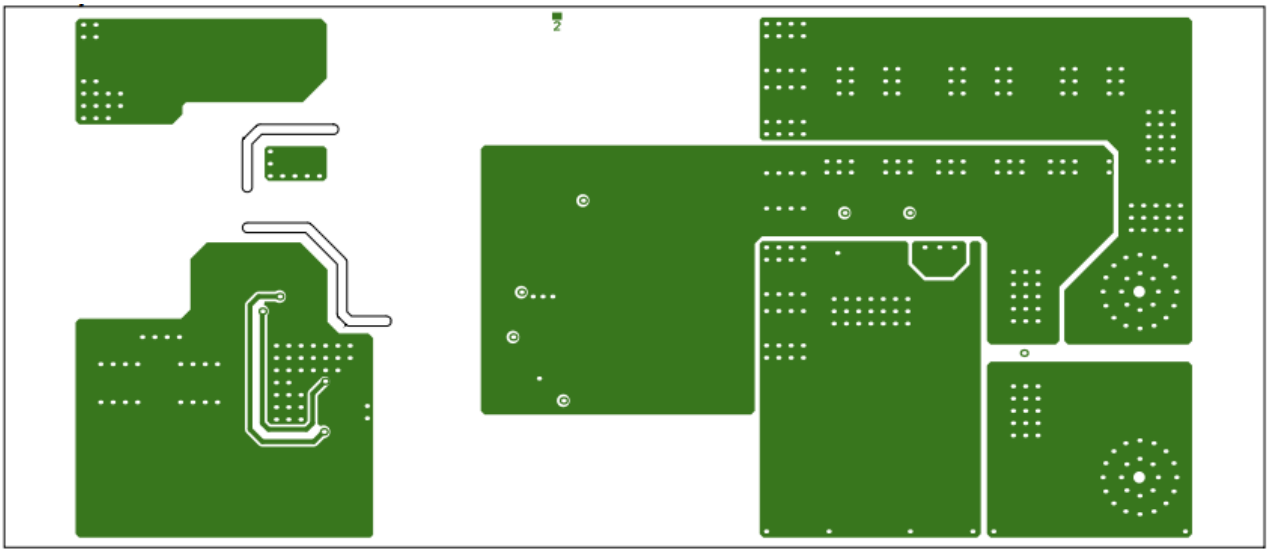


Figure 10 – DER-952Q Mid-Layer 2 PCB Layout.

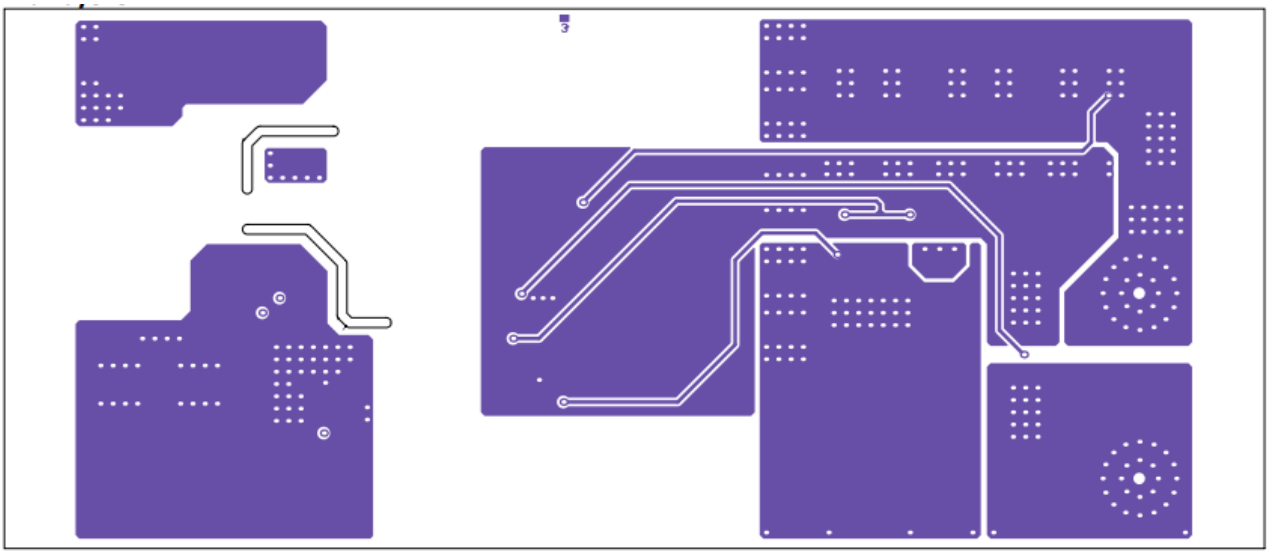


Figure 11 – DER-952Q Mid-Layer 3 PCB Layout.

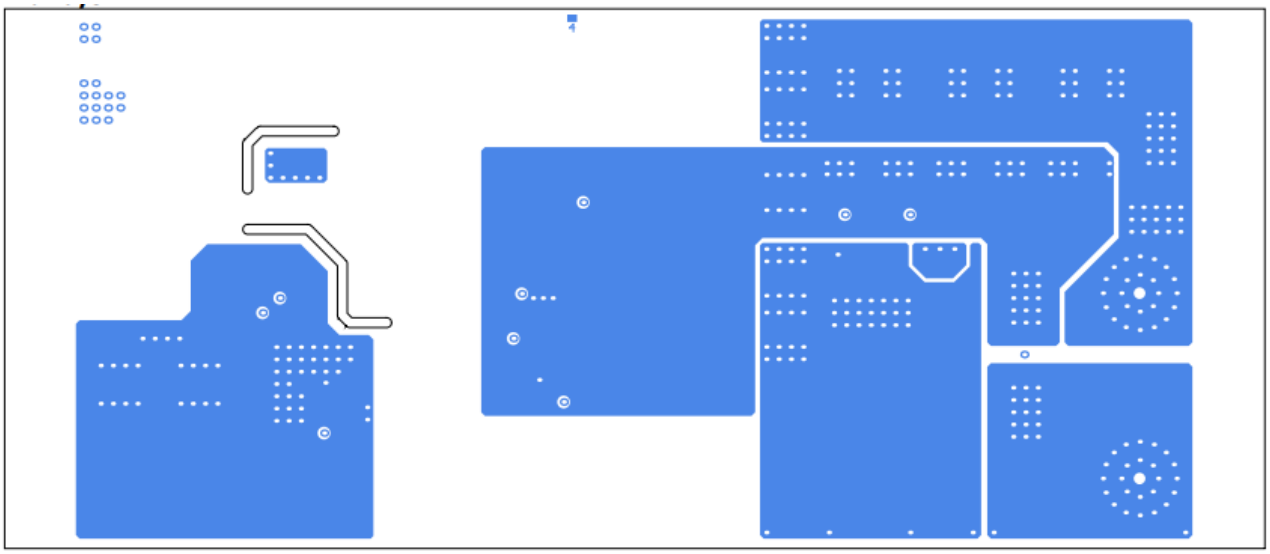


Figure 12 – DER-952Q Mid-Layer 4 PCB Layout.

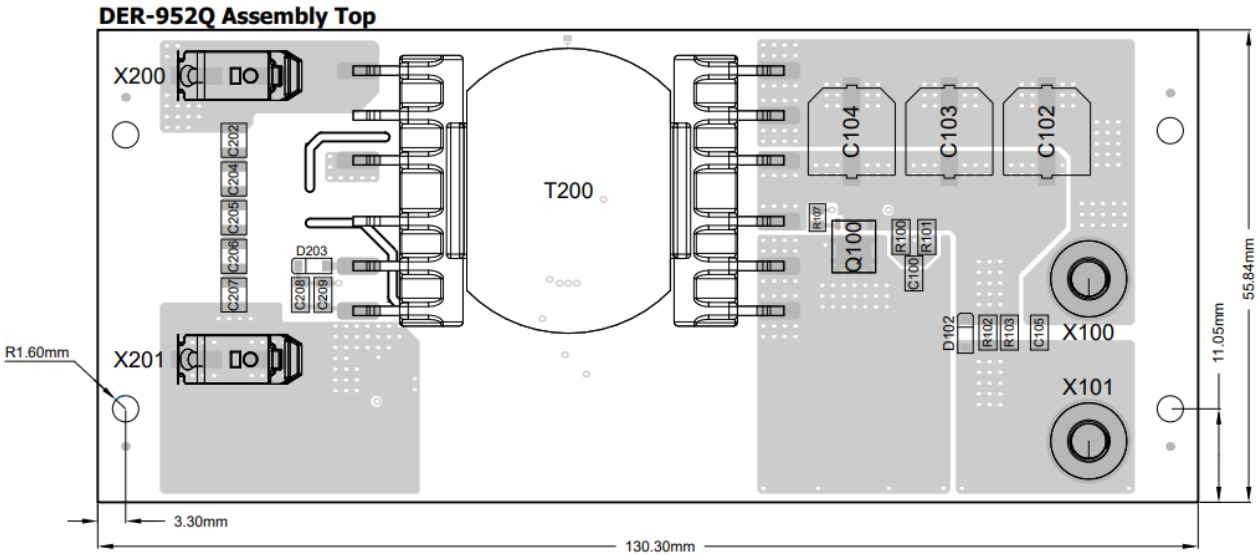


Figure 13 – DER-952Q PCB Assembly (Top).

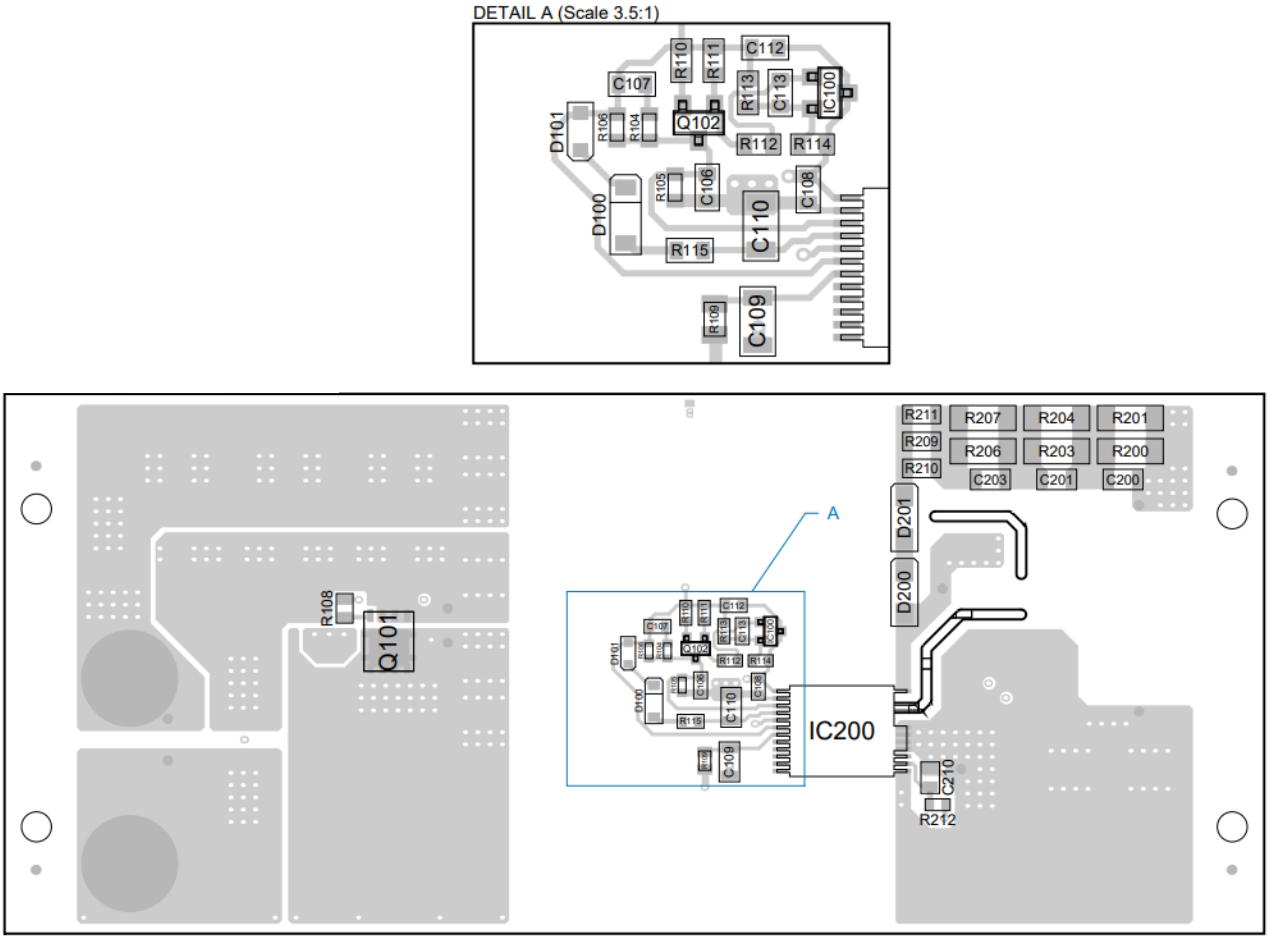


Figure 14 – DER-952Q PCB Assembly (Bottom).

6 Bill of Materials

Item	Qty	Designator	Description	MFR Part Number	Manufacturer
1	1	C100	Ceramic Chip Capacitor 1000 pF C0G 630V 5% 1206	CGA5F4C0G2J102J085AA	TDK
2	3	C102, C103, C104	Polymer Aluminum Capacitor 560 µF AL 25V 20% 10.3X10.3mm	EEH-ZU1E561P	Panasonic
3	1	C105	Ceramic Chip Capacitor 1 µF X7R 50V 10% 1206	CGA5L3X7R1H105K160AE	TDK
4	1	C106	Ceramic Chip Capacitor 330 pF C0G 50V 5% 0603	CGA3E2C0G1H331J080AA	TDK
5	1	C107	Ceramic Chip Capacitor 10 nF X7R 50V 10% 0603	C0603C103K5RACAUTO7411	KEMET
6	1	C108	Ceramic Chip Capacitor 2200 pF C0G 50V 5% 0603	GCM1885C1H222JA16D	Murata
7	1	C109	Ceramic Chip Capacitor 330 pF C0G 500V 10% 1206	C1206C331KCGACAUTO	KEMET
8	1	C110	Ceramic Chip Capacitor 2.2 µF X7R 25V 20% 1206	CGA5L2X7R1E225M160AA	TDK
9	1	C113	Ceramic Chip Capacitor 1 µF X7R 25V 20% 0603	CGA3E1X7R1E105M080AC	TDK
10	3	C200, C201, C203	Ceramic Chip Capacitor 22 nF X7R 250V 10% 1206	GCJ31BR72E223KXJ1L	Murata
11	5	C202, C204, C205, C206, C207	Ceramic Chip Capacitor 150 nF X7R 500V 10% 1210	C1210X154KCRACAUTO	KEMET
12	2	C208, C209	Ceramic Chip Capacitor 10 µF X7R 50V 10% 1206	CGA5L1X7R1H106K160AC	TDK
13	1	C210	Ceramic Chip Capacitor 470 nF X7R 16V 10% 0805	AC0805KKX7R7BB474	YAGEO
14	1	D100	Zener Diode 15 V 365 mW SOD123	PDZ15BGWX	Nexperia
15	1	D101	Diode Standard 100 V 250 mA SOD-323	BAS16J,115	Nexperia
16	1	D102	Schottky Diode 40 V 3 A SOD-123W	PMEG4030ER-QX	Nexperia
17	2	D200, D201	Diode SCHOTTKY 1 kV 1 A DO-214AC (SMA)	ACURA107-HF	Comchip
18	1	D203	Diode Standard 200 V 225 mA (DC) SMT SOD-123	BAS21GWX	Nexperia
19	1	IC100	Voltage References Automotive, high-bandwidth, low-IQ programmable shunt regulator	ATL431LIBQDBZRQ1	Texas Instruments
20	1	IC200	InnoSwitch3-AQ Vmos InSOP-24D CV/CC QR Flyback Switcher IC with Integrated 1700 V Switch and FluxLink Feedback for Automotive Applications	INN3949CQ	Power Integrations
21	2	Q100, Q101	N-Channel MOSFET 120 V 90 A (Ta), 90 A (Tc) 2.9 W (Ta) PowerDI5060-8	DMT12H007LPS-13[8]	Diodes, Inc.
22	1	Q102	40 V / 0.2 A PNP bipolar transistor SOT-23	MMBT3906-7-F	Diodes, Inc.
23	2	R100, R101	Thick Film Chip Resistor 12 Ω 0.25W 200V 5% 1206	AC1206JR-0712RL	YAGEO
24	2	R102, R103	Current Sense Resistor 0.01 Ω 0.25W 200V 0.5% 1206	WSL1206R0100DEA	Vishay
25	1	R104	Thick Film Chip Resistor 10 kΩ 0.1W 75V 5% 0603	AC0603JR-0710KL	YAGEO
26	1	R105	Thick Film Chip Resistor 10.2 kΩ 0.1W 150V 1% 0603	RMCF0603FT10K2	Stackpole
27	1	R106	Thick Film Chip Resistor 110 kΩ 0.1W 150V 5% 0603	RMCF0603JT110K	Stackpole
28	2	R107, R108	Thick Film Chip Resistor 3.9 Ω 0.125W 150V 5% 0805	RMCF0805JT3R90	Stackpole
29	1	R109	Thick Film Chip Resistor 100 Ω 0.125W 150V 5% 0805	RMCF0805JT100R	Stackpole
30	1	R110	Thick Film Chip Resistor 470 kΩ 0.1W 150V 5% 0603	RMCF0603JT470K	Stackpole
31	1	R111	Thick Film Chip Resistor 33 kΩ 0.1W 150V 5% 0603	RMCF0603JT33K0	Stackpole
32	1	R112	Thick Film Chip Resistor 11 kΩ 0.1W 150V 5% 0603	RMCF0603JT11K0	Stackpole
33	1	R113	Thick Film Chip Resistor 110 kΩ 0.1W 150V 1% 0603	RMCF0603FT110K	Stackpole
34	1	R114	Thick Film Chip Resistor 24.9 kΩ 0.1W 150V 1% 0603	RMCF0603FT24K9	Stackpole
35	1	R115	Thick Film Chip Resistor 100 Ω 0.1W 5% 0603	RMCF0603JT100R	Stackpole

[8] DMT12H007LPS-13 is not AEC-Q qualified.

36	6	R200, R201, R203, R204, R206, R207	MELF Resistors 150 kΩ 1W 200V 2% MELF 0207	CMB02070X1503GB200	Vishay
37	3	R209, R210, R211	Thick Film Chip Resistor 43 Ω 0.25W 5% 1206	RMCF1206JT43R0	Stackpole
38	1	R212	Thick Film Chip Resistor 4.7 kΩ 0.1W 150V 5% 0603	RMCF0603JT4K70	Stackpole
39	1	T200	86 W Power Transformer		Power Integrations
40	2	T200-Core	SSP-95A POT/3319 Ferrite Core		Sunshine
41	1	T200-Bobbin	Customized bobbin		Power Integrations
42	2	X100, X101	1 Pin Screw Terminal, Power Tap M5 Surface Mount	7466105R	Würth
43	1	X200	TERM BLOCK 1POS SIDE ENTRY SMD RED	SM99S01VBNN04G7	METZ CONNECT
44	1	X201	TERM BLOCK 1POS SIDE ENTRY SMD BLACK	SM99S01VBNN00G7	METZ CONNECT

Table 4 – DER-952Q Bill of Materials[9].

[9] All components are AEC-Q qualified except the SR MOSFET, connectors, and transformer.

7 Transformer Specification (T200)

7.1 Electrical Diagram

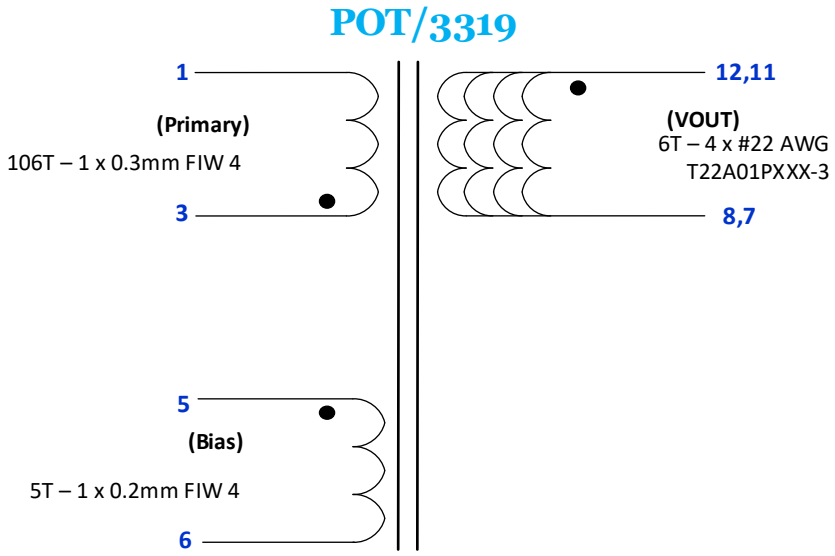


Figure 15 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power	Output power secondary-side			86	W
Input voltage Vdc	Flyback topology	300	800	900	V
Switching frequency	Flyback topology			38	kHz
Duty cycle	Flyback topology	13.2		44.5	%
Np:Ns			17.67		
Rdc	Primary-side		1.66		Ω
Rdc	Secondary-side		6.03		mΩ
Coupling capacitance	Primary-side to secondary-side Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 3 to pin 7, with pins 1 - 3 shorted and pins 7 - 12 shorted at 25°C			137	pF
Primary inductance	Measured at 1 V_{PK-PK}, 100 kHz frequency, between pin 1 to pin 3, with all other windings open at 25 °C		2663		µH
Part to part tolerance	Tolerance of Primary Inductance	-5.0		5.0	%
Primary leakage inductance	Measured between pin 1 to pin 3, with all other windings shorted.			26.63	µH

Table 5 – Transformer (T200) Electrical Specifications.

7.3 Transformer Build Diagram

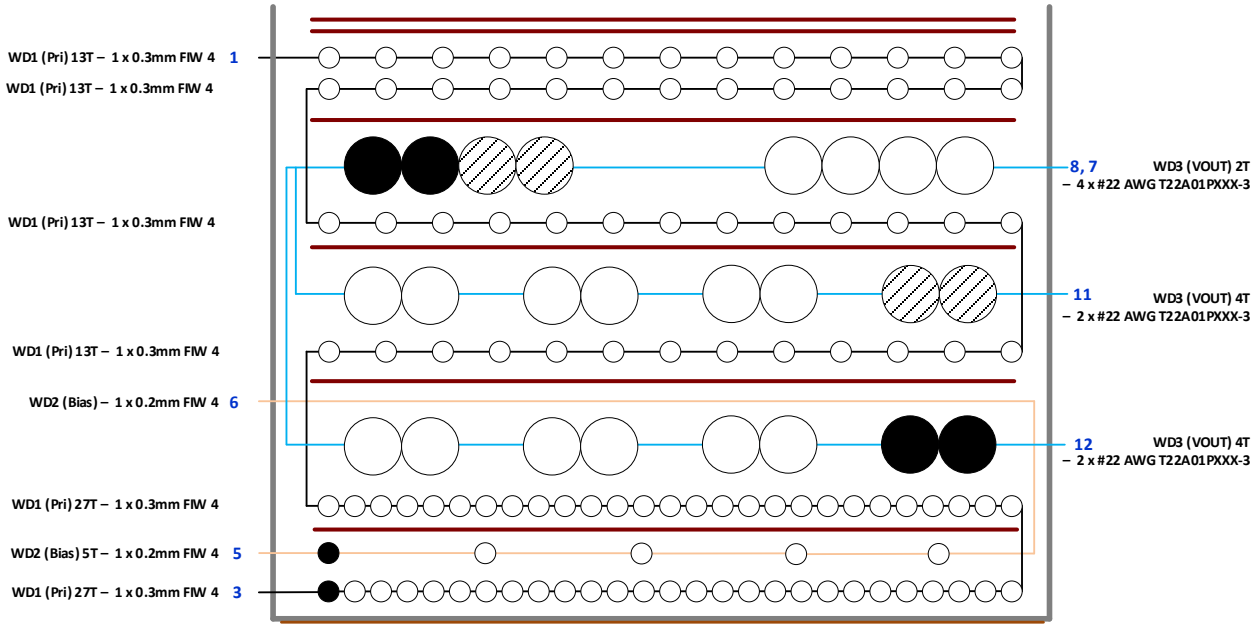


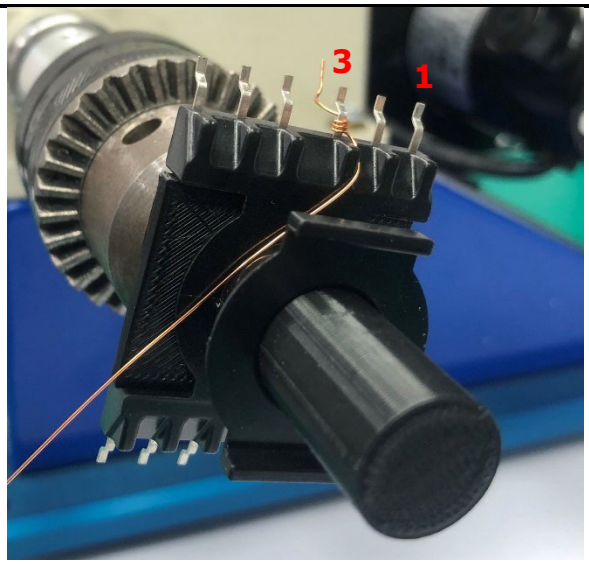
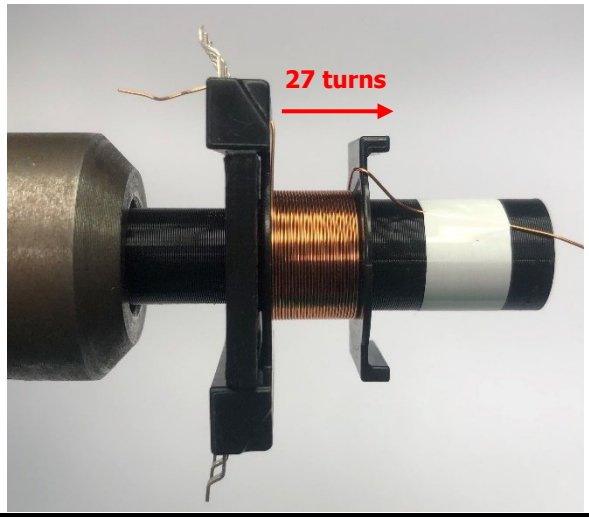
Figure 16 – Transformer Build Diagram.

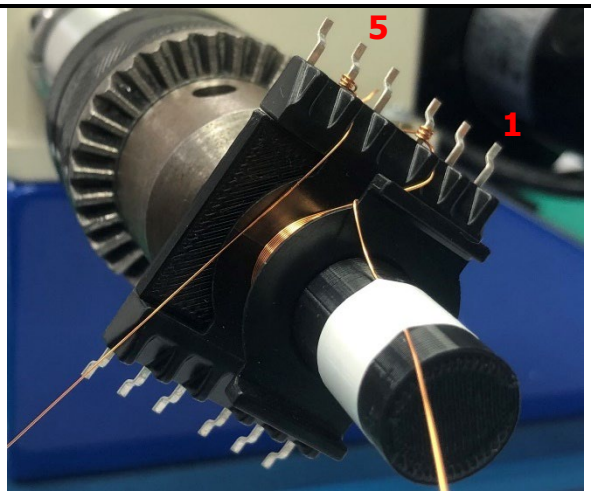
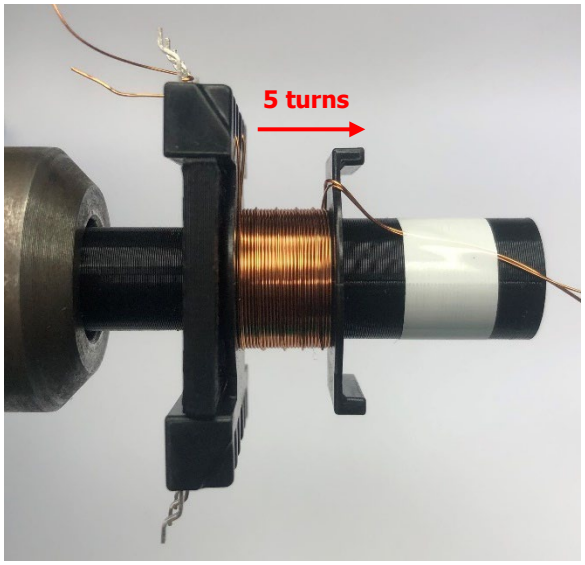
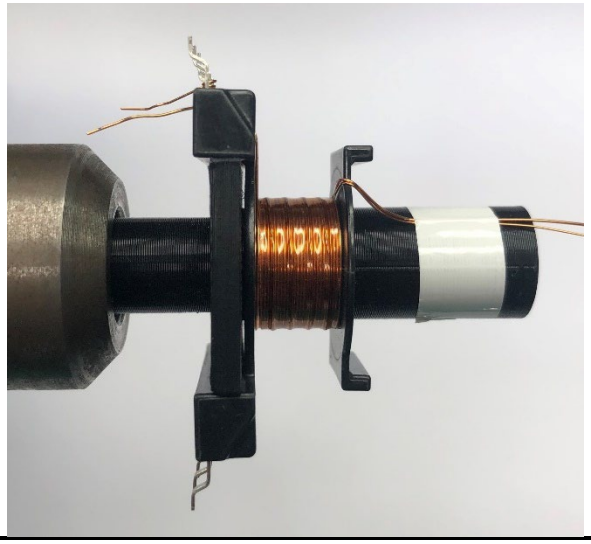
7.4 Material List

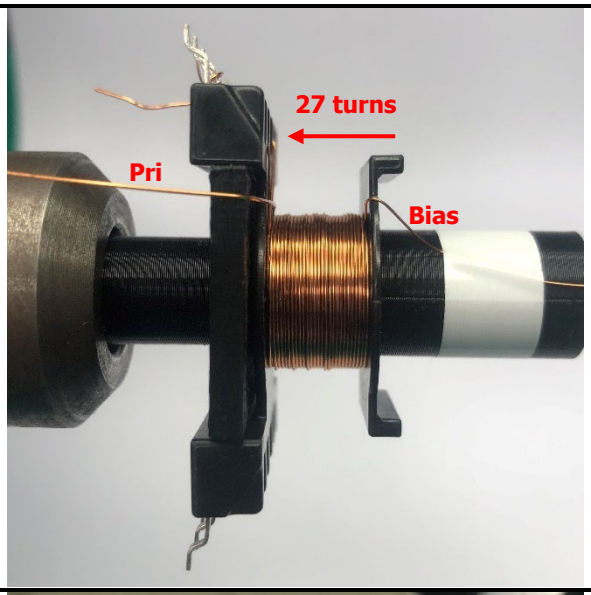
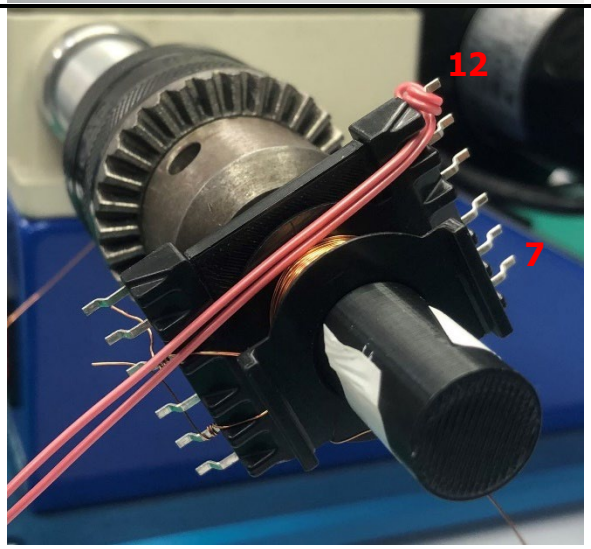
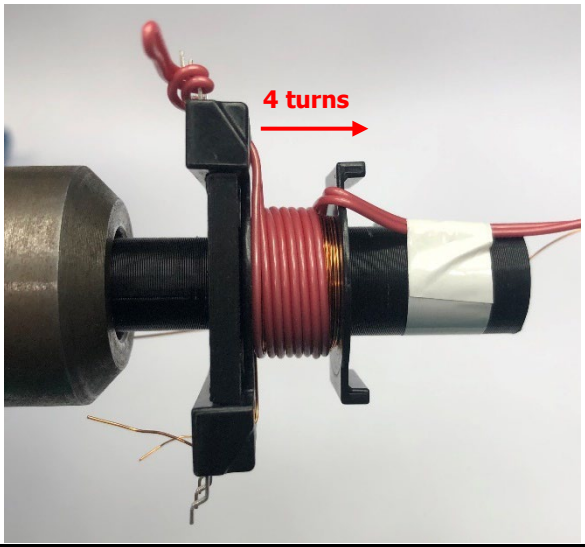
Item	Description	Qty	UOM	Material	Manufacturer
[1]	Bobbin: MCT-POT3301	1	PC	Phenolic	MyCoilTech
[2]	Core: POT33/19	2	PCS	SSP-95A (or equivalent)	Sunshine
[3]	WD1 (Pri): 0.30 mm FIW 4, Class F	6250	mm	Copper Wire	Elektrisola
[4]	WD2 (Bias): 0.20 mm FIW 4, Class F	300	mm		Elektrisola
[5]	WD3 (VOUT): T22A01PXXX-3, AWG #22 PFA .003”	1800	mm		Rubadue
[5]	3M Polyimide Film Tape 5413, width: 0.38in (9.65mm)		mm	3M 5413 0.38" X 36YD (or equivalent)	3M

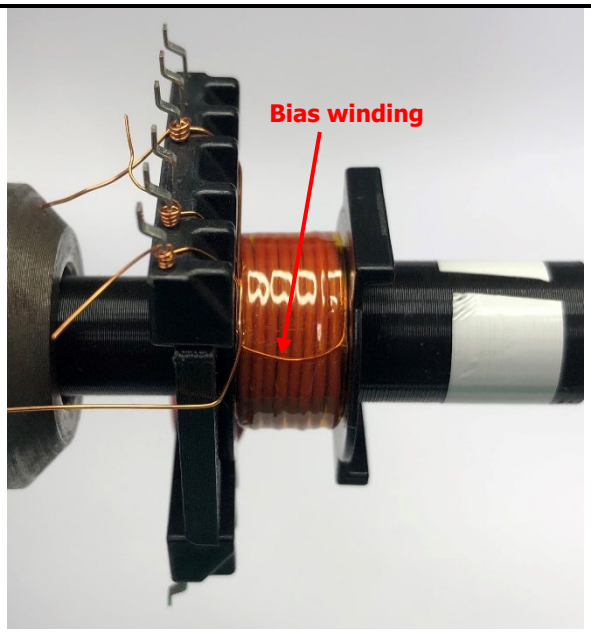
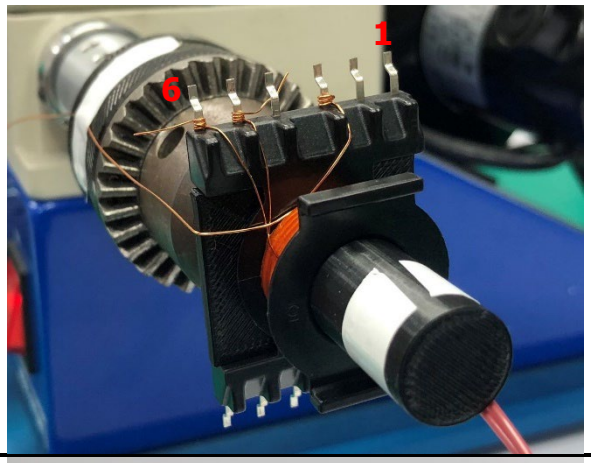
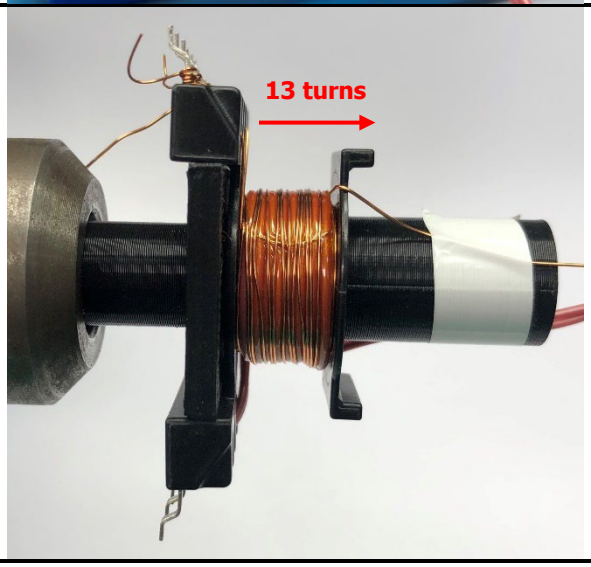
Table 6 – Transformer (T200) Material List.

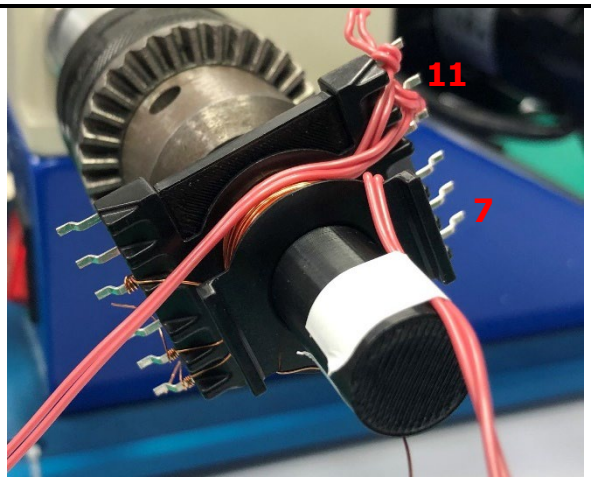
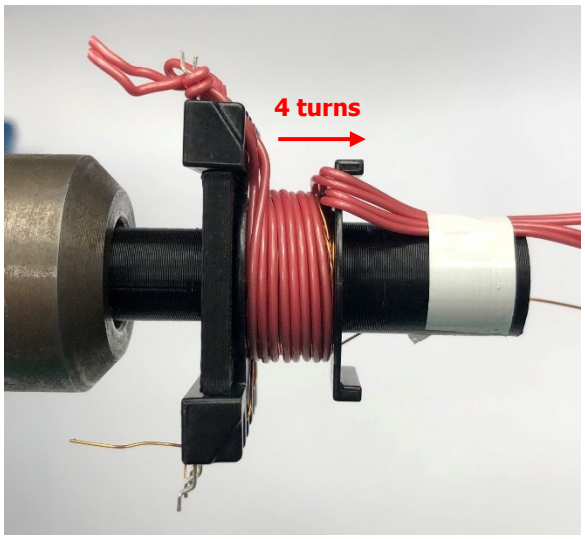
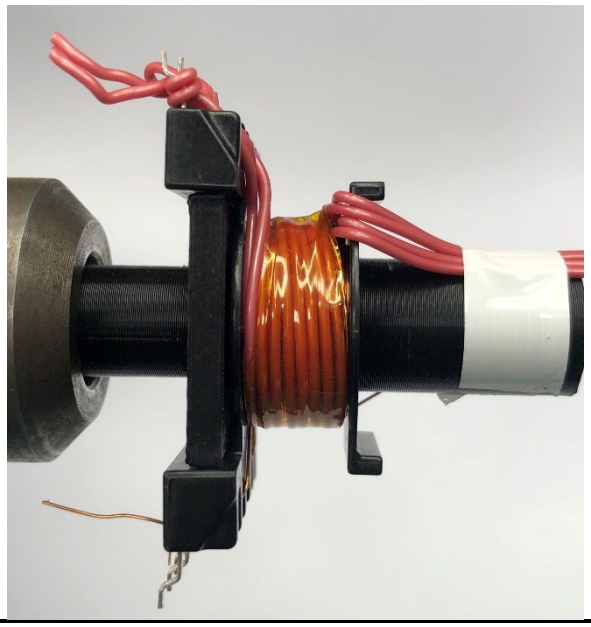
7.5 Winding Instructions

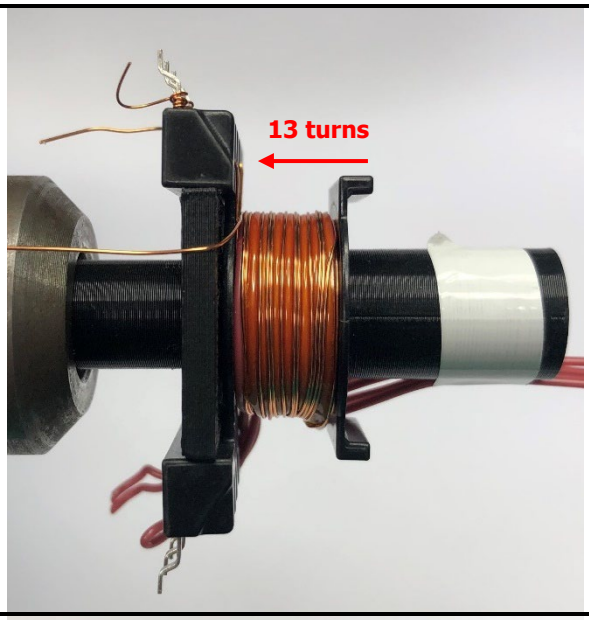
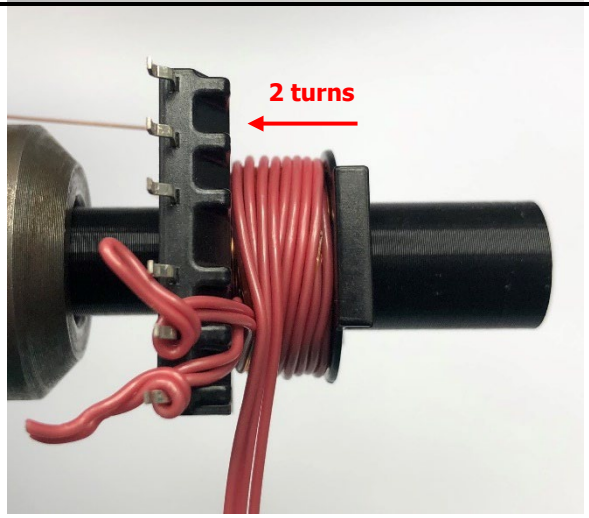
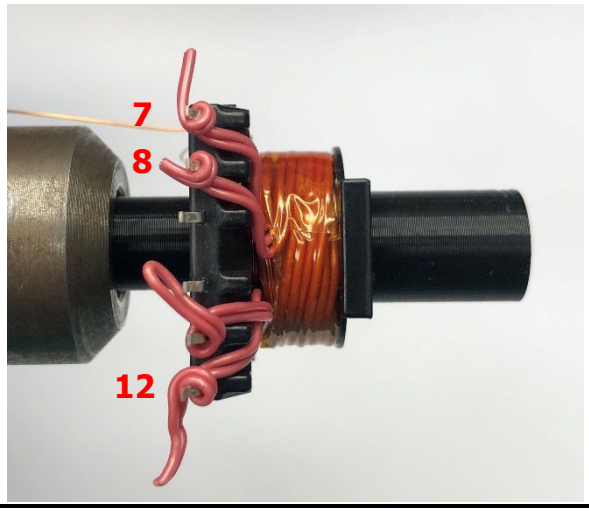
WD1 (Pri)	 	Use 0.3 mm FIW4 wire. Start on PIN 3. Wind the primary winding's first layer, 27 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.

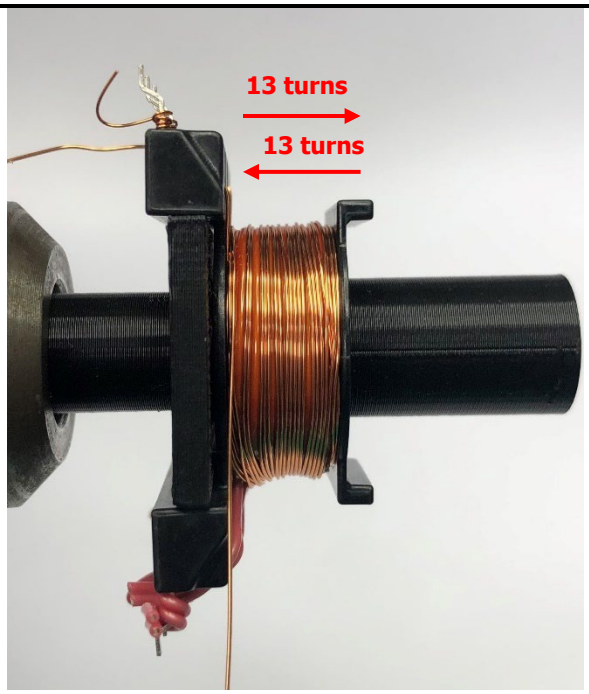
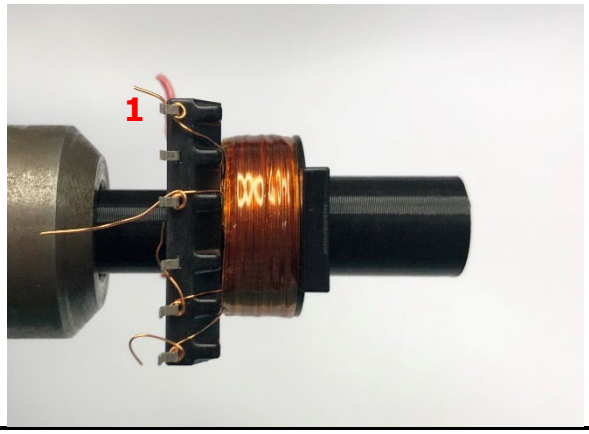
WD2 (Bias)	  	Use 0.2 mm FIW4 wire. Start on PIN 5. Wind the bias winding, 5 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet. Secure the winding using 1 layer of tape.

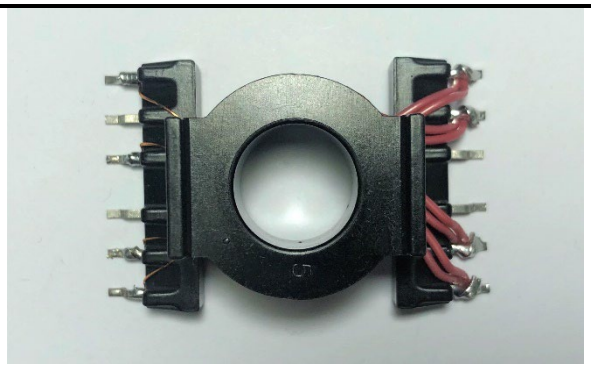
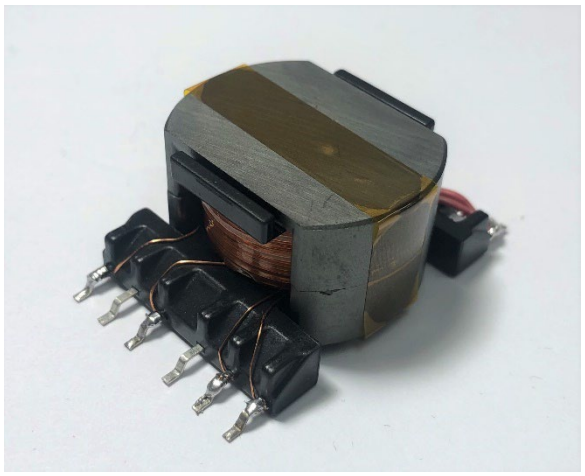
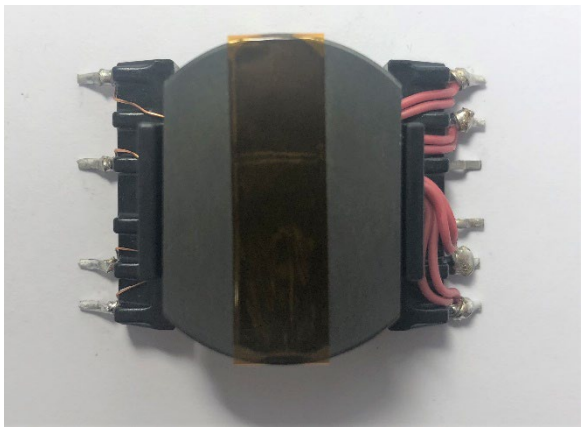
WD1 (Pri)		Continue winding the primary wire. Wind the primary winding's second layer, 27 turns from right to left. Spread the winding evenly along the bobbin's width. Do not terminate yet.
WD3 (VOUT)	 	Use 2 x #22 AWG T22A01PXXX-3. Start on PIN 12. Wind the secondary winding's first layer, 4 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.

WD2 (Bias)	 	No additional turns. Terminate bias winding at PIN 6 by laying it flat across the bobbin's width. Secure using 1 layer of tape.
WD1 (Pri)		Continue winding the primary wire. Wind the primary winding's third layer, 13 turns from left to right. Spread the winding evenly along the bobbin's width. Do not terminate yet.

WD3 (VOUT)	  	Use another 2 x #22 AWG T22A01PXXX-3. Start on PIN 11 Wind the additional secondary winding layer, 4 turns from left to. Spread the winding evenly along the bobbin's width. Do not terminate yet. Secure using 1 layer of tape.

WD1 (Pri)		Continue winding the primary wire. Wind the primary winding's fourth layer, 13 turns from right to left. Spread the winding evenly along the bobbin's width. Do not terminate yet.
WD3 (VOUT)	 	Continue winding the secondary wire. Combining the 4 wires of the secondary winding, wind 2 turns from right to left. Spread the winding evenly along the bobbin's width. Secure using 1 layer of tape. Terminate secondary winding at PINs 7 and 8. *PIN 7 and 8 can be interchanged since they are shorted on the PCB*

WD1 (Pri)	 	Continue winding the primary wire. Wind the primary winding's fifth layer, 13 turns from left to right. Spread the winding evenly along the bobbin's width. Continue winding the primary wire for the final layer, 13 turns from right to left. Spread the winding evenly along the bobbin's width. Secure using 2 layers of tape. Terminate the primary winding at PIN 1.

Finishing	  	Cut and solder the wires. Mount the gapped core using glue (a 0.375” polyester film electrical tape can be used as an alternative). Remove pins 2 and 4.

8 Transformer Design Spreadsheet

1	DCDC_InnoSwitch3AQ_Flyback_031423; Rev.3.5; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-AQ Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VOUT	13.50		13.50	V	Output Voltage
4	**OPERATING CONDITION 1**					
5	VINDC1	900.00		900.00	V	Input DC voltage 1
6	IOUT1	6.370		6.370	A	Output current 1
7	POUT1		Info	86.00	W	The device is capable of delivering 70W at the specified input voltage. Verify thermal performance.
8	EFFICIENCY1			0.85		Converter efficiency for output 1
9	Z_FACTOR1			0.50		Z-factor for output 1
11	**OPERATING CONDITION 2**					
12	VINDC2	300.00		300.00	V	Input DC voltage 3
13	IOUT2	6.370		6.370	A	Output current 3
14	POUT2		Info	86.00	W	The device is capable of delivering 70W at the specified input voltage. Verify thermal performance.
15	EFFICIENCY2			0.85		Converter efficiency for output 3
16	Z_FACTOR2			0.50		Z-factor for output 3
69	**PRIMARY CONTROLLER SELECTION**					
70	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
71	VDRAIN_BREAKDOWN	1700		1700	V	Device breakdown voltage
72	DEVICE_GENERIC			INN39X9		Device selection
73	DEVICE_CODE	INN3949CQ		INN3949CQ		Device code
74	PDEVICE_MAX			70	W	Device maximum power capability
75	RDSON_25DEG			0.62	Ω	Primary switch on-time resistance at 25°C
76	RDSON_125DEG			1.10	Ω	Primary switch on-time resistance at 125°C
77	ILIMIT_MIN			1.767	A	Primary switch minimum current limit
78	ILIMIT_TYP			1.900	A	Primary switch typical current limit
79	ILIMIT_MAX			2.033	A	Primary switch maximum current limit
80	VDRAIN_ON_PRSW			0.34	V	Primary switch on-time voltage drop
81	VDRAIN_OFF_PRSW			1170	V	Peak drain voltage on the primary switch during turn-off
85	**WORST CASE ELECTRICAL PARAMETERS**					
86	FSWITCHING_MAX	35000		35000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
87	VOR	240.0		240.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
88	KP			1.025		Measure of continuous/discontinuous mode of operation
89	MODE_OPERATION			DCM		Mode of operation
90	DUTYCYCLE			0.439		Primary switch duty cycle
91	TIME_ON_MIN			4.09	us	Minimum primary switch on-time
92	TIME_ON_MAX		Info	14.37	us	Maximum primary switch on-time is greater than 11.75us: Increase the controller switching frequency or increase the VOR
93	TIME_OFF			16.29	us	Primary switch off-time
94	LPRIMARY_MIN			2530.7	uH	Minimum primary magnetizing inductance
95	LPRIMARY_TYP			2663.9	uH	Typical primary magnetizing inductance
96	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
97	LPRIMARY_MAX			2797.1	uH	Maximum primary magnetizing inductance
99	**PRIMARY CURRENT**					
100	IAVG_PRIMARY			0.312	A	Primary switch average current
101	IPEAK_PRIMARY			1.575	A	Primary switch peak current

102	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
103	IRIPPLE_PRIMARY			1.575	A	Primary switch ripple current
104	IRMS_PRIMARY			0.573	A	Primary switch RMS current
108	**TRANSFORMER CONSTRUCTION PARAMETERS**					
109	**CORE SELECTION**					
110	CORE	POT33/19		POT33/19		Core selection
111	CORE NAME			POT33/19-JP95		Core code
112	AE			147.4	mm^2	Core cross sectional area
113	LE			51.0	mm	Core magnetic path length
114	AL			5500	nH	Ungapped core effective inductance per turns squared
115	VE			7517	mm^3	Core volume
116	BOBBIN NAME			POT33/19		Bobbin name
117	AW			49.4	mm^2	Bobbin window area - only the bobbin width and height are used to assess fit by the magnetics builder
118	BW			10.50	mm	Bobbin width
119	BH			4.70	mm	Bobbin height
120	MARGIN			0.0	mm	Bobbin safety margin
122	**PRIMARY WINDING**					
123	NPRIMARY			106		Primary winding number of turns
124	BPEAK			3725	Gauss	Peak flux density
125	BMAX			2756	Gauss	Maximum flux density
126	BAC			1378	Gauss	AC flux density (0.5 x Peak to Peak)
127	ALG			237	nH	Typical gapped core effective inductance per turns squared
128	LG			0.748	mm	Core gap length
130	**SECONDARY WINDING**					
131	NSECONDARY	6		6		Secondary winding number of turns
133	**BIAS WINDING**					
134	NBIAS			5		Bias winding number of turns
138	**PRIMARY COMPONENTS SELECTION**					
139	**LINE UNDERVOLTAGE/OVERVOLTAGE**					
140	UVOV Type	UV Only		UV Only		Input Undervoltage/Overvoltage protection type
141	**UNDERVOLTAGE PARAMETERS**					
142	BROWN-IN REQUIRED	30.00		30.00	V	Required DC bus brown-in voltage threshold
143	UNDERVOLTAGE ZENER DIODE	BZM55C9V1		BZM55C9V1		Undervoltage protection zener diode
144	VZ			9.10	V	Zener diode reverse voltage
145	VR			6.80	V	Zener diode reverse voltage at the maximum reverse leakage current
146	ILKG			2.00	uA	Zener diode maximum reverse leakage current
147	BROWN-IN ACTUAL			22.99 - 29.55	V	Actual brown-in voltage range using standard resistors
148	BROWN-OUT ACTUAL			19.76 - 26.44	V	Actual brown-out voltage range using standard resistors
149	**OVERVOLTAGE PARAMETERS**					
150	OVERVOLTAGE REQUIRED		Info		V	For UV Only design, overvoltage feature is disabled
151	OVERVOLTAGE DIODE		Info			OV diode is used only for the overvoltage protection circuit
152	VF				V	OV diode forward voltage
153	VRRM				V	OV diode reverse voltage
154	PIV				V	OV diode peak inverse voltage
155	LINE_OVERVOLTAGE				V	For UV Only design, line overvoltage feature is disabled
156	**DC BUS SENSE RESISTORS**					
157	RLS_H			0.70	MΩ	Connect five 140 kOhm DC bus upper sense resistors to the V-pin for the required UV/OV threshold

158	RLS_L			261	kΩ	DC bus lower sense resistor to the V-pin for the required UV/OV threshold
161	**BIAS WINDING**					
162	VBIAS			9.00	V	Rectified bias voltage
163	VF_BIAS			0.70	V	Bias winding diode forward drop
164	VREVERSE_BIASDIODE			51.45	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
165	CBIAS			22	uF	Bias winding rectification capacitor
166	CBPP			0.47	uF	BPP pin capacitor
170	**SECONDARY COMPONENTS SELECTION**					
171	**FEEDBACK COMPONENTS**					
172	RFB_UPPER			100.00[10]	kΩ	Upper feedback resistor (connected to the output terminal)
173	RFB_LOWER			10.20	kΩ	Lower feedback resistor
174	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
178	**MULTIPLE OUTPUT PARAMETERS**					
179	**OUTPUT 1**					
180	VOUT1			13.50	V	Output 1 voltage
181	IOUT1	6.370		6.370	A	Output 1 current
182	POUT1			86.00	W	Output 1 power
183	IRMS_SECONDARY1			11.306	A	Root mean squared value of the secondary current for output 1
184	IRIPPLE_CAP_OUTPUT1			9.340	A	Current ripple on the secondary waveform for output 1
185	NSECONDARY1			6		Number of turns for output 1
186	VREVERSE_RECTIFIER1			64.44	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
187	SRFET1	DMT12H007LPS-13		DMT12H007LPS-13		Secondary rectifier (Logic MOSFET) for output 1
188	VF_SRFET1			0.80	V	SRFET on-time drain voltage for output 1
189	VBREAKDOWN_SRFET1			120	V	SRFET breakdown voltage for output 1
190	RDSON_SRFET1			14	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
218	PO_TOTAL			86.00	W	Total power of all outputs

Table 7 – DER-952Q PIXls Spreadsheet.

[10] Actual value implemented on the unit is 110 kΩ as requirement for implementing the *Precision Voltage Regulator* circuit.

9 Performance data

Note: 1. Measurements were taken with the unit under test set-up inside a thermal chamber in a high-voltage (HV) safety room.

Figure 17 – High-Voltage Test Set-up.

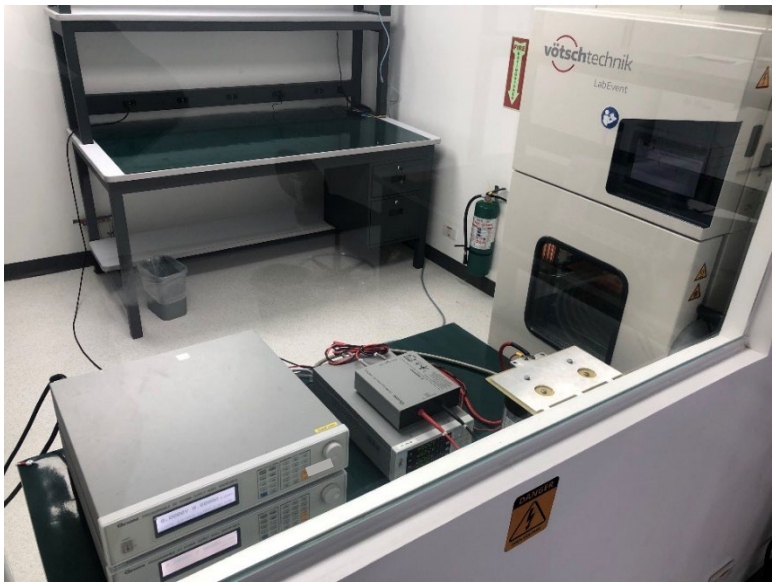


Figure 18 – Test Set-up Inside the High-Voltage Room.

2. Unit under test was placed under a box inside the thermal chamber to eliminate the effects of airflow.

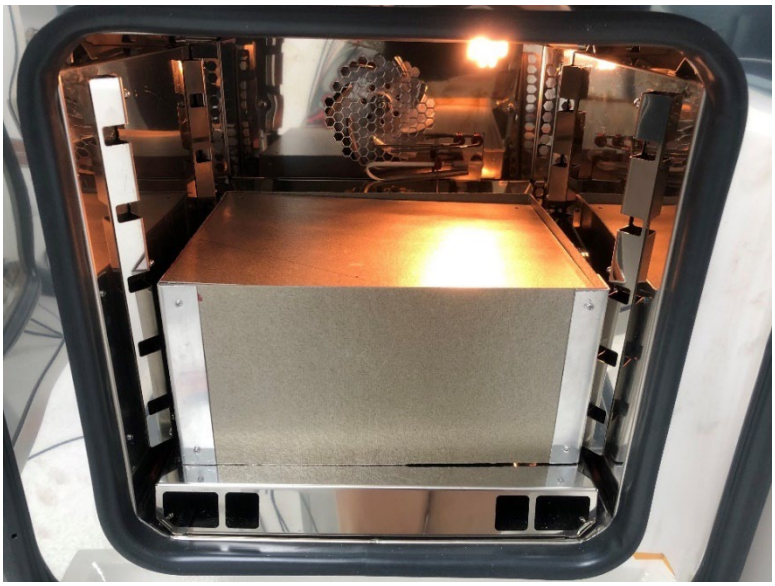


Figure 19 – Unit Under Test Placed Under a Box to Eliminate the Effect of Airflow.

3. Unit under test was soaked for 5 minutes at full load condition with every change in the input voltage during the start of every test sequence. For every loading condition, the unit under test was soaked for at least 1 min before measurements were taken.

4. List of equipment used for testing

Equipment Type	Model Number	Specifications	Manufacturer
Power Supply	62024P-600-8	600 V/8 A/2400 W DC PSU	Chroma
Power Supply	HP20 757 152	2kV/750 mA/1.5 kW	Iseg
Electronic Load	DL3021	150 V/40A/200W DC ELOAD	Rigol
Electronic Load	PEL-2020A	80V/20A/100W DC ELOAD	GW Instek
Power Meter	66205	600 V/30A 10kHz Digital Meter	Chroma
Power Meter	WT310E	600 V/20 A 100kHz Digital Meter	Yokogawa
Current Meter	DMM-4050	Precision Multimeter	Tektronix
High Voltage Measurement	TT-SI 9010A	70 MHz 7000 V Differential Probe	Testec
High Voltage Measurement	TT-SI 9110	100 MHz 1400 V Differential Probe	Testec
Low Voltage Measurement	701937	500 MHz 600 V Passive Probe	Yokogawa
Output Current Measurement	701928	100 MHz 30 A_{rms} Current Probe	Yokogawa
Component Current Measurement	CWTUM/015/B	30 MHz 30 A_{peak} Rogowski Coil	CWT
Component Current Measurement	CWTUM/06/R	30 MHz 120 A_{peak} Rogowski Coil	CWT
Thermocouple Measurement	GL840	20 channel Data Logger	Graphtec
Thermal Image	TiX580	1000°C Thermal Imagin Camera	Fluke
Oscilloscope	DLM5058	2.5GS/s 500MHz Mixed Signal	Yokogawa

9.1 No-Load Input Power

Figure 20 shows the test set-up diagram for no-load input current acquisition. The voltage metering point is placed before the ammeter; this is done to prevent the voltage-sensing bias current from affecting the input current measurement. The ammeter used was Chroma Digital Power Meter 66205.

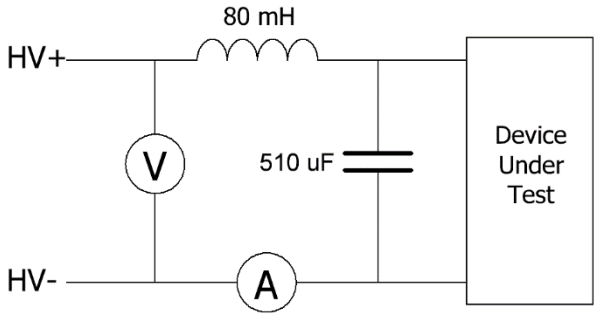


Figure 20 – No-Load Input Power Measurement Diagram.

The unit was soaked for ten minutes before starting data averaging fifty thousand samples over one minute. Analog filtering is also enabled to improve measurement accuracy.

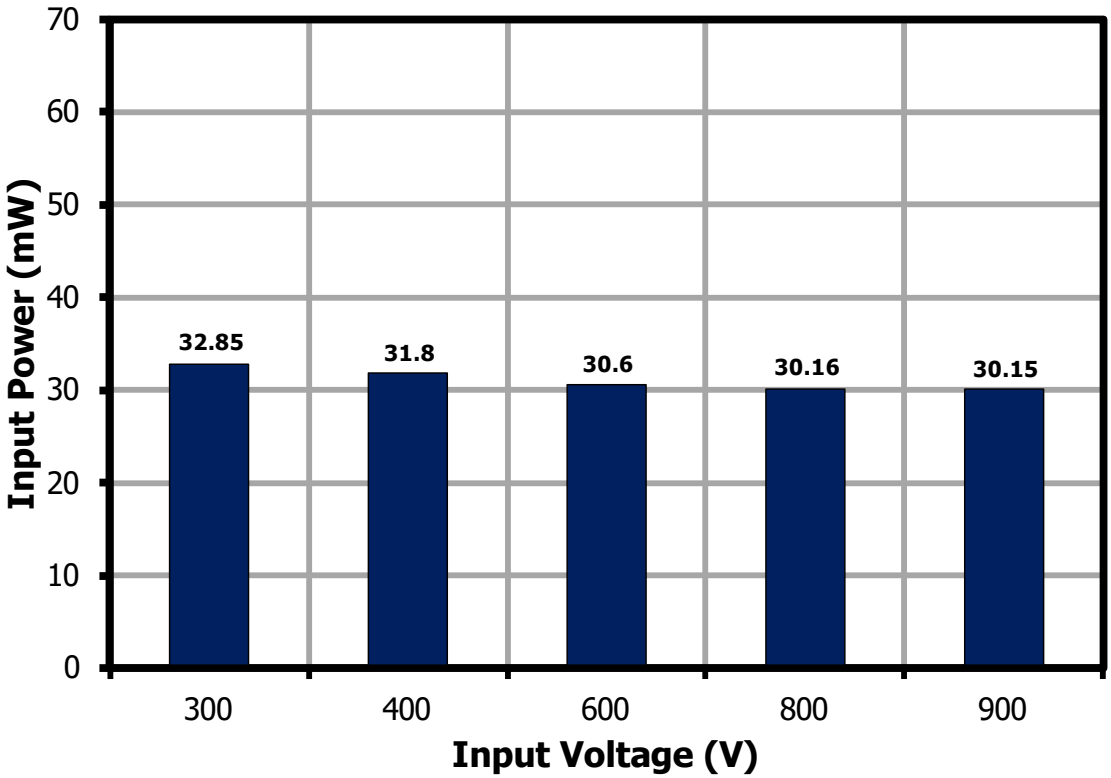


Figure 21 – No-Load Input Power vs. Input Voltage (25 °C Ambient).

9.2 Efficiency

9.2.1 Line Efficiency

Line efficiency describes how input voltage affects the unit's overall efficiency. The points in the graph are taken from 100% load conditions.

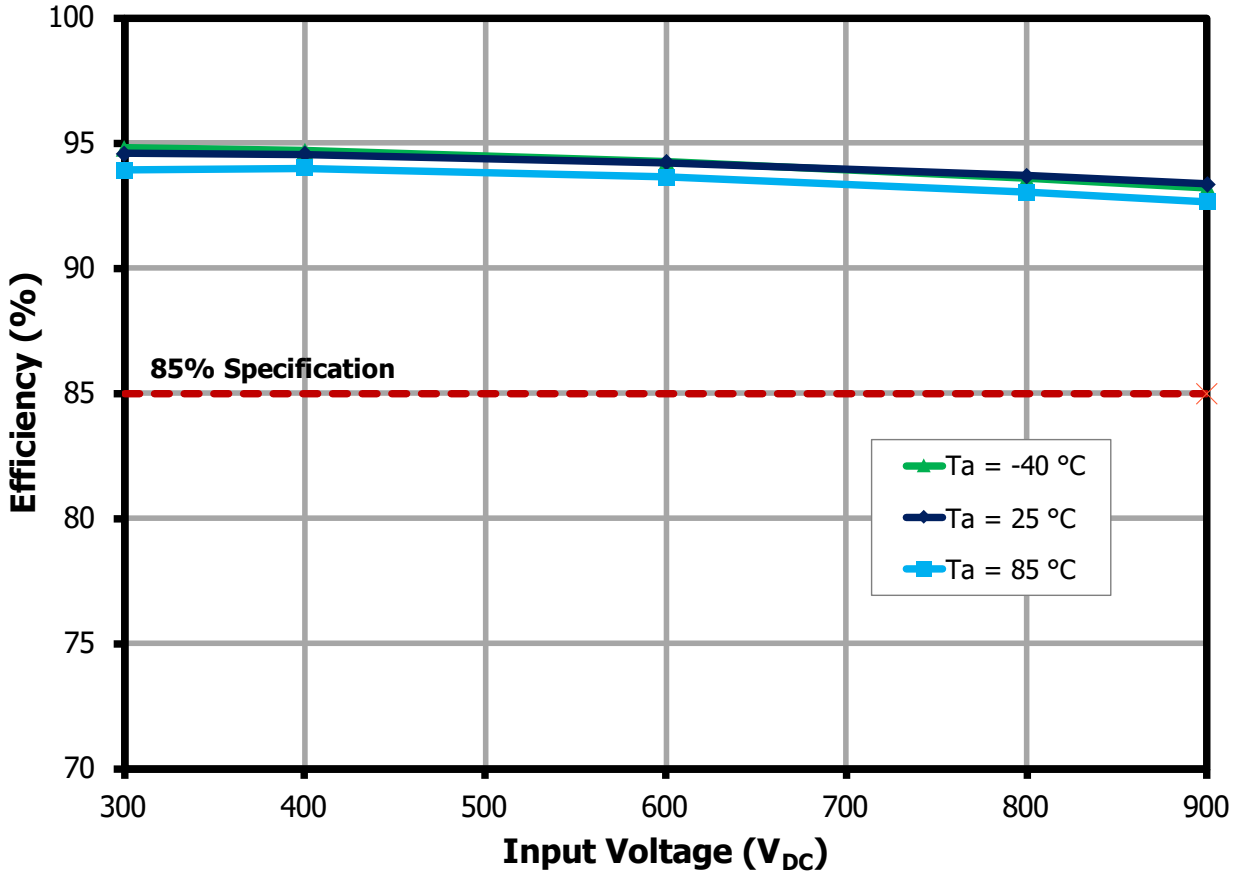


Figure 22 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 Load Efficiency

Load efficiency describes how the change in output loading conditions affects the unit's overall efficiency.

9.2.2.1 Load Efficiency at 85 °C Ambient

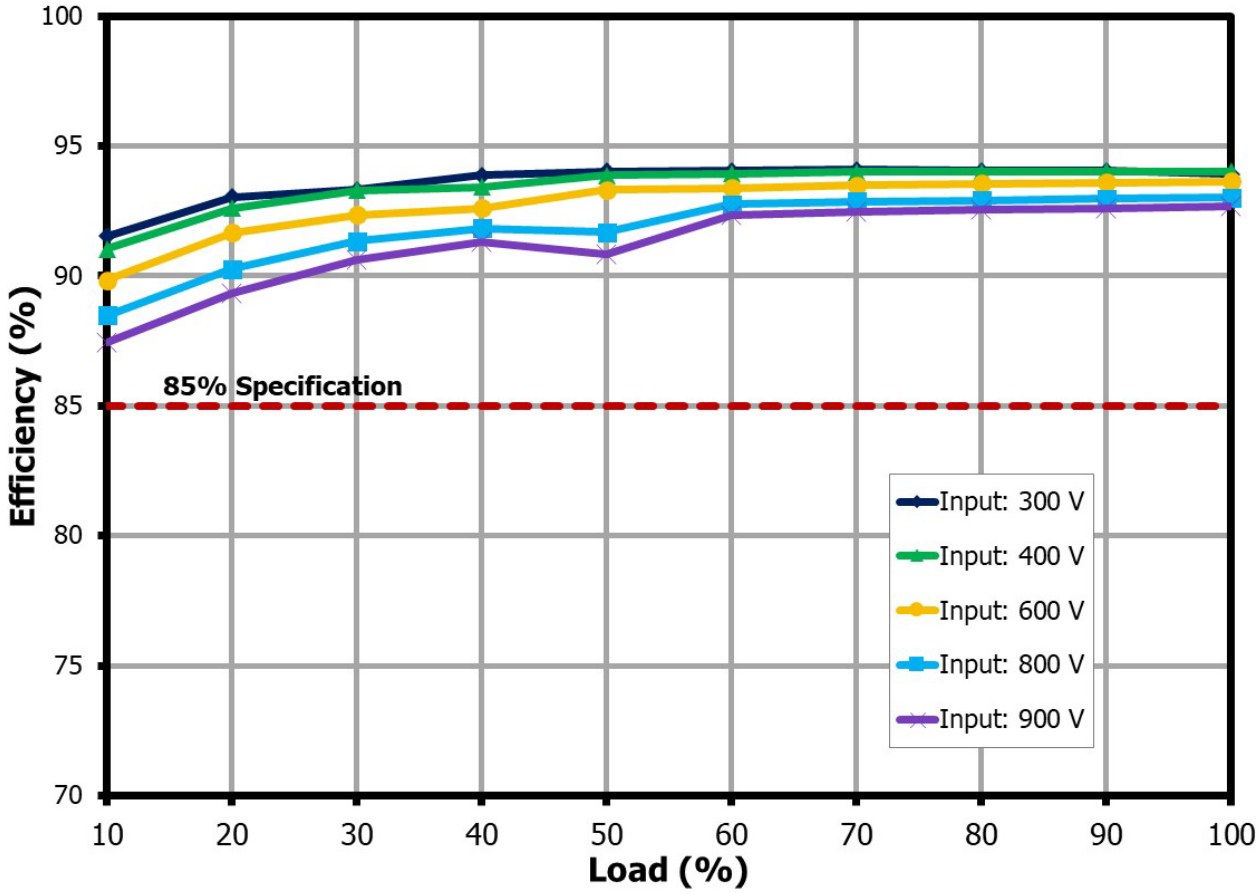


Figure 23 – Efficiency vs. Load at Different Input Voltages (85 °C Ambient).

9.2.2.2 Load Efficiency at 25 °C Ambient

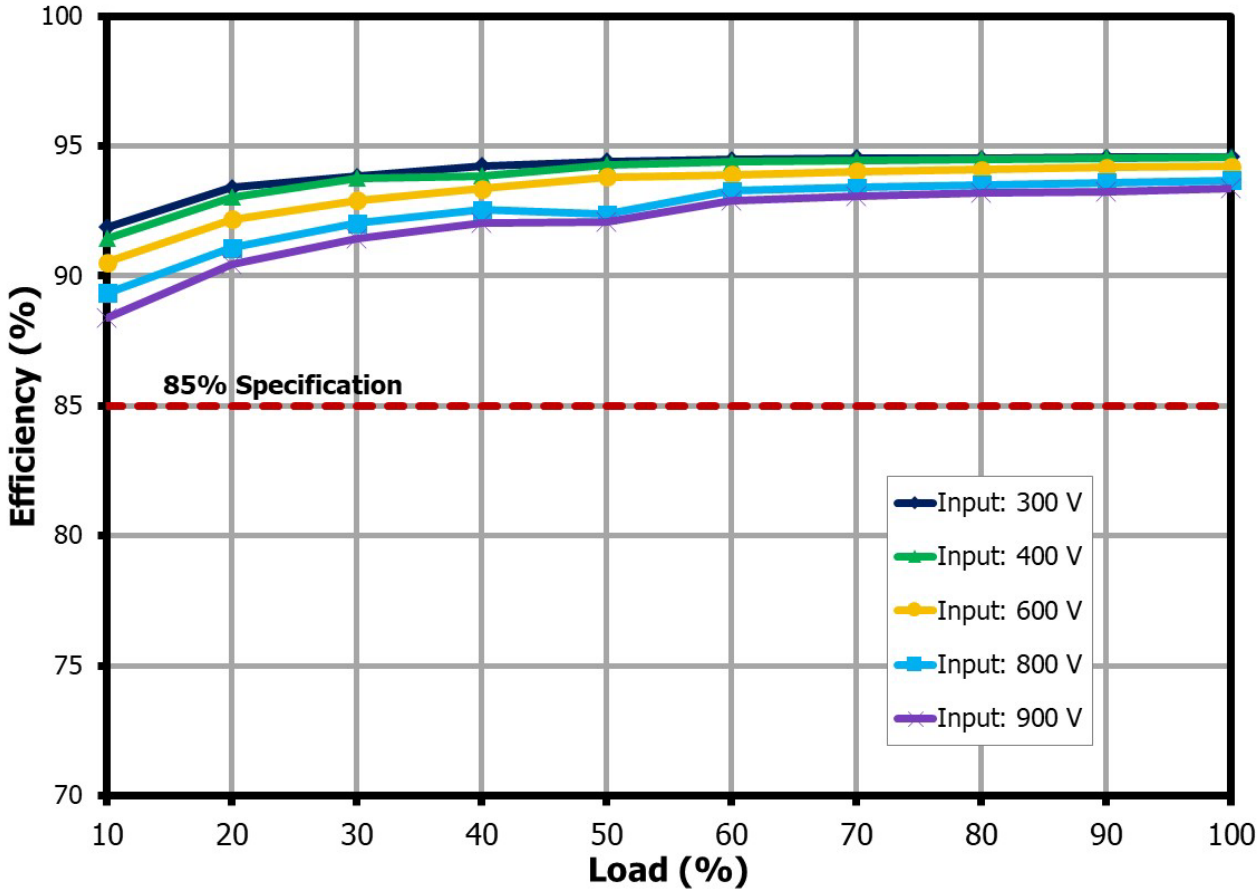


Figure 24 – Efficiency vs. Load at Different Input Voltages (25 °C Ambient).

9.2.2.3 Load Efficiency at -40 °C Ambient

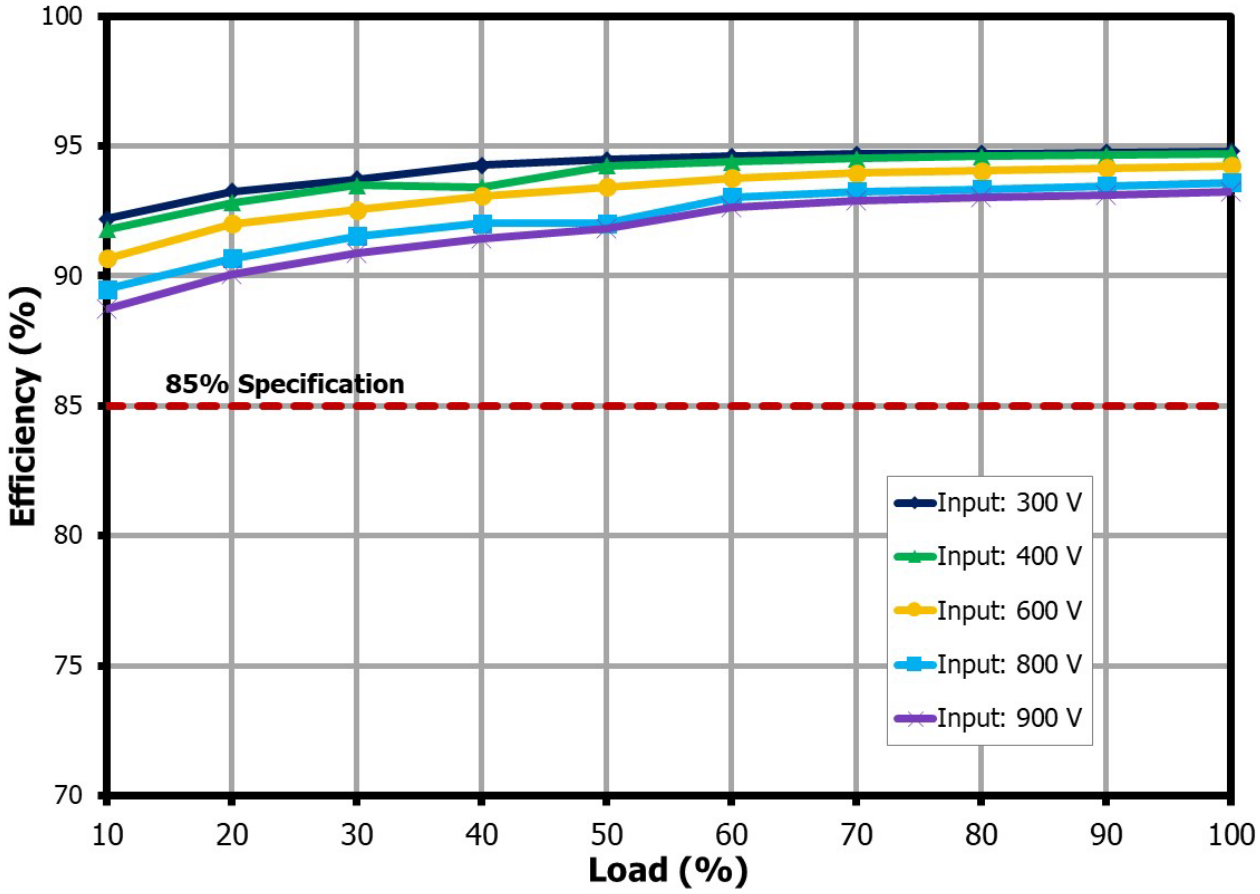


Figure 25 – Efficiency vs. Load at Different Input Voltages (-40 °C Ambient).

9.3 Output Line and Load Regulation

9.3.1 Load Regulation

Load Regulation describes how the change in output loading conditions affects the average output voltage of the unit.

9.3.1.1 Load Regulation at 85 °C Ambient

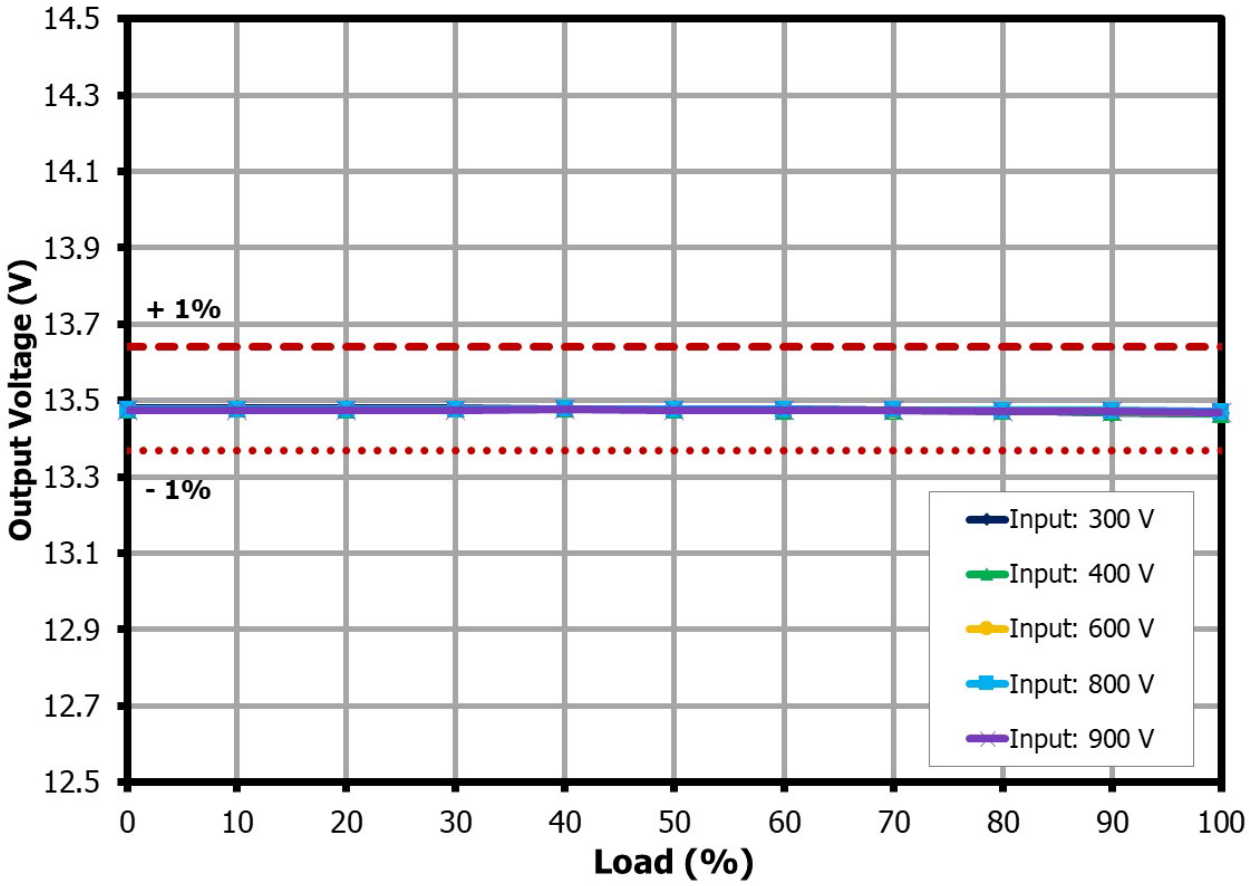


Figure 26 – Output Regulation vs. Load at Different Input Voltages (85 °C Ambient).

9.3.1.2 Load Regulation at 25 °C Ambient

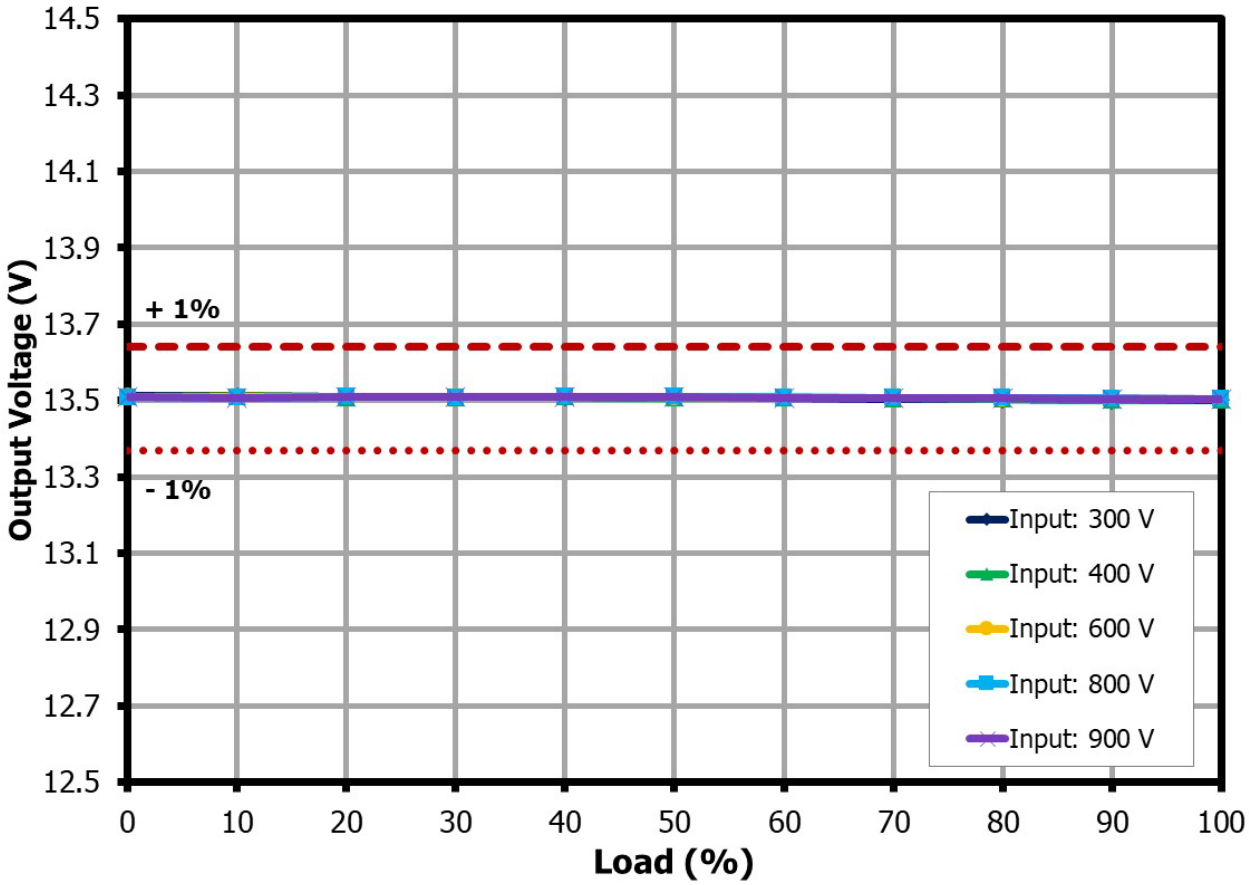


Figure 27 – Output Regulation vs. Load at Different Input Voltages (25 °C Ambient).

9.3.1.3 Load Regulation at -40 °C Ambient

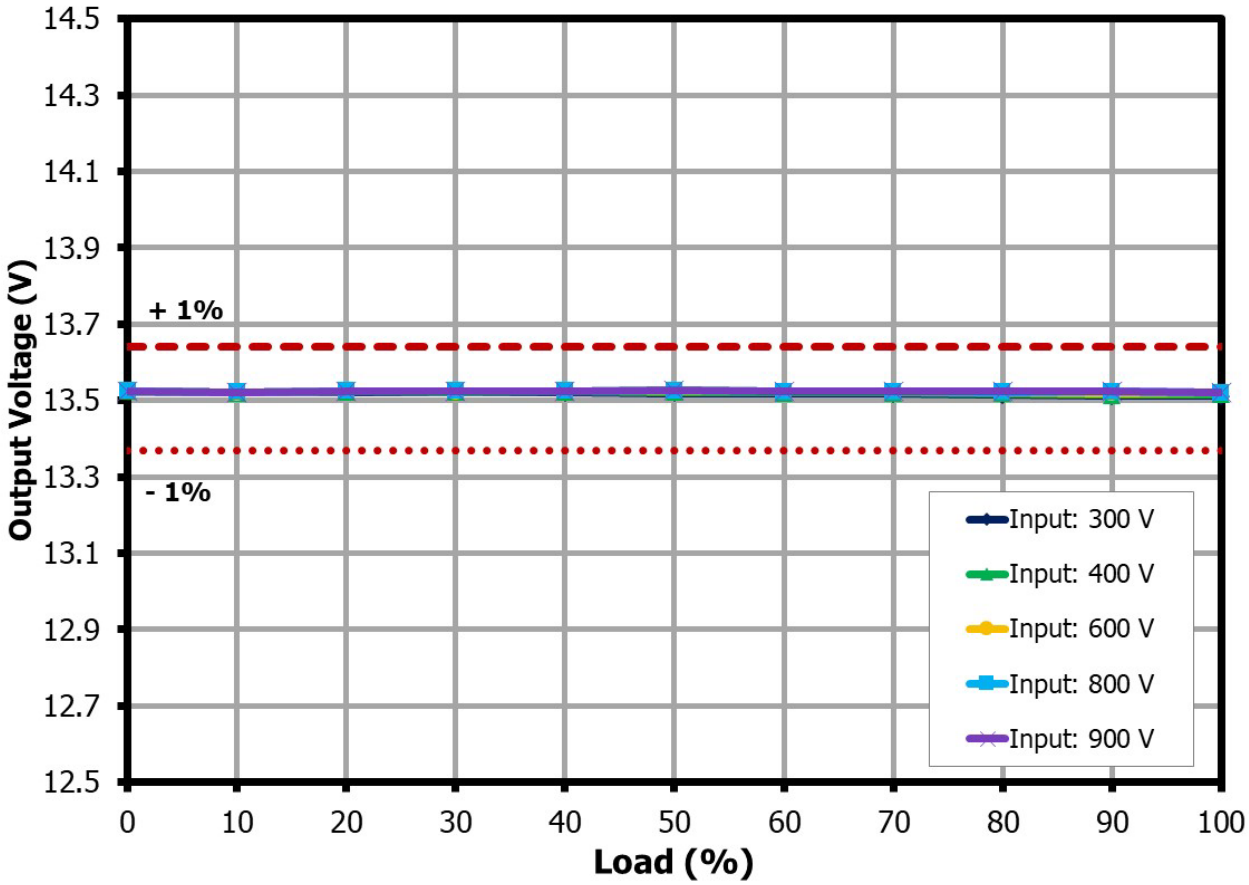


Figure 28 – Output Regulation vs. Load at Different Input Voltages (-40 °C Ambient).

9.3.2 Line Regulation

Line Regulation describes how a change in input voltage conditions affects the average output voltage of the unit. The points in the following graph are only taken from 100% load conditions.

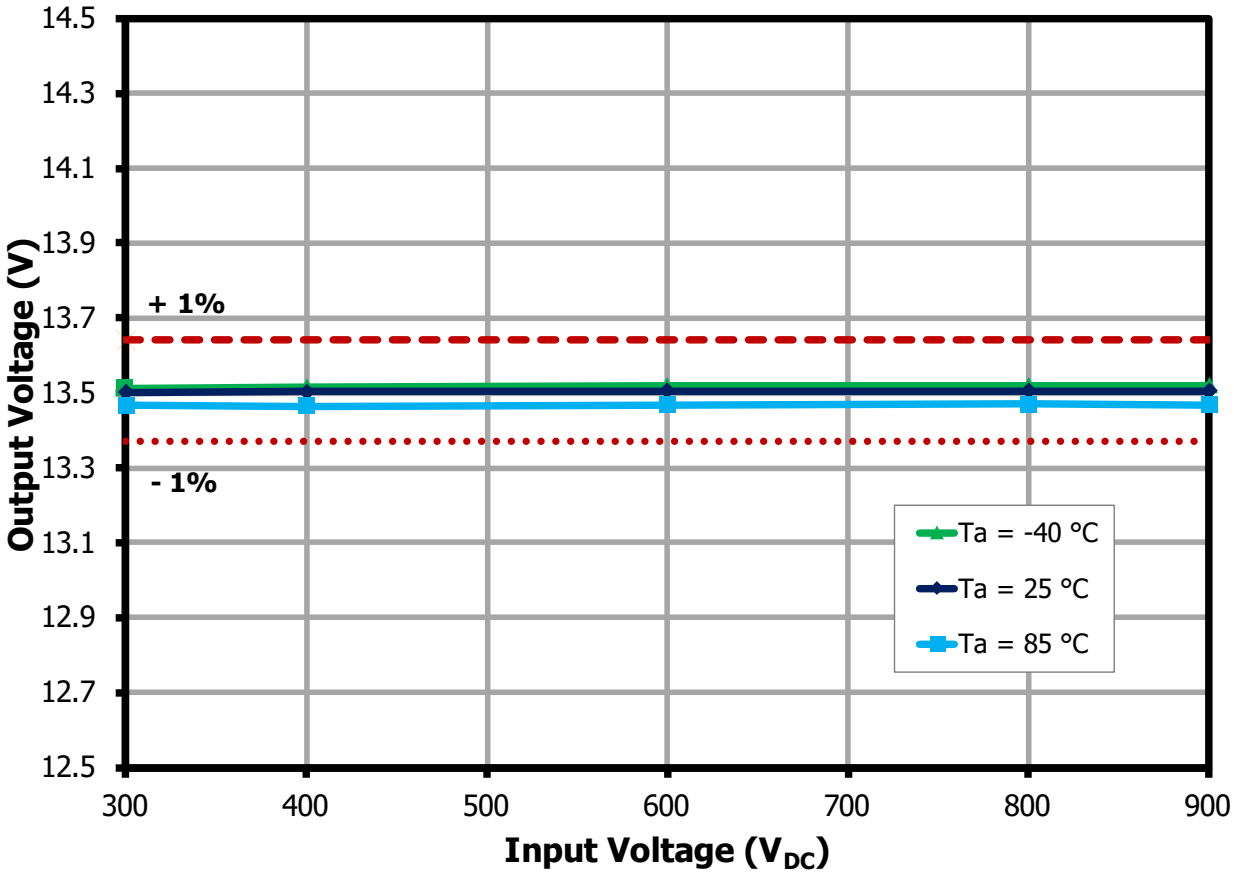


Figure 29 – Output Voltage vs Input Voltage at Full Load.

10 Thermal Performance

10.1 Thermal Data at 85 °C Ambient Temperature

The unit was placed inside a thermal chamber and soaked for at least 1 hour to allow component temperatures to settle. Figure 19 shows the setup for thermal measurement.

Critical Components	Input Voltage		
	300	800	900
InnoSwitch3-AQ (IC200)	106.85	115.4	118.55
Primary Snubber Resistor (R207)	110.6	110.35	110.3
Transformer Winding (T200)	133.75	138.4	138.55
Transformer Core (T200)	124.7	131.3	131.35
SR MOSFET (Q101)	109.25	112	111.6
SR MOSFET (Q100)	109.6	112.1	111.8
Secondary Snubber Resistor (R101)	102.8	105.3	105.3
Output Capacitor (C104)	101.35	103.35	102.15

Table 8 – Thermal Data at 85 °C at Different Input Voltages (°C).

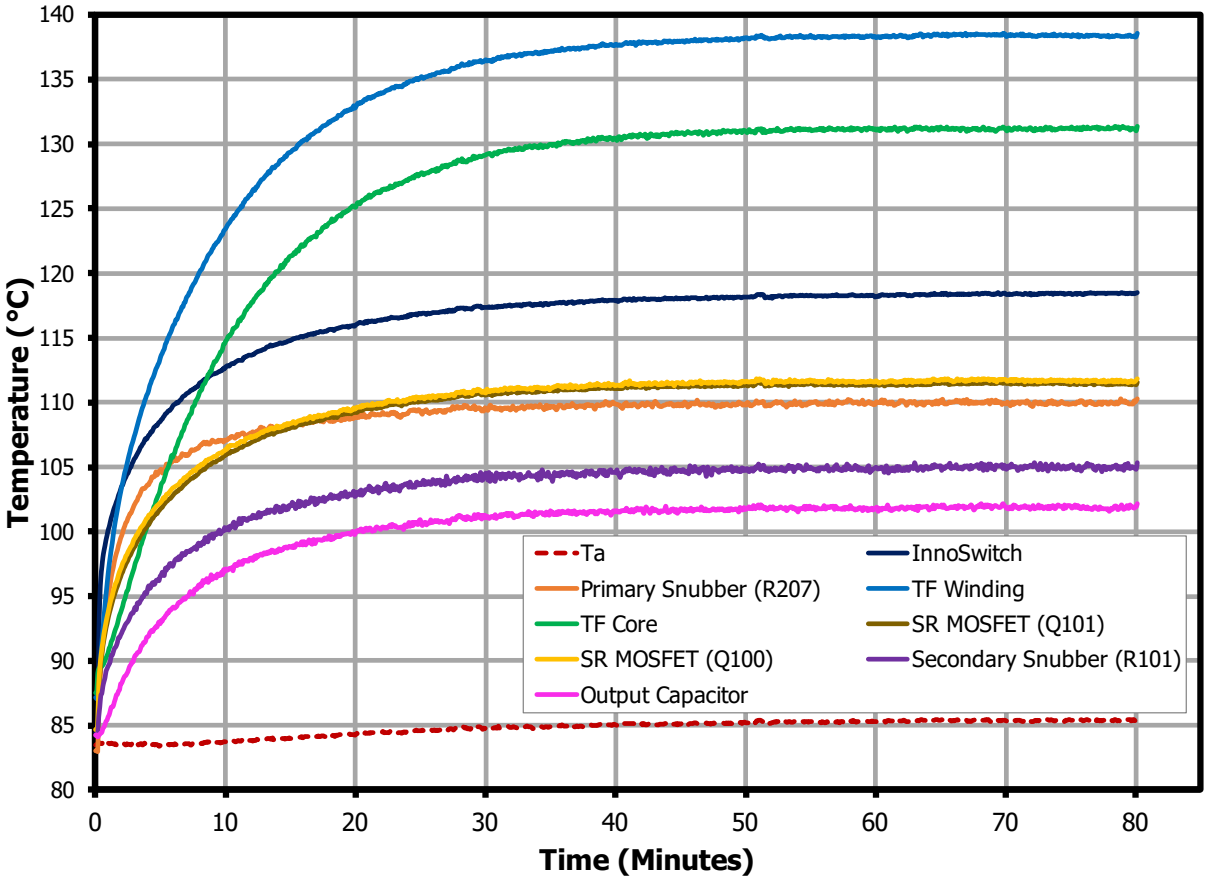


Figure 30 – Component Temperatures at 85 °C Ambient, 900 V Input.

10.2 Thermal Image Data at 25 °C Ambient Temperature

The following thermal scans are captured using a Fluke thermal imager after soaking for at least 1 hour in an enclosure to minimize the effect of airflow.

Critical Components	Input Voltage		
	300	800	900
InnoSwitch3-AQ (IC200)	48.2	58.4	62.1
Primary Snubber Resistors	57.4	56.8	56.3
Transformer (T200)	63.6	68.7	70.5
SR MOSFET (Q101)	52.3	54.8	54.3
SR MOSFET (Q100)	50.7	53.0	54.1
Secondary Snubber Resistor (R101)	45.4	48.3	49.7
Output Capacitor (C104)	45.0	45.7	46.8

Table 9 – Thermals Data at 25 °C at Different Input Voltages (°C).

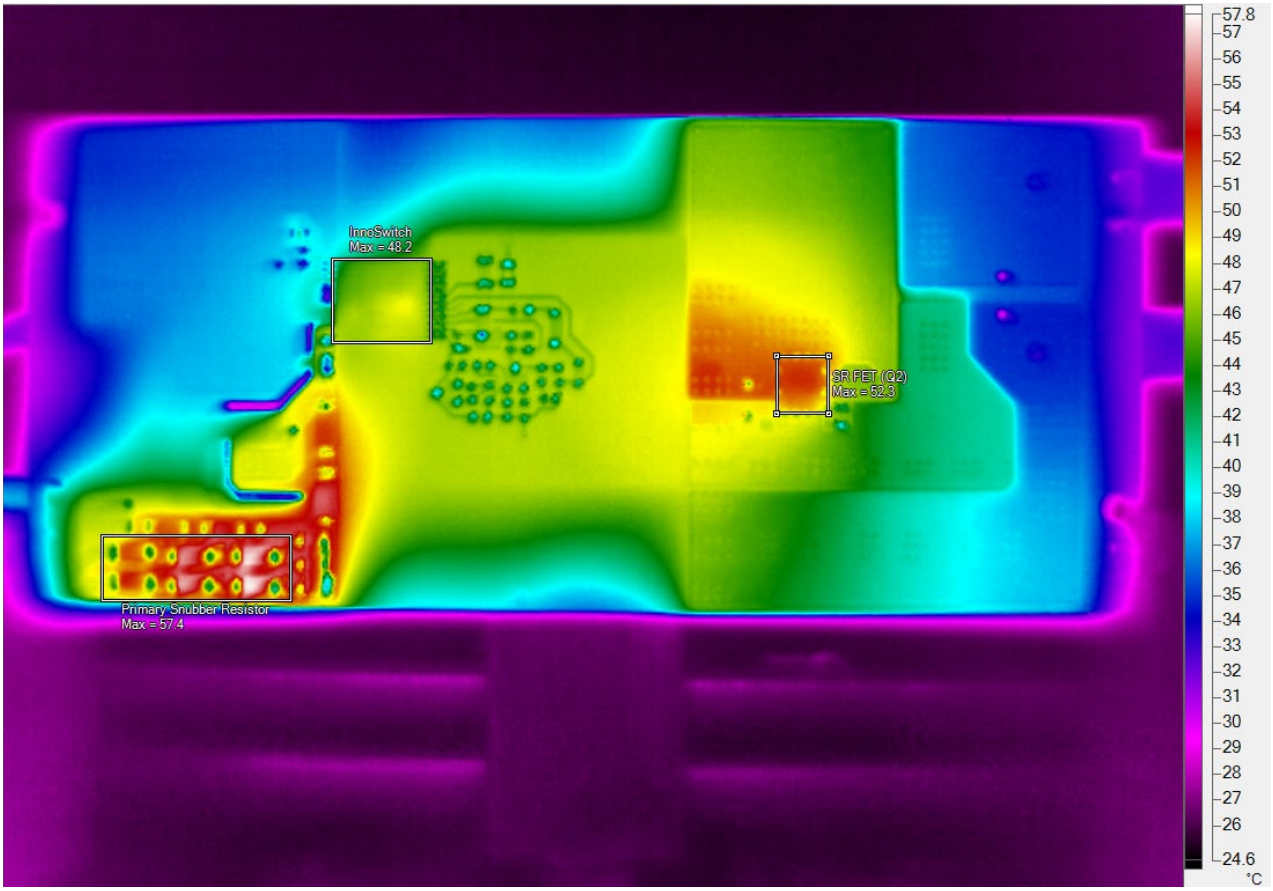


Figure 31 – PCB Bottom Thermal Scan at 300 V Input.

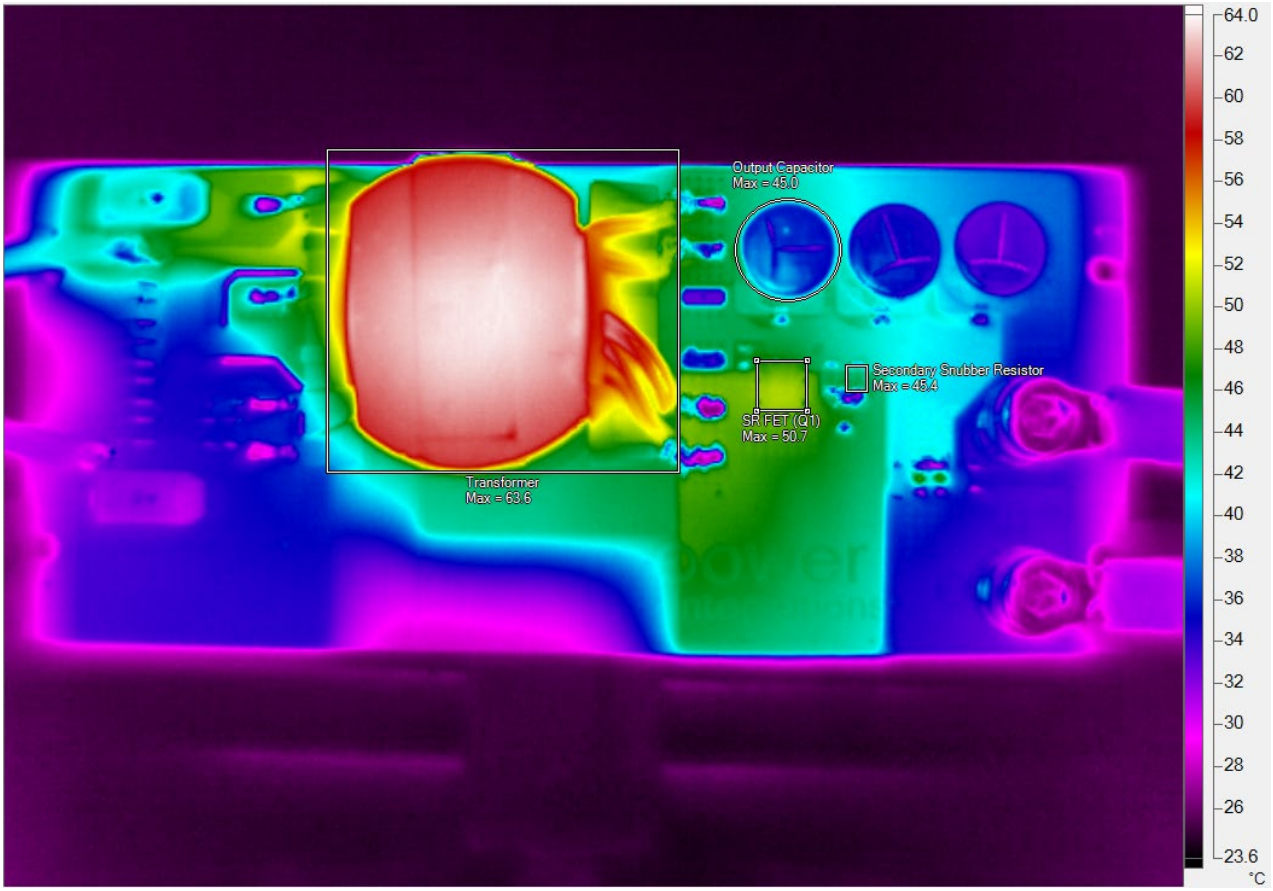


Figure 32 – PCB Top Thermal Scan at 300 V Input.

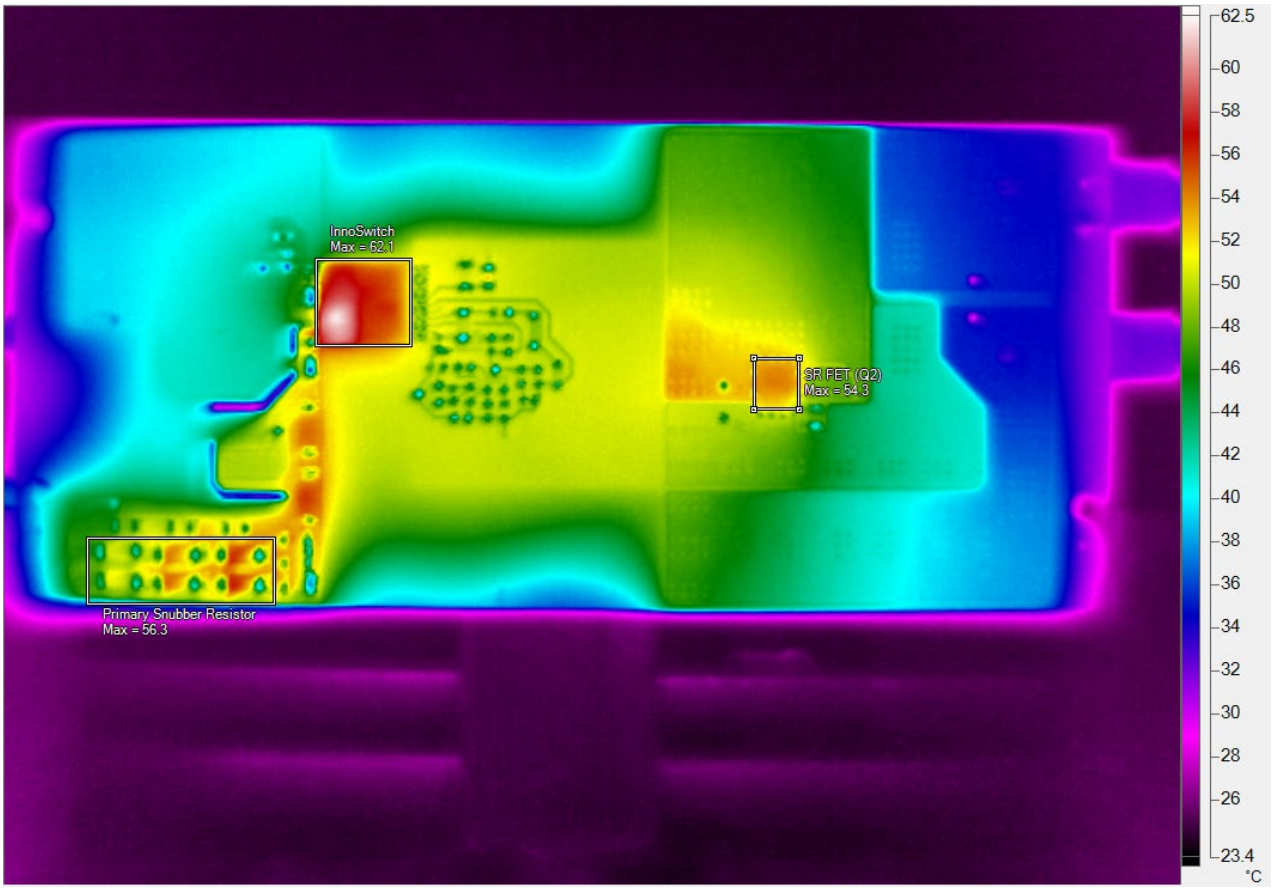


Figure 33 – PCB Bottom Thermal Scan at 900 V Input.

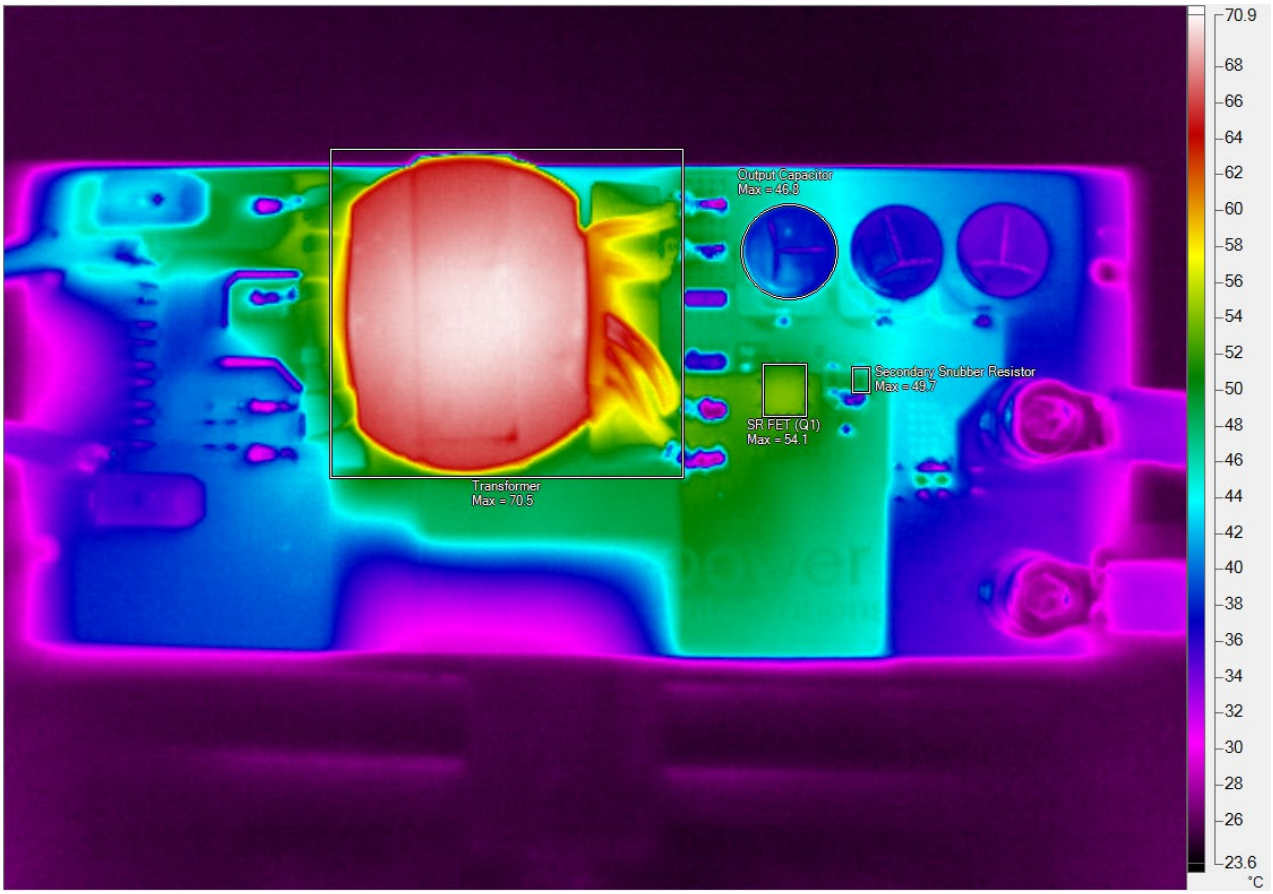


Figure 34 – PCB Top Thermal Scans at 900 V Input.

11 Waveforms

11.1 Start-Up Waveforms

The following measurements were taken by connecting the unit under test to a DC link capacitor charged[11] to different test input voltages. Constant resistance load configuration was used for all start-up tests.

11.1.1 Output Voltage and Current at 25 °C Ambient Temperature[12,13]

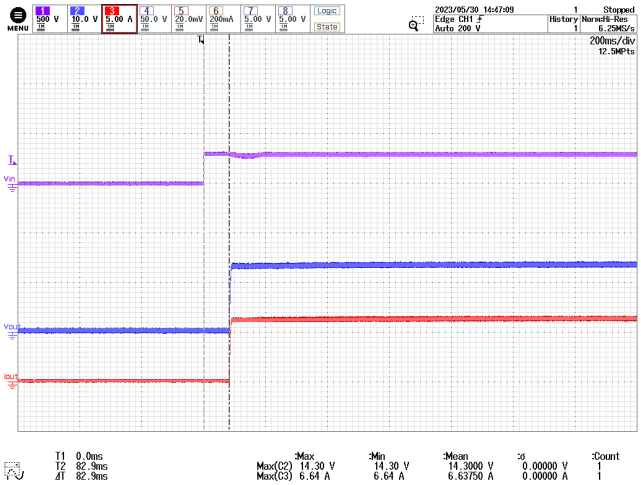


Figure 35 – Output Voltage and Current.
300 V_{DC}, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

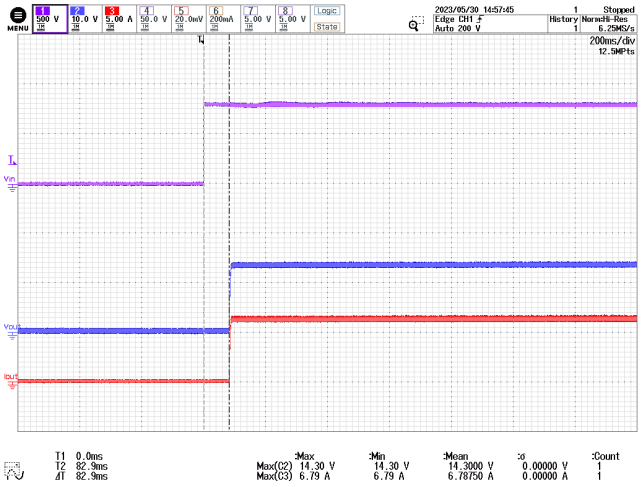


Figure 36 – Output Voltage and Current.
800 V_{DC}, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

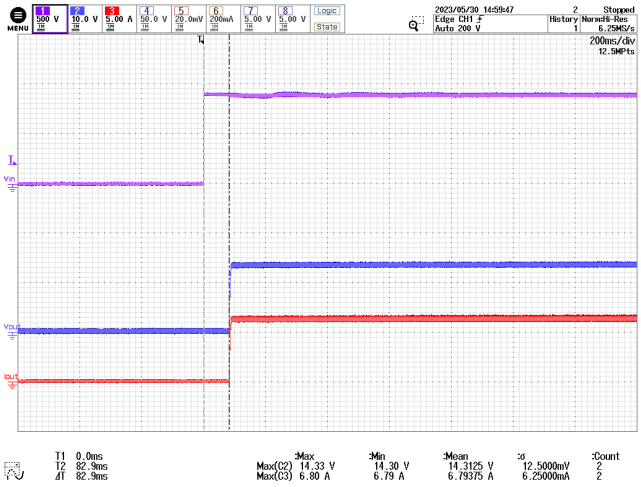


Figure 37 – Output Voltage and Current.
900 V_{DC}, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

[11] Inrush current was limited by adding a 10 Ω series resistor between the DC link capacitor and the unit under test.
[12] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[13] Current waveforms were measured using a Yokogawa current probe.

11.1.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient Temperature[14,15]

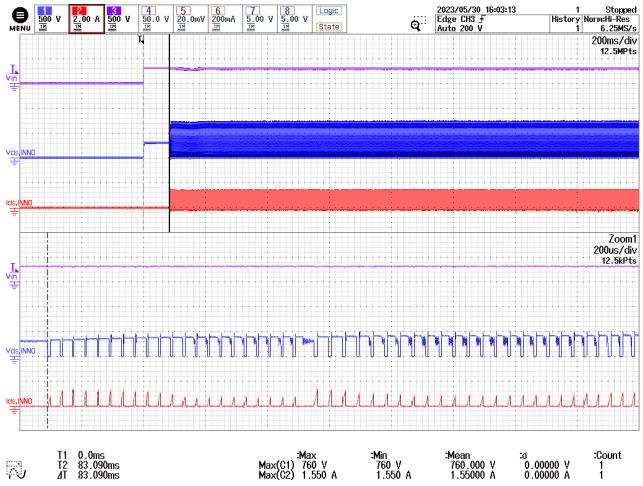


Figure 38 – INN3949CQ Drain Voltage and Current.
300 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

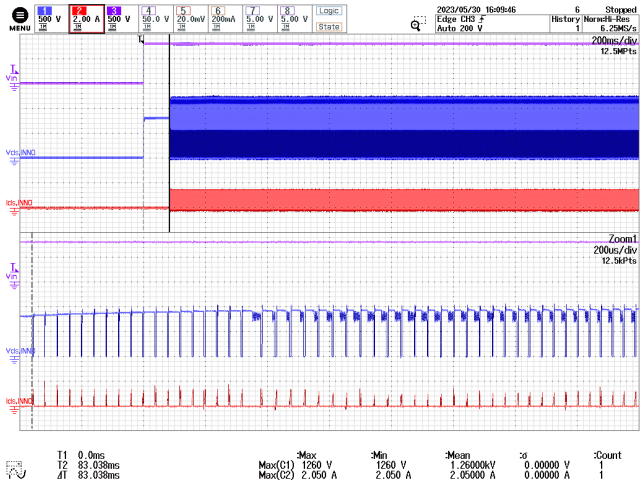


Figure 39 – INN3949CQ Drain Voltage and Current.
800 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

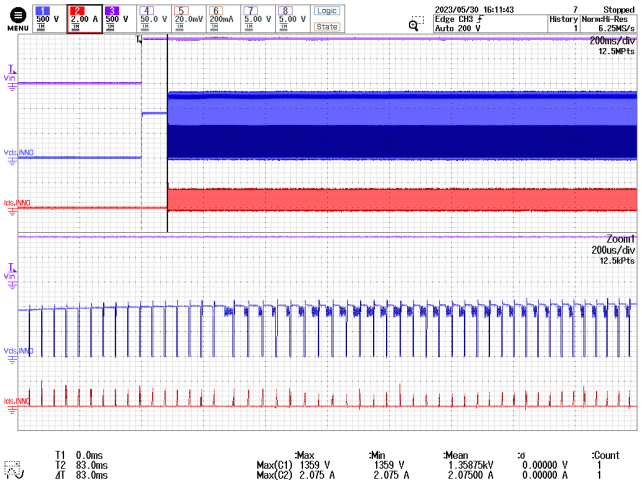


Figure 40 – INN3949CQ Drain Voltage and Current.
900 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[14] The time between when V_{IN} is turned on and the InnoSwitch starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[15] Current waveforms were measured using a Yokogawa current probe.

11.1.3 SR FET Drain Voltage and Current at 25 °C Ambient Temperature[16,17]

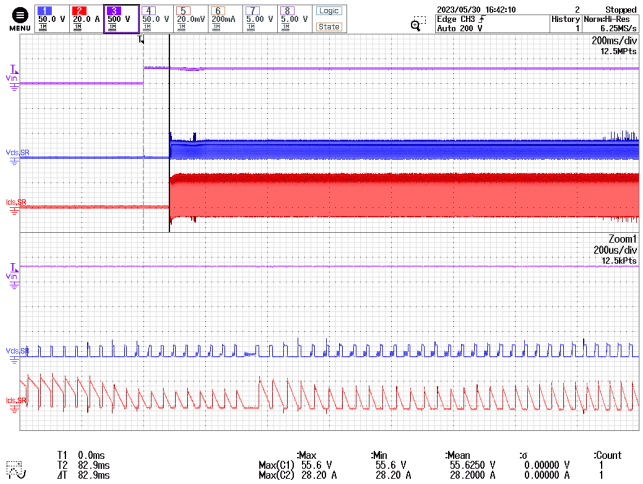


Figure 41 – SR FET Drain Voltage and Current.
300 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

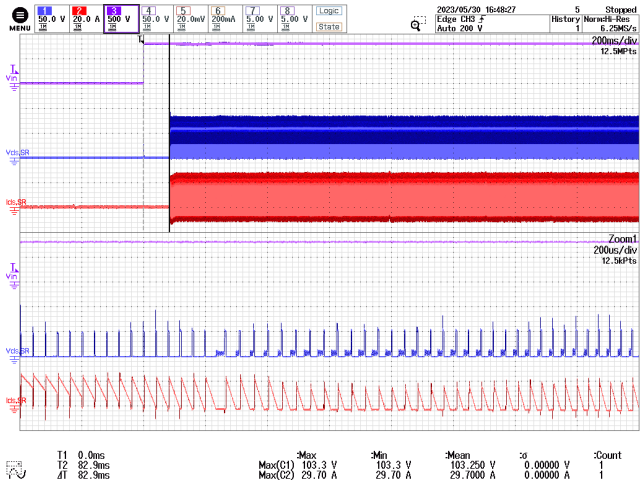


Figure 42 – SR FET Drain Voltage and Current.
800 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

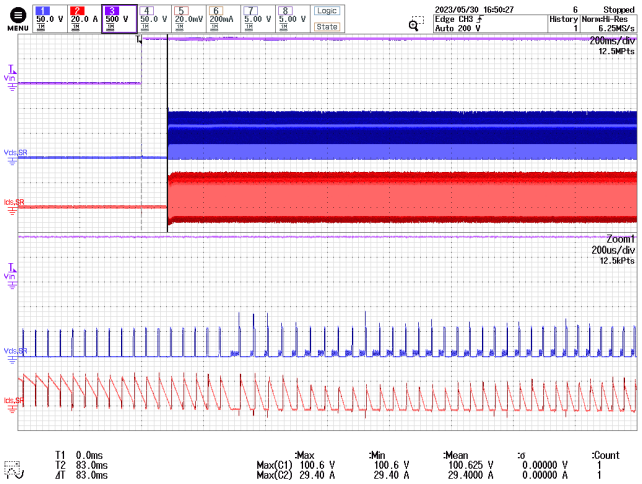


Figure 43 – SR FET Drain Voltage and Current.
900 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[16] The time between when V_{IN} is turned on and the SR FET starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[17] Current waveforms were measured using a Yokogawa current probe.

11.1.4 Output Voltage and Current at -40 °C Ambient Temperature[18,19]

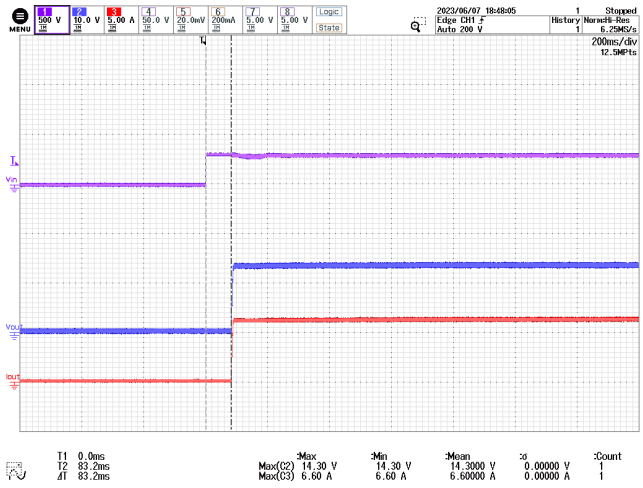


Figure 44 – Output Voltage and Current.
300 V_{DC}, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

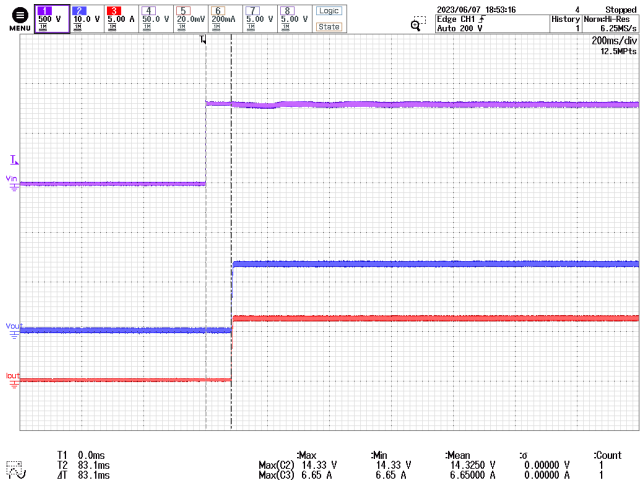


Figure 45 – Output Voltage and Current.
800 V_{DC}, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

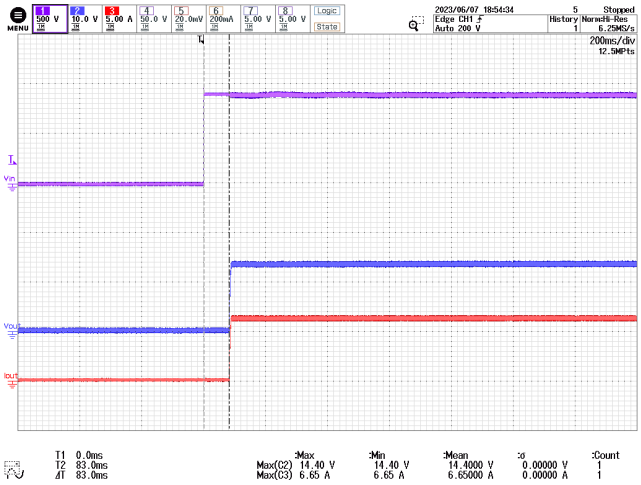


Figure 46 – Output Voltage and Current.
900 V_{DC}, 2.12 Ω Load.
CH1: V_{IN}, 500 V / div.
CH2: V_{OUT}, 10 V / div.
CH3: I_{OUT}, 5 A / div.
Time: 200 ms / div.

[18] Voltage dip on the V_{IN} waveform is due to the effective line impedance from the DC link capacitor to the unit under test.
[19] Current waveforms were measured using a Yokogawa current probe.

11.1.5 InnoSwitch3-AQ Drain Voltage and Current at -40 °C Ambient Temperature[20,21]

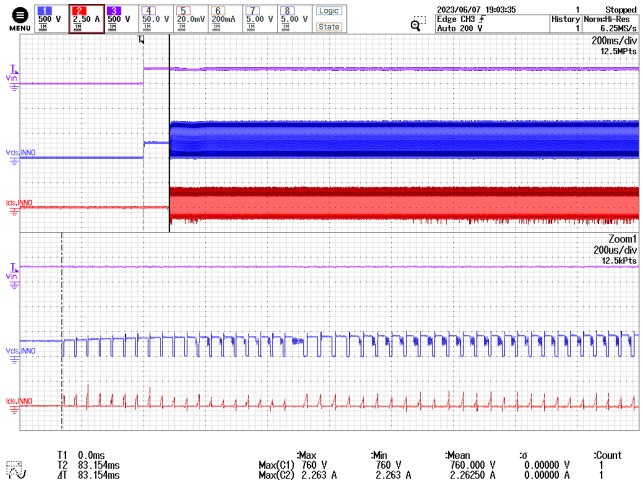


Figure 47 – INN3949CQ Drain Voltage and Current.
300 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

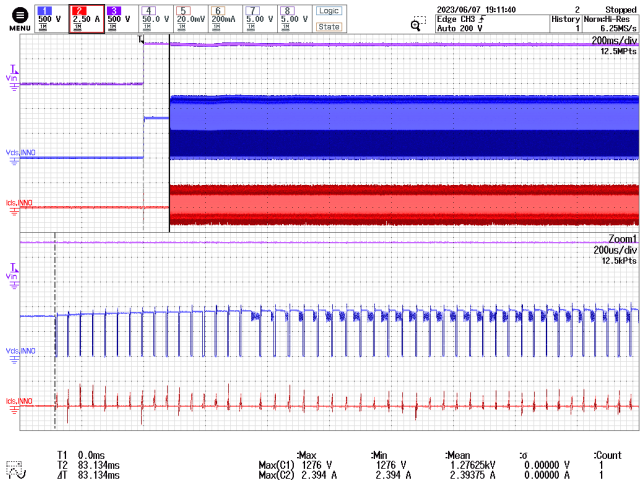


Figure 48 – INN3949CQ Drain Voltage and Current.
800 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

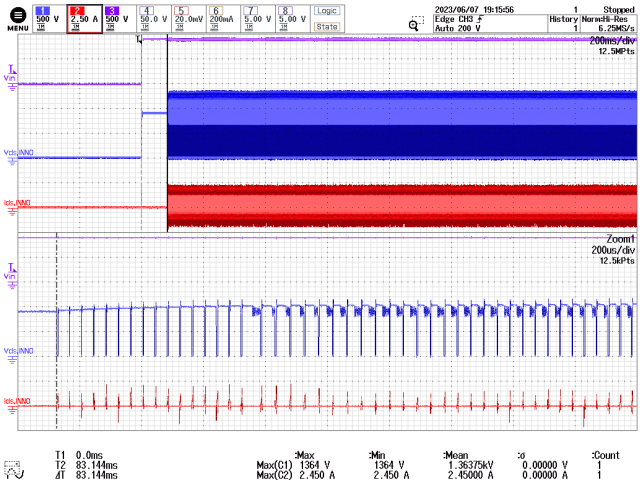


Figure 49 – INN3949CQ Drain Voltage and Current.
900 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2.50 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[20] The time between when V_{IN} is turned on and the InnoSwitch starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[21] Current waveforms were measured using a Rogowski coil.

11.1.6 SR FET Drain Voltage and Current at -40 °C Ambient Temperature[22,23]

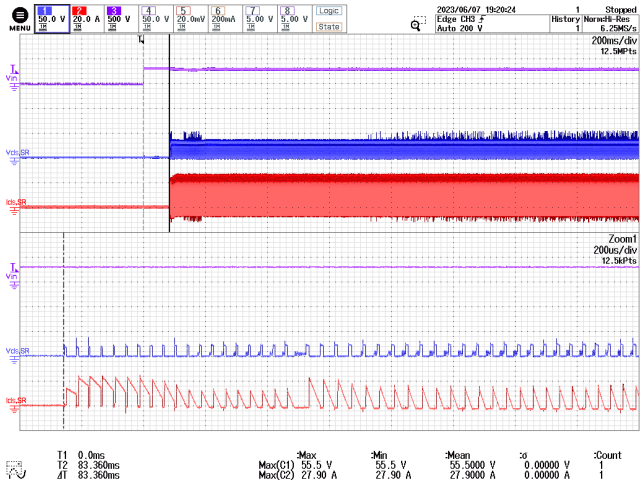


Figure 50 – SR FET Drain Voltage and Current.
300 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

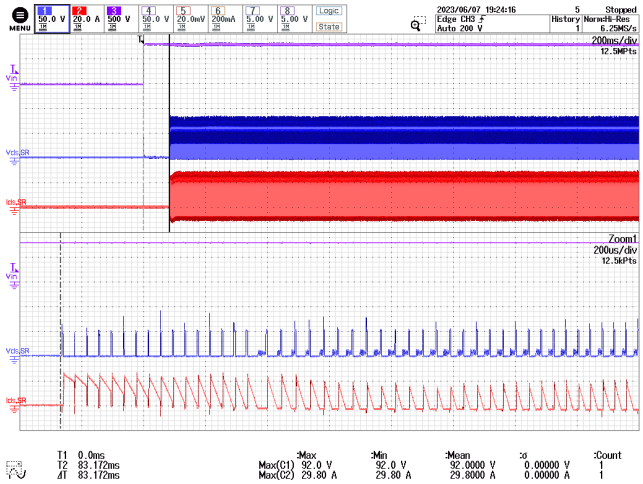


Figure 51 – SR FET Drain Voltage and Current.
800 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

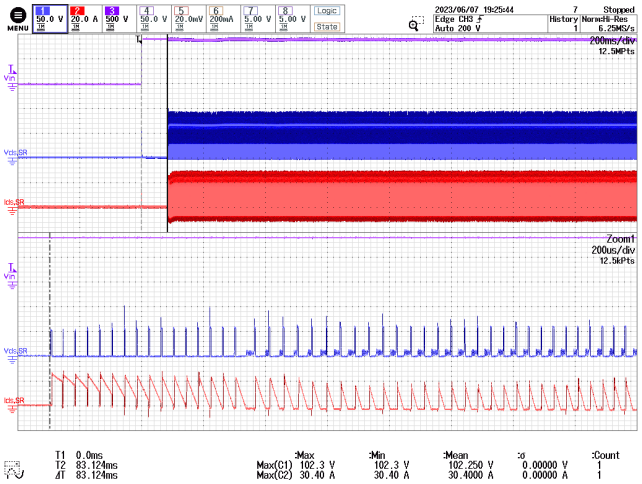


Figure 52 – SR FET Drain Voltage and Current.
900 V_{DC}, 2.12 Ω Load.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
CH3: V_{IN}, 500 V / div.
Time: 200 ms / div.

[22] The time between when V_{IN} is turned on and the SR FET starts switching is due to the additional t_{AR} delay of InnoSwitch3.
[23] Current waveforms were measured using a Rogowski coil.

11.2 Steady-State Waveforms

11.2.1 Switching Waveforms at 85 °C Ambient Temperature

11.2.1.1 Normal Operation Component Stress

	Steady-State Switching Waveforms 85 °C Ambient, Full Load					
Input	**INN3949CQ**			**SR FETs**		
V_{IN} (V)	**I_D (A_{PK})**	**V_{DS} (V_{PK})**	**V_{STRESS} (%)**	**I_D (A_{PK})[24]**	**V_{DS} (V_{PK})[25]**	**V_{STRESS} (%)**
300	1.625	740	43.53	34.4	57.6	48.00
600	1.325	1065	62.65	35	67	55.83
800	1.4	1266	74.47	33.8	87.9	73.25
900	1.5	1361	80.06	34	98	81.67

Table 10 – Summary of Critical Component Voltage Stresses at 85 °C Ambient Temperature.

[24] SR FET current is the sum of Q100 and Q101 currents.
[25] SR FET voltage was taken from Q101.

11.2.1.2 InnoSwitch3-AQ and SR FET[26] Drain Voltage at 85 °C Ambient Temperature

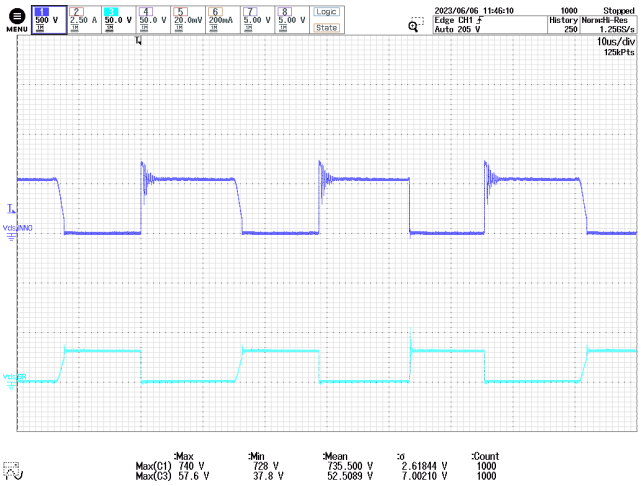


Figure 53 – InnoSwitch3-AQ and SR FET Drain Voltage.[27]
300 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 10 µs / div.

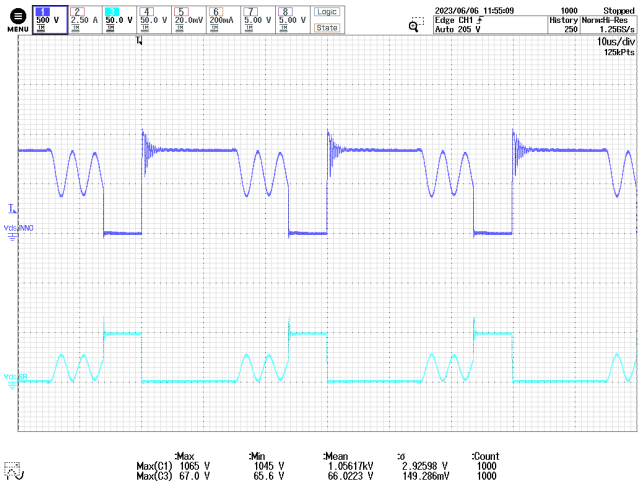


Figure 54 – InnoSwitch3-AQ and SR FET Drain Voltage.
600 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 10 µs / div.

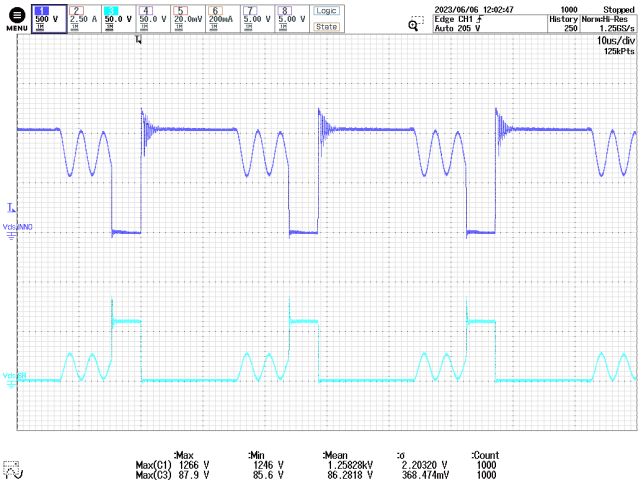


Figure 55 – InnoSwitch3-AQ and SR FET Drain Voltage.
800 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 10 µs / div.

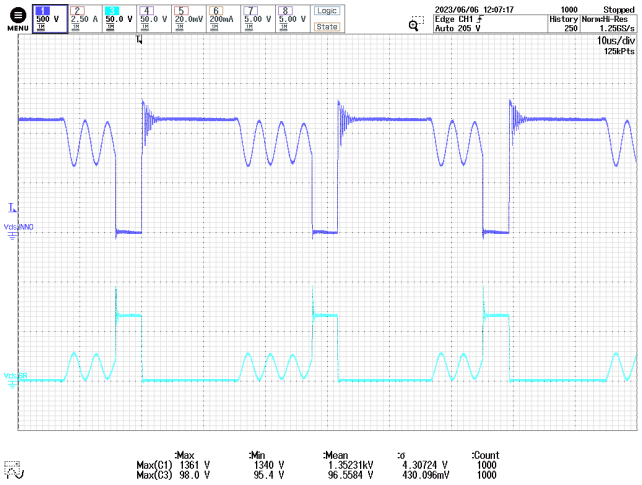


Figure 56 – InnoSwitch3-AQ and SR FET Drain Voltage.
900 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 10 µs / div.

[26] SR FET voltage waveform was taken from Q101.
[27] Intermittent spikes on the SR FET V_{DS} waveform are due to the unit operating intermittently in CCM at 300 V_{IN}.

11.2.2 Switching Waveforms at 25 °C Ambient Temperature

11.2.2.1 Normal Operation Component Stress

	Steady-State Switching Waveforms 25 °C Ambient, Full Load					
Input	**INN3949CQ**			**SR FETs**		
V_{IN} (V)	**I_D (A_{PK})**	**V_{DS} (V_{PK})**	**V_{STRESS} (%)**	**I_D (A_{PK})[28]**	**V_{DS} (V_{PK})[29]**	**V_{STRESS} (%)**
300	1.54	770	45.29	33.2	38	31.67
600	1.555	1060	62.35	33	68	56.67
800	1.56	1270	74.71	33.4	87.5	72.92
900	1.72	1370	80.59	33.8	97.1	80.92

Table 11 – Summary of Critical Component Voltage Stresses at 25 °C Ambient Temperature.

[28] SR FET current is the sum of Q100 and Q101 currents.
[29] SR FET voltage was taken from Q101.

11.2.2.2 InnoSwitch3-AQ Drain Voltage and Current at 25 °C Ambient Temperature

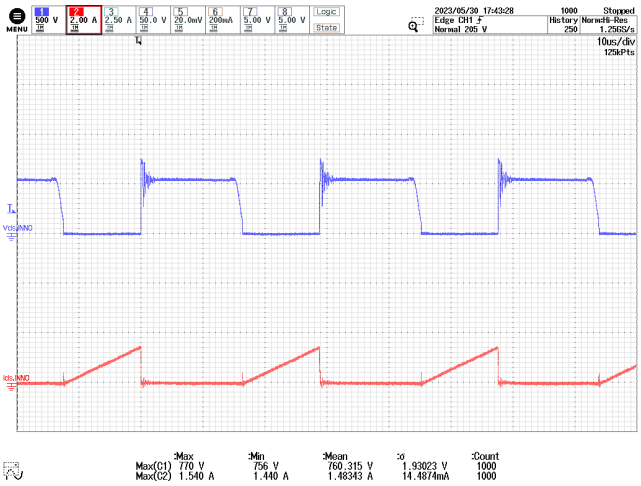


Figure 57 – InnoSwitch3-AQ Drain Voltage and Current.
300 V_{DC}, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
Time: 10 µs / div.

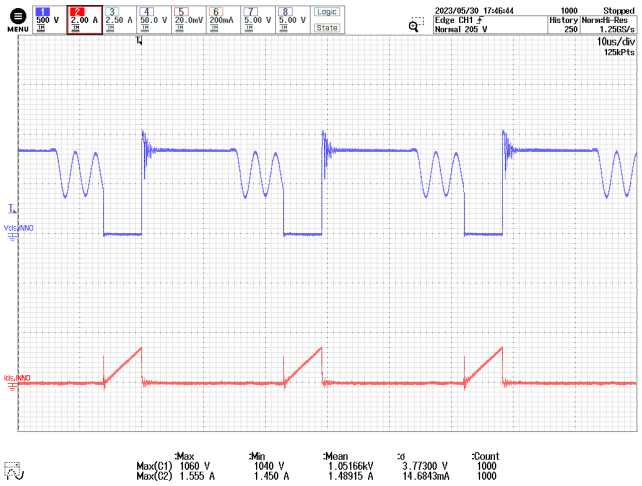


Figure 58 – InnoSwitch3-AQ Drain Voltage and Current.
600 V_{DC}, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
Time: 10 µs / div.

Figure 59 – InnoSwitch3-AQ Drain Voltage and Current.
800 V_{DC}, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
Time: 10 µs / div.

Figure 60 – InnoSwitch3-AQ Drain Voltage and Current.
900 V_{DC}, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $I_{D,INNO}$, 2 A / div.
Time: 10 µs / div.

11.2.2.3 SR FET Drain Voltage and Current at 25 °C Ambient Temperature[30]

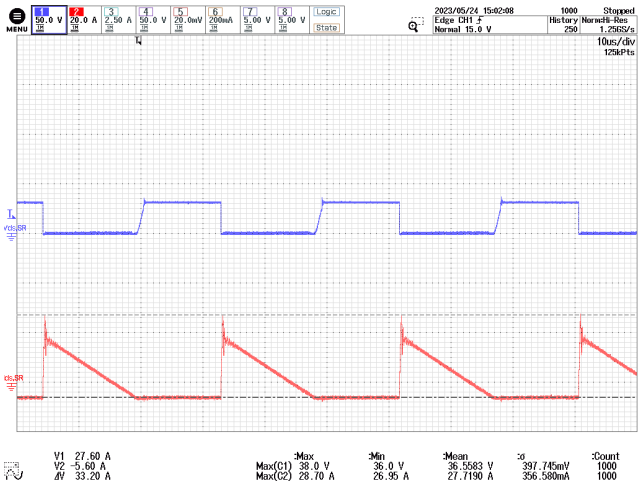


Figure 61 – SR FET Drain Voltage and Current.
300 V_{DC}, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
Time: 10 µs / div.

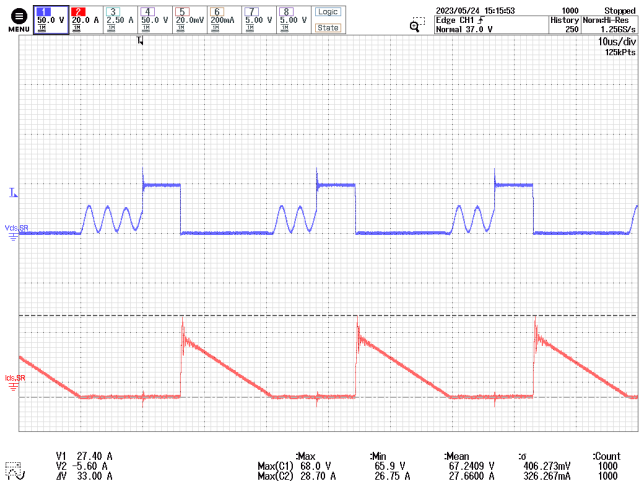


Figure 62 – SR FET Drain Voltage and Current.
600 V_{DC}, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
Time: 10 µs / div.

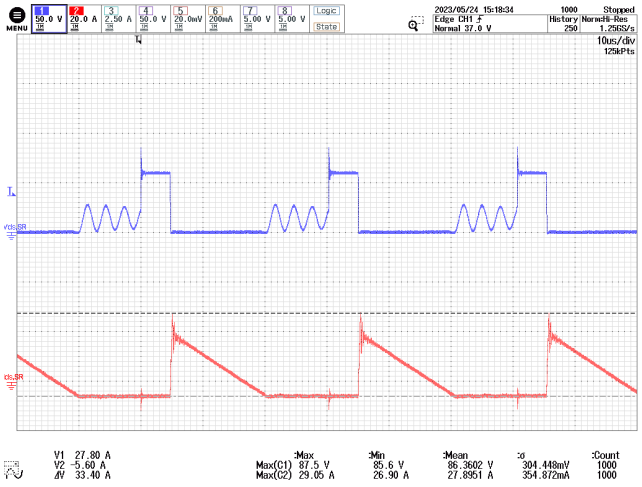


Figure 63 – SR FET Drain Voltage and Current.
800 V_{DC}, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
Time: 10 µs / div.

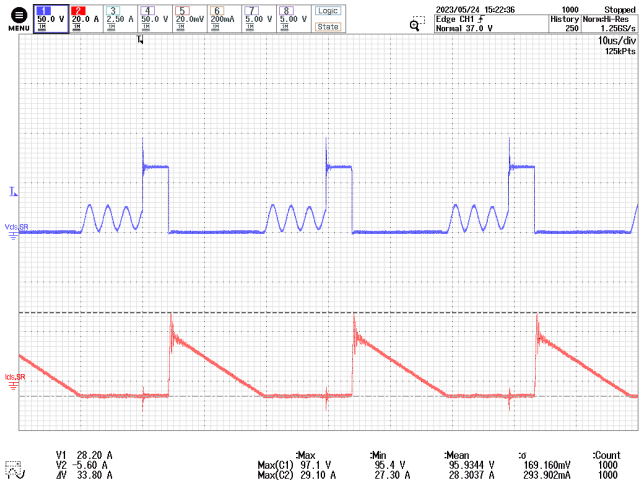


Figure 64 – SR FET Drain Voltage and Current.
900 V_{DC}, 6.37 A Load, 25 °C Ambient.
CH1: $V_{DS,SRFET}$, 50 V / div.
CH2: $I_{D,SRFET}$, 20 A / div.
Time: 10 µs / div.

[30] SR FET voltage waveform was taken from Q101.

11.2.2.4 Short-Circuit Response

The unit was tested by applying an output short-circuit during normal working conditions and then removing the short-circuit to see if the unit would recover and operate normally. The expected response during short-circuit is for the unit to go to AR (auto-restart) mode and attempt recovery every 1.7 to 2.11 seconds. Full load configuration is at 2.12 ohms constant resistance.

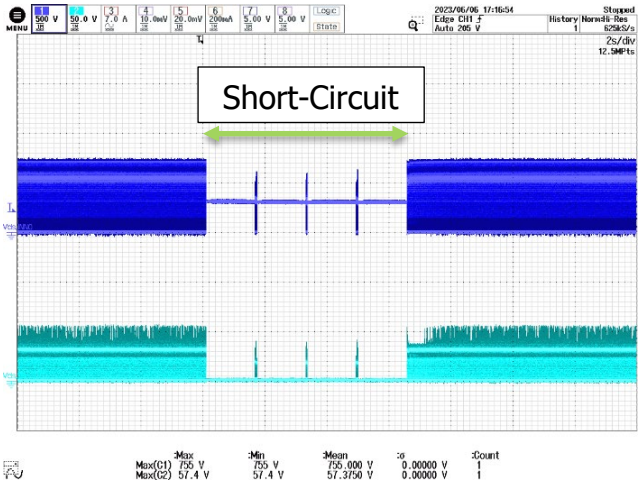


Figure 65 – InnoSwitch3-AQ and SR FET Drain Voltage. 300 V_{DC}, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 2 s / div.

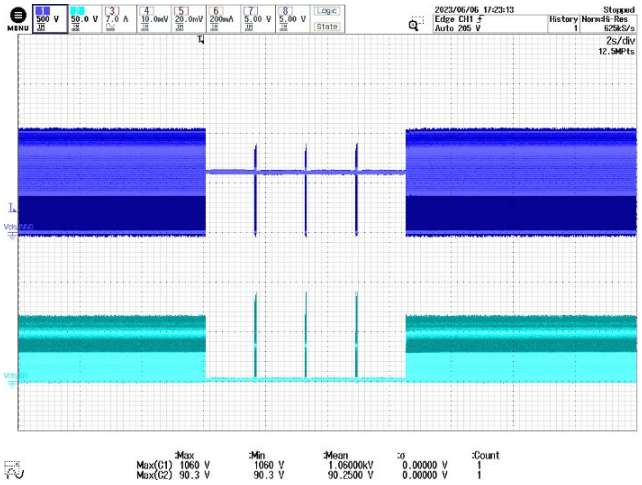


Figure 66 – InnoSwitch3-AQ and SR FET Drain Voltage. 600 V_{DC}, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 2 s / div.

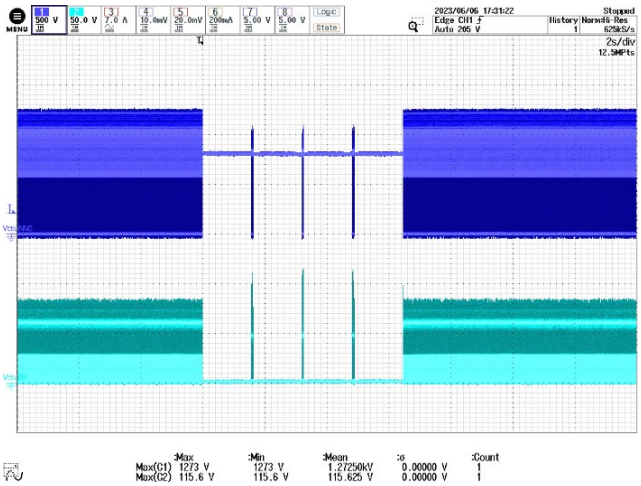


Figure 67 – InnoSwitch3-AQ and SR FET Drain voltage. 800 V_{DC}, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 2 s / div.

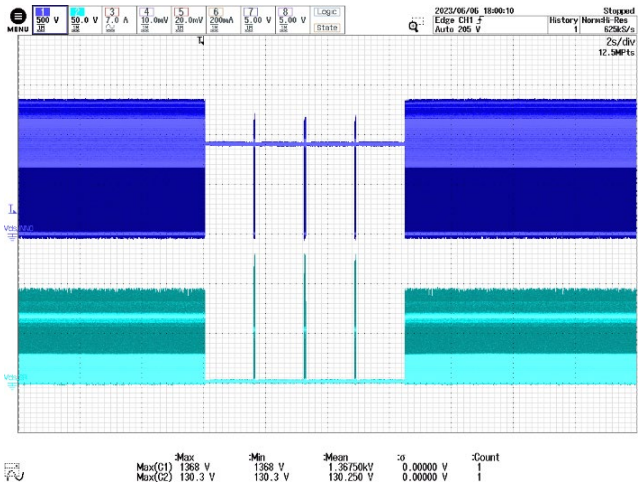


Figure 68 – InnoSwitch3-AQ and SR FET Drain voltage. 900 V_{DC}, Full Load-Short-Full Load, 85 °C Ambient.
CH1: $V_{DS,INNO}$, 500 V / div.
CH2: $V_{DS,SRFET}$, 50 V / div.
Time: 2 s / div.

11.3 Load Transient Response

Output voltage waveform on the board was captured with dynamic load transient from 0% to 50%, 50% to 100%, and 10% to 90%. The duration for the load states is set to 100 ms, and the load slew rate is 100 mA / μs. The test is done at 85 °C ambient temperature.

Dynamic Load Settings	V_{IN} (V)	$V_{OUT(MAX)}$ (V)	$V_{OUT(MIN)}$ (V)
0% to 50%	300	13.63	13.34
	600	13.66	13.36
	800	13.66	13.32
	900	13.67	13.31
50% to 100%	300	13.77	13.22
	600	13.74	13.22
	800	13.70	13.30
	900	13.67	13.29
10% to 90%	300	13.71	13.20
	600	13.70	13.31
	800	13.71	13.27
	900	13.71	13.28

Table 12 – Load Transient Response.

11.3.1 Output Voltage Ripple with 0% to 50% Transient Load at 85 °C Ambient Temperature

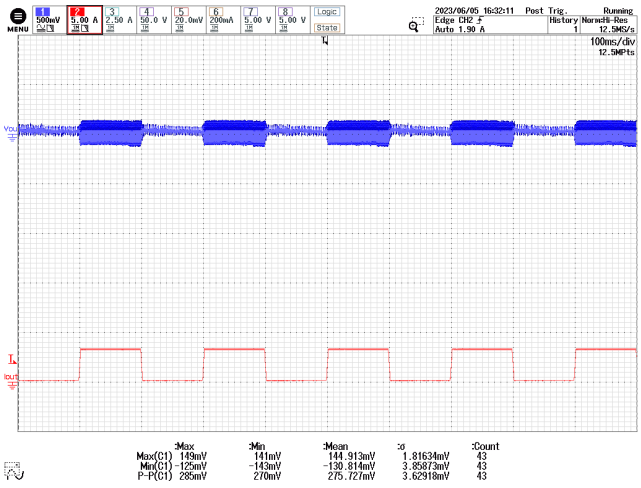


Figure 69 – Output Voltage and Current.
300 V_{DC}, 0 A to 3.185 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

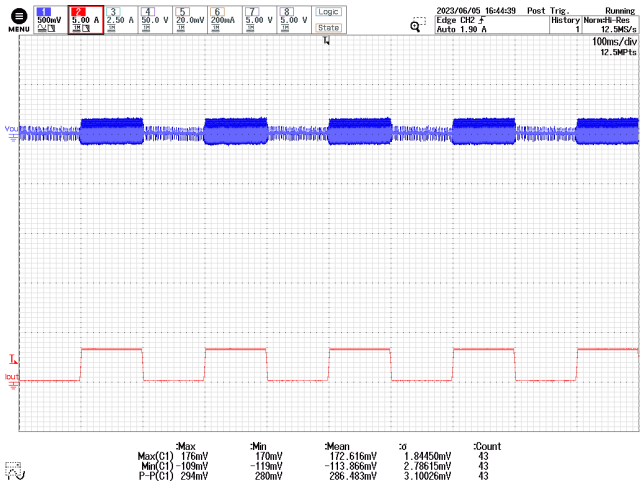


Figure 70 – Output Voltage and Current.
600 V_{DC}, 0 A to 3.185 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

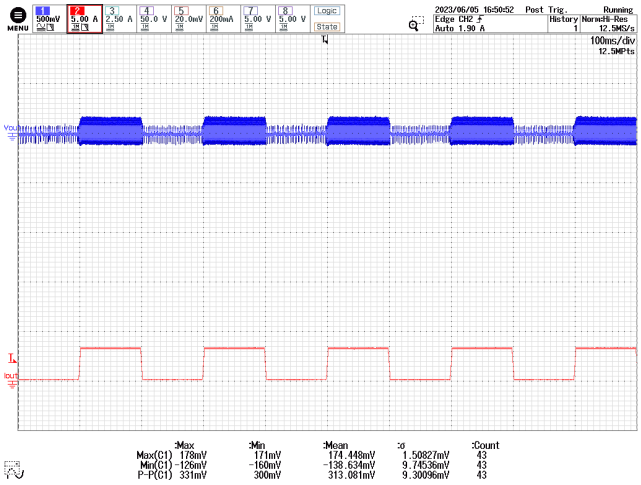


Figure 71 – Output Voltage and Current.
800 V_{DC}, 0 A to 3.185 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

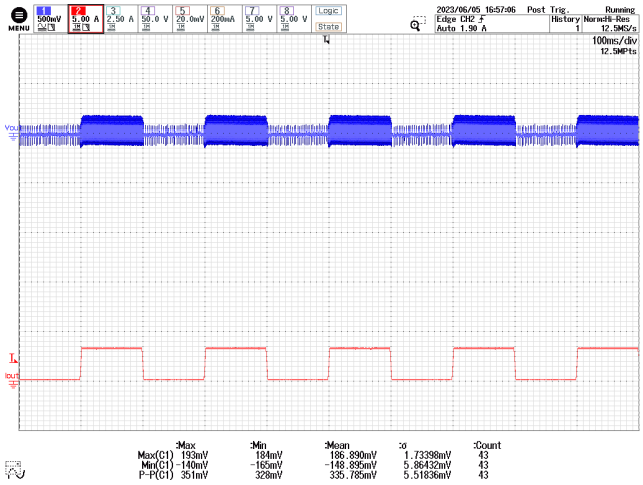


Figure 72 – Output Voltage and Current.
900 V_{DC}, 0 A to 3.185 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

11.3.2 Output Voltage Ripple with 50% to 100% Transient Load at 85 °C Ambient Temperature

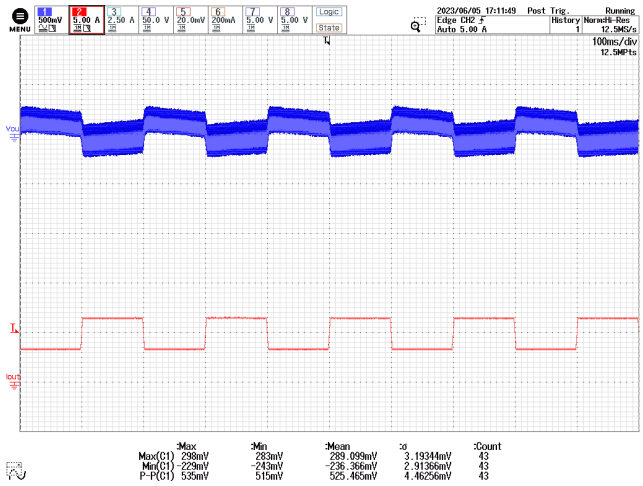


Figure 73 – Output Voltage and Current.
300 V_{DC},
3.185 A to 6.37 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

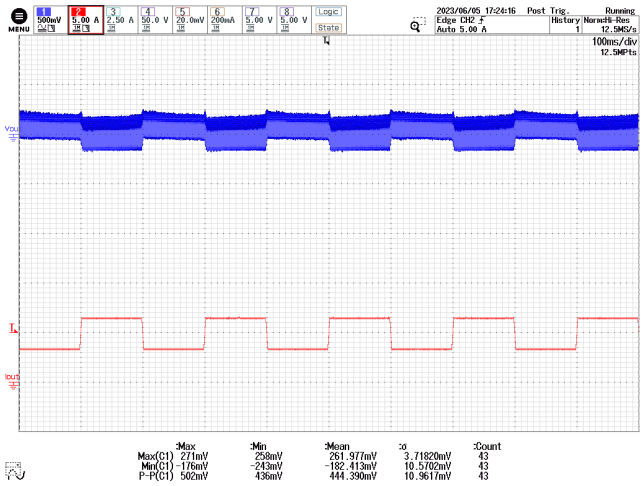


Figure 74 – Output Voltage and Current.
600 V_{DC},
3.185 A to 6.37 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

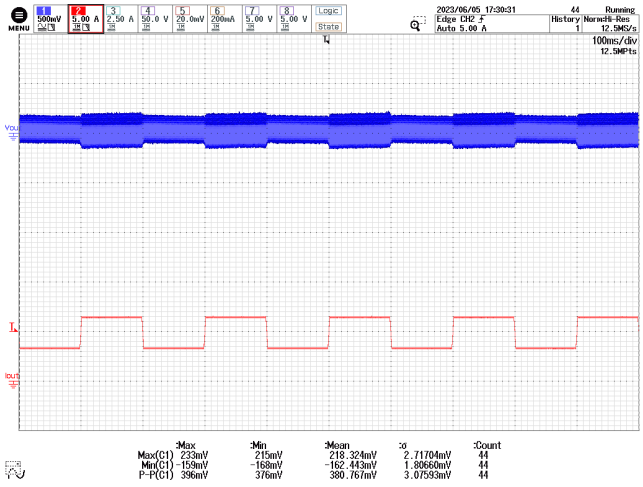


Figure 75 – Output Voltage and Current.
800 V_{DC},
3.185 A to 6.37 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

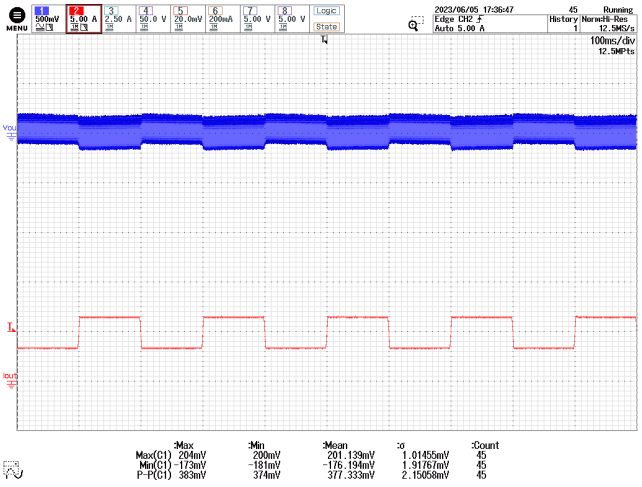


Figure 76 – Output Voltage and Current.
900 V_{DC},
3.185 A to 6.37 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

11.3.3 Output Voltage Ripple with 10% to 90% Transient Load at 85 °C Ambient Temperature

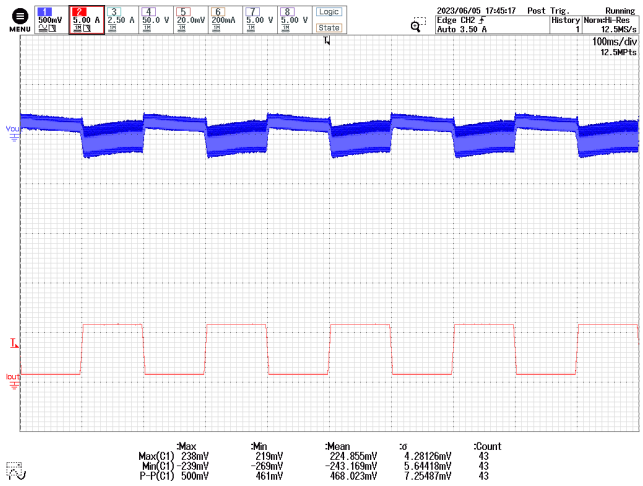


Figure 77 – Output Voltage and Current.
300 V_{DC},
637 mA to 5.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

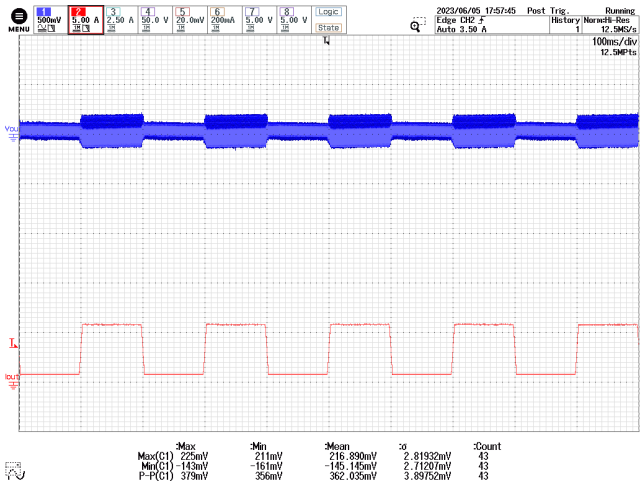


Figure 78 – Output Voltage and Current.
600 V_{DC},
637 mA to 5.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

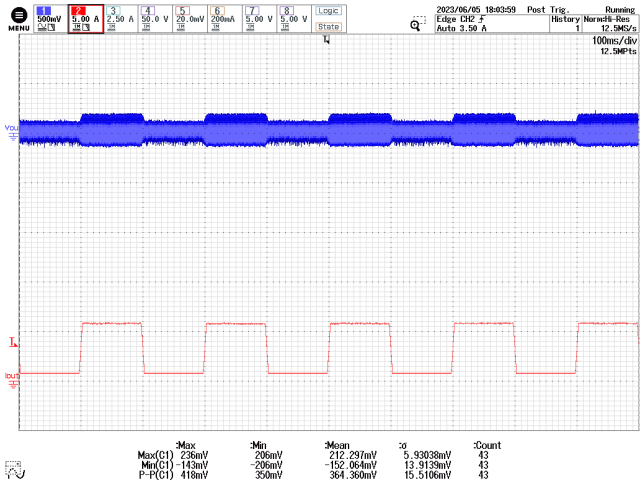


Figure 79 – Output Voltage and Current.
800 V_{DC},
637 mA to 5.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

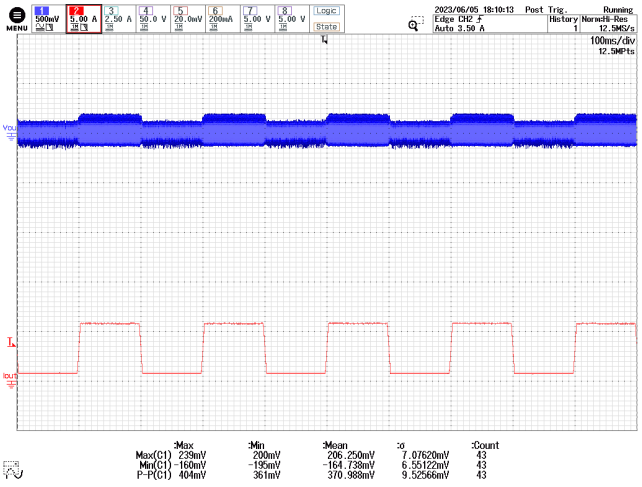


Figure 80 – Output Voltage and Current.
900 V_{DC},
637 mA to 5.73 A Transient Load,
85 °C Ambient.
CH1: V_{OUT}, 500 mV / div.
CH2: I_{OUT}, 5 A / div.
Time: 100 ms / div.

11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

A modified oscilloscope test probe is used for output voltage ripple measurements to reduce spurious signals due to pick-up. Details of the probe modification are provided in Figure 81 and Figure 82 below.

A CT2708 probe adapter is affixed with a 1 μF / 50 V ceramic capacitor placed in parallel across the probe tip and GND terminal. A twisted pair of wires kept as short as possible is soldered directly to the probe and the output terminals.

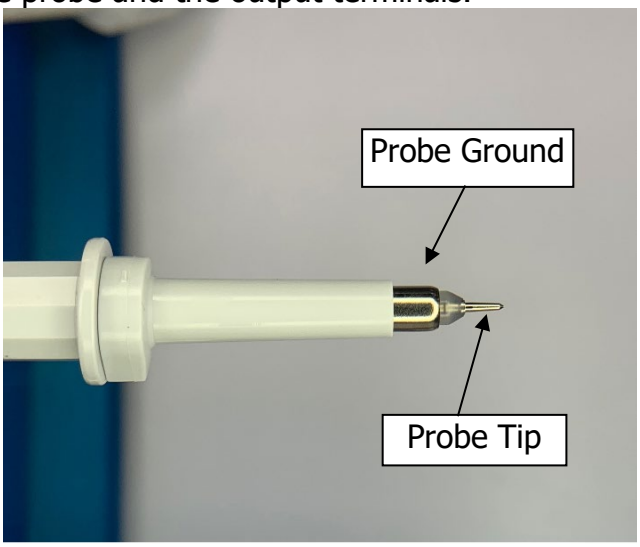


Figure 81 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

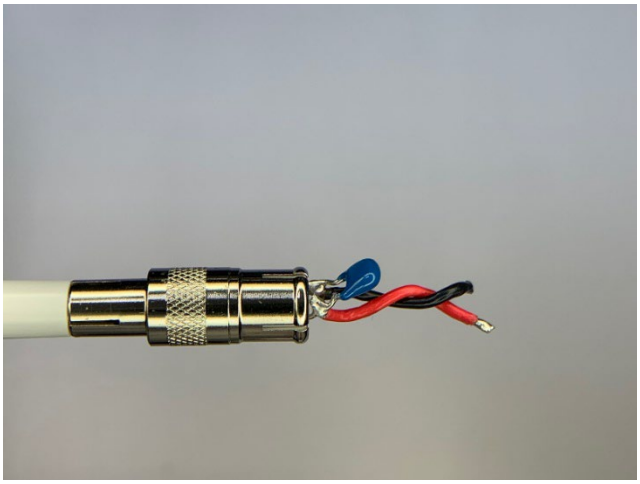


Figure 82 – Oscilloscope Probe with Cal Test CT2708 BNC Adapter. (Modified with Wires for Ripple Measurement, and a Parallel Decoupling Capacitor Added.)

11.4.2 Output Voltage Ripple Waveforms

Output voltage ripple waveform at full load was captured at the output terminals using the ripple measurement probe with a decoupling capacitor.

11.4.2.1 Output Voltage Ripple at 85 °C Ambient Constant Full Load[31]

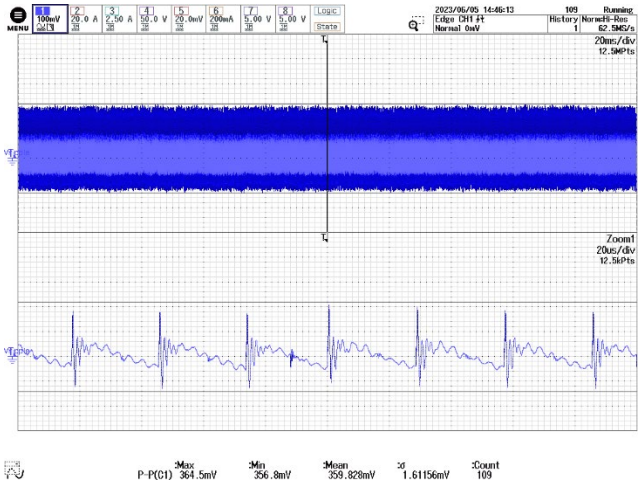


Figure 83 – Output Voltage Ripple.
300 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 359.83 mV.

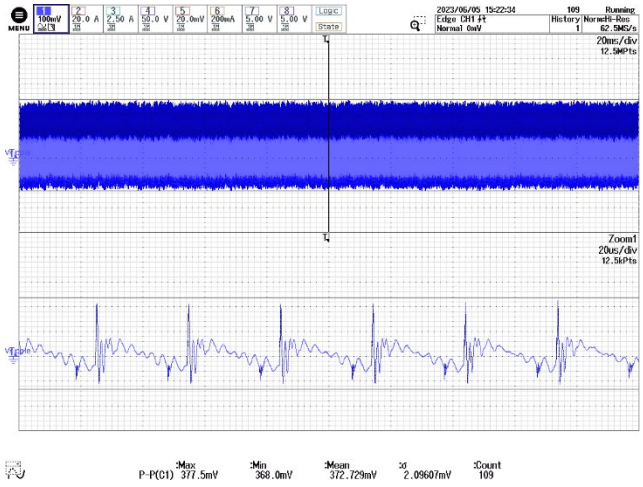


Figure 84 – Output Voltage Ripple.
600 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 372.73 mV.

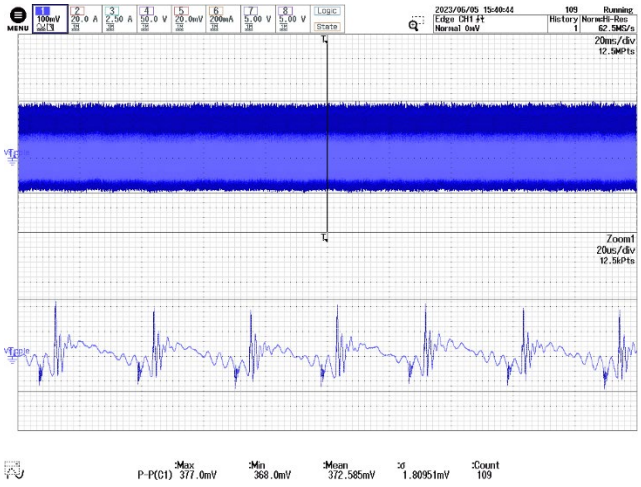


Figure 85 – Output Voltage Ripple.
800 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 372.59 mV.

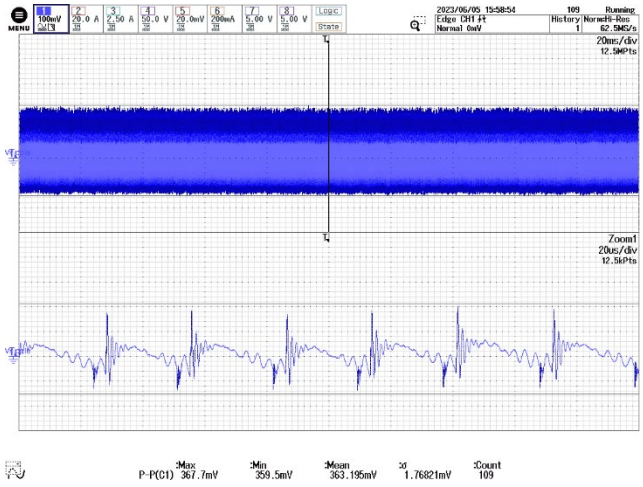


Figure 86 – Output Voltage Ripple.
900 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 363.20 mV.

[31] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.2 Output Voltage Ripple at 25 °C Ambient Constant Full Load[32]

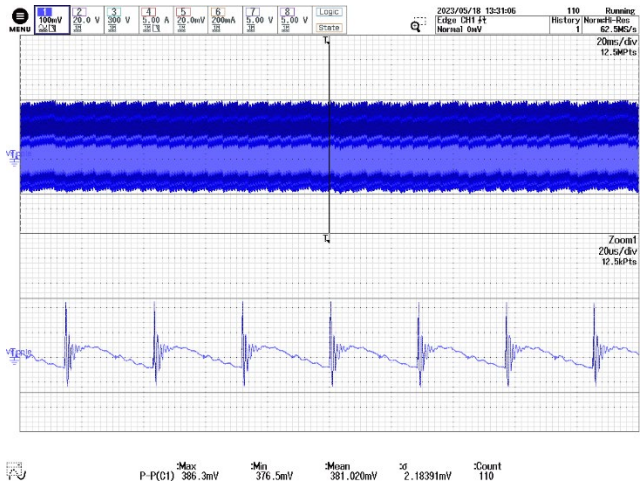


Figure 87 – Output Voltage Ripple.
300 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 381.02 mV.

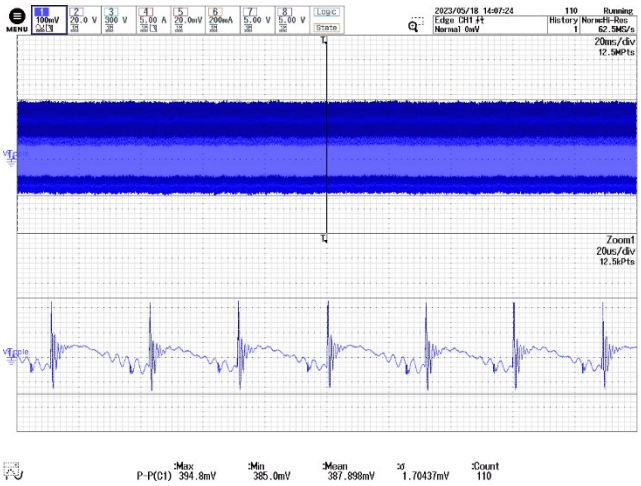


Figure 88 – Output Voltage Ripple.
600 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 387.90 mV.

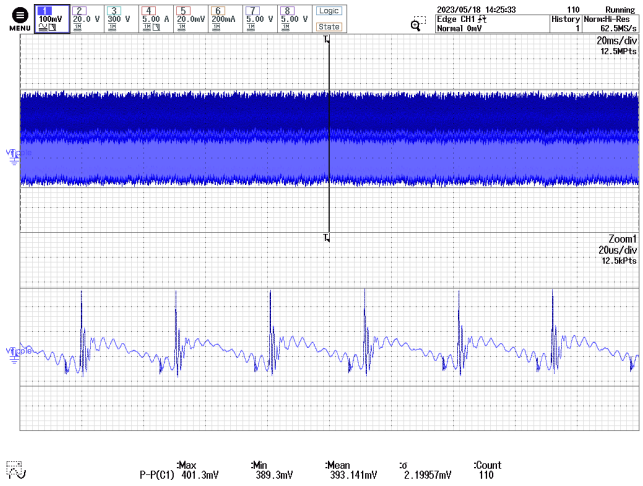


Figure 89 – Output Voltage Ripple.
800 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 393.14 mV.

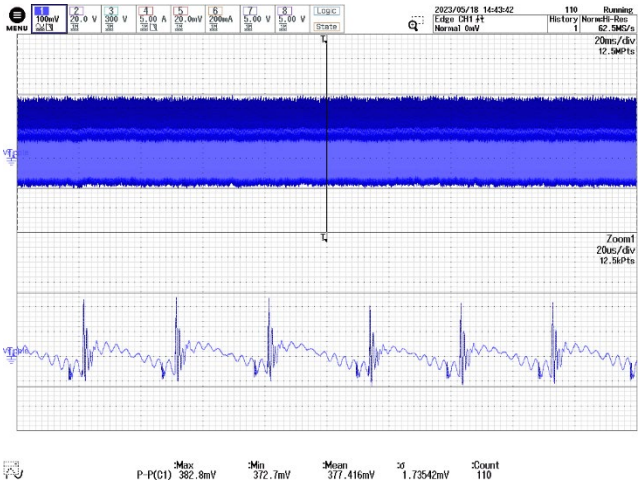


Figure 90 – Output Voltage Ripple.
900 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 377.42 mV.

[32] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.2.3 Output Voltage Ripple at -40 °C Ambient Constant Full Load[33]

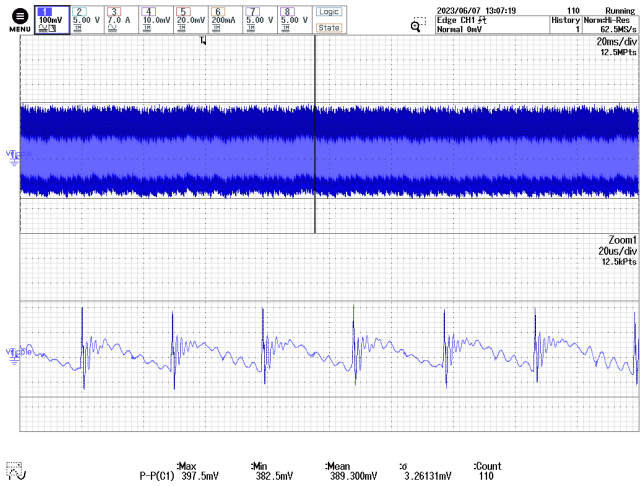


Figure 91 – Output Voltage Ripple.
300 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 389.30 mV.

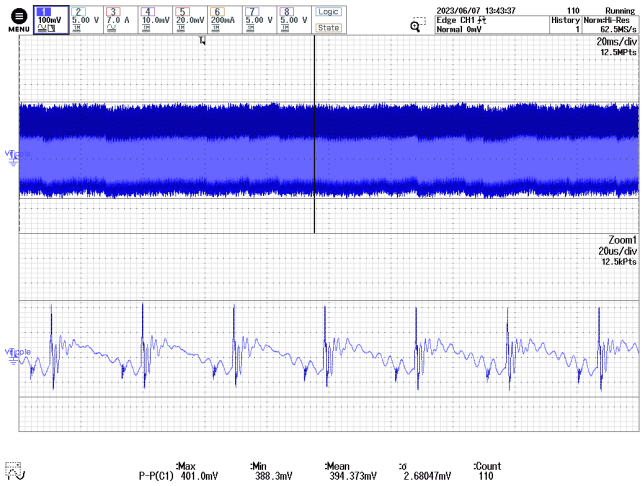


Figure 92 – Output Voltage Ripple.
600 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 394.37 mV.

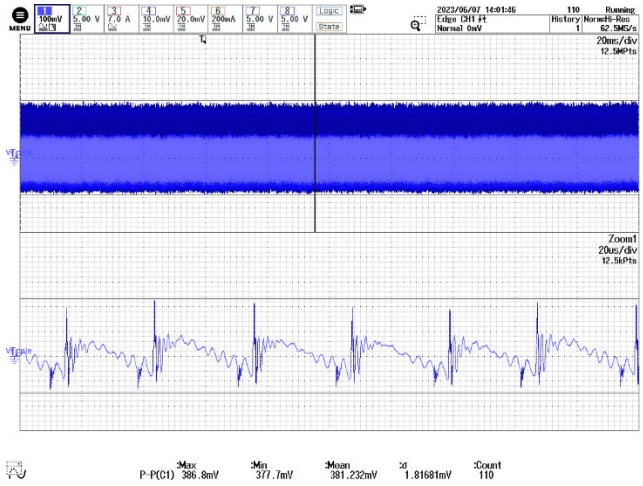


Figure 93 – Output Voltage Ripple.
800 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 381.23 mV.

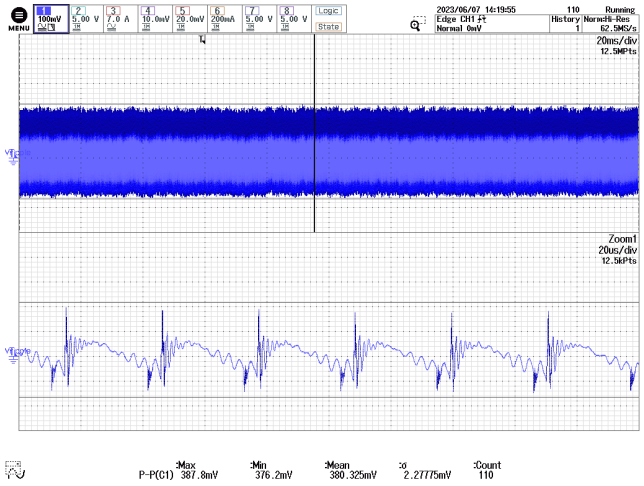


Figure 94 – Output Voltage Ripple.
900 V_{DC}, 6.37 A Load, 85 °C Ambient.
CH1: V_{OUT}, 100 mV / div.
Time: 20 ms / div.
V_{RIPPLE} = 380.33mV.

[33] Peak-to-peak voltage measurement recorded in each oscilloscope capture is the worst-case ripple which includes both the low frequency and high frequency switching voltage ripple (top portion of each capture).

11.4.3 Output Ripple vs. Load

11.4.3.1 Output Ripple at 85 °C Ambient

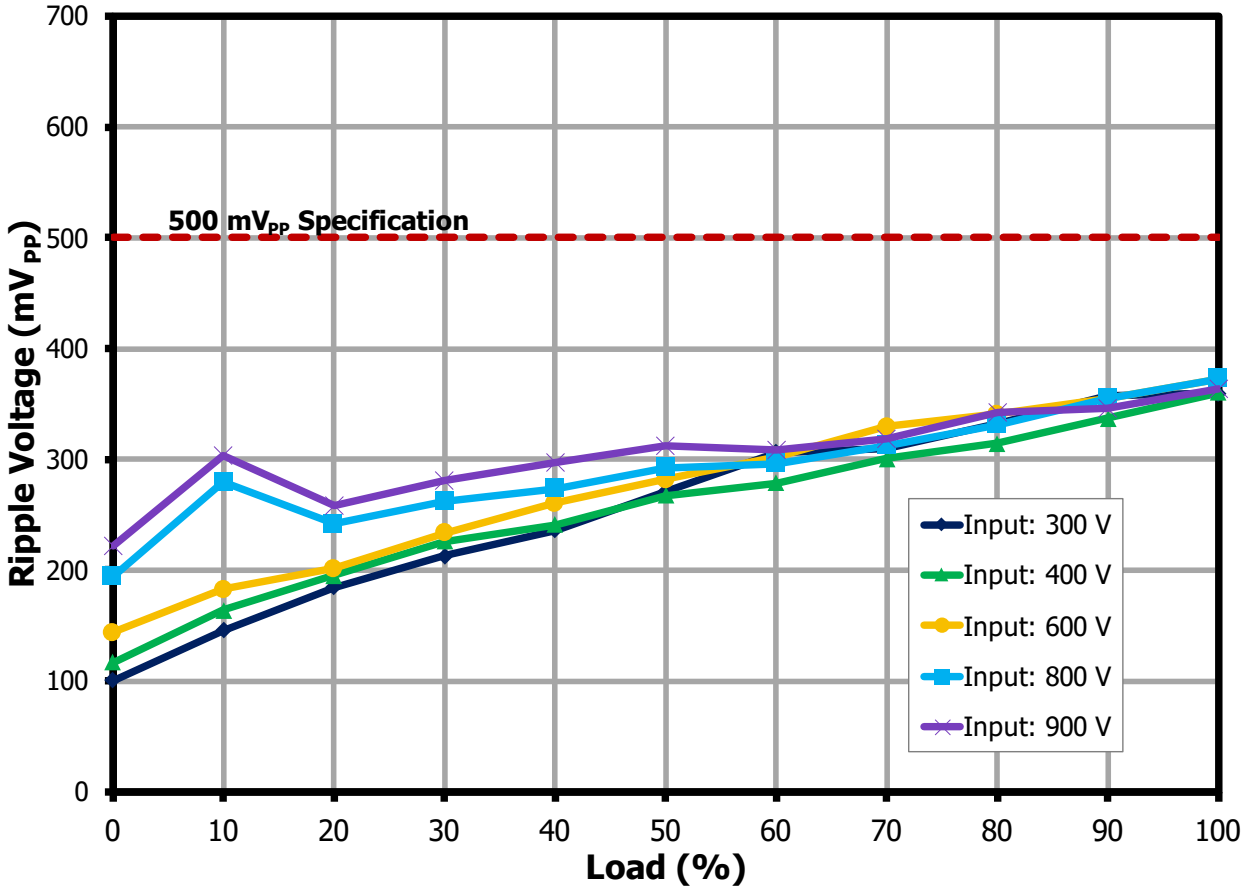


Figure 95 – Output Ripple Voltage Across Full Load Range (85 °C Ambient).

11.4.3.2 Output Ripple at 25 °C Ambient

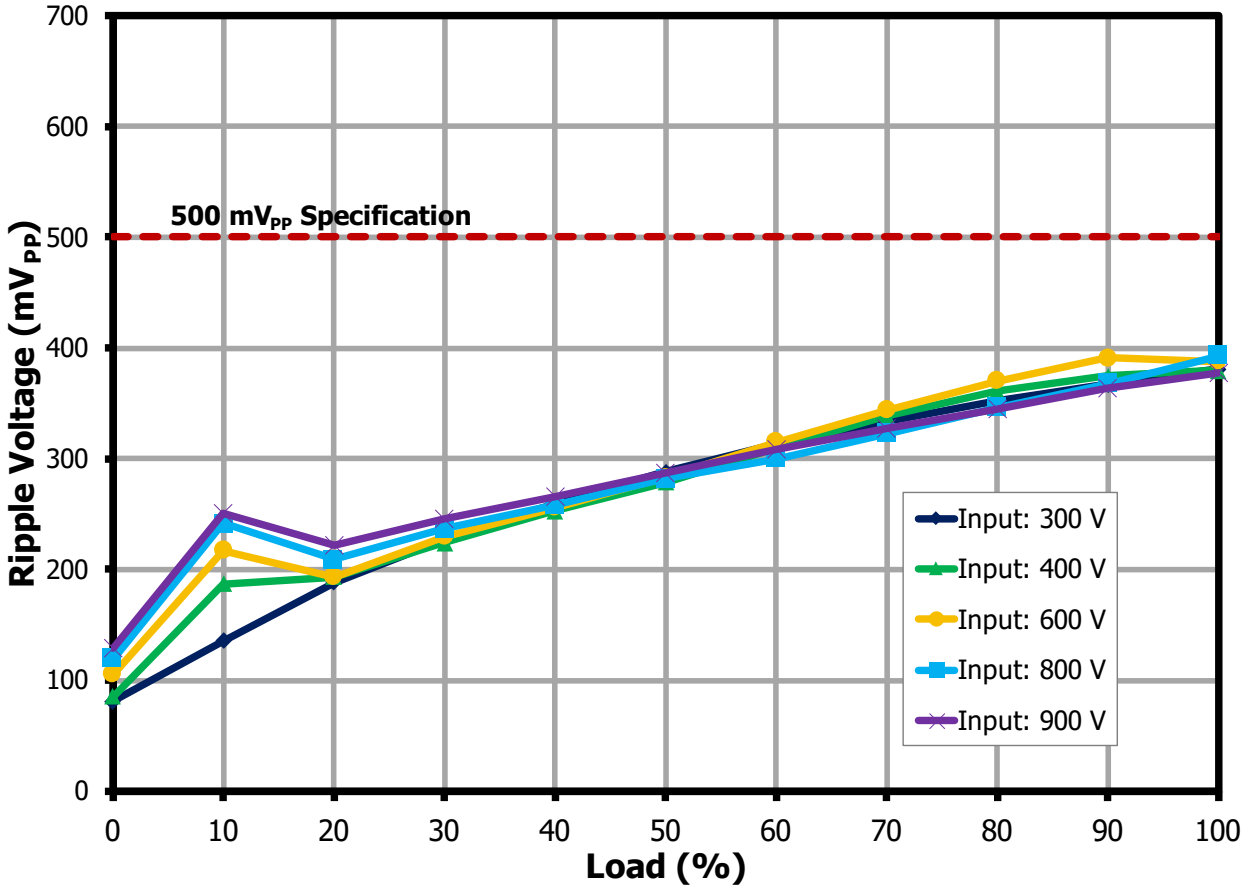


Figure 96 – Output Ripple Voltage Across Full Load Range (25 °C Ambient).

11.4.3.3 Output Ripple at -40 °C Ambient

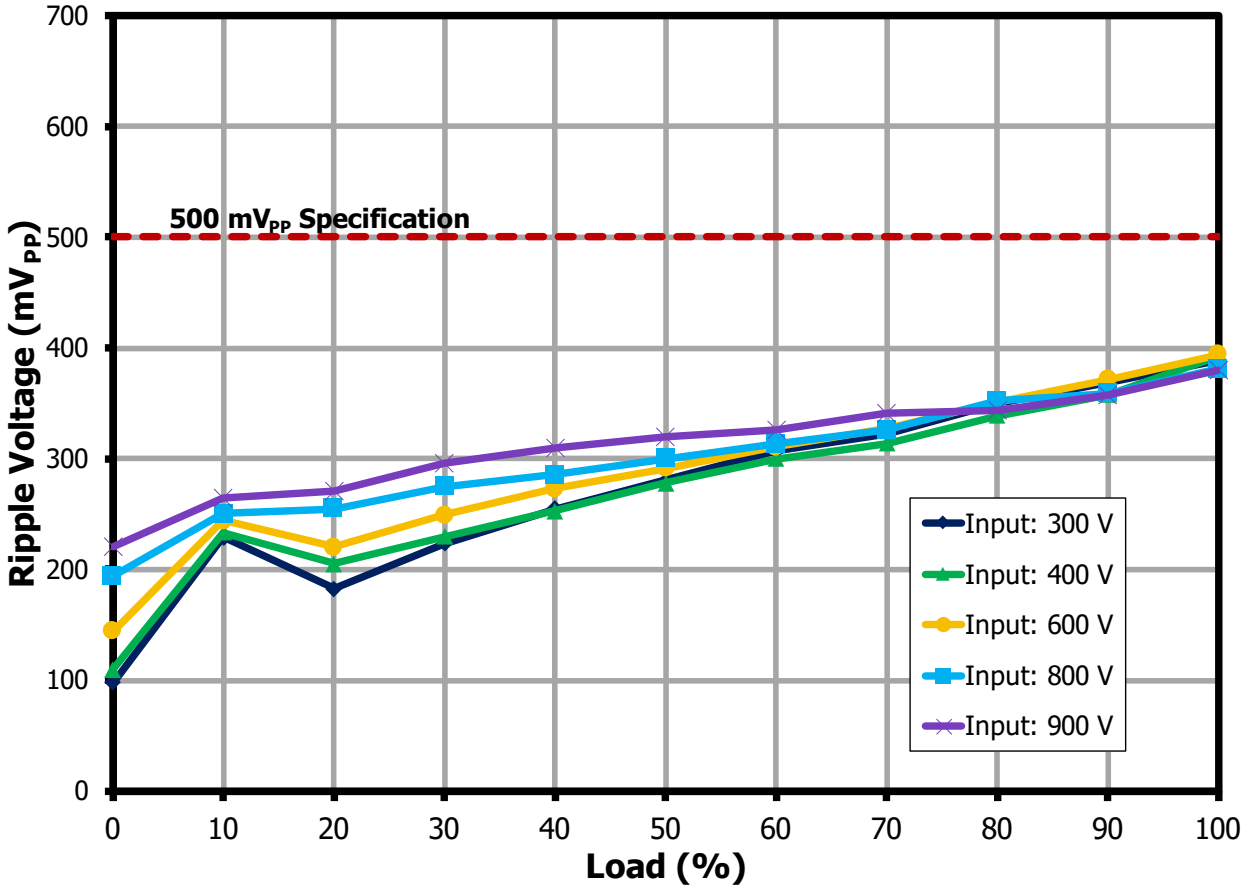


Figure 97 – Output Ripple Voltage Across Full Load Range (-40 °C Ambient).

12 Output Overload

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C for at least 30 minutes before turning on the unit under test. The unit was soaked for at least 20 minutes for every change in the input voltage during the start of each test sequence. For every loading condition, the unit under test was soaked for at least 60 seconds before the voltage and current measurements on the output were taken.

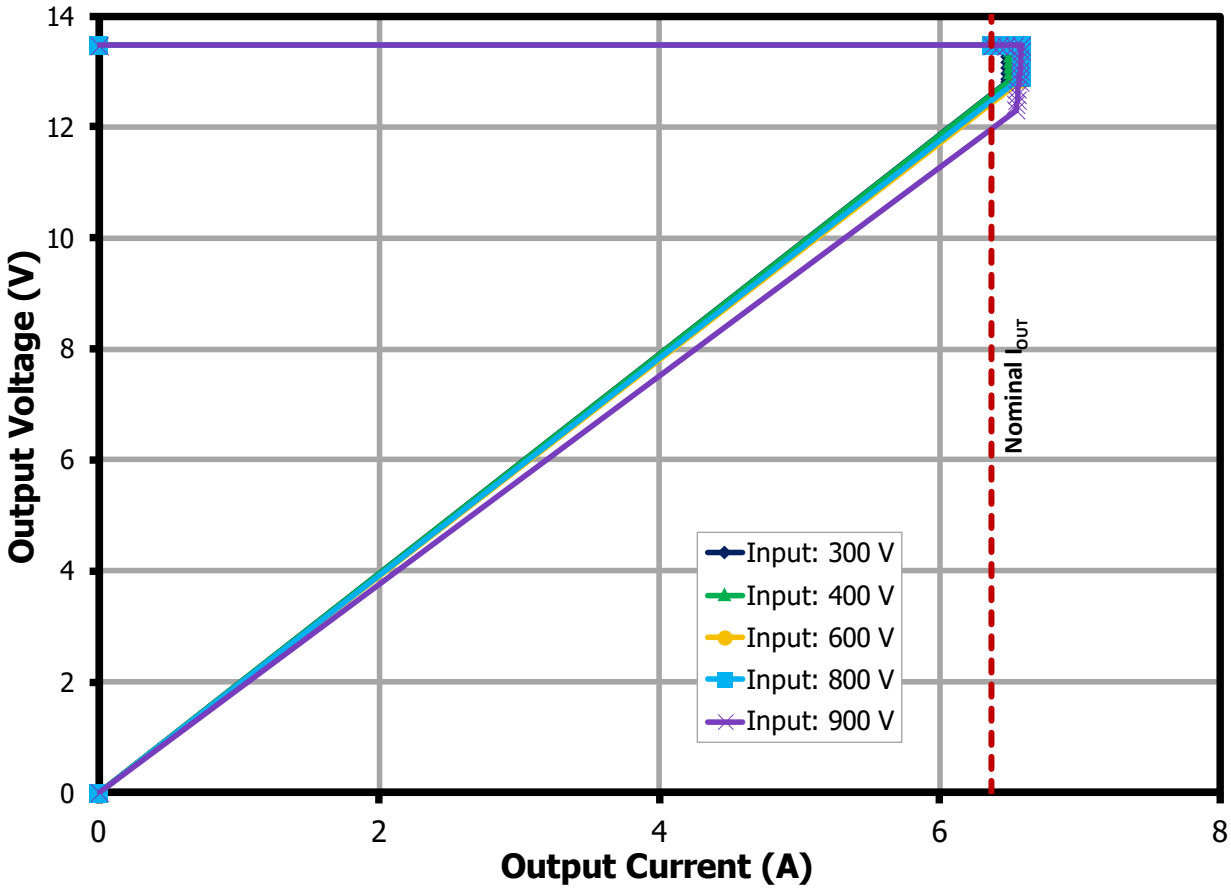


Figure 98 – Output Overload Curve at 85 °C Ambient Temperature.

13 Maximum Output Power

The unit under test was placed inside a thermal chamber. The chamber was pre-heated to 85 °C for at least 30 minutes before turning on the unit under test. The unit was soaked for at least 30 minutes for every change in the input voltage and loading condition during the start of each test sequence to allow component temperatures to settle. Maximum output power capability at a given input voltage was determined by finding the maximum loading condition in which the unit doesn't enter auto-restart (AR) mode operation or trigger any overtemperature protection. Case temperatures for select critical components were also considered in determining the maximum output power capability.

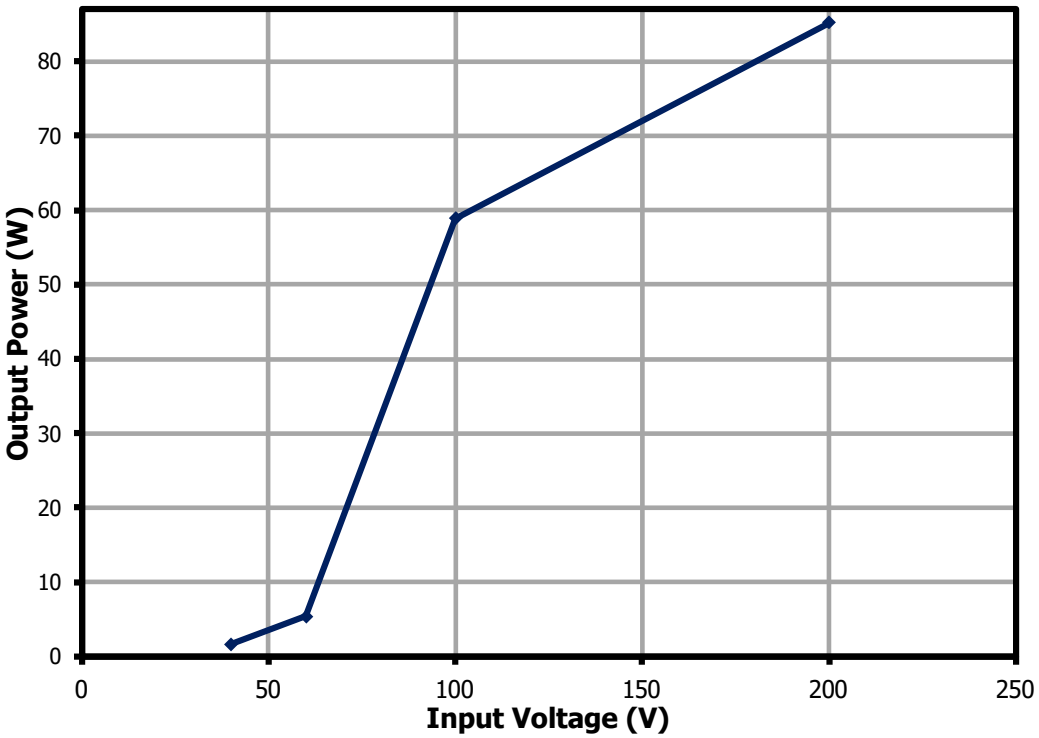


Figure 99 – Maximum Output Power Curve at 85 °C Ambient Temperature.

Input Voltage (V)	PIXls Calculated Maximum Output Power[34] (W)	Measured Maximum Output Power (W)	Limiting Factor for Measured Maximum Output Power	Value
200	86	86	Design maximum output power reached	86 W
100	86	58.85	Transformer winding temperature	134.30 °C
60	5.1	5.42	InnoSwitch3-AQ power limit	-
40	2.1	1.63	InnoSwitch3-AQ power limit	-

Table 13 – Maximum Output Power Capability Limiting Factor.

[34] Calculated maximum output power was only determined by using the PIXls "Input Voltage Set-Points Analysis" feature. Component thermal calculations were not included in this column.

14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
15-Aug-23	MR, JS	1.0	Initial Release.	Apps & Mktg
06-May-24	JS	1.1	Text Changes. Updated Schematic. Updated No-Load Figure.	Apps & Mktg

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