Design Example Report

Title	***220 W Power Factor Corrected LLC Power Supply Using HiperPFS™-5 PFS5178F and HiperLCS™2-HB LCS7265C and HiperLCS2-SR LSR2000C***
Specification	90 VAC – 265 VAC Input; 24 V at 9.2 A Output
Application	Display, Power Tools, and General Adapters
Author	Applications Engineering Department
Document Number	DER-672
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Revision	1.2

Summary and Features

- Integrated PFC and LLC stages for a very low component count design
- Quasi-resonant DCM control ensures low switching losses, small inductor size, and permits use of low-cost boost diode
- High frequency (up to 250 kHz) LLC for small transformer size.
- >96% full load PFC efficiency at 115 VAC
- >97% full load LLC efficiency
  - System efficiency 94% / 95.5% at 115 VAC / 230 VAC
- Hiper PFS5 can support self-bias for PFC stage during start-up conditions
- Hiper LCS2 can support self-bias for DC-DC and PFC stage (if self-bias is not available on PFC stage)
- Eliminates heat sinks for powers up to 220 W

Power Integrations
5245 Hellyer Avenue, San Jose, CA 95138 USA.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.power.com

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer to provide the AC input to the prototype board.
Since there is no separate bias converter in this design, ~280 VDC is present on bulk capacitor C10 immediately after the supply is powered down. For safety, this capacitor must be discharged with an appropriate resistor (10 k / 2 W is adequate), or the supply must be allowed to stand ~10 minutes before handling.

1 Introduction

This engineering report describes a 24 V, 220 W reference design power supply that can operate from 90 VAC to 265 VAC for Display, Power Tools, and General Adapters. The power supply uses a Quasi-resonant Discontinuous Conduction Mode (DCM) PFC front-end with an LLC DC-DC converter operating at 120 kHz for high efficiency power conversion.

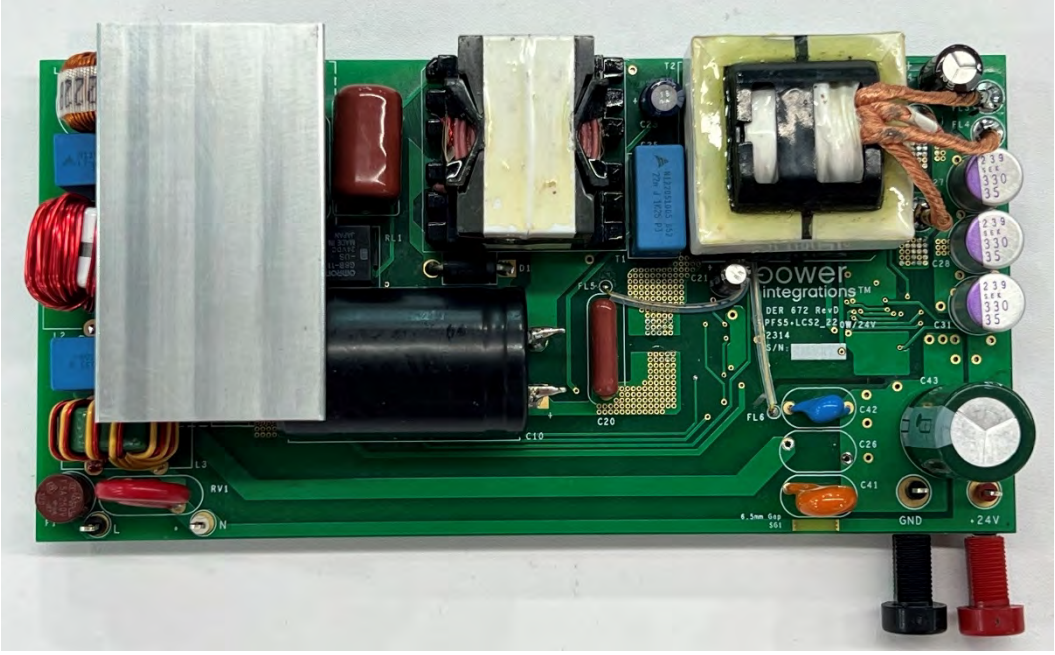


Figure 1 – DER-672, Top View.

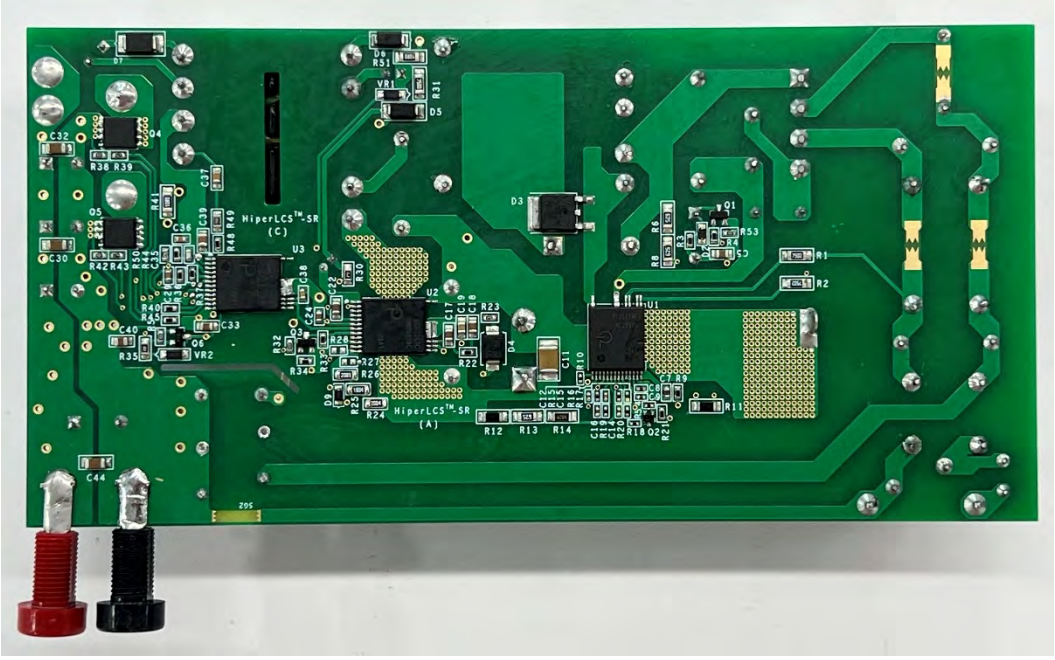


Figure 2 – DER-672, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input Voltage Frequency	 V_{IN} f_{LINE}	 90 47	 50/60	 265 64	 VAC Hz	 2 Wire Input.
Main Converter Output Output Voltage Output Ripple Output Current	 V_{LG} $V_{RIPPLE(LG)}$ I_{LG}	 0.00	 24 	 240 9.2	 V mV_{PK-PK} A	 (220W) Full Load. Within 1% of output, Full Load.
Total Output Power Continuous Output Power	 P_{OUT}	 	 220	 	 W	
Efficiency Total system at Full Load	 η_{Main}	 	 94 95.5	 	 %	 Measured at 115 VAC, Full Load. Measured at 230 VAC, Full Load.
No Load Input Power Total system at No-Load	$PIN_{No-Load}$		100		mW	Measured at 230 VAC.
Environmental Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	ºC	See Thermal Section for Conditions.

3 Schematic

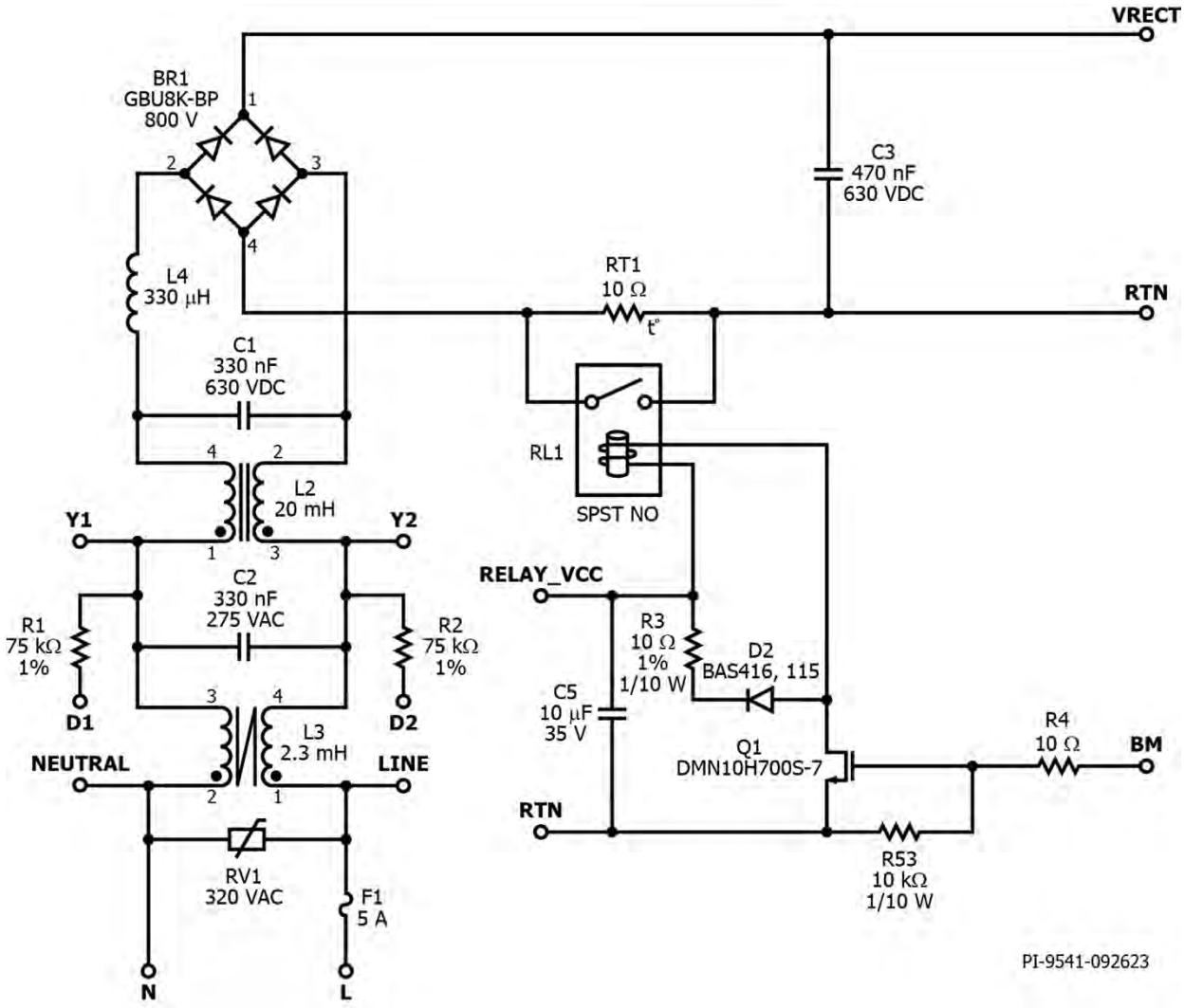


Figure 3 – Input Filter and Bridge Rectifier Schematic.

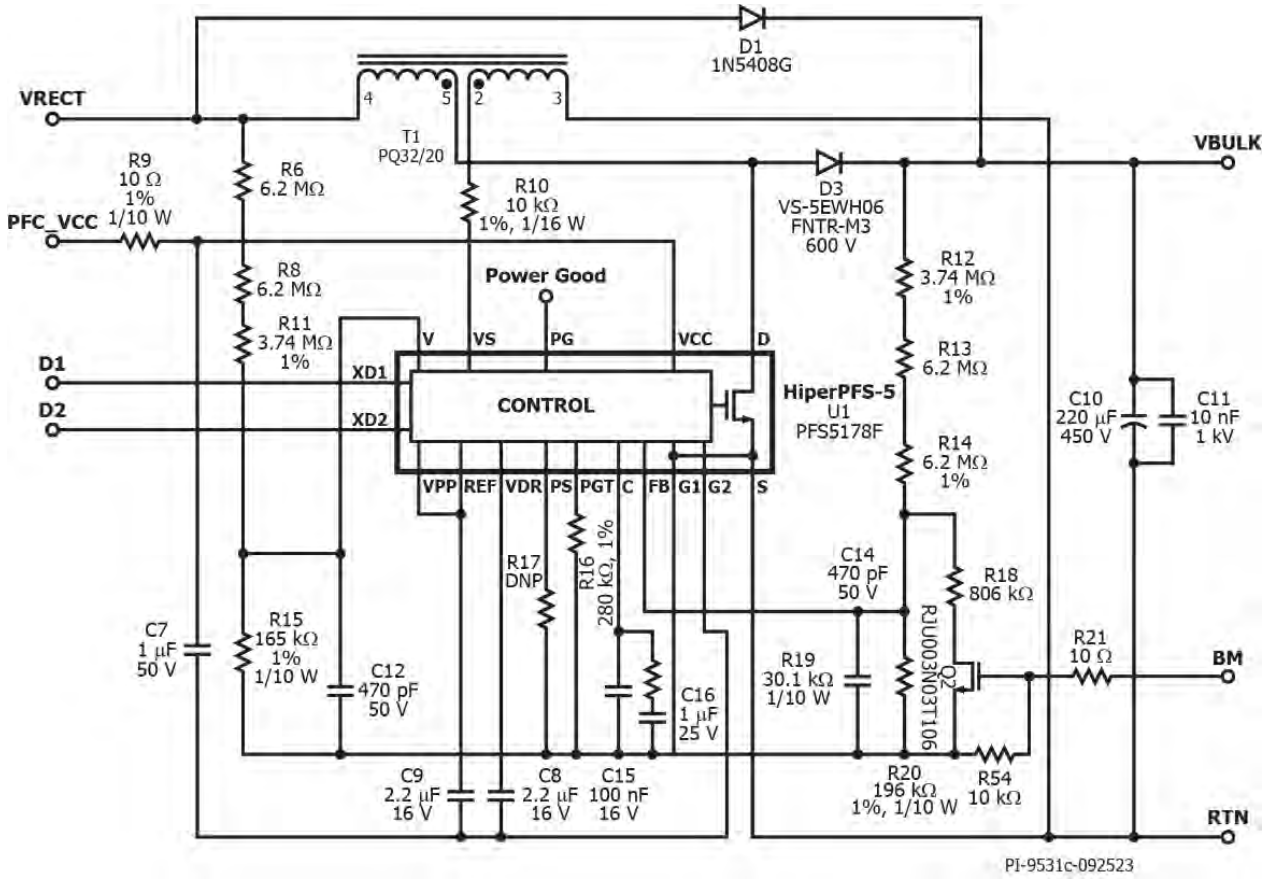


Figure 4 – PFC Stage Schematic.

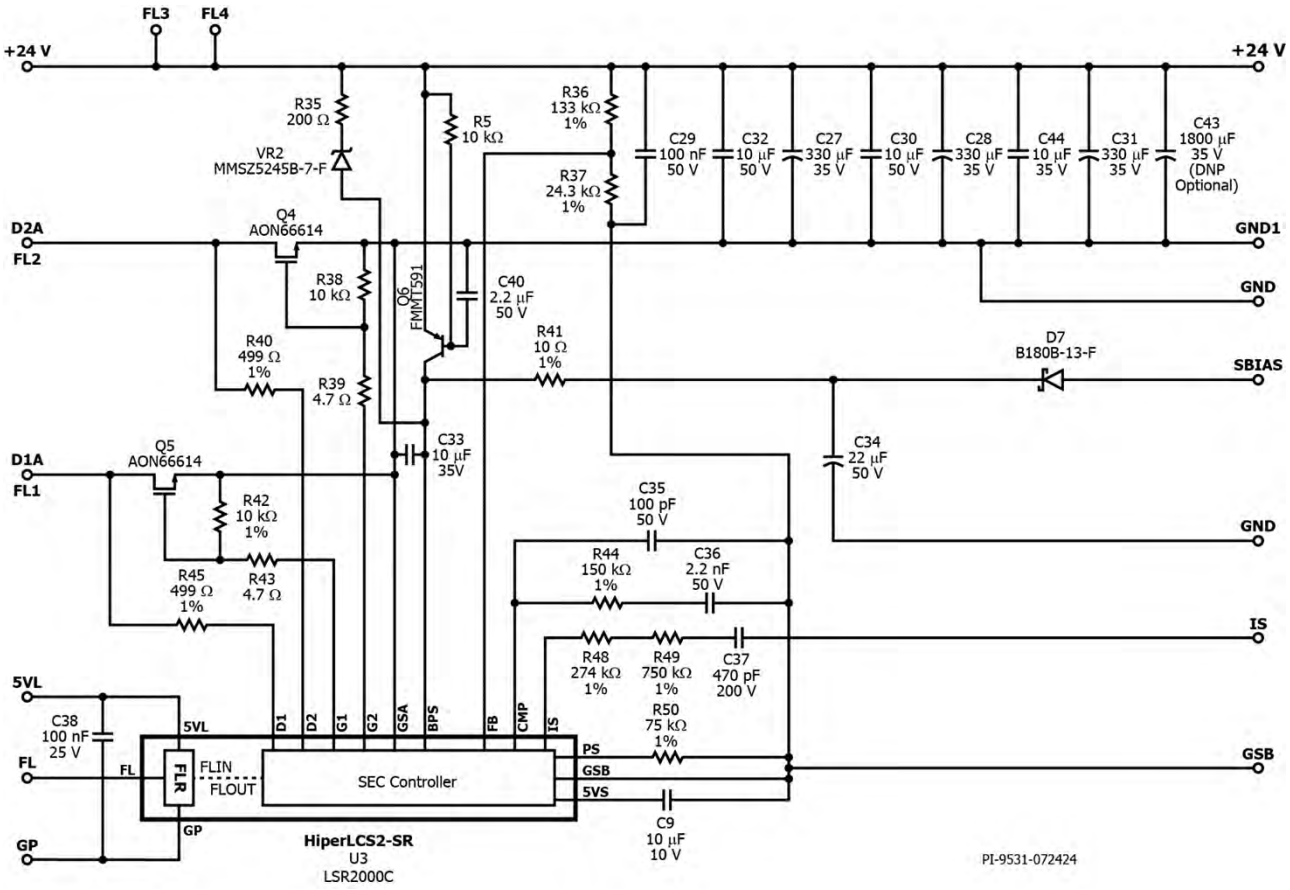


Figure 5– LLC Stage (Primary Section) Schematic.

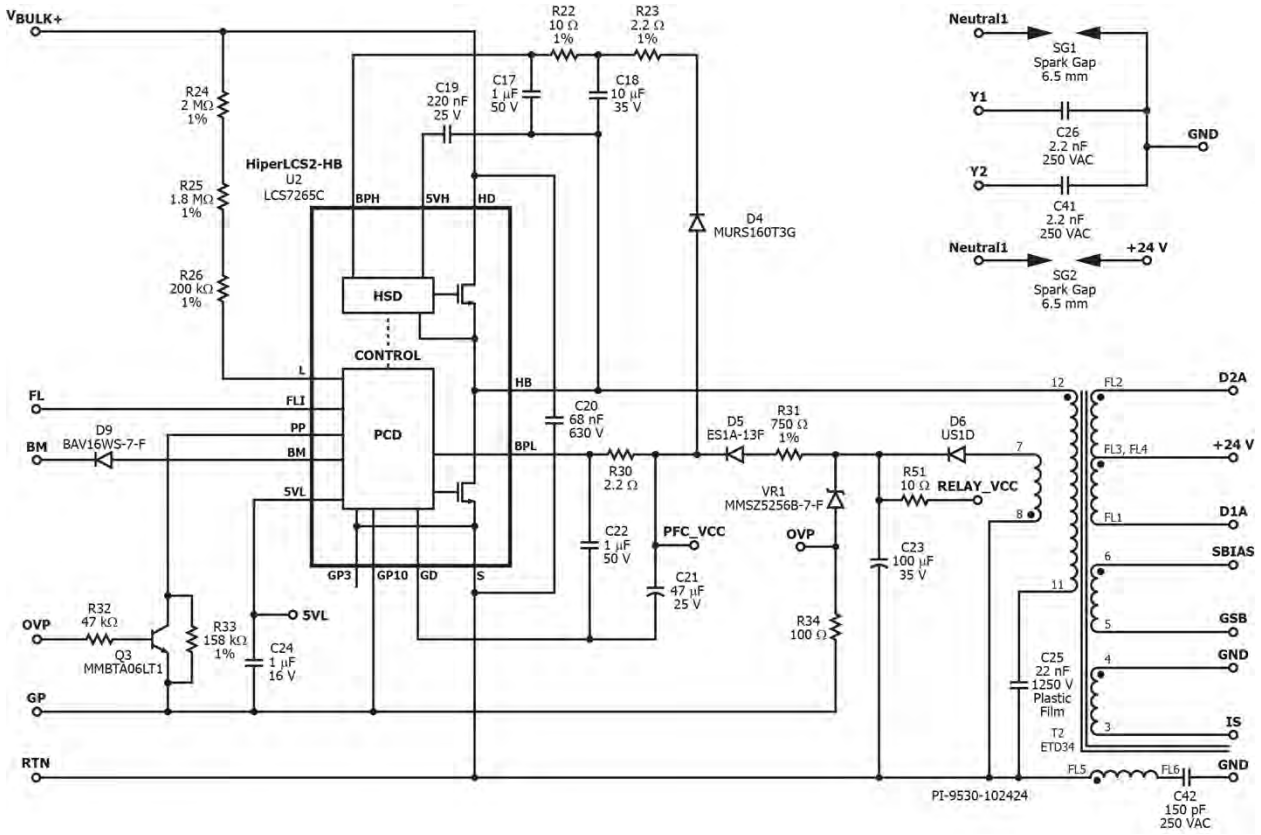


Figure 6– LLC Stage (Secondary Section) Schematic.

4 Circuit Description

4.1 *EMI Filtering / Rectifier Stage*

Figure 3 shows the schematic of the EMI and Rectifier Section/Stage. Fuse F1 protects in case of a primary overcurrent fault/failure. Varistor RV1 protects against differential mode line surge. Inductors L2 and L3 are used to control common mode noise, while C1, C2, C3, and L4 are used to control differential mode noise. Resistors R1 and R2 are connected to the integrated X-capacitor discharge pin of HiperPFS-5 IC to bring down the voltage across C1 and C2 to safe levels when the PSU is disconnected from the AC mains. AC input is rectified through bridge diode BR1 and a 10 Ω thermistor RT1 is used to limit inrush current during start-up. RL1 is used to bypass thermistor RT1 after initial start-up, its operation is controlled by BM pin from HiperLCS-2 HB (U2), when a significant amount of load is drawn from the main output, BM pin will transition from low to high which will turn-on Q1 to provide current to the coil of RT1 shorting out RT1 to maximize efficiency. On the other hand, during very light loads/ no load condition BM will transition from high to low, de-energizing RL1 which will result in lower input power consumption.

4.2 *PFC Stage*

Figure 4 is the schematic of the PFC stage containing the HiperPFS-5 controller (U1). T1 is the magnetic component or PFC choke with auxiliary winding for valley sensing. D1 is the bypass diode used to pre-charge bulk capacitor C10 and inrush current path when AC is first applied before PFC operates. D3 is the boost diode while components R12, R13, R14, and R20 provide output voltage feedback to U1. Additional feedback components R18 and Q2 is used to change the PFC voltage between 320V and 400V which is also controlled by BM pin of U2, at very light loads and no load, condition PFC voltage is set to 320V to minimize input power consumption. PFC voltage will then shift to 400V when significant amounts of load is applied on the output for better system efficiency. Components R19, C15, and C16 are for loop compensation. Resistors R6, R8, R11, and R15 provide input voltage information to U2. ZVS is achieved by sensing the inductor voltage from an auxiliary winding in the PFC choke that is fed to U1 through resistor R10. Capacitor C9 is used as an external bypass capacitor to supply control circuitry inside U1. Capacitor C8 is used as bypass capacitor to supply the driver section of U1. Resistor R16 is used to set the bulk voltage level in which the PG pin (pin 7 of U1) will be on high impedance state, this will signal the DC-DC stage to turn off when the bulk voltage is low. Resistor R17 is used to program the power delivery of HiperPFS-5 IC, if left open it will deliver 100% of the nominal power.

4.3 *LLC Stage*

The schematic in Figure 5 shows the primary power section of the LLC containing the integrated half-bridge MOSFETs while Figure 6 shows the main controller/ isolation device of the LLC which allows secondary side feedback sensing and SR management.

4.3.1 *LLC Primary*

The high-voltage input-bus is filtered through capacitor C10. Line sense (L pin) detects input bus voltage via resistors (R24, R25, and R26). A power-good (PG) signal can be received at PP-pin via resistors (R27, and R28) and is referenced to 5VL (pin 6 of U2). The LCS2-HB (U2) will initiate soft-start when L-pin rises above UVplus threshold or if PG pin of PFC-stage (Hiper-PFS5), is asserted (pulled low). Primary-side detected output overvoltage is sensed from the primary bias-winding (pins 7 and 8 of transformer T2), via Zener diode VR1 and resistor R34 and coupled to the PP pin via resistor R32 and transistor Q3. When overvoltage occurs, Zener VR1 conducts and current will be pulled from PP pin to ground via transistor Q3. Resistor R33 programs the PP pin primary frequency range and fault-response. Diode D9 may couple from BM pin to an external in-rush relay drive circuit and/or command to change PFC voltage as a function of light-load. Note BM transitions to low state when in light load burst mode.

Capacitors C24 and C22, decouple the 5VL and BPL respectively to GP (small signal primary ground). The primary return power-ground (RTN) is connected to S-pin (SOURCE), primary-bias winding and capacitor. The RTN ground is kelvin connected to the negative-pin of bulk-capacitor C10. From a layout point of view, it is very important to keep the small signal GP ground, separate from system power-ground (RTN). Note: the RTN power-ground is intended to offer the low-impedance path for system noise events, whereby secondary coupled noise currents can be safely delivered to RTN/bulk-cap ground without disturbing primary small-signal ground (GP).

Diode D6 rectifies primary bias winding voltage and capacitor C23 decouples to RTN ground. Capacitor C22 provides local high-frequency cycle-to-cycle decoupling at the BPL-pin. Before switching the BPL pin charges both capacitor C22, and C21 (via resistor R30). Capacitor C21 provides sufficient energy storage to sustain startup switching prior to primary bias winding contribution. Capacitor C21 is sized to also provide boot-strap energy to the LCS-2 high-side bias via diode-D4 and resistor R23. Capacitor C21 also provides start-up bias to external PFC stage. Capacitor C21 should be sized to provide sufficient bias energy during startup and for bootstrap, the capacitance of C21 should be greater than 5x the capacitance of high-side bias capacitor C18.

Resistor R30 limits output current from BPL in the event of a large current draw from external PFC stage. Diode D5 is used as blocking diode, to block BPL charge current to C23 prior to bias-winding activation. During normal operation the bias current comes from the bias winding to capacitor C23. The BPL-pin has an internal shunt regulator to limit BPL voltage. Resistor R31 limits the BPL shunt-current when BPL shunt-voltage-clamping is active. This in turn limits the power-dissipation in the BPL during this condition. Note: pay careful attention to the steady state bias-winding voltage. If voltage is above BPL clamp threshold, this may lead to additional unnecessary dissipation in the BPL circuit and thereby risk unintentional thermal shutdown of LCS-2. Note that the bias winding voltage may vary over a 25% range from zero to full output load. For best no-load performance, the bias winding is intended to deliver a minimum of 15 V to the bias winding at zero load

conditions, while the shunt will engage if the bias winding grossly exceeds 21 V at the BP pin.

High-side bootstrap is charged via diode D4, then resistor R23 into capacitor C18 during low-side power MOSFET-on period. During the first few switching cycles at startup, capacitor C18 typically starts with no charge and resistor R23 limits the bootstrap current into capacitor C18. The C18 charge current flows through the low-side power MOSFET, so the removal of resistor R23 may result in safety current limit being triggered under start-up conditions. Resistor R22 and capacitor C17 provide further low-frequency filtering to the BPH pin. High-side 5VH is decoupled via capacitor C19. Note that all high-side decoupling is with reference to HB-pin.

Resonant tank inductor components T2 pins 11/12 (integrated transformer includes resonance inductance LR and magnetizing inductance LM), are connected from HB in series through resonant capacitor C25 to primary return RTN (primary power ground). Capacitor C42 (coupled to RTN), is a safety Y-cap used to couple an inverted primary winding signal from an auxiliary winding to the secondary ground to cancel out common mode noise across the isolation barrier which helps lower conducted EMI emissions.

4.3.2 *LLC Secondary*

The LSR-SR (U3) has isolated primary side pins. Pin 5VL receives 5VL voltage from LCS2-HB. Pin GP couples to primary small signal ground (GP). Capacitor C38 provides local decoupling to the 5VL and GP pins of U3. The FL pin provides a fluxlink signal to the primary LCS-HB.

Transformer output pins T2 FL3/FL4 provide the positive output voltage, which is rectified and filtered by capacitors C27, C28, C29 C30, C31, C32, C43, and C44. These capacitors combine to provide low ESR which mostly defines the output ripple of the system, and their combined capacitance should be chosen to match the desired burst off-time. These capacitors are decoupled to secondary power ground (GND). Transformer output pins T2 FL1/FL2 respectively provide the transformer return path via synchronous rectifier MOSFETs Q4 and Q5. The secondary power path is from T2 FL3/FL4 through capacitors C27, C28, C29, C30, C31, C32, C43, and C44 and the return path via MOSFETs Q4 and Q5 to transformer T2 FL1/FL2. Note: for best matching of the two secondary power-phases, it is important to equalize the secondary power path such that path-lengths via Q4 and Q5 are equal.

Capacitor C33 decouples the BPS to GSA (secondary SR-drive ground). Capacitor C39 decouples 5VS to GSB (secondary small signal ground). Diode D7 and capacitor C34, rectify and filter the secondary bias winding T2 pin 6 (with respect to output power ground GND). Resistor R41 forms an additional high-frequency filter to capacitor C33.
At start-up the LCS2-HB primary side controls switching until the LCS2-SR secondary takes control. During primary control the output voltage will continue to rise. There is a period

of time (T_{WAKE}), from when the secondary BPS voltage exceeds UV-plus, to when the LCS2-SR is ready to take system control. In some applications the BPS (bias winding voltage) rises more slowly than Vout (+24V) which allows Vout to exceed regulation prior to secondary control. To avoid this situation, components Q6, R5 and C40 form a start-up circuit to provide fast initial bias to BPS directly from Vout prior to secondary bias winding activation. In some designs, Zener Diode VR2 and R35 may be required to provide a small pre-load to ensure output maintains regulation during no load conditions.

Small signal secondary ground GSB is used for feedback and compensation. Output voltage is sensed via resistor R36 and R37 with local capacitor decoupling C29 to GSB (small-signal secondary ground), to remove any high-frequency noise.
Compensation is provided between CMP and GSB, via components R44, C35 andC36 which provide a pole (R44, C36) and zero (R44, C35) and a final pole (C35). The transformer IS winding T2 pin 3 (T2 pin 4 grounded to GSB secondary small signal -ground), provides a high frequency medium voltage small-signal which is capacitor coupled via C37 and then via resistors R48 and R49 to the IS pin.

Synchronous MOSFET Q4 and Q5 drive is coupled from G1 and G2 pins via resistors R39 and R43. The drive resistors are optional and intended to limit super high-frequency MOSFET drive ring. In the case of FMEA open-connection condition from G1 and G2 to Q1 and Q2 gate, local pull-down resistors R38 and R42 are present to ensure the MOSFET Q4 and Q5 remain off. SR-ground GSA is used to return SR-gate-drive. The D1 and D2 pins sense the synchronous rectifier Q4 and Q5 drain voltages via resistors R40 and R45, respectively. The resistors are required to limit below-ground sensing current into the D1 and D2 pins. These resistor values can be increased to offer adjustment to SR turn-off threshold. Increasing resistor value will cause SR to turn off at higher SR current. Note: the D1 and D2 signal paths, are from Pins D1 and D2 to resistors R40 and R45 and through the SR-MOSFETs (Q4, Q5) to and back to GSA. The total path length D1, R45, Q5, GSB and D2, R40, Q4, GSB should be equal, to ensure optimal SR functionality.

The PS pin resistor R50 programs secondary-side user selection such as burst threshold option, CV or CC mode.

5 PCB Layout

Below shows the printed circuit board (PCB) used for the unit under test (UUT). Shown are the top (Figure 7) and bottom (Figure 8) side layout for reference and information on the connection and routing of the components. The dimensions of the board are 83mm x 168mm.

PCB specifications:

- Layer count: 2 layers
- Solder mask: Green
- Silkscreen: White
- Finish: LF HASL
- Board Thickness: 1.6 mm
- Copper Thickness: 2 oz (2.8 mils)
- Material: FR4

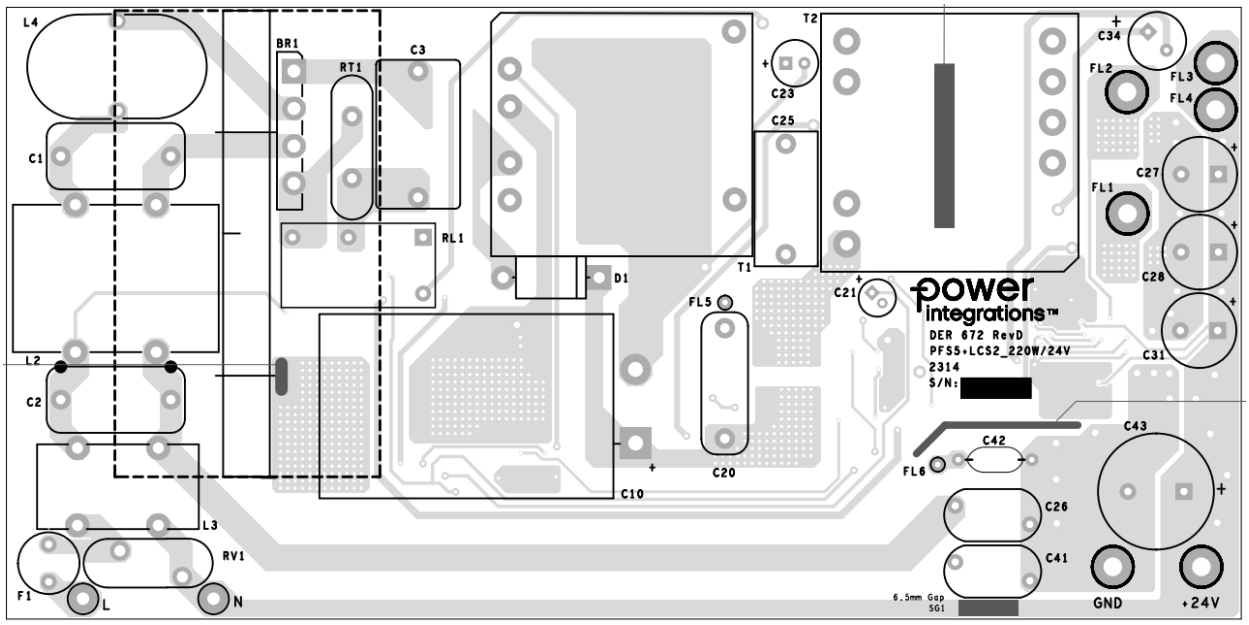


Figure 7 – Top Side PCB.

Figure 8 –Bottom Side PCB.

6 Bill of Materials

6.1 ***Electrical Parts***

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 8 A, Bridge Rectifier, GBU Case	GBU8K-BP	Micro Commercial Co.
2	2	C1 C2	CAP, FILM, 0.33 uF, 20%, 760VDC (330VAC), RAD	B32912B3334M	Epcos
3	1	C3	470 nF, 630 V, Polypropylene Film	ECW-F6474JL	Panasonic
4	3	C5 C18 C33	10 µF ±10% 35V Ceramic Capacitor X5R 0805 (2012 Metric)	C2012X5R1V106K125AC	TDK Corporation
5	1	C7	1 uF, ±10%, 50 V, Ceramic, X5R, -55°C ~ 85°C, 0603 (1608 Metric),	CL10A105KB8NNNC	Samsung Electro-Mechanics
6	2	C8 C9	2.2 uF, ±10%, 16 V, Ceramic, X7R, -55°C ~ 85°C, 0402 (1005 Metric)	GRM155R61C225KE44D	Murata
7	1	C10	220 µF, 450 V, Aluminum Electrolytic Capacitors Radial, Can - Snap-In, 1.206Ohm @ 120Hz, 3000 Hrs @ 85°C, (25 x 40)	SLPX221M450C7P3	Cornell Dubilier Electronics (CDE)
8	1	C11	10 nF, 1k V, Ceramic, X7R, 1812	VJ1812Y103KXGAT	Vishay
9	2	C12 C14	470 pF, ±5%, 50V, C0G, NP0, -55°C ~ 125°C, Low ESL, 0402 (1005 Metric)	C0402C471J5GACTU	Kemet
10	1	C15	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
11	1	C16	1 uF 25 V, Ceramic, X5R, 0402 REPLACEMENT FOR 20-09142-00 a replacment for 20-00844-00	TMK105BJ105MV-F	Taiyo Yuden
12	2	C17 C22	1 uF, ±10% ,50 V, Ceramic, X7R, Boardflex Sensitive, 0805 (2012 Metric),-55°C ~ 125°C	CGA4J3X7R1H105K125AE	TDK Corp
13	1	C19	220 nF, 25 V, Ceramic, X7R, 0805	CC0805KRX7R8BB224	Yageo
14	1	C20	68 nF, 630 V, Film	ECQ-E6683KF	Panasonic
15	1	C21	47 uF, 25 V, Electrolytic, Very Low ESR, 300 mOhm, (5 x 11)	EKZE250ELL470ME11D	Nippon Chemi-Con
16	1	C23	100 uF, 35 V, Electrolytic, Low ESR, 180 mOhm, (6.3 x 15)	ELXZ350ELL101MF15D	Nippon Chemi-Con
17	1	C24	1 uF 16 V, Ceramic, X7R, 0603	CL10B105KO8VPNC	Samsung
18	1	C25	22 nF, 1250 V, Film	B32652A7223J	Epcos
19	2	C26* C41	3.3 nF, Ceramic, Y1	440LD33-R	Vishay
20	3	C27 C28 C31	330µF, ±20%, 35V, Aluminum Polymer Capacitor Radial, Can, 18mOhm, 1000 Hrs @ 125°C	35SEK330M	Panasonic
21	1	C29	0.1 µF (100 nF) ±10% 50V Ceramic Capacitor X7R 0603 (1608 Metric)	GCM188R71H104KA57D	Murata
22	3	C30 C32 C44	10µF, 10%, 50V, Ceramic, X7R, -55°C ~ 125°C, 1206 (3216 Metric), 0.126" L x 0.063" W (3.20mm x 1.60mm)	CL31B106KBHNNNE	Samsung Electro-Mechanics America, Inc.
23	1	C34	100 uF, 50 V, Electrolytic, Very Low ESR, 74 mOhm, (8 x 11.5)	EKZE500ELL101MHB5D	Nippon Chemi-Con
24	1	C35	100 pF 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
25	1	C36	2.2 nF 50 V, Ceramic, X7R, 0603	C0603C222K5RACTU	Yageo
26	1	C37	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
27	1	C38	100 nF, 0.1µF, ±10%, 25V, Ceramic Capacitor, X7R, General Purpose, -55°C ~ 125°C, 0603 (1608 Metric)	CL10B104KA8NFNC	Samsung Electro-Mechanics
28	1	C39	10 µF, ±10%, 16V, X7R, Ceramic Capacitor, Surface Mount, MLCC 0805 (2012 Metric)	CL21B106KOQNNNE	Samsung
29	1	C40	2.2 uF, ±10%, 50 V, Ceramic, X7R, 0805 (2012 Metric)	UMK212BB7225KG-T	Taiyo Yuden
30	1	C42	150 pF ±10%, 440VAC, X1, Y1, Ceramic Capacitor B, Radial, Disc,0.256" Dia (6.50mm),LS 0.394" (10.00mm)	CD45-B2GA151K-NKA	TDK Corporation

31	1	C43	1800 uF, 35 V, Electrolytic, Very Low ESR, 16 mOhm, (16 x 25)	EKZE350ELL182ML25S	Nippon Chemi-Con
32	1	D1	1000 V, 3 A, Recitifier, DO-201AD	1N5408G	ON Semiconductor
33	1	D2	Diode, Low Leakage, 85 V, 200 mA, SOD323	BAS416,115	NXP Semiconductors
34	1	D3	Diode, Standard, 600 V, 5A, Surface Mount, D-PAK (TO-252AA), TO-252-3, DPak (2 Leads + Tab), SC-63	VS-5EWH06FNTR-M3	Vishay General Semiconductor - Diodes Division
35	1	D4	600 V, 1 A, Ultrafast Recovery, 35 ns, SMB Case	MURS160T3G	On Semi
36	1	D5	50 V, 1 A, General Purpose, DO-214AC	ES1A-13-F	Diode Inc.
37	1	D6	DIODE ULTRA FAST, SW, 200V, 1A, SMA	US1D-13-F	Diodes, Inc
38	1	D7	80 V,1 A, Schottky, SMD, DO-214AA	B180B-13-F	Diodes Inc
39	1	D9	75 V, 0.15 A, Switching, SOD-323	BAV16WS-7-F	Diode Inc.
40	1	F1	5 A, 250V, Slow, TR5	37215000411	Wickman
41	1	L2	Common Mode Choke, 20 mH ±15%, 28mm O.D., 19.5mm Th	32-00436-00	PI
42	1	L3	Common Mode Choke, 2.3 mH, ±15%, 21.7mm O.D., 11.5mm Th	32-00437-00	PI
43	1	L4	330 uH, 3.3 A, Vertical Toroidal	2218-V-RC	Bourns
44	1	Q1	N-Channel, 100 V, 700mA (Ta), 400mW (Ta), Surface Mount SOT-23-3, TO-236-3, SC-59	DMN10H700S-7	Diodes Incorporated
45	1	Q2	MOSFET, N-CH, 30V, 300MA, SOT-323	RJU003N03T106	Rohm Semi
46	1	Q3	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1	Infineon Tech
47	2	Q4 Q5	MOSFET, N-Channel,60 V,80 A, 56.5 (Tc), 5.0W (Ta), Surface Mount, 8-DFN-EP (5x6)	AONS666140	Alpha & Omega Semiconductor Inc.
48	1	Q6	PNP, 60V 1000MA, SOT-23	FMMT591TA	Zetex Inc
49	2	R1 R2	RES, 75.0 k, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7502V	Panasonic
50	5	R3 R4 R9 R21 R22	RES, 10 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
51	4	R5 R38 R42 R53	RES, 10 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
52	3	R6 R8 R13	RES, 6.2 M, 5%, 1/4 W, Thick Film, 1206	RC1206FR-076M2L	YAGEO
53	1	R10	RES, 10.0 k, 1%, 1/16 W, Thick Film, 0402	RC0402FR-0710KL	Yageo
54	2	R11 R12	RES, 3.74 M, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay Dale
55	1	R14	RES, 6.2 M, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
56	1	R15	RES, 165.0 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1653X	Panasonic
57	1	R16	RES, 280.0 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2803X	Panasonic
58	1	R17*	RES, 0 R, 1/16 W, Thick Film, 0402	CRCW04020000Z0ED	Vishay Dale
59	1	R18	RES, 806.0 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF8063X	Panasonic
60	1	R19	RES, 30.1 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF3012X	Panasonic
61	1	R20	RES, 196.0 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1963X	Panasonic
62	1	R23	RES, 2.2 R, 1%, 1/16 W, Thick Film, 0603	ERJ-3RQF2R2V	Panasonic
63	1	R24	RES, 2 M, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2004V	Panasonic
64	1	R25	RES, 1.8 M, 1%, 1/16 W, Thick Film, 0805	ERJ-6ENF1804V	Panasonic
65	1	R26	RES, 200 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2003V	Panasonic
66	1	R27*	RES, 22.6 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2262V	Panasonic
67	1	R28*	RES, 20 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ203V	Panasonic
68	1	R30	RES, 2.2 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ2R2V	Panasonic
69	1	R31	RES, 750 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7500V	Panasonic

70	1	R32	RES, 47 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
71	1	R33	RES, 158 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1583V	Panasonic
72	1	R34	RES, SMD, 100, 1%, 1/10W, ±100ppm/°C, -55°C ~ 155°C,0603 (1608 Metric), Moisture Resistant, Thick Film	RC0603FR-07100RL	Yageo
73	1	R35	RES, 200 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ201V	Panasonic
74	1	R36	RES, 133 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1333V	Panasonic
75	1	R37	RES, 24.3 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2432V	Panasonic
76	2	R39 R43	RES, 4.7 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ4R7V	Panasonic
77	2	R40 R45	RES, 499 R, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF4990V	Panasonic
78	2	R41 R51	RES, 10 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF10R0V	Panasonic
79	1	R44	RES, 150 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF1503V	Panasonic
80	1	R48	RES, 274 k, 1%, 1/10 W, Thick Film, 0603	ERJ-3EKF2743V	Panasonic
81	1	R49	RES, 750 k, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF7503V	Panasonic
82	1	R50	RES, 75 k, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ753V	Panasonic
83	1	R54	RES, 10 K, 5%, 1/16 W, Thick Film, 0402	RC0402JR-0710KL	Yageo
84	1	RL1	RELAY, GEN PURPOSE, SPST, 5A, 24V, PC Mount, 1 Form A	G6B-1114P-US-DC24	OMRON
85	1	RT1	NTC Thermistor, 10 Ohms, 5 A	CL-60	GE Sensing
86	1	RV1	320 Vac, 80 J, 14 mm, RADIAL	V320LA20AP	Littlefuse
87	1	T1	Bobbin, PQ32/20, Vertical, 12 pins	YC-PQ3220	Ying Chin
88	1	T2	Bobbin, ETD34, Horizontal, 12 pins	WS-53404	Win Shine Tech Inc.
89	1	U1	PFGCZ test symbol with 28 pins AND EP, InSOP-T28F	PFGCZ	Power Integrations
90	1	U2	HiperLCS2-HB, LCS7265C, InSOP-24C	LCS7265C	Power Integrations
91	1	U3	HiperLCS2-SR, LSR2000C-H002, InSOP-24D	LSR2000C-H002	Power Integrations
92	1	VR1	DIODE ZENER 30V 500MW SOD123	MMSZ5256B-7-F	Diodes, Inc
93	1	VR2	DIODE ZENER 15V 500MW SOD123	MMSZ5245B-7-F	Diodes, Inc

** Do Not Populate (DNP), refer to schematic notes if need to populate*

6.2 ***Mechanical Parts***

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	HS1	FAB, HEATSINK, DER-672 Bridge, AL, 3003, .080”	PI Custom	Custom
2	1	LINE	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
3	1	NEUTRAL	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
4	1	TE1	Terminal, Eyelet, Tin Plated Brass	190	Zierick

7 Magnetics

7.1 ***PFC Choke (T1) Specification***

7.1.1 *Electrical Diagram*

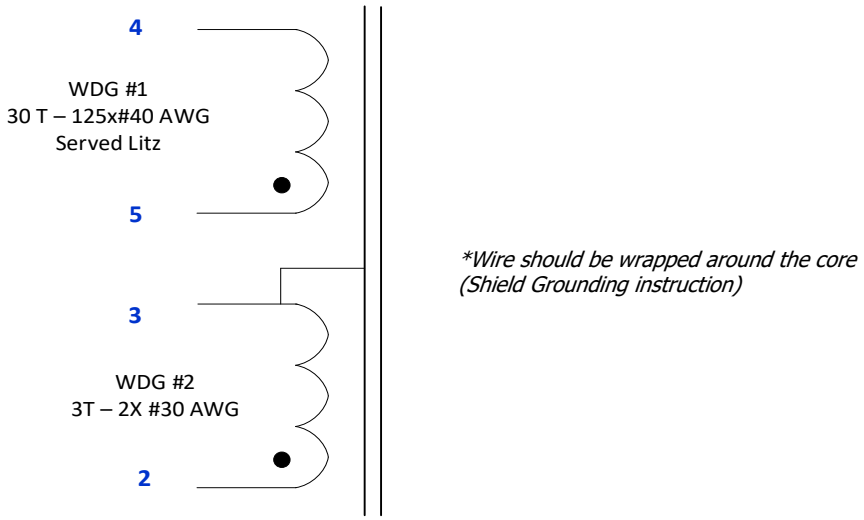


Figure 9 – PFC Choke Electrical Diagram.

7.1.2 *Electrical Specifications*

Inductance	Pins 4-5 measured at 100 kHz, 0.4 V_{RMS}.	140 µH ±5%

7.1.3 *Material List*

Item	Description
[1]	Core: TDK PC95PQ32/20Z-12.
[2]	Bobbin: PQ32/20, Vertical, 12 Pins.
[3]	Litz Wire: 125 x #40 AWG Single Coated Solderable, Served.
[4]	Magnet Wire: #30 AWG.
[5]	Tape, Polyester Film: 3M 1350-F1 or Equivalent, 9 mm Wide.
[6]	Varnish: Dolph BC-359, or Equivalent.
[7]	#33 Bus Wire

7.1.4 *Inductor Build Diagram*

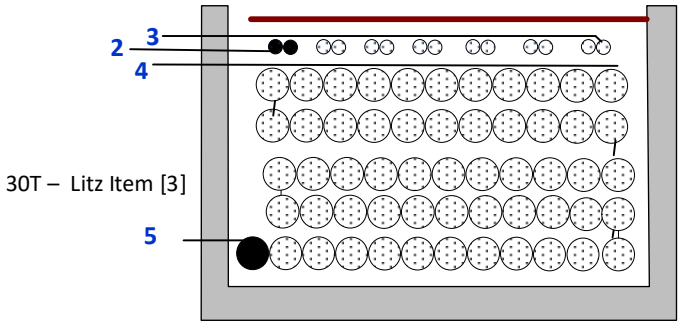


Figure 10 – PFC Choke Build Diagram.

7.1.5 *Inductor Illustrations*

Bobbin Pin-out reference:

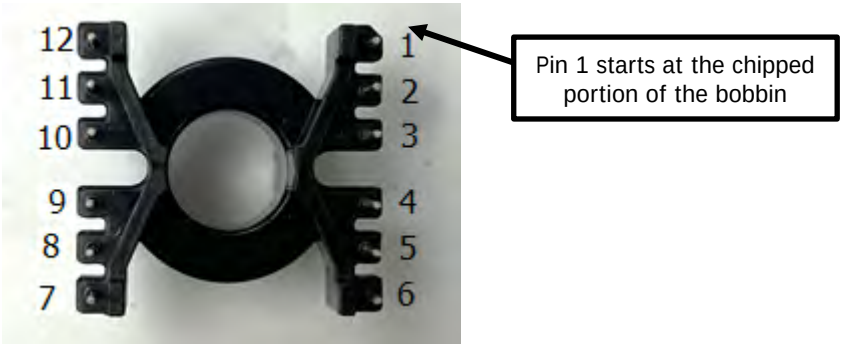
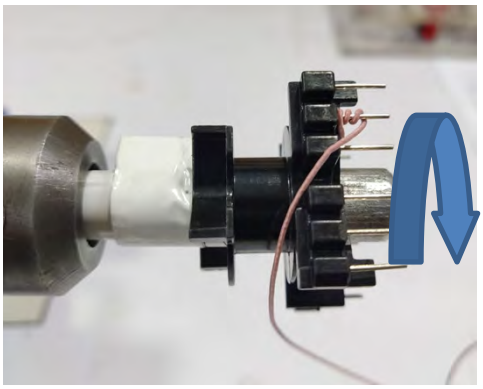
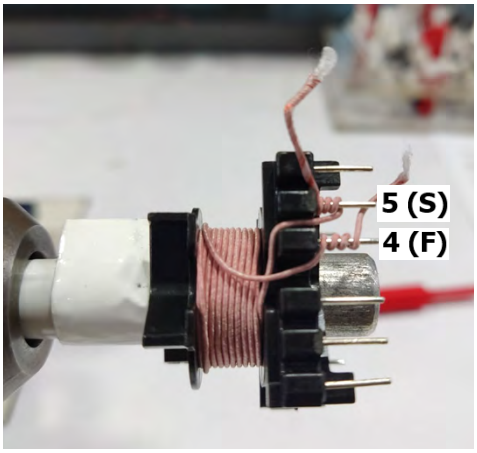
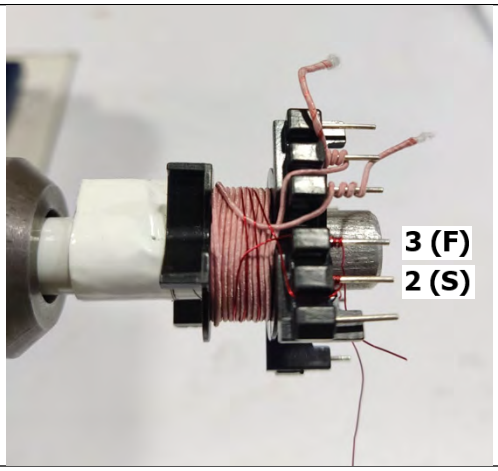
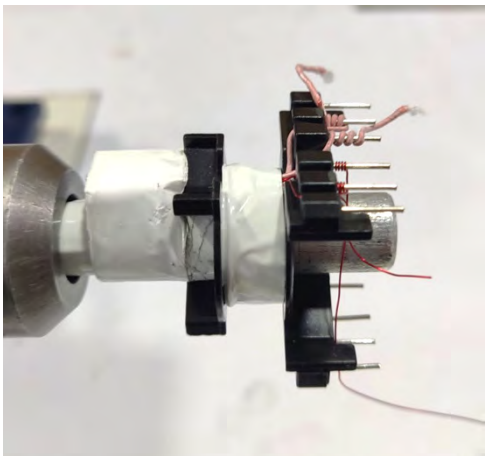
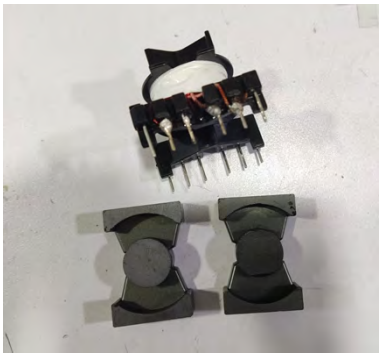
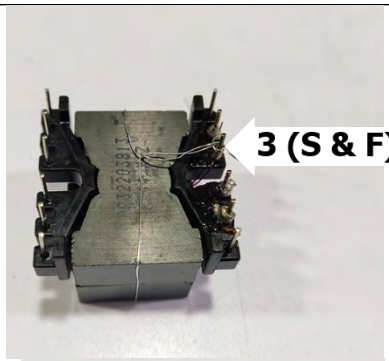
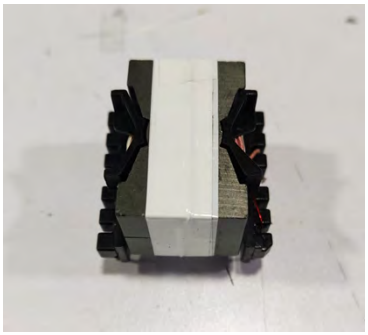


Figure 11 – PFC Choke Bobbin Pin-out (bottom view).

Winding Layer	Illustration	Winding Instruction
WD1		Place the bobbin on the mandrel with the pin side to the right. Rotate the bobbin in a clockwise direction i.e. top side moving away from the operator.
		Start at pin 5, wire 30T of item [3] forming 3 layers with tight tension to fill the bobbin width in a neat flat wind. Terminate winding at pin 4.
WD2		Start at pin 2, wire 3T of 2 strands of item [4] in a clockwise direction. Terminate at pin 3.

		
Insulation layer		Add 1T of tape, item [5].
		Solder windings 2, 3, 4 and 5 to their respective pins. Grind core to achieve 140uH inductance.
Shield grounding		Start at pin 3, wind 1T of item [7] across the middle core and terminate at pin 3 as well.

	 	
FINISH		Add 2 to 3 layers of tape along the outside surface of the core. Dip in varnish, item [6] and cure in oven as required.

7.2 *LLC Transformer (T2) Specification*

7.2.1 *Electrical Diagram*

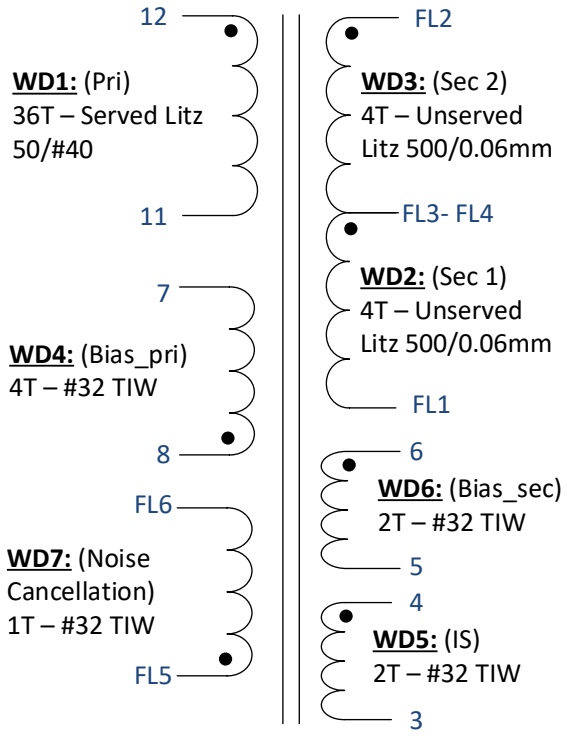


Figure 12 – LLC Transformer Electrical Diagram.

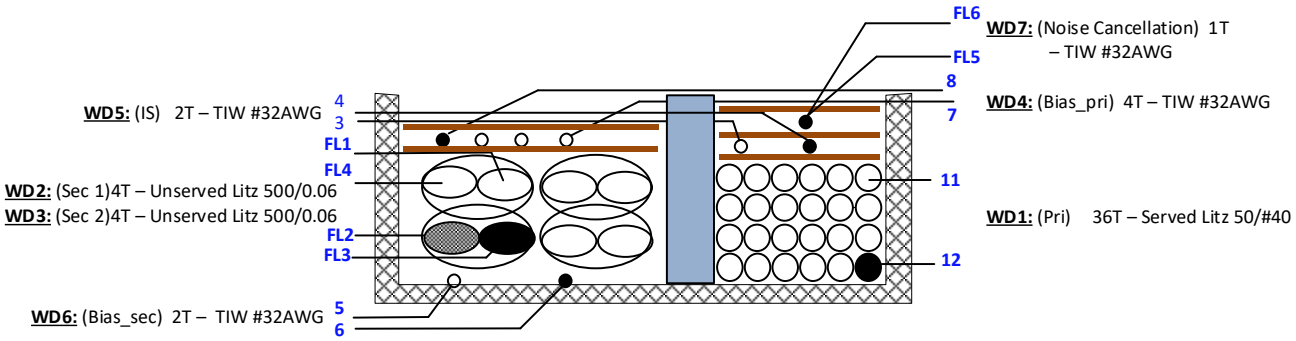
7.2.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 3, 4, 5, 6, FL1-FL3, FL2-FL4 to pins 7, 8, 11, 12.	3000 VAC
Primary Inductance (Lpri)	Pins 11-12, all other windings open, measured at 100 kHz, 1 V_{RMS}	470 µH ±5%
Primary Leakage1 (LlkpALL)	Pins 11-12, short ALL other pins except IS-winding, measured at 100 kHz, 1 V_{RMS}	88.0 µH ±5%
Primary Leakage2 (LkpIS)	Measured at pins 11-12 (100 kHz, 1 V_{RMS}), Short ONLY IS-winding Pins 3&4.	95 µH
Primary Leakage3 (LkpSEC1)	Measured at pins 11-12 (100 kHz, 1 V_{RMS}), Short ONLY FL2, FL3, FL4	85 µH
Primary Leakage4 (LkpSEC2)	Measured at pins 11-12 (100 kHz, 1 V_{RMS}), Short ONLY FL1, FL3, FL4	85 µH
Resonant Frequency (fres)	Pins 11-12, all other windings open	2.2 MHz

7.2.3 *Material List*

Item	Description
[1]	Core: ETD34 – 3C97 (Ferroxcube) or Equivalent.
[2]	Bobbin with Cover: ETD34-H, 12 Pins (6/6).
[3]	Litz Wire: 50/ #40 AWG_Served Litz.
[4]	Litz Wire: 500/0.060 mm_Unserved Litz.
[5]	Triple Insulated Wire: #32 AWG.
[6]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 7 mm Wide.
[7]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 12 mm Wide.
[8]	Teflon tube
[9]	Varnish: Dolph BC-359, or Equivalent.
[10]	Epoxy: Deycon, 5minute Epoxy, Mfg Part No: 14270

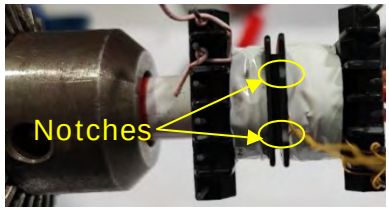
7.2.4 *Build Diagram*



Notes: ***1. WD2(SEC1) & WD3(SEC2) must exit at the top side of the bobbin on removed pins 1&2.***
2. Wire leads 7&8(WD4) should be twisted together before crossing the isolation barrier.
3. Wire leads 3&4(WD5) should be twisted together before crossing the isolation barrier.

Figure 13 – LLC Transformer Build Diagram.

7.2.5 *Winding Preparation*

WD2 & WD3 Secondary	Prepare 2 pc of Item [4] at around 15in. long each. ➢ Put labels on WD2(Sec1) FL1 on one end, FL3 on the other end. ➢ Put labels on WD3(Sec2) FL2 on one end, FL4 on the other end. Tightly twist together WD2 and WD3 with FL1 &FL4 on one end and FL2&FL3 on opposite end. (Needs to be twisted together for balanced leakage inductance between WD2 and WD3).
BOBBIN	Remove pins 1, 2, 9 and 10 to fit bobbin footprint in the PCB. Add a notch across the bobbin spacer to hold the wires crossing from one chamber to another. 

7.2.6 *Transformer Illustrations*

Bobbin Pin-out reference:

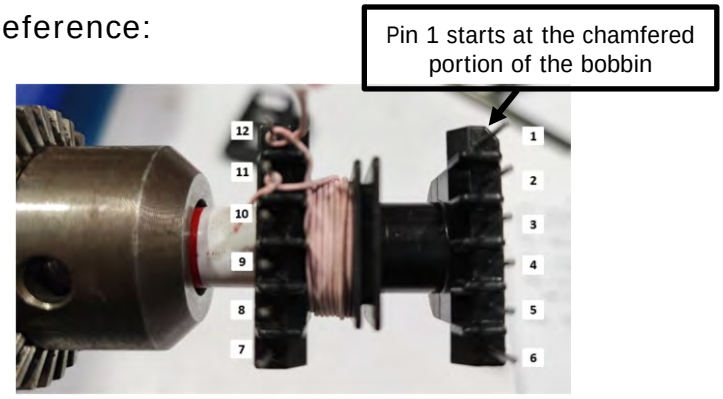
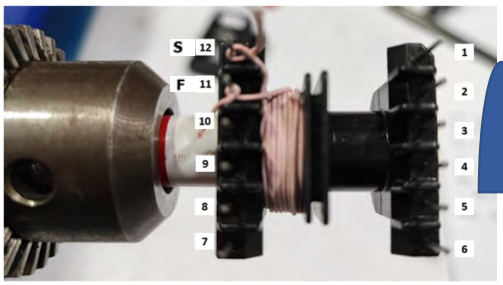
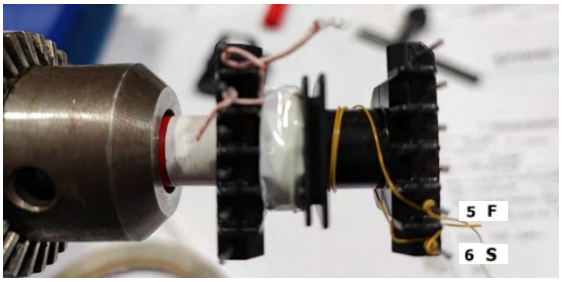
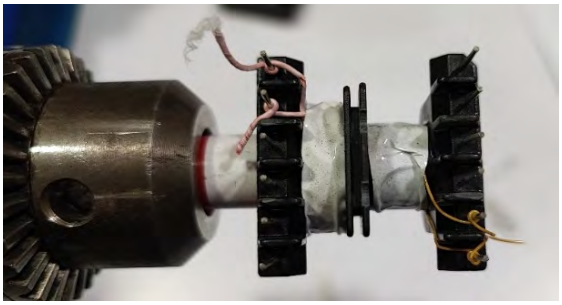
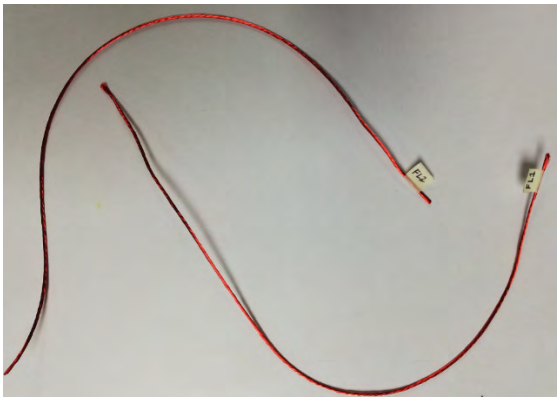
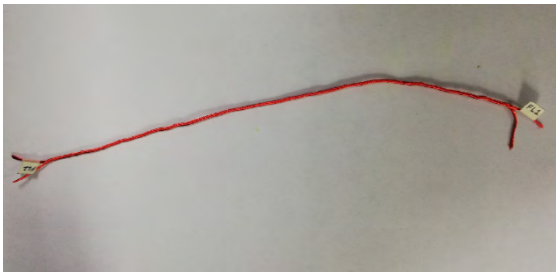
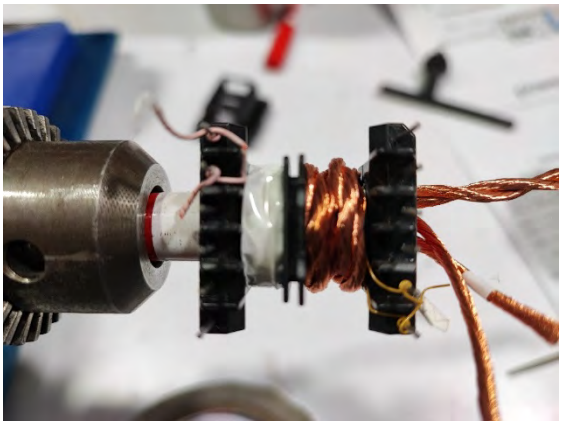
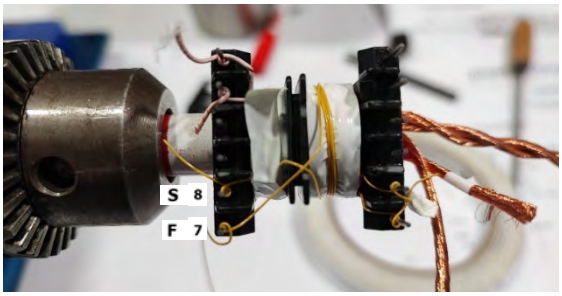
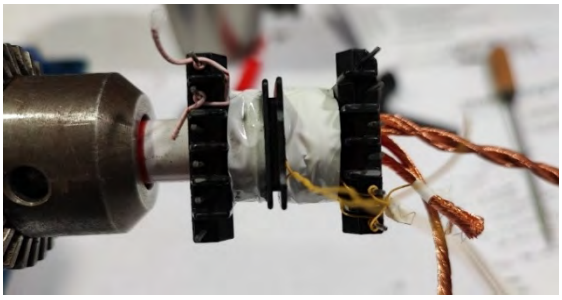
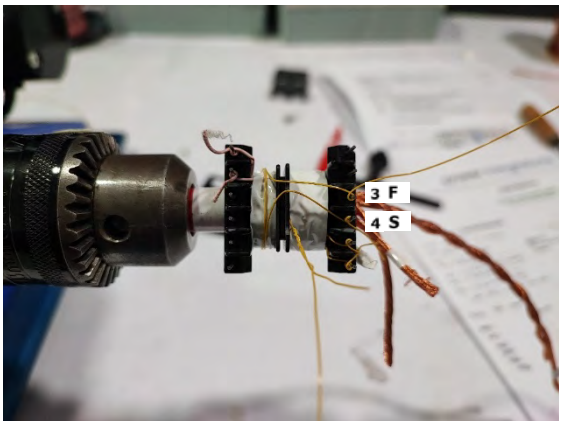
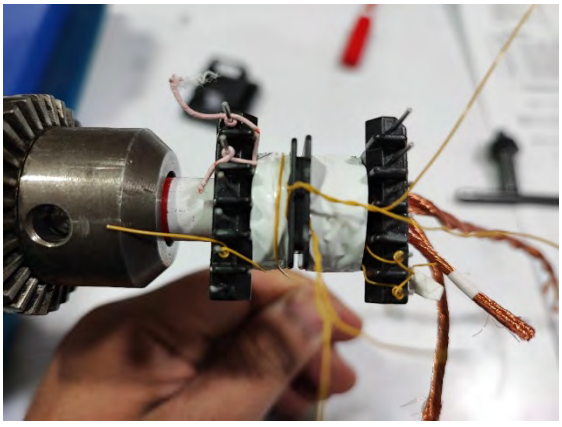
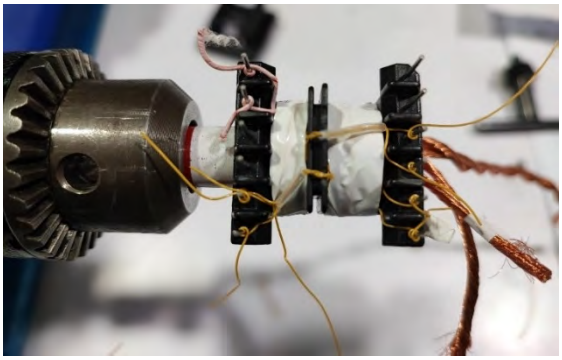
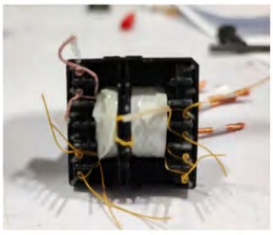
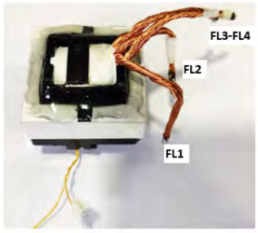
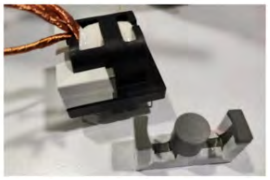
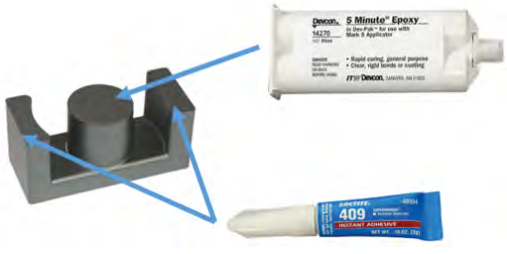
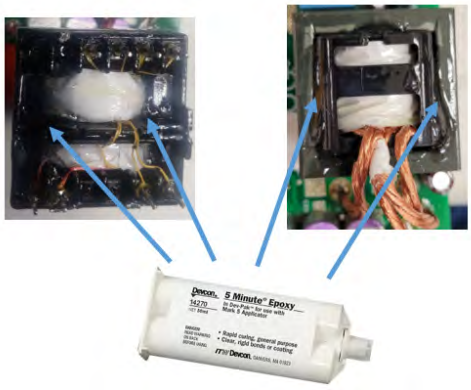


Figure 14 – LLC Transformer Bobbin Pin-out.

Winding Layer	Illustration	Winding Instruction
WD1		Start at pin 12, wind 36 turns of wire item [3] in 1 layer, with tight tension from left to right. At the last turn, terminate the wire back to the left at pin 11. Add 1 layer of tape item [6].
WD6	 	Add 1 layer of tape item [6]. Start at pin 6, wind 2 turns of wire item [5]. Terminate the other end at pin 5. Add 1 layer of tape item [7].

WD2 and WD3	 	Prepare 2 pc of Item [4] at around 16in long for each wire. For the first wire, label one end as FL1 and for the second wire, label one end as FL2. With the labels on different ends, tightly twist both wires using the winding machine (80 – 100 turns).
WD2 & WD3 (Cont.)		Wind 4T of the twisted pair from the top of the bobbin starting at the end labeled FL2. Terminate the other end at the top as well.
WD4		Add 1 layer of tape item [7]. Wind 4T of item [5] starting with pin8 and end on pin7. Wire with cross the bobbin spacer. Mark the dot-end of the wire. Twist the ends of the wire and leave it floating temporarily.

		Add 1 layer of tape item [7] on primary chamber.
WD 5		Wind 2T of item [5] starting with pin4 and end on pin3. Wire with cross the bobbin spacer. Mark the dot-end of the wire. Twist the ends of the wires before crossing the isolation barrier and leave it floating temporarily. Add 1 layer of tape item [7] on primary chamber.
WD7		Wind 1T of item [5] with both ends twisted together and floating from the bottom of the bobbin. Add teflon tube item [8] in both ends of the wire. Add 1 layer of tape item [7] on primary chamber.

WD4 & WD5 Teflon Tubing		Add approximately 10 mm of teflon tubing at the twisted ends of WD4 and WD5 before terminating to their respective pins. Add 1 layer of tape item [6] & [7] on primary and secondary side of the chamber, respectively.
FINISH	   	Solder windings 1, 4, 5 and 6 to their respective pins and enclose the bobbin with its shroud/cover and with windings 2 and 3 exiting from the top. Grind core to achieve 470uH primary inductance.
IMPROVEMENT FOR AUDIBLE NOISE	 	Add epoxy item [10] on the center of the core leg, just enough to fill the gap then add one small drop of glue on the side legs just to hold it in place. Then wrap one layer of tape along the outside surface of the core. Dip the transformer in varnish item [9]. Add epoxy item [10] along the sides of the varnished transformer and allow to dry.

7.3 ***Common Mode Choke (L3) Specification***

7.3.1 *Electrical Diagram*

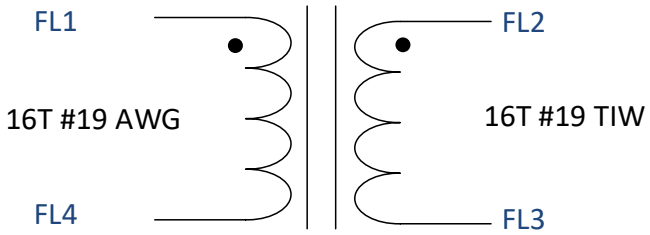


Figure 15 – Inductor Electrical Diagram.

7.3.2 *Electrical Specifications*

Inductance	FL1-4 or FL2-3, measured at 100 kHz, 0.4 V_{RMS}	2.3 mH, ±15%

7.3.3 *Material List*

Item	Description
[1]	Ferrite Core Toroid: Encom Ltd., YJ15K-T18/10/7C. **PI P/N 30-00398-00**
[2]	Magnet Wire: #19 AWG
[3]	Triple Insulated Wire: #19 AWG, Furukawa TEX-E or Equivalent.

7.3.4 *Construction Details*

1. Wind 16 turns of items [2] and [3] together as shown in the figure below.

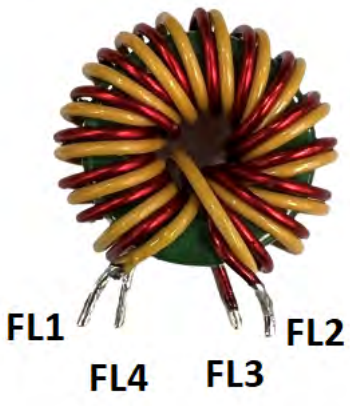


Figure 16 – Finished Inductor.

7.4 ***Common Mode Choke (L2) Specification***

7.4.1 *Electrical Diagram*

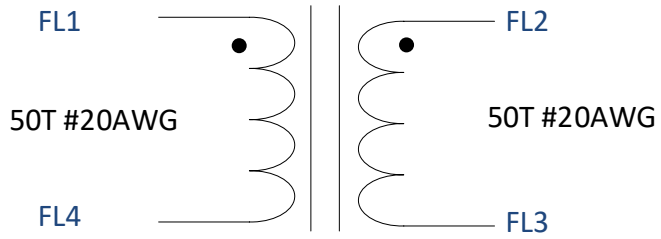


Figure 17 – Inductor Electrical Diagram.

7.4.2 *Electrical Specifications*

Inductance	FL1-4 or FL2-3, measured at 100 kHz, 0.4 V_{RMS}	20mH ± 15%
Leakage Inductance	FL1-4 and short FL2-3, vice versa at 100kHz, 0.4 V_{RMS}	80uH ± 10%
DCR	FL1-4 or FL2-3, measured at 100 kHz, 0.4 V_{RMS}	65mΩ ± 5%

7.4.3 *Material List*

Item	Description
[1]	5975007601 Fair-Rite Core **Non-PI**
[2]	Magnet Wire: #20 AWG
[3]	Winding Spacer (12.85mm width)

7.4.4 *Construction Details*

1. Insert PCB spacer inside the core to equally separate their winding windows. The spacer width should be as thick as the core (min 12.85mm) so that windings (especially the start wdg) are isolated from each other.

Figure 18 – Core Preparation.

2. Core Insulation Instruction
   - After adding the spacer in the core, add a layer of tape (13mm) around it to prevent magnet wire from damage or scratch during winding process.
   - Attach the tape layer from the outside diameter to the inside and then cut the overlaps accordingly so that the edge (both outside and inside) of the core will be covered during folding.

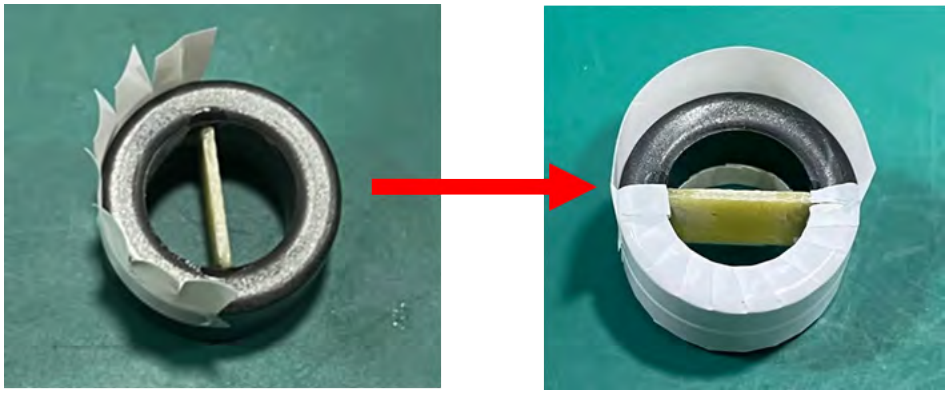


Figure 19 – Core Insulation.

   - Repeat the process until the circumference of the core is fully covered.

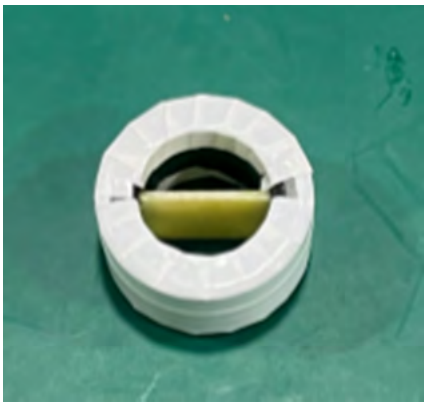


Figure 20 – Finished Core Insulation.

3. Wind 50 turns of item [2] on each side as shown in the figure below.

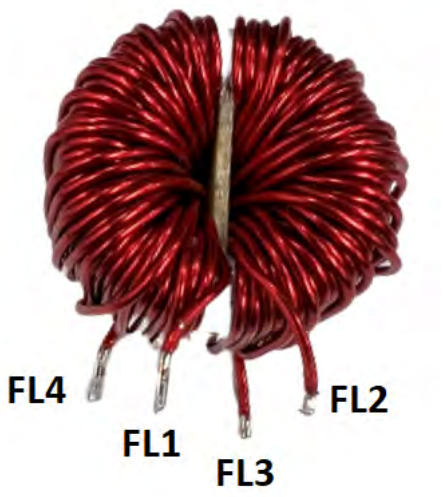


Figure 21 – Finished Inductor.

8 PFC Design Spreadsheet

1	Hiper_PFS-5_Boost_010623; Rev.1.1; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	Discontinuous Mode Boost Converter Design Spreadsheet
2	Enter Application Variables					
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN			90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other voltages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX			265	VAC	Maximum AC input voltage
6	VBROWNIN			82	VAC	Expected Typical Brown-in Voltage per IC specifications; Line impedance not accounted for.
7	VBROWNOUT			71	VAC	Expected Typical Brown-out voltage per IC specifications; Line impedance not accounted for.
8	VO			400	VDC	Nominal load voltage
9	PO	230		230	W	Nominal Output power
10	fL			50	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate	0.9500		0.9500		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			380	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
15	T_HOLDUP			20	ms	Holdup time
16	VHOLDUP_MIN			320	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
19	KP and INDUCTANCE					
20	LPFC_MIN (0 bias)			130	uH	Minimum PFC inductance value
21	LPFC_TYP (0 bias)			137	uH	LPFC value used for calculations. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation.
22	LPFC_MAX (0 bias)			144	uH	Maximum PFC inductance value
23	LP_TOL	5.0		5.0	%	Tolerance of PFC Inductor Value (ferrite only)
24	LPFC_PEAK			137	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
25	KP_ACTUAL			1.11		Actual KP calculated from LPFC_DESIRED
26	Basic Current Parameters					
27	IAC_RMS			2.69	A	AC input RMS current at VACMIN and Full Power load
28	IL_RMS			3.15	A	Inductor RMS current (calculated at VACMIN and Full Power Load)

29	IO_DC			0.58	A	Output average current/Average diode current
30	PFS Parameters					
31	PFS Package			F		HiperPFS package selection
32	PFS Part Number	PFS5178F		PFS5178F		If examining brownout operation, over-ride autopick with desired device size
33	Self-Supply Feature	Yes		Yes		Device self-supply feature. Select "Yes" to select device with self-supply feature or "No" for device without self-supply
34	PS_FACTOR	1.0		1.0		Programmable output power selection factor
35	PO_MAX_DEV			240	W	Maximum output power of the device
36	IOCP min			8.09	A	Minimum Current limit
37	IOCP typ			9.30	A	Typical current limit
38	IOCP max			10.51	A	Maximum current limit
39	IP			7.07	A	MOSFET peak current
40	IRMS			2.73	A	PFS MOSFET RMS current
41	RDSON			0.21	Ohms	Typical RDSon at 100 'C
42	FS_PK			85.9	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
43	FS_AVG			75.5	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
44	PCOND_LOSS_PFS			1.568	W	Estimated PFS Switch conduction losses
45	PSW_LOSS_PFS			0.030	W	Estimated PFS Switch switching losses
46	PFS_TOTAL			1.598	W	Total Estimated PFS Switch losses
47	TJ Max			100	deg C	Maximum steady-state junction temperature
48	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
49	HEATSINK Theta-CA			34.75	°C/W	Maximum thermal resistance of heatsink
50	INDUCTOR DESIGN					
51	Material and Dimensions					
52	Core Type	Ferrite		Ferrite		Enter "Sendust", "Iron Powder" or "Ferrite"
53	Core Material	PC44/PC95		PC44/PC95		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
54	Core Geometry	PQ		PQ		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
55	Core	PQ32/20		PQ32/20		Core part number
56	Ae			170.00	mm^2	Core cross sectional area
57	Le			55.50	mm	Core mean path length
58	AL			6530.00	nH/t^2	Core AL value
59	Ve			9.44	cm^3	Core volume
60	HT (EE/PQ/EQ/RM/POT) / ID (toroid)			5.12	mm	Core height/Height of window; ID if toroid
61	MLT			67.1	mm	Mean length per turn
62	BW			8.98	mm	Bobbin width
63	LG			1.30	mm	Gap length (Ferrite cores only)
64	Flux and MMF Calculations					
65	BP_TARGET (ferrite only)	3000		3000	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap

66	B_OCP (or BP)			2964	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
67	B_MAX			1899	Gauss	Peak flux density at AC peak, VACMIN and Full Power Load, nominal inductance, minimum IOCP
68	µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
69	µ_MAX (powder only)			N/A	%	actual µ at peak current divided by µ at zero current, at VACMIN, full load (powder only)
70	µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
71	I_TEST			9.3	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
72	B_TEST			2623	Gauss	Flux density at I_TEST and maximum tolerance inductance
73	µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
74	Wire					
75	TURNS			30		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
76	ILRMS			3.15	A	Inductor RMS current
77	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
78	AWG	40		40	AWG	Inductor wire gauge
79	Filar	125		125		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
80	OD (per strand)			0.079	mm	Outer diameter of single strand of wire
81	OD bundle (Litz only)			1.23	mm	Will be different than OD if Litz
82	DCR			0.074	ohm	Choke DC Resistance
83	P AC Resistance Ratio			0.42		Ratio of total copper loss, including HF AC, to the DC component of the loss
84	J			5.18	A/mm^2	Estimated current density of wires. It is recommended that 4 < J < 6
85	Layers			4.34		Estimated layers in winding
86	Auxiliary Winding					
87	N_AUX	3		3		Recommended auxiliary winding number of turns to ensure the supply to the VS pin
88	V_VS_MAX			1.52	V	Maximum voltage across the auxiliary winding
89	V_VS_MIN			-37.48	V	Minimum voltage across the auxiliary winding
90	RVS			10.00	kohm	Recommended series resistor to the VS pin. Place as close as possible to the VS pin of Hiper-PFS5
91	Loss Calculations					
92	BAC-p-p			1834	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
93	LPFC_CORE_LOSS			0.242	W	Estimated Inductor core Loss
94	LPFC_COPPER_LOSS			0.824	W	Estimated Inductor copper losses
95	LPFC_TOTAL_LOSS			1.066	W	Total estimated Inductor Losses
96	PFC Diode					

97	PFC Diode Part Number	Auto		LXA06T600		PFS Diode Part Number
98	Type / Part Number			Qspeed		PFC Diode Type / Part Number
99	Manufacturer			PI		Diode Manufacturer
100	VRRM			600.0	V	Diode rated reverse voltage
101	IF			6.00	A	Diode rated forward current
102	Qrr			71.0	nC	Qrr at High Temperature
103	VF			2.00	V	Diode rated forward voltage drop
104	PCOND_DIODE			1.163	W	Estimated Diode conduction losses
105	PSW_DIODE			0.000	W	Estimated Diode switching losses
106	P_DIODE			1.163	W	Total estimated Diode losses
107	TJ Max			100.0	deg C	Maximum steady-state operating temperature
108	Rth-JS			2.00	degC/W	Maximum thermal resistance (Junction to heatsink)
109	HEATSINK Theta-CA			49.11	degC/W	Maximum thermal resistance of heatsink
110	IFSM			50.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
111	Output Capacitor					
112	COUT	220		220	uF	Minimum value of Output capacitance
113	VO_RIPPLE_EXPECTED			8.8	V	Expected ripple voltage on Output with selected Output capacitor
114	T_HOLDUP_EXPECTED			27.5	ms	Expected holdup time with selected Output capacitor
115	ESR_LF			0.92	ohms	Low Frequency Capacitor ESR
116	ESR_HF			0.37	ohms	High Frequency Capacitor ESR
117	IC_RMS_LF			0.37	A	Low Frequency Capacitor RMS current
118	IC_RMS_HF			1.41	A	High Frequency Capacitor RMS current
119	CO_LF_LOSS			0.124	W	Estimated Low Frequency ESR loss in Output capacitor
120	CO_HF_LOSS			0.734	W	Estimated High frequency ESR loss in Output capacitor
121	Total CO LOSS			0.858	W	Total estimated losses in Output Capacitor
122	Input Bridge (BR1) and Fuse (F1)					
123	I^2t Rating			15.45	A^2*s	Minimum I^2t rating for fuse
124	Fuse Current rating			4.13	A	Minimum Current rating of fuse
125	VF			0.90	V	Input bridge Diode forward Diode drop
126	IAVG			2.57	A	Input average current at VBROWNOUT.
127	PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
128	PCOND_LOSS_BRIDGE			4.360	W	Estimated Bridge Diode conduction loss
129	CIN	0.33		0.33	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
130	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
131	CIN_PLOSS			0.020	W	Input Capacitor Loss
132	RT1			9.37	ohms	Input Thermistor value
133	D_Precharge			1N5407		Recommended precharge Diode
134	PFS5 Small Signal Components					
135	RVS			10.0	kOhms	VS pin resistor for valley sensing. This resistor should be optimized such that proper delay is introduced from the instant the voltage on the sense winding goes below the Vvs2 threshold

						to the instant when the cascode turns-on (valley sensing). Must be tested on the bench
136	RPS			> 400	kOhms	Power programmability resistor. Leaving PS pin open is acceptable
137	RV1			4.0	MOhms	Line sense resistor 1
138	RV2			6.0	MOhms	Line sense resistor 2
139	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
140	RV4			155.5	kOhms	Description pending, could be modified based on feedback chain R1-R4
141	C_V			0.514	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
142	C_VCC			1.0	uF	Supply decoupling capacitor
143	C_C			100	nF	Feedback C pin decoupling capacitor
144	Power good Vo lower threshold VPG(L)	280		280	V	Vo lower threshold voltage at which power good signal will trigger
145	PGT set resistor			269.5	kohm	Power good threshold setting resistor
146	Feedback Components					
147	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
148	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
149	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor
150	RFB_4			155.5	kohms	Feedback network, lower divider resistor
151	CFB_1			0.514	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
152	RFB_5			40.2	kohms	Feedback network: zero setting resistor
153	CFB_2			1000	nF	Feedback component- noise suppression capacitor
154	Loss Budget (Estimated at VACMIN)					
155	PFS Losses			1.598	W	Total estimated losses in PFS
156	Boost diode Losses			1.163	W	Total estimated losses in Output Diode
157	Input Bridge losses			4.360	W	Total estimated losses in input bridge module
158	Input Capacitor Losses			0.020	W	Total estimated losses in input capacitor
159	Inductor losses			1.066	W	Total estimated losses in PFC choke
160	Output Capacitor Loss			0.858	W	Total estimated losses in Output capacitor
161	EMI choke copper loss			0.724	W	Total estimated losses in EMI choke copper
162	Total losses			9.788	W	Overall loss estimate
163	Efficiency			95.92	%	Estimated efficiency at VACMIN, full load.
164	HiperPFS-5 Integrated CAPZero Function					
165	Total Series Resistance (Rcapzero1+Rcapzero2)			1.046	MOhms	Maximum total series resistor value to discharge X-capacitors with time constant of 1 second. Resistors must be connected to D1 and D2 pins of the

						HiperPFS-5 part for integrated CAPZero function
166	EMI Filter Components Recommendation					
167	CX2	330		330	nF	X-capacitor after differential mode choke and before bridge, ratio with Po
168	LDM_calc			384	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
169	CX1	330		330	nF	X-capacitor before common mode choke, ratio with Po
170	LCM			10.0	mH	Typical common mode choke value
171	LCM_leakage	75		75	uH	Estimated leakage inductance of CM choke, typical from 30~60uH
172	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
173	LDM_Actual			309	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
174	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
175	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
176	Note: CX2 can be placed between CM choke and DM choke depending on EMI design requirement.					

9 LLC Transformer Design Spreadsheet

1	ACDC_HiperLCS2_031622; Rev.1.0; Copyright Power Integrations 2022	INPUT	INFO	OUTPUT	UNITS	LCS2 Design Spreadsheet
2	General					
3	Description			>		LCS7265C-360W-24V-15A-SynchRF-36T-4T-380uH-88uH-22nF-115kHz
4	Input Parameters					
5	VIN MIN	280		280	V	Brownout Threshold Voltage
6	VIN RES	400		400	V	Input Voltage at Resonance - lower Vres to lower Npri
7	VIN NOM	400		400	V	Nominal Input Voltage - default CRM Vres=Vnom (or DCM Vres>Vnom, CCM Vres<Vnom)
8	VIN MAX			430	V	Maximum Input Voltage - decrease Vmax to lower Fmax
9	PFC	YES		YES		Input Option
10	Output Parameters					
11	Vout1			24.00	V	Main Output Voltage
12	Iout1 PK	15.0		15.0	A	Peak Main Output Current - default = 200% of Iout1Cont - used to select device size - higher power lower Llk
13	Pout1 PK			360.0	W	Main Output Peak Power
14	Iout1 CONT	9.2		9.2	A	Continuous Main Output Current - default 50% of Ppeak - used to select device size - losses calculated at this power level
15	Pout1 CONT			220.8	W	Continues Main Output Power
16	External CC	NO		NO		Use external CC operation
17	Vout1 Min (CC)				V	Minimum Output Voltage when operating in CC - lower VoutMin lowers Lm and also lowers efficiency
18	VCC				V	Output current sense resistor voltage when operating at CC-threshold
19	RCC				mOhm	Output current sense resistor value
20	RCC Rated Power				W	Output current sense resistor rated power
21	Estimated Parameters, Design Choices and Selections					
22	FS Range	1		1		Frequency Range
23	FS Vnom (Target)			120.0	kHz	Switching Frequency at VinNom
24	Output Rectifier	SynchRF		SynchRF		Output Rectifier
25	Ron_SR1	3.6		3.6	mOhms	Sync. Rectifier ON Resistance
26	VF_SR1	0.7		0.7	V	Output Diode Average Voltage Drop

27	Design Results					
28	DESIGN RESULT			Design Passed		Current Design Status
29	Device Variables					
30	DEVNAME	LCS7265C		LCS7265C		PI Device Name
31	COSS			166	pF	Equivalent Coss of selected device
32	RDSON			0.410	Ohms	RDSON of selected device
33	Fault Response	NON_LATCHING		NON_LATCHING		..
34	Tank Circuit Components & Operation Frequency Range					
35	LP Nominal			468.04	uH	Nominal Primary Inductance
36	Lm			380.0	uH	Magnetizing inductance of transformer - modified by Kz, Device size and frequency
37	Lres			88.1	uH	Series resonant or primary leakage inductance - modified by Pmax
38	Cres	22.00		22.00	nF	Series resonant capacitor.
39	f_calc@Vbrownout			75.8	kHz	Frequency at PoutCont at Vbrownout, full load - adjust VinBrownout
40	f_calc@resonance			114.3	kHz	Frequency at PoutCont at Vres (defined by Lres and Cres) - adjust Vres)
41	f_calc@Vnom			115.4	kHz	Frequency at PoutCont at Vnom - adjust FS Vnom Target or Vnom
42	f_calc@Vinmax			137.1	kHz	Expected frequency at maximum input voltage and full load; Heavily influenced by n_eq and primary turns
43	VINGmaxInversion			253.0	V	Minimum Input Voltage for negative Gain at 100% load. Below this voltage the Gain becomes positive (unstable loop)
44	Core Dimensions/TRF Mechanical Parameters					
45	AE			167.00	mm^2	Transformer Core Cross-sectional area
46	VE			12.5	cm^3	Transformer Core Volume
47	MLT			66.00	mm	Middle Length of a Turn
48	AW			147.00	mm^2	Core Window area
49	BW			19.60	mm	Bobbin Winding Width
50	Bobbin Chambers			2		Bobbin Chambers
51	ChambDist	3.20		3.20	mm	Width of bobbin with no windings - empty space between primary/secondary generates leakage inductance
52	Bobbin Height			6.00	mm	Height of the bobbin, maximum Stack height
53	Prim. Bobbin Chamber Width			4.64	mm	Part of the bobbin allocated for primary
54	Sec. Bobbin Chamber Width			11.76	mm	Part of the bobbin allocated for secondary

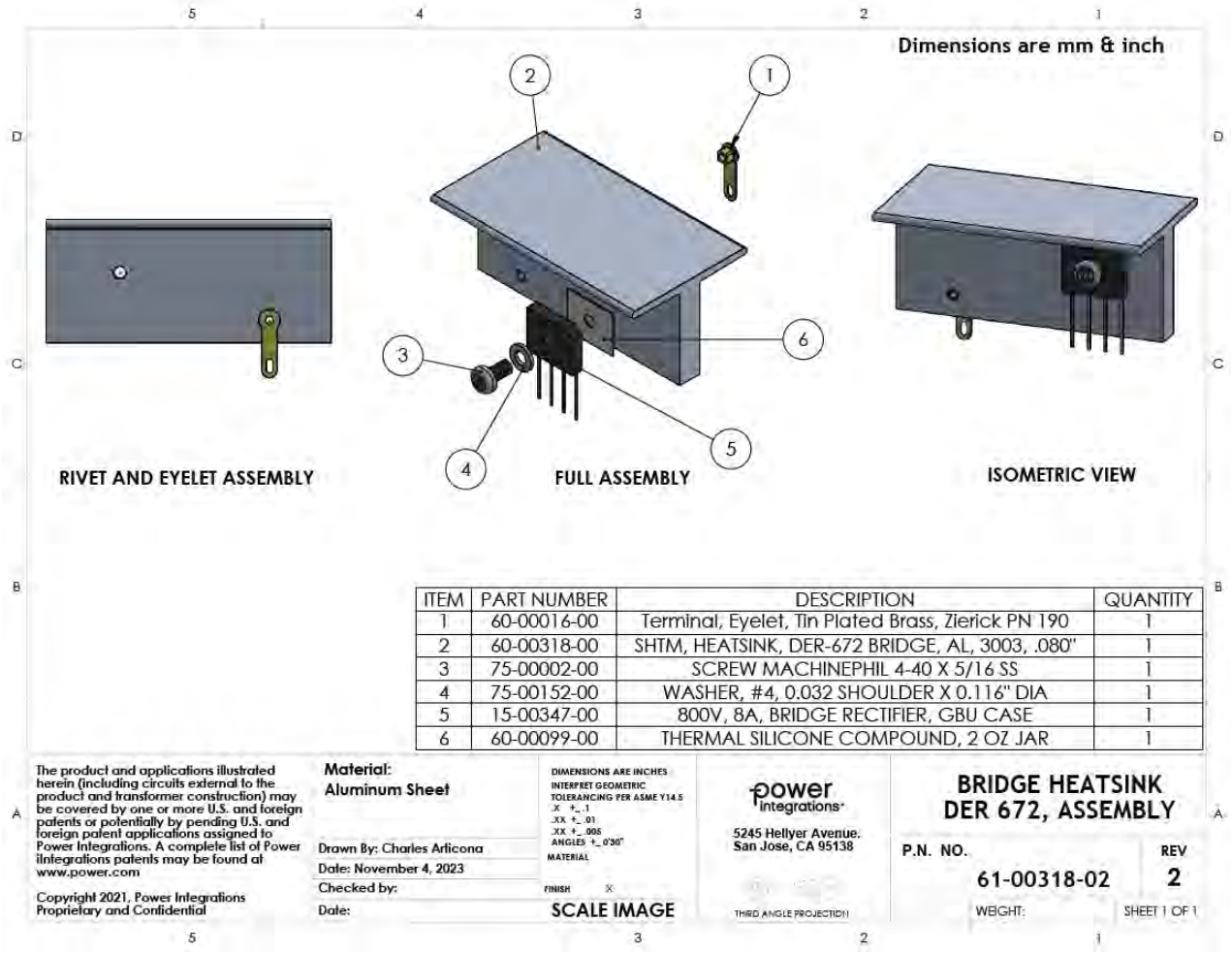
55	K-PD			0.35		Penetration Depth multiplier (for Single Strand LITZ calculation)
56	Transformer Generic Parameters					
57	CR_TYPE	ETD34		ETD34		Transformer Core Type
58	FR_TYPE	3C95		3C95		Magnetic material used
59	BACmax Actual			161.68	mT	Estimated Flux Density at Vnom - increase Ns to reduce Bmax
60	Use Litz Primary	YES		YES		Primary Windings Bundled (served) Yes/No
61	Use Litz Secondary	YES		YES		Secondary Windings Bundled (served) Yes/No
62	Fixed Litz Bundles	NO		NO		Use preferred Litz Wire Bundles (yes) - or use customer bundle (no)
63	kSecChamb	0.60		0.60		Percentage of Bobbin Chamber Width used for Secondary Windings - Adjust to change Used Percentage of Primary/Secondary Windows
64	Transformer Primary Parameters					
65	Npri			36		Calculated Primary Winding Total Number of Turns
66	Iprim RMS			1.39	A	Transformer Primary Winding RMS Current at PoutCont and VinNom
67	Prim. Wire Type			LITZ		Primary Wire Type
68	Primary LIz Wire Type	SERVED		SERVED		Litz Insulation type, SERVED bundled with sleave, UNSERVED loose wires
69	Target Prim. Current density			6.0	A/mm^2	Primary current density target - reduce target to increase copper
70	Prim. Single Strand Wire Gauge			40	AWG	Single Strand Gauge (LITZ) / AWG (ECW)
71	Prim. Single Strand Diameter			0.08	mm	Primary Single Strand Copper Diameter
72	Number of Prim. Strands	50		50		Prim. Number of Strands (LITZ) / Fillars (ECW)
73	Actual Prim. Current Density			5.55	A/mm^2	Actual Primary Current Density
74	Actual Prim. Copper Diameter			0.57	mm	Primary Equivalent Total Copper Diameter
75	Actual Prim. External Diameter			0.72	mm	Primary Wire External Diameter (bundle size - copper plus insulation plus fill)
76	Layers Primary			6.00		Not Rouned Primary number of layers
77	Primary Window Usage			72.41	%	Used Percentage of Available Primary Winding Window - Maximum copper gives 100%
78	Main Output Parameters					
79	NSec	4		4		Secondary Number of Turns
80	ISRMS			11.86	A	Transformer Secondary Winding RMS Current

81	Sec. Wire Type			LITZ		Main Output Wire Type
82	Secondary LIZ Wire type	UNSERVED		UNSERVED		Litz Insulation type, SERVED bundled with sleave, UNSERVED loose wires
83	Target Sec. Current density			8.0	A/mm^2	Secondary current density target - reduce target to increase copper
84	Sec. Single Strand Wire Gauge			40	AWG	Single Strand Gauge (LITZ) / AWG (ECW)
85	Sec. Single Strand Diameter			0.08	mm	Secondary Single Strand Copper Diameter
86	Number of Sec. Strands	500		500		Sec. Number of Strands (LITZ) / Fillars (ECW)
87	Actual Sec. Curr Density			4.72	A/mm^2	Sec. Actual Current Density
88	Actual Sec. Copper Diameter			1.79	mm	Secondary Equivalent Total Copper Diameter
89	Actual Sec. External Diameter			2.29	mm	Secondary Wire External Diameter(bundle size - copper plus insulation plus fill)
90	Layers Secondary			1.60		Not Rouned Secondary number of layers
91	Secondary Window Usage			76.32	%	Used Percentage of Available Secondary Winding Window - Maximum copper gives 100%
92	Losses					
93	CoreLoss			0.37	W	Core Losses at VinNom
94	Pr.WindLoss			0.54	W	Primary Winding Losses at VinNom and PoutCont
95	Sec.WindLoss			0.35	W	Secondary Winding Losses at VinNom and PoutCont
96	CO ESR Loss			0.06	W	Secondary Winding Losses at VinNom and PoutCont
97	PLOSS Switch			0.40	W	Single Primary Switch Conduction Loss at VinNom and PoutCont
98	PLOSS Output Rectifier			0.19	W	Single Output Rectifier Conduction Loss at VinNom and PoutCont
99	PLOSS RCC			0.00	W	Current sense resistor power loss at VinNom and PoutCont
100	PLOSS Total			2.49	W	Total Loss at VinNom and PoutCont
101	Circuit Components					
102	RZ1			150	kOhm	Control Zero (boost high-frequency gain)
103	CP2			100	pF	Control Pole2 (roll-off high-frequency gain)
104	Cp1			2.2	nF	Control Pole1 (roll-off low-frequency gain)
105	Resr CO			1.00	mOhms	ESR of the output capacitor
106	COmin			1618	uF	Min CO to satisfy burst conditions
107	RD1			500	Ohm	RD1 Resistor value
108	RD2			500	Ohm	RD2 Resistor value
109	CBPL			1	uF	CBPL Capacitor Value /25V

110	CBPH			1	uF	CBPH Capacitor Value /25V
111	C5VL			1	uF	C5VL Capacitor Value /10V
112	C5VH			220	nF	C5VH Capacitor Value /10V
113	C5VFL			100	nF	C5VLFL Capacitor Value /10V
114	C5VS			10	uF	C5VS Capacitor Value /10V
115	CBPS			10	uF	CBPS Capacitor Value /35V
116	RL			4800	kOhms	L-pin Input Voltae (Vin) Sense Resistor
117	RPP			158	kOhms	RPP Resistor /1% E96 series
118	RPS			75	kOhms	RPS Resistor /1% E96 series
119	Bias, IS Circuit & Feedback Components					
120	NS1			3		Primary Bias Turns
121	NSB			2		Secondary Bias Turns
122	NVIS			2		Secondary (Is) Sense Turns
123	RIS			1040	kOhms	Rris Resistor Value
124	CIS			470	pF	IS sense winding coupling capacitor
125	RFBH			129.8	kOhm	Calculated value of top feedback resistor. use series closest resistor 1% E96
126	RFBL			24.0	kOhm	Calculated value of low feedback resistor. use series closest resistor 1% E96
127	Currents and Winding loss elements					
128	Iprim RMS			1.39	A	Transformer Primary Winding RMS Current at PoutCont at VinNom
129	ISRMS			11.86	A	Transformer Secondary Winding RMS Current at PoutCont at VinNom
130	Irms_SR			7.23	A	Secondary Rectifier RMS Current at PoutCont at VinNom
131	Irms_CO1			7.48	A	Output Capacitor RMS Current at PoutCont at VinNom
132	RdcPrim			0.21	Ohms	Primary Winding DC Resistance
133	RacPrim			0.28	Ohms	Primary Winding AC Resistance
134	RdcSec			2.349	mOhms	Secondary Winding DC Resistance
135	RacSec			2.486	mOhms	Secondary Winding AC Resistance
136	Errors, Warnings, Information					
137	Information			0		Number of variables required bench functionality check. Check the variables with "Info" in the third column .

138	Design Warnings			0		Number of variables whose values exceed electrical/datasheet specifications. Check the variables with "Err" in the third column .
139	Design Errors			0		The list of design variables which result in an infeasible design.
140	Advanced Settings					
141	Kz	1.0		1.0		coefficient of surplus ZVS energy @ Vnom - raise Kz to lower Vin(GmaxInv) - Kz should be >= 1.0 to ensure ZVS operation
142	Tdd1_Vinnom			250	ns	Half-bridge slew at 100% load @ Vnom - raise Tdd1 to lower ZVS currents
143	Coupling			0.89		Transformer Coupling
144	Cpri			40.00	pF	Stray Capacitance at transformer primary

10 Bridge Heat Sink



ITEM	PART NUMBER	DESCRIPTION	QUANTITY
1	60-00016-00	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	1
2	60-00318-00	SHTM, HEATSINK, DER-672 BRIDGE, AL, 3003, .080"	1
3	75-00002-00	SCREW MACHINEPHIL 4-40 X 5/16 SS	1
4	75-00152-00	WASHER, #4, 0.032 SHOULDER X 0.116" DIA	1
5	15-00347-00	800V, 8A, BRIDGE RECTIFIER, GBU CASE	1
6	60-00099-00	THERMAL SILICONE COMPOUND, 2 OZ JAR	1

Figure 22 – Bridge Heat Sink Assembly Drawing.

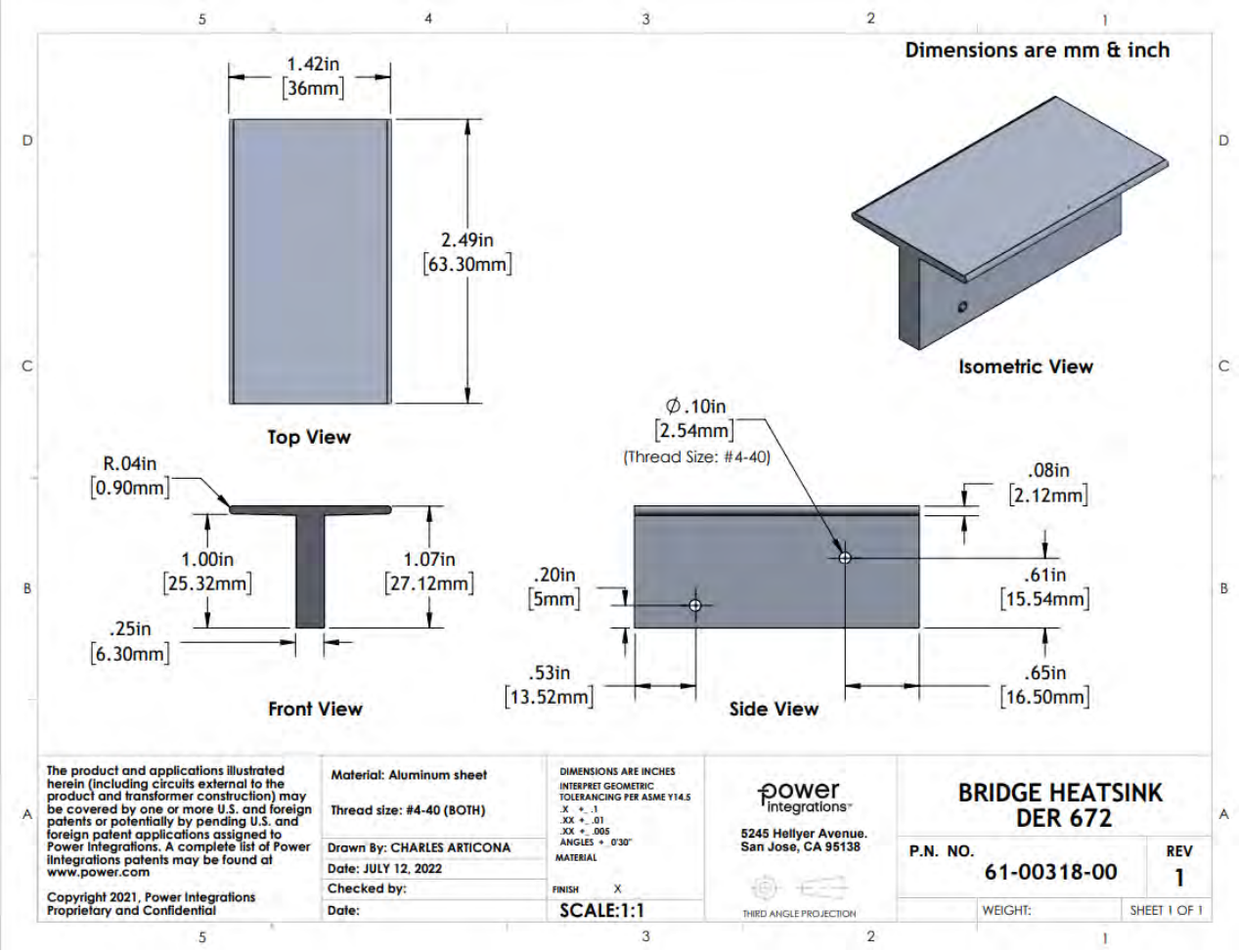


Figure 23 – Bridge Heat Sink Sheet Metal Drawing.

11 Performance Data

This section provides a summary of the unit under test's performance under certain line and load conditions. Furthermore, it gives an overview of the set up and conditions under which the unit was tested into.

11.1 *Total Efficiency*

The graph below shows the total efficiency of the unit with respect to output power and different line voltages. A variable AC source was used to supply a Sine wave input and a DC electronic load set to CC mode was used as load on the output.

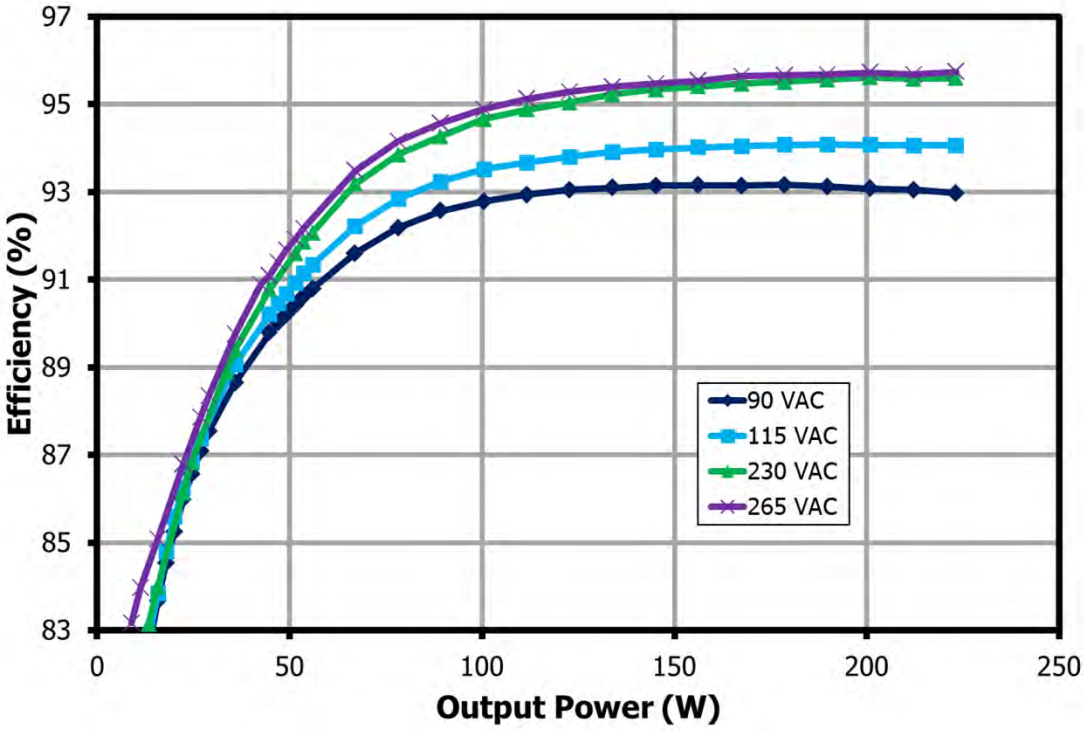


Figure 24 – Total Efficiency vs. Load, 24 V Output.

Load (W)	Efficiency (%)			
	90 VAC	115 VAC	230 VAC	265 VAC
22 W (10% Load)	85.98	86.24	86.13	86.80
44 W (20% Load)	89.79	90.21	90.79	91.09
110W (50% Load)	92.94	93.67	94.89	95.13
220 W (100% Load)	92.97	94.06	95.60	95.75

11.2 *No-Load Input Power*

The total no-load input power of the unit was measured at room temperature with system soak time of 5 minutes and an integration time of 15 minutes. The output was completely disconnected from the load and no other probes were connected aside from the input power meter.

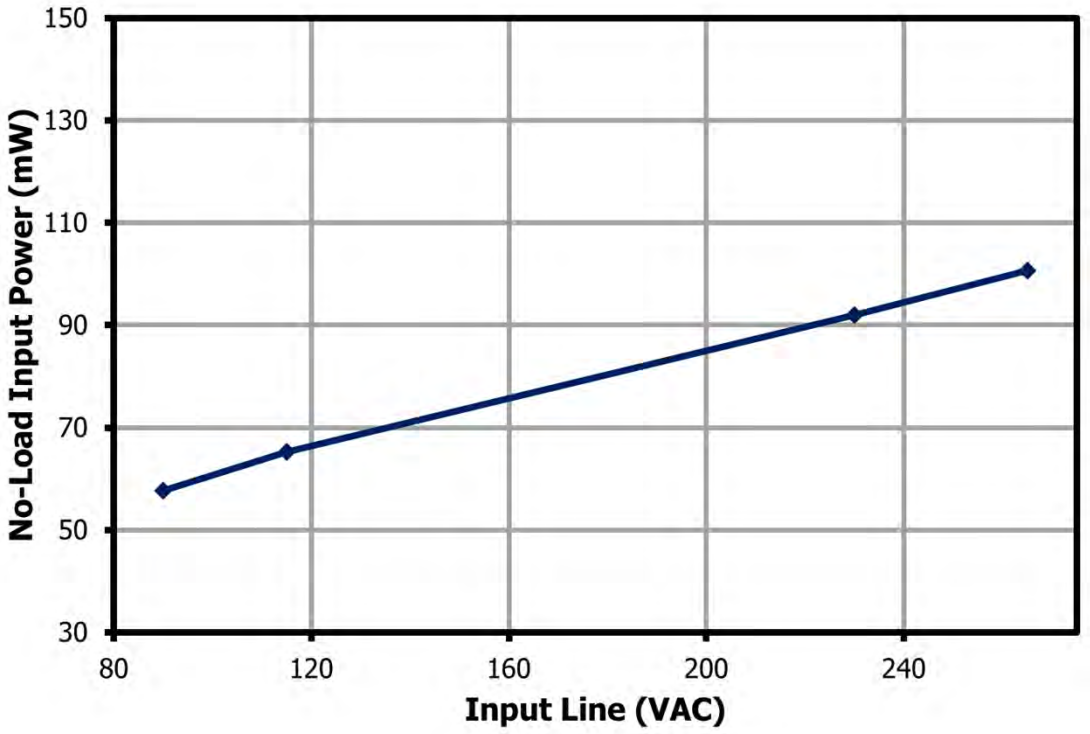


Figure 25 – No-Load Input Power vs. Input Voltage.

Input Line (VAC)	No Load Input Power (mW)
90	57.66
115	65.21
230	92.03
265	100.75

11.3 *Power Factor*

Power Factor was measured at different line voltages with varying loads using a power meter. A variable AC source was used to supply a Sine wave input and a DC electronic load set to CC mode was used as load on the output.

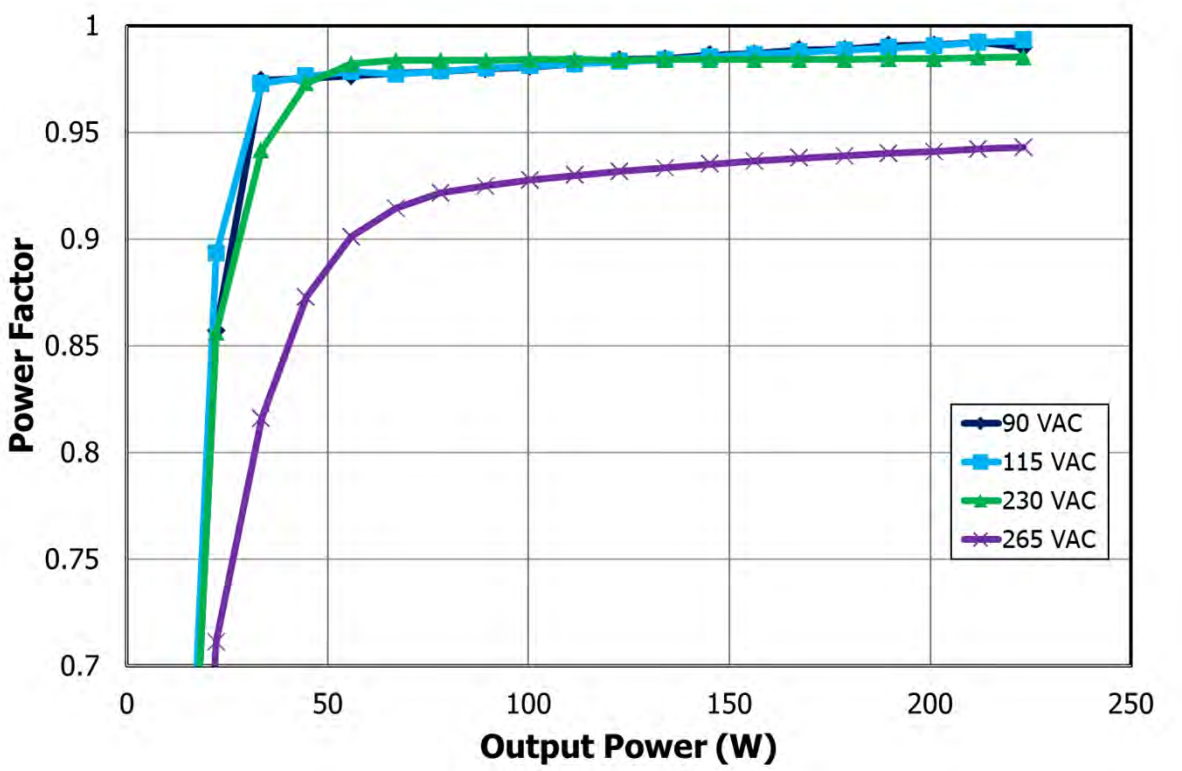


Figure 26 – Power Factor vs. Output Power.

Load (W)	Power Factor			
	90 VAC	115 VAC	230 VAC	265 VAC
22 W (10% Load)	0.8572	0.8933	0.8563	0.7115
44 W (20% Load)	0.9754	0.9763	0.973	0.8728
110W (50% Load)	0.982	0.9821	0.984	0.9298
220 W (100% Load)	0.9897	0.9932	0.9853	0.9429

11.4 *Total Harmonic Distortion (THD)*

Total harmonic Distortion is the measure of the harmonic distortion present in a signal compared to the fundamental frequency. The graph below shows THD with respect to output power and was measured at two line voltages, 115VAC and 230VAC.

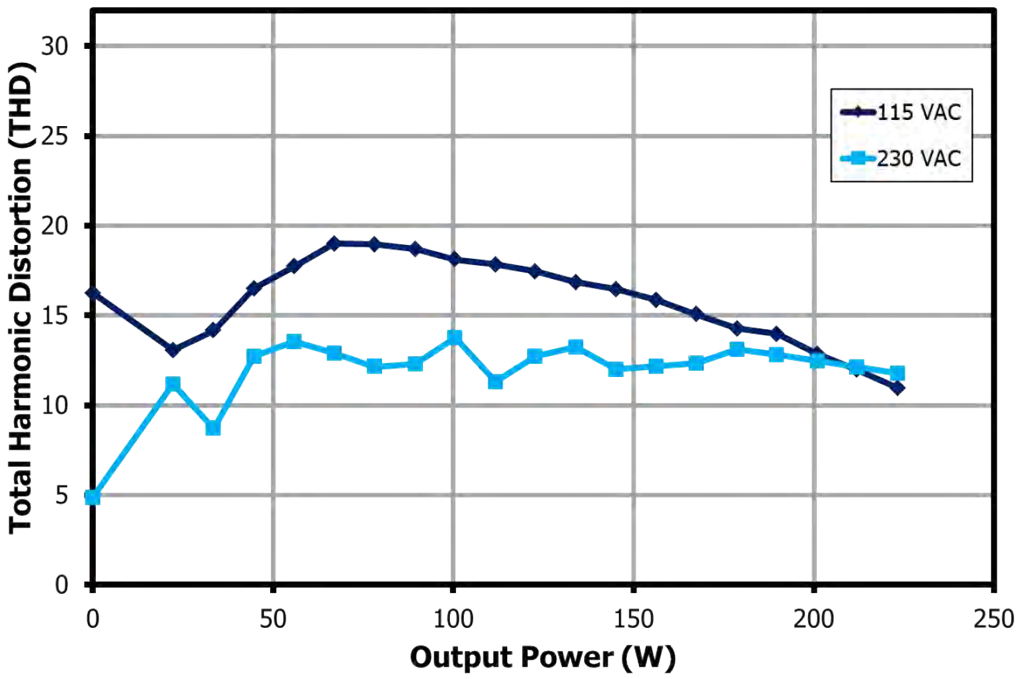


Figure 27 – Total Harmonic Distortion.

11.5 *Line Regulation*

Line regulation was measured with an AC source connected to the input supply which is varied at 10 V interval with an electronic load set in CCH mode to draw a constant current output from the power supply.

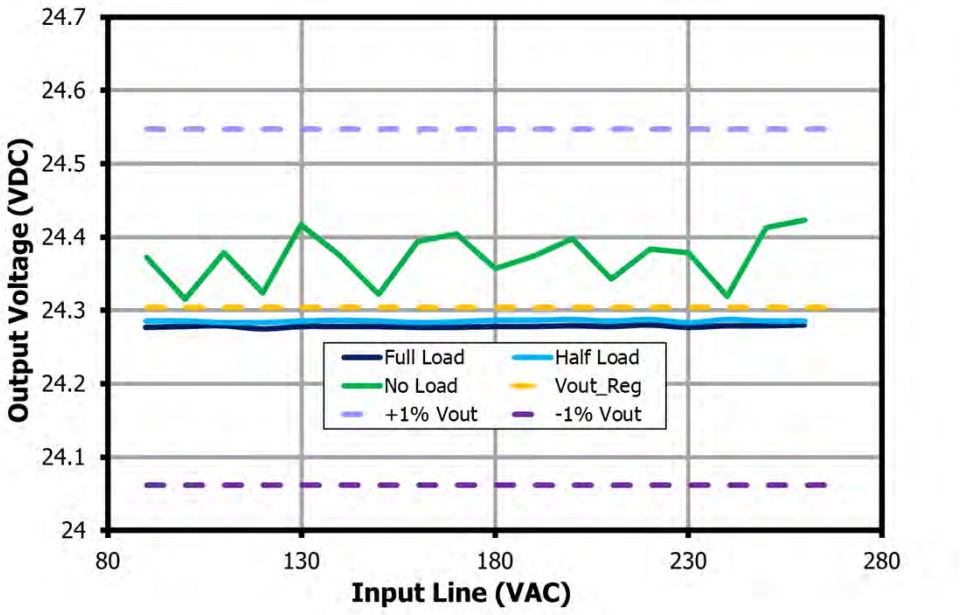


Figure 28 – Line Regulation.

11.6 *Load Regulation*

Load regulation was measured by decreasing the load from full load down to light loads using an DC electronic load as a load on the output. The test was repeated on different line voltages.

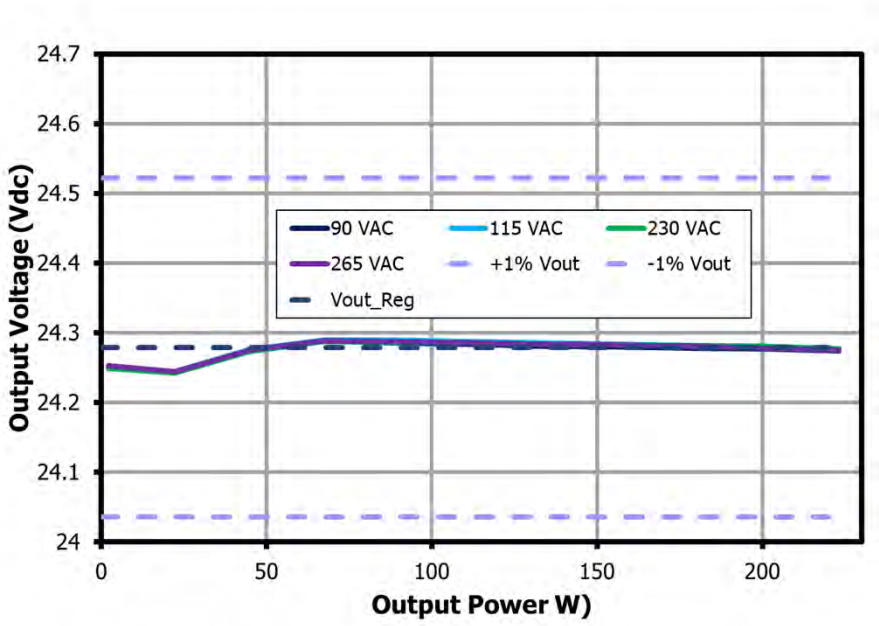


Figure 29 – Load Regulation.

12 Waveforms

The figures below show the expected waveforms for different input voltage and output loading conditions set for the UUT.

12.1 *Input Current, 100% Load*

Input current was measured at varying line voltages with an Electronic Load set to CC mode at full load, 9.2A.

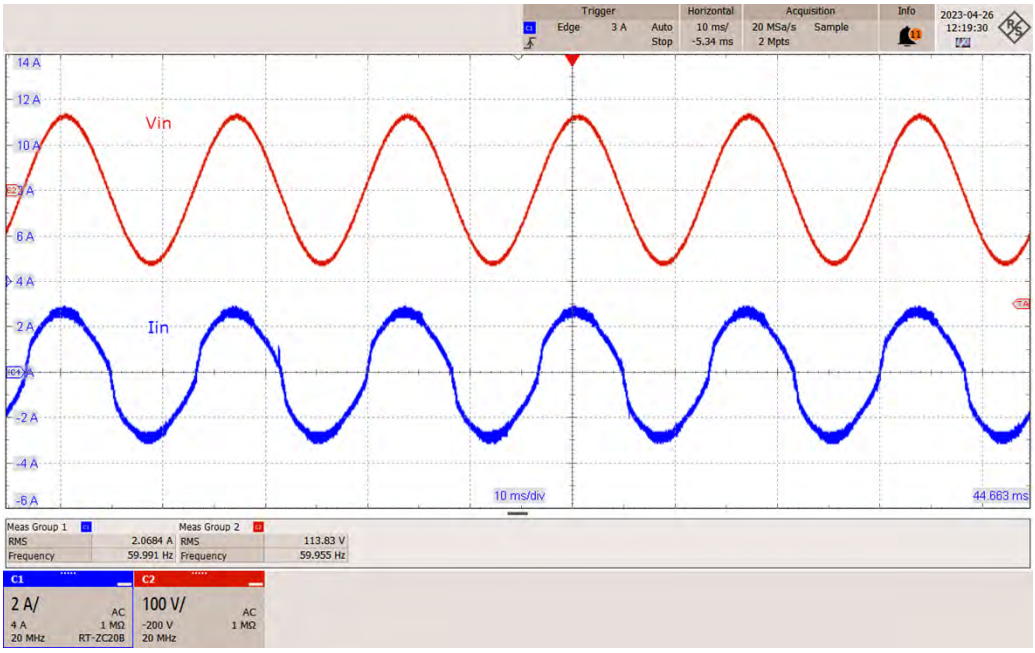


Figure 30 – Input Current, 115 VAC, 60Hz, 10ms/div.
Blue: I_{IN}, 2A / div
Red: V_{IN}, 100V / div

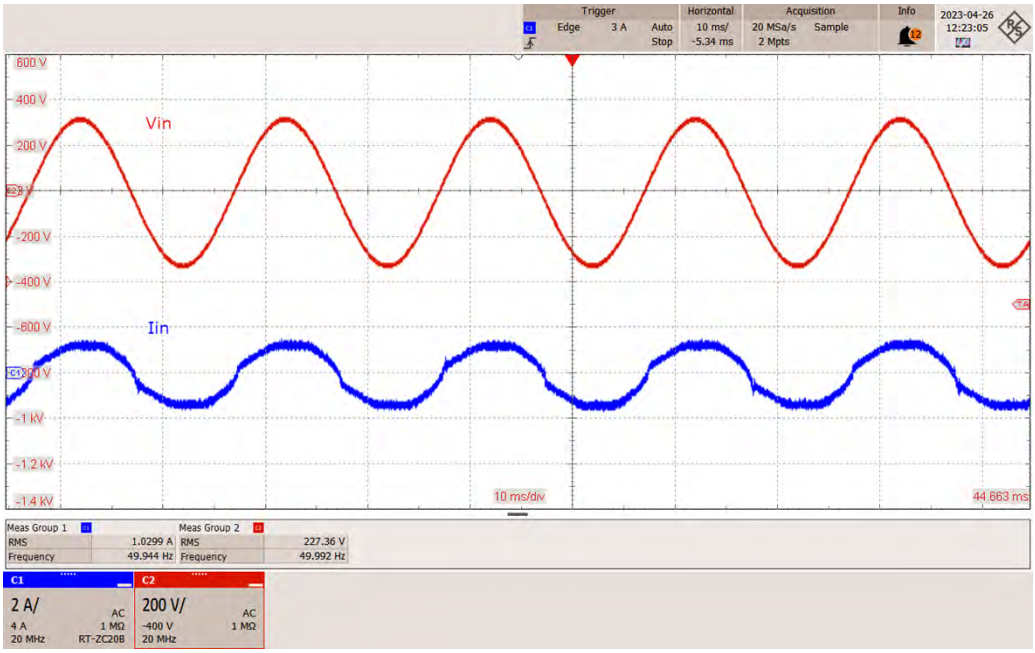


Figure 31 – Input Current, 230 VAC,
50 Hz, 10ms/div.
Blue: I_{IN}, 2A / div
Red: V_{IN}, 200V / div

12.2 *LLC Primary Voltage and Current*

Shown in the figures below are the half-bridge voltage and current of the LLC section with the output loaded using an electronic load set to CC mode and varied at different loading conditions full load, half load and no load.

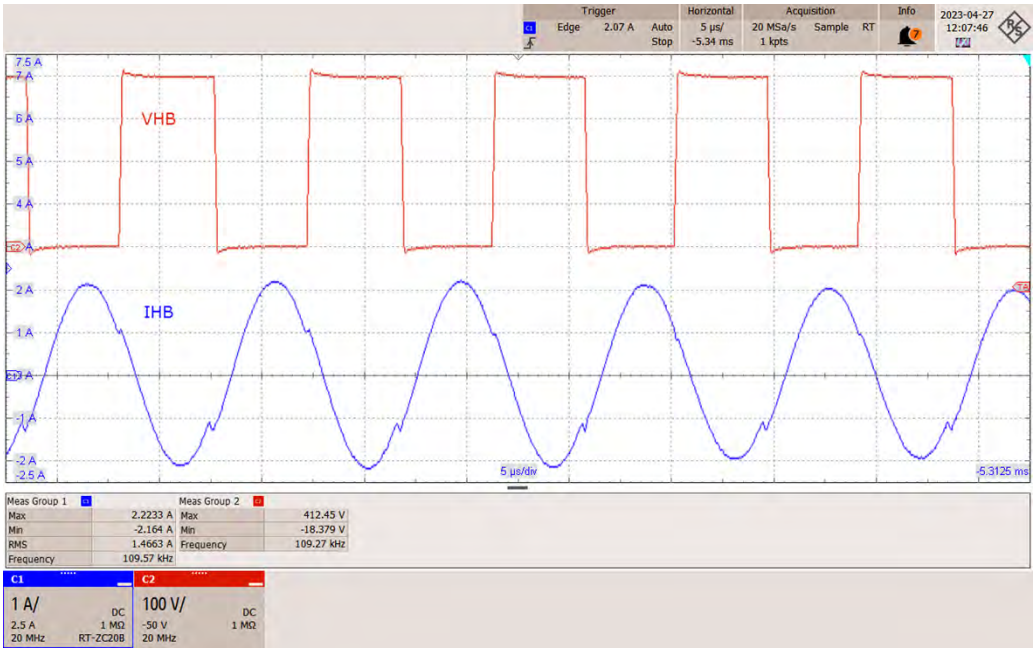


Figure 32 – LLC Stage Primary Voltage and Current, Full Load.
Time Division: 5 us / div.
Blue: HB Current, 1 A / div.
Red: HB Voltage, 100 V / div.

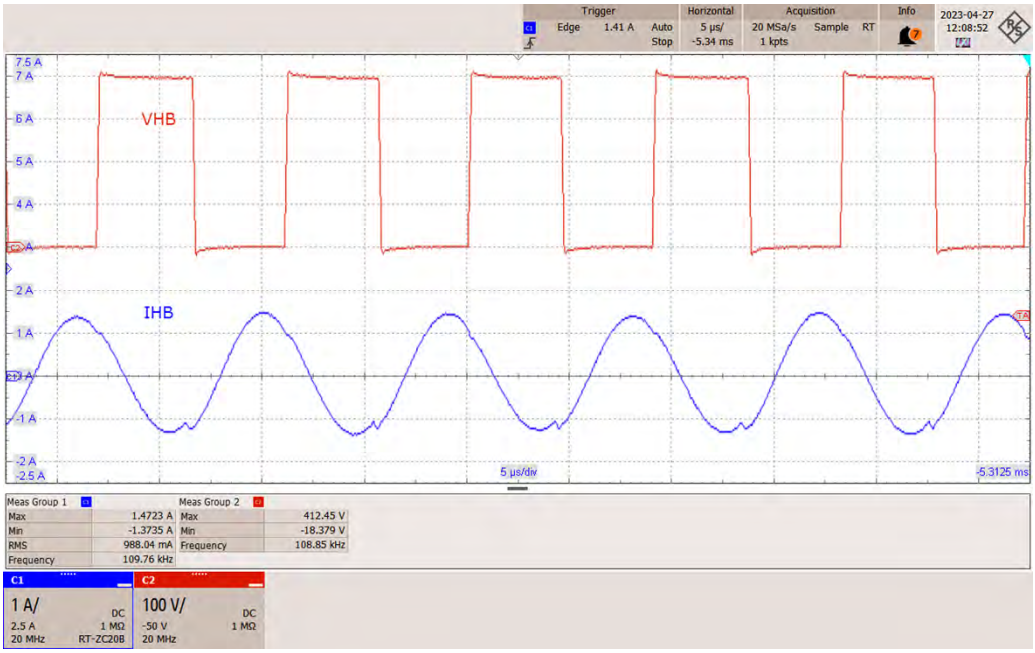


Figure 33 – LLC Stage Primary Voltage and Current, 50% Load.
Time Division: 5 us / div.
Blue: HB Current, 1 A / div.
Red: HB Voltage, 100 V / div.

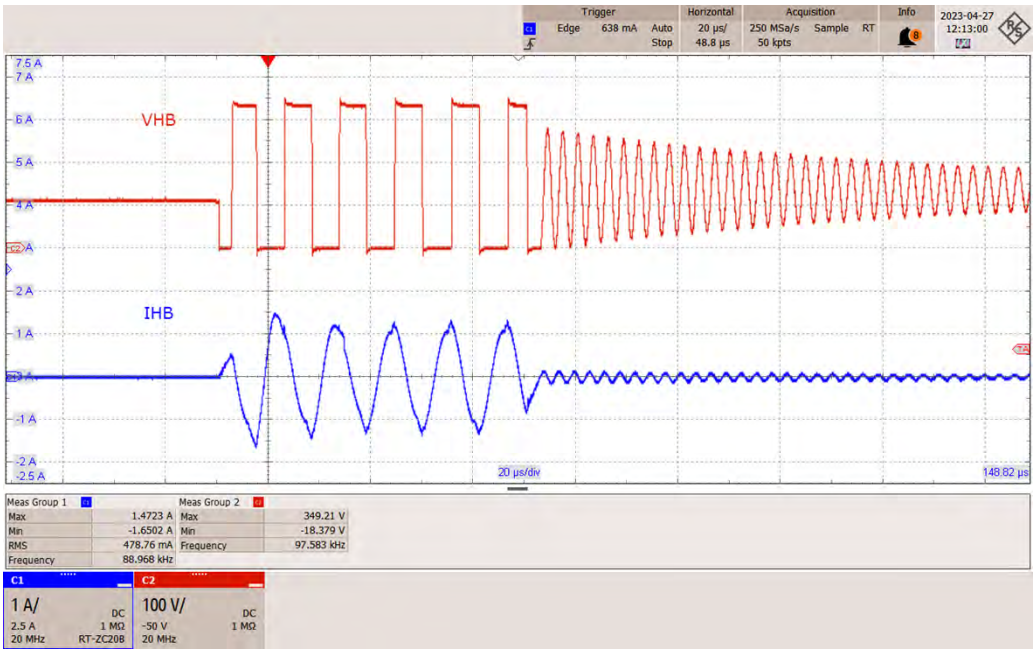


Figure 34 – LLC Stage Primary Voltage and Current, No-Load.
Time Division: 20 us / div.
Blue: HB Current, 1 A / div.
Red: HB Voltage, 100 V / div.

12.3 *SR Waveforms*

Drain-source voltage across synchronous rectifiers Q4 and Q5 were measured with output load set to CC mode in full load. The illustration shows that there are no missing SR pulses each cycle and bot SR FETs switches at a time.

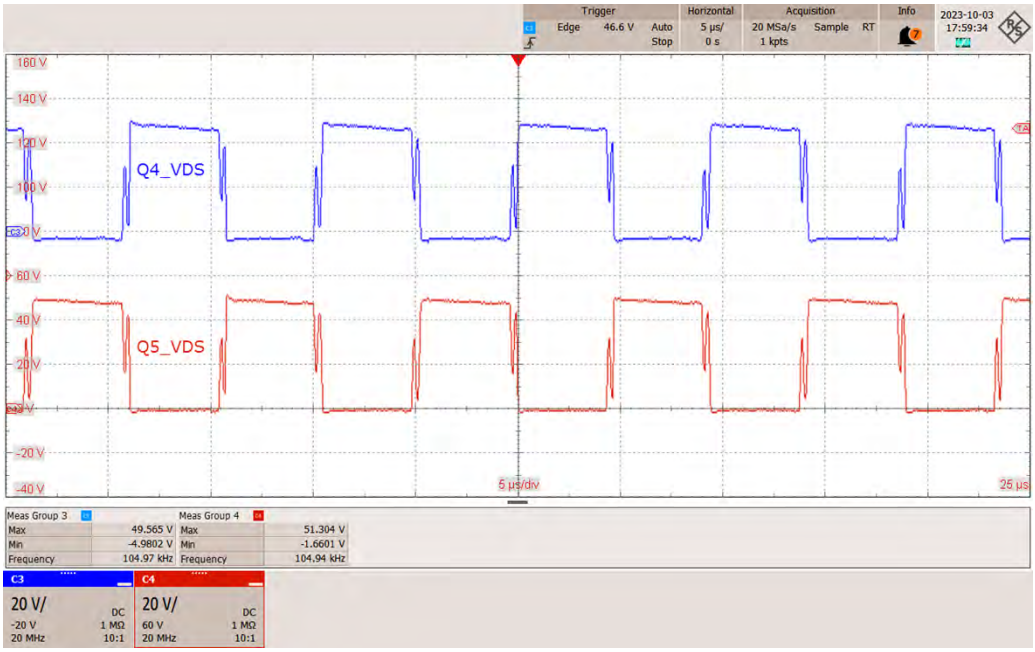


Figure 35 – Output Rectifier Peak Reverse Voltage
~~Zoom~~ Time Division: 5 us / div.
Blue: Q_4 V_{DS}, 20 V / div.
Red: Q_5 V_{DS}, 20 V / div.

12.4 *PFC Voltage and Current, 100% Load*

The figures below show CRM and DCM operation with valley switching of HiperPFS-5. It was measured at four different input voltages and the electronic load set to CC mode at full load, 9.2A.

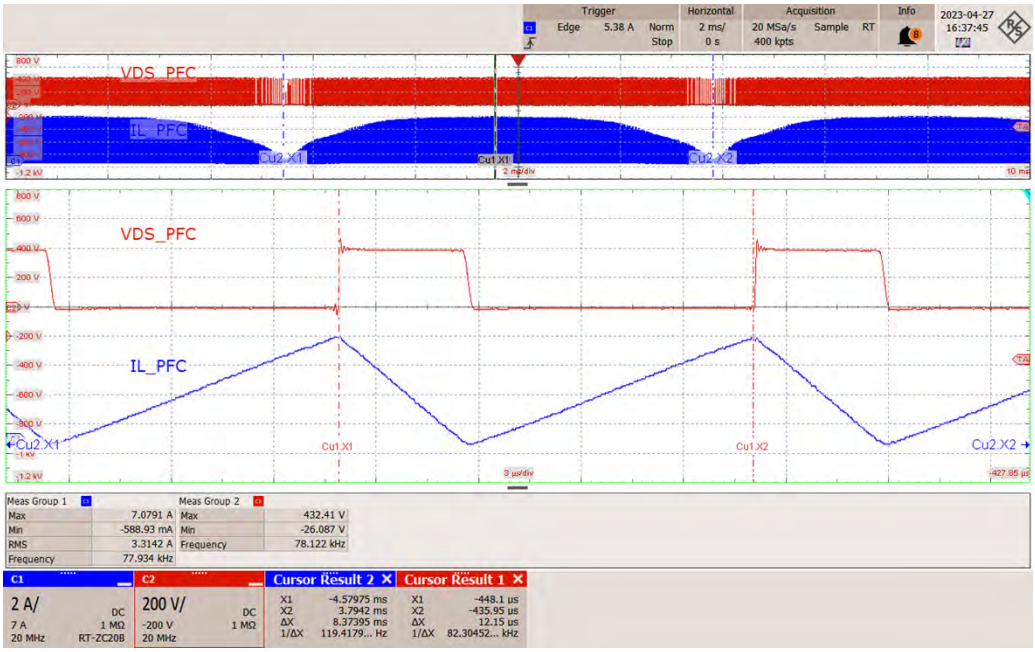


Figure 36 – V_{DS} and Choke Current, 90 VAC.
Time Division: 2 ms / div
Zoom Time Division: 3 us / div.
Blue: IL_PFC, 2 A / div.
Red: VDS_PFC, 200 V / div.

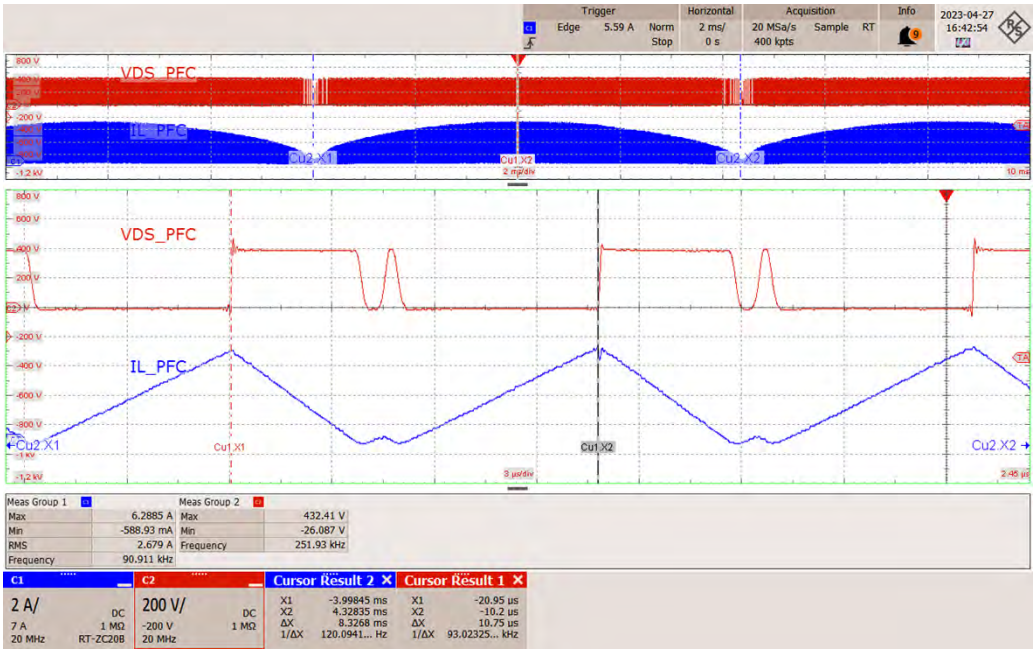


Figure 37 – V_{DS} and Choke Current, 115 VAC.
Time Division: 2 ms / div
Zoom Time Division: 3 us / div.
Blue: IL_PFC, 2 A / div.
Red: VDS_PFC, 200 V / div.

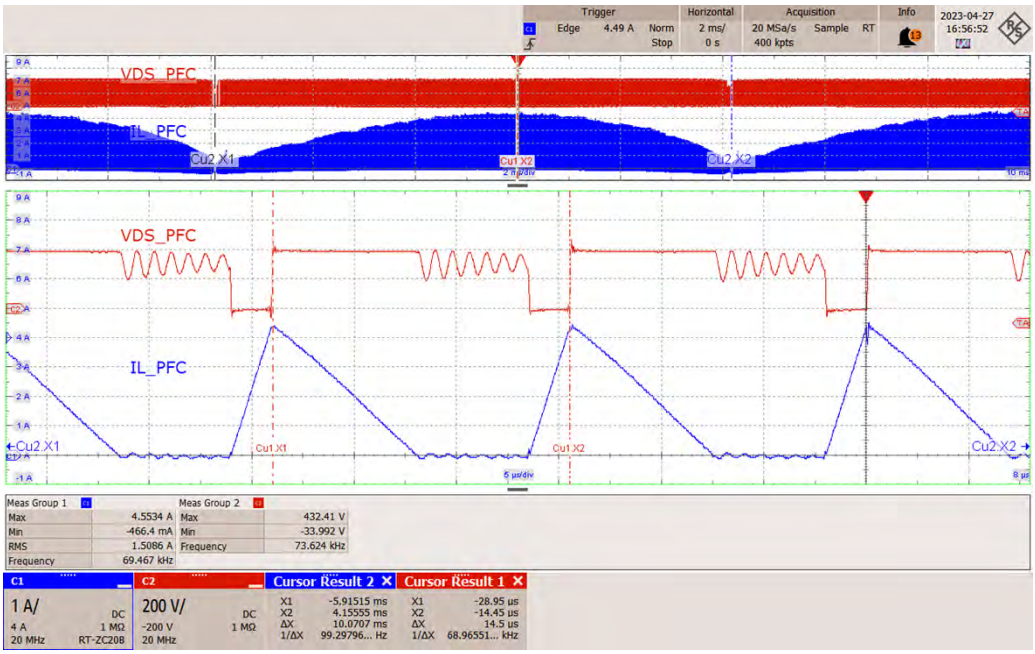


Figure 38 – V_{DS} and Choke Current, 230 VAC.
Time Division: 2 ms / div
Zoom Time Division: 5 us / div.
Blue: IL_PFC, 1 A / div.
Red: VDS_PFC, 200 V / div.

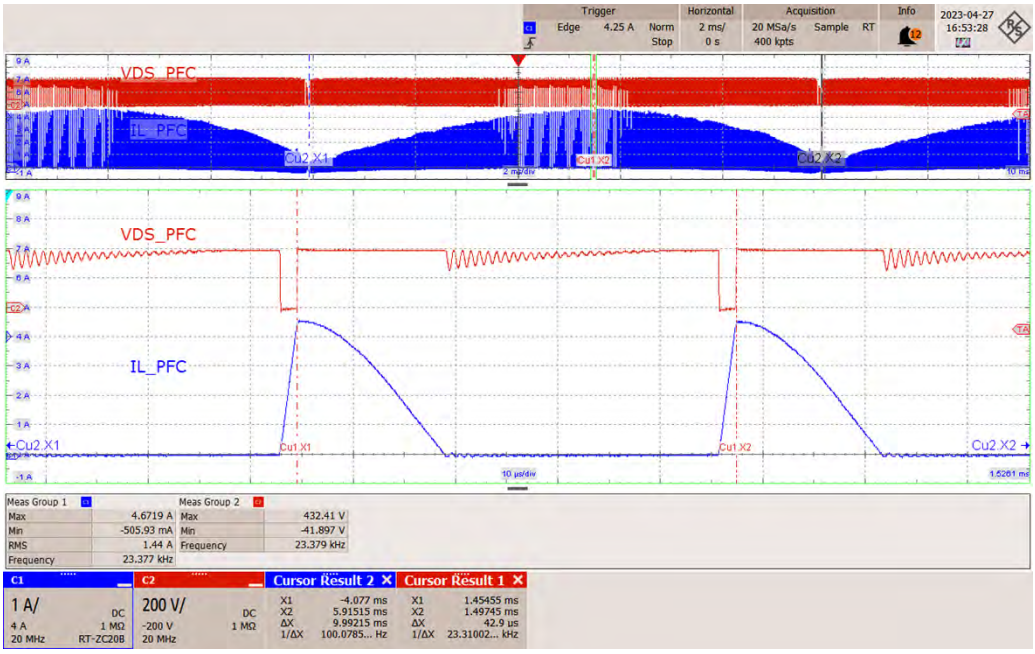


Figure 39 – V_{DS} and Choke Current, 265 VAC.
Time Division: 2 ms / div
Zoom Time Division: 10 us / div.
Blue: IL_PFC, 1 A / div.
Red: VDS_PFC, 200 V / div.

12.5 *Start Up Waveforms*

Startup waveforms was supplied through an AC source, whilst varying the input voltage and the output was connected to an electronic load set to full load. The load was completely disconnected at no load condition.
The figures below show the waveforms of V_{BULK}, VAC and V_{OUT} during start-up at both full load and no-load.

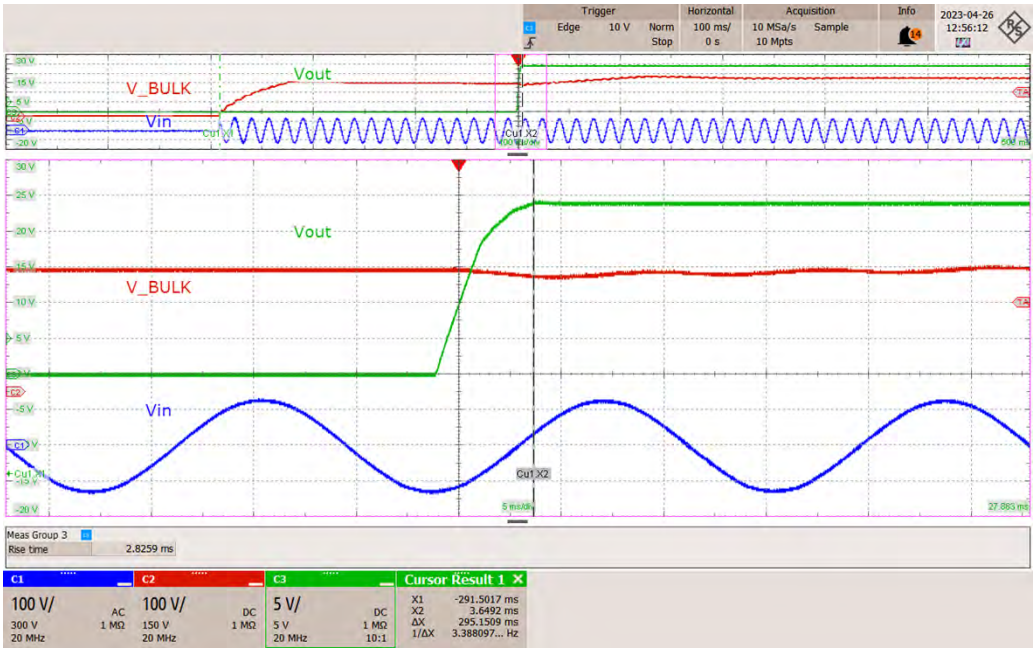


Figure 36 – Unit Start-up. 90 VAC, Full Load.
Regulation Time: 295.15 ms, V_{OUT} Rise Time: 2.8259 ms
Zoom Time Division: 5 ms / div.
Blue: V_{IN}, 100 V / div. Red: V_{BULK}, 100 V / div. Green: V_{OUT}, 5 V / div.

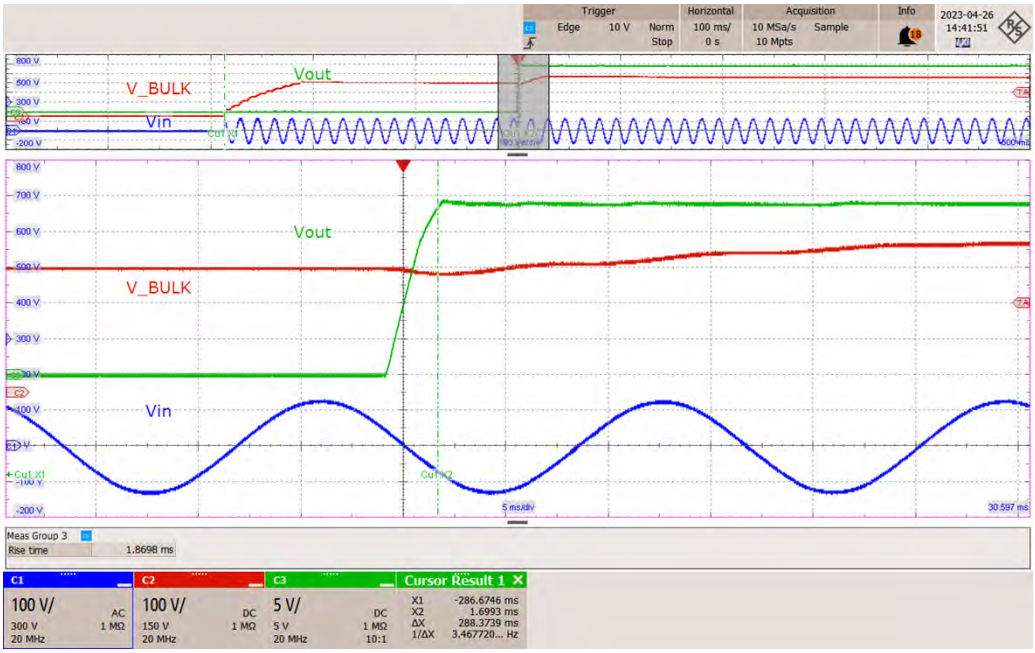


Figure 37 – Unit Start-up. 90 VAC, No Load.
Regulation Time: 288.37 ms, V_{OUT} Rise Time: 1.8698 ms
Zoom Time Division: 5 ms / div.
Blue: V_{IN}, 100 V / div. Red: V_{BULK}, 100 V / div. Green: V_{OUT}, 5 V / div.

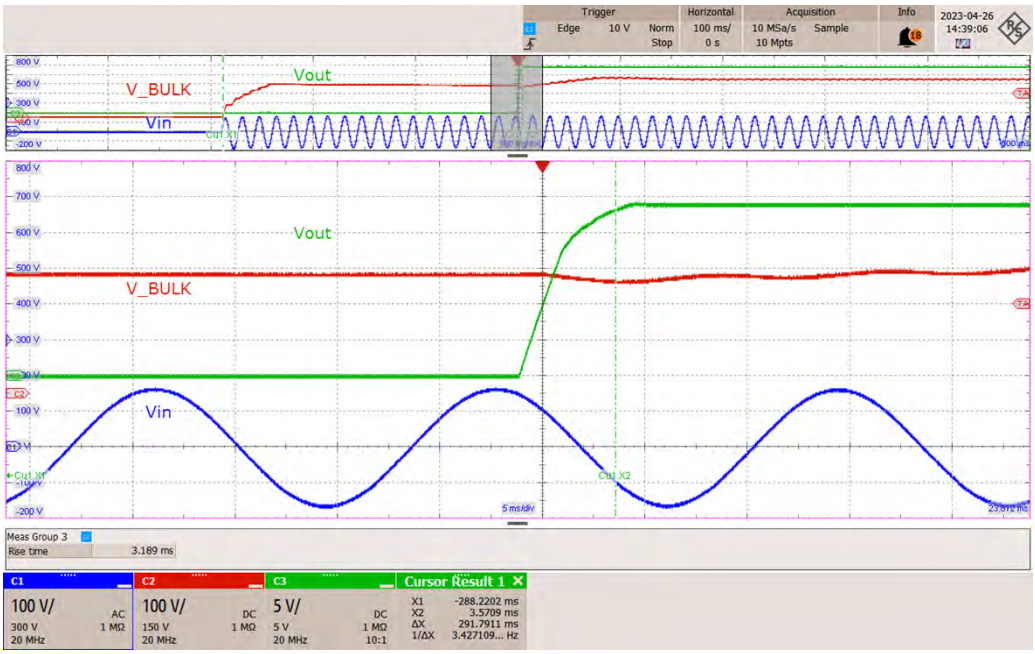


Figure 38 – Unit Start-up. 115 VAC, Full Load.
Regulation Time: 308.92 ms, V_{OUT} Rise Time: 3.0536 ms
Zoom Time Division: 5 ms / div.
Blue: V_{IN}, 100 V / div. Red: V_{BULK}, 100 V / div. Green: V_{OUT}, 5 V / div.

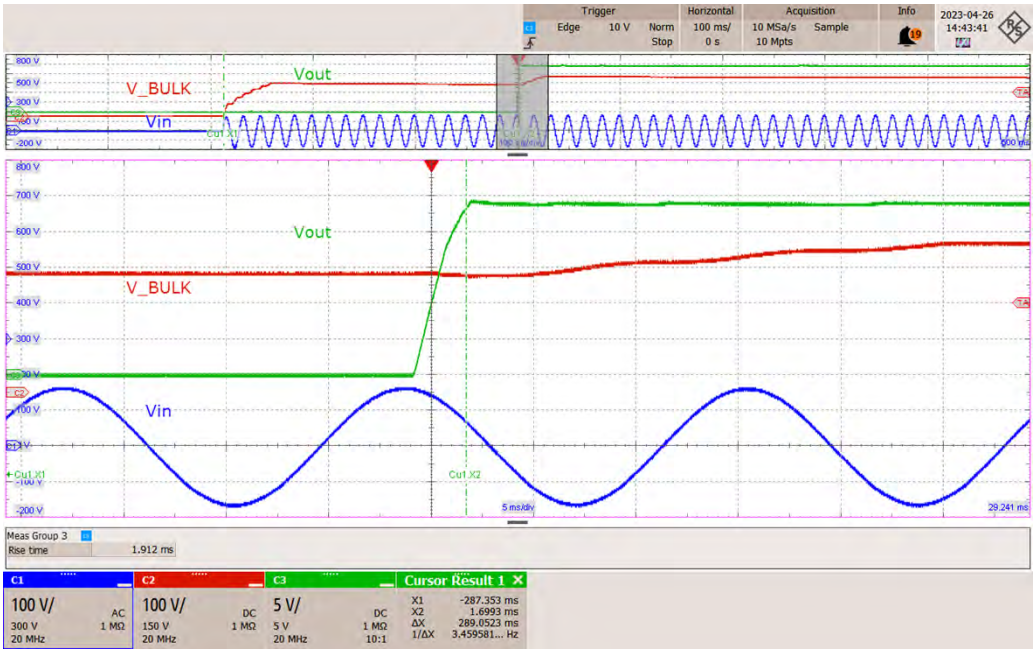


Figure 43 – Unit Start-up. 115 VAC, No Load.
Regulation Time: 289.05 ms, V_{OUT} Rise Time: 1.912 ms
Zoom Time Division: 5 ms / div.
Blue: V_{IN}, 100 V / div. Red: V_{BULK}, 100 V / div. Green: V_{OUT}, 5 V / div.

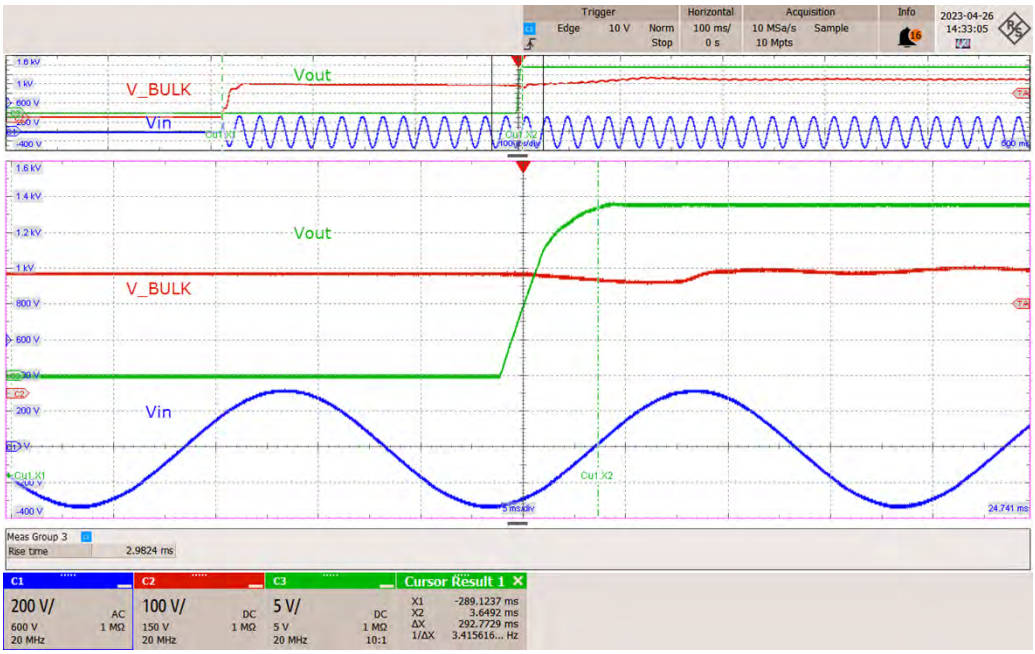


Figure 44 – Unit Start-up. 230 VAC, Full Load.
Regulation Time: 292.77 ms, V_{OUT} Rise Time: 2.9824 ms
Zoom Time Division: 5 ms / div.
Blue: V_{IN}, 200 V / div. Red: V_{BULK}, 100 V / div. Green: V_{OUT}, 5 V / div.

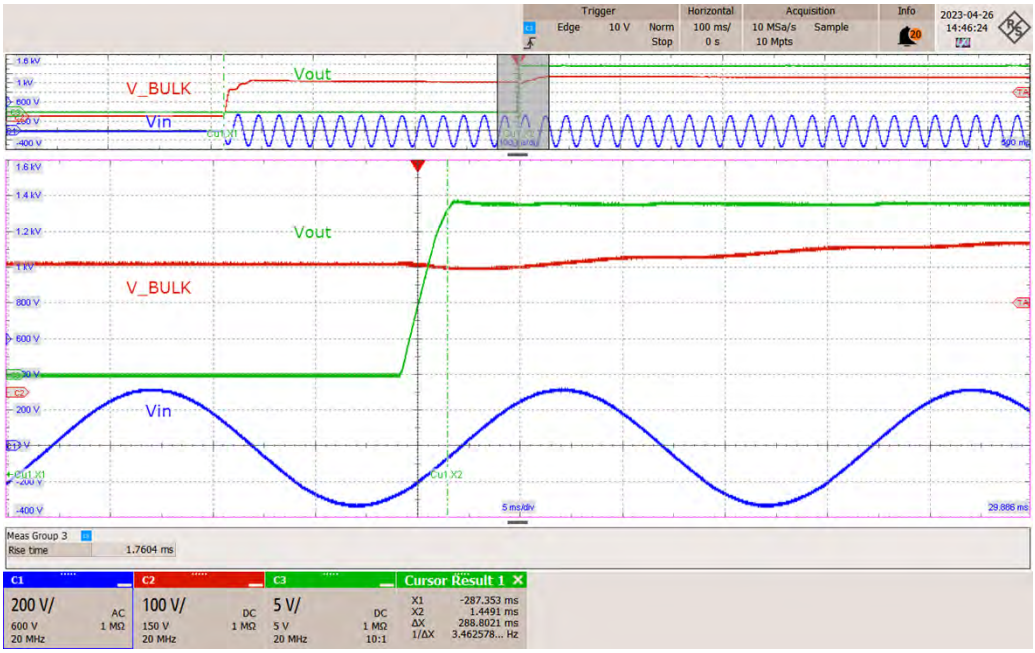


Figure 45 – Unit Start-up. 230 VAC, No Load.
Regulation Time: 288.80 ms, V_{OUT} Rise Time: 1.7604 ms
Zoom Time Division: 5 ms / div..
Blue: V_{IN}, 200 V / div. Red: V_{BULK}, 100 V / div. Green: V_{OUT}, 5 V / div.

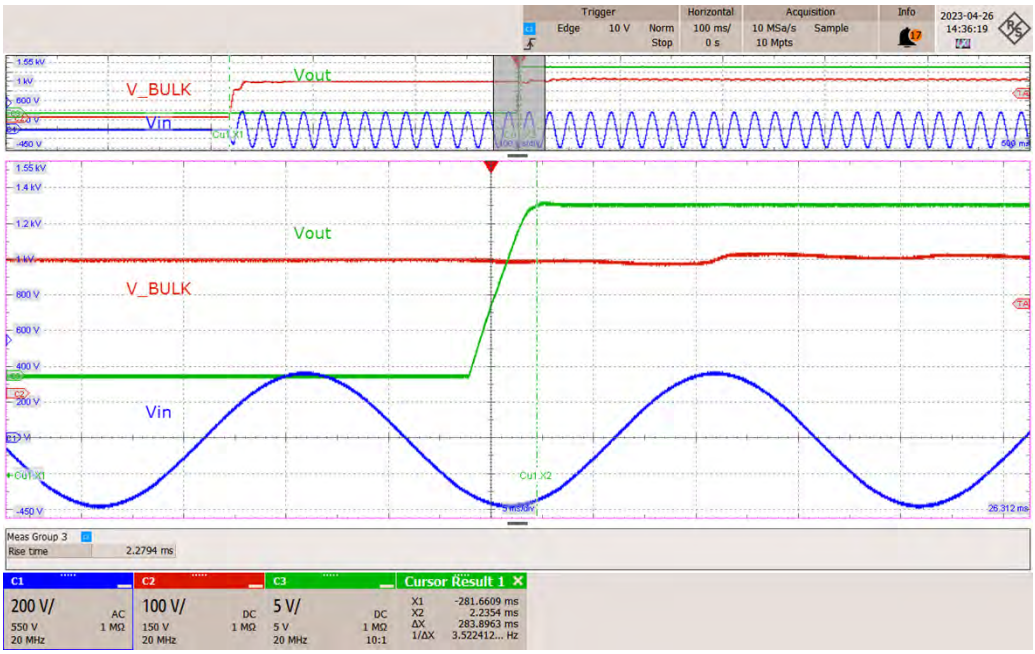


Figure 46 – Unit Start-up. 265 VAC, Full Load.
Regulation Time: 283.90 ms, V_{OUT} Rise Time: 2.2794 ms
Zoom Time Division: 5 ms / div.
Blue: V_{IN}, 200 V / div. Red: V_{BULK}, 100 V / div. Green: V_{OUT}, 5 V / div.

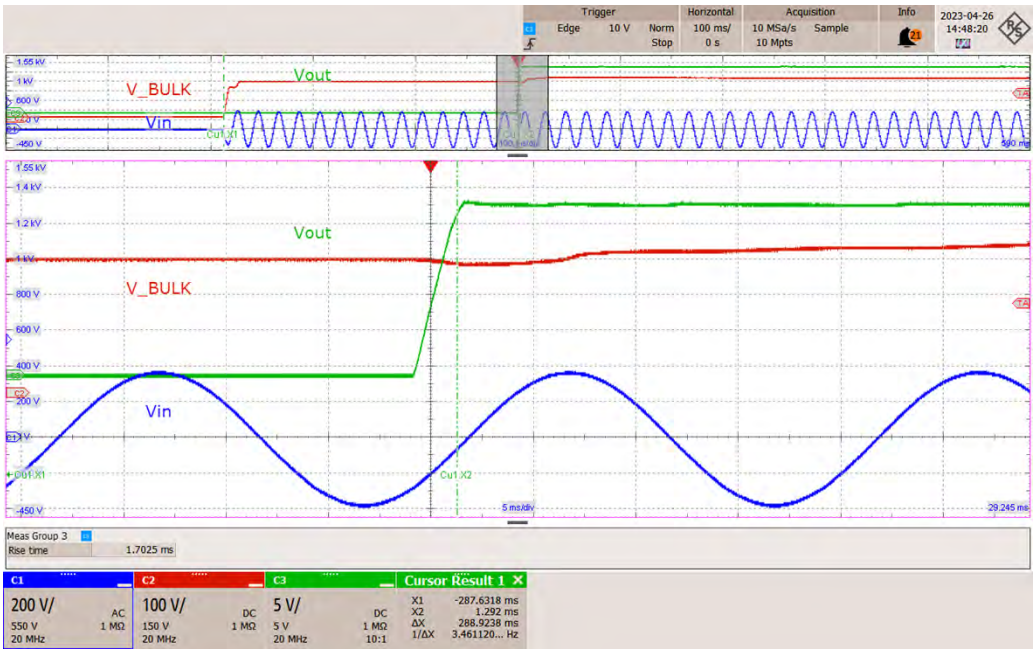


Figure 47 – Unit Start-up. 265 VAC, No Load.
Regulation Time: 288.92 ms, V_{OUT} Rise Time: 1.7025 ms
Zoom Time Division: 5 ms / div.
Blue: V_{IN}, 200 V / div. Red: V_{BULK}, 100 V / div. Green: V_{OUT}, 5 V / div.

12.6 *Burst Operation Waveforms*

Burst Mode is generally used for system efficiency, output regulation and to limit the burst frequency envelope below audio frequency.
Shown below are the different burst mode of the LLC converter that can be encountered during light load conditions.

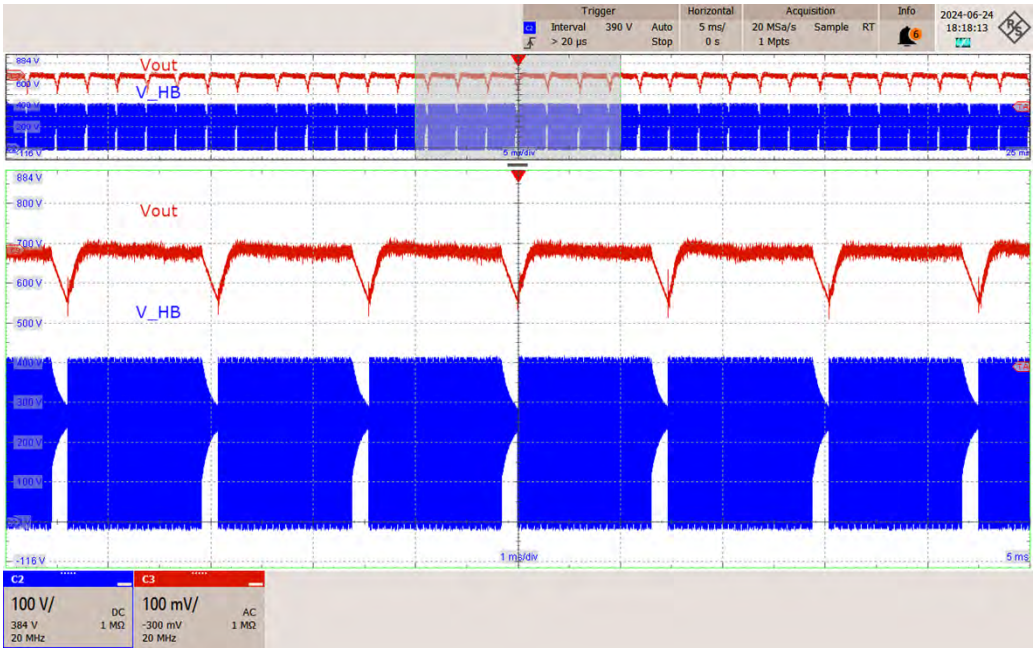


Figure 48 –Burst Operation During Light Load Condition (2.0A), 230 VAC
Time Division: 5 ms / div
Zoom Time Division: 1 ms / div
Blue: V_{HB}, 100 V / div. Red: V_{OUT}, 100 mV / div.

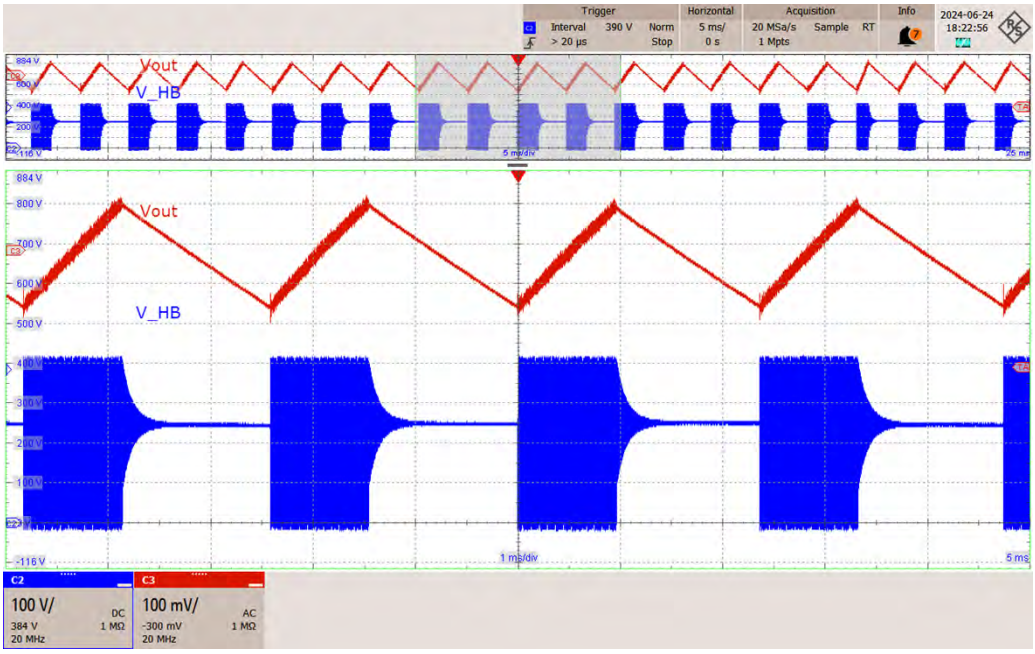


Figure 49 –Burst Operation During Light Load Condition (0.5A), 230 VAC
Time Division: 5 ms / div
Zoom Time Division: 1 ms / div
Blue: V_{HB}, 100 V / div. Red: V_{OUT}, 100 mV / div.

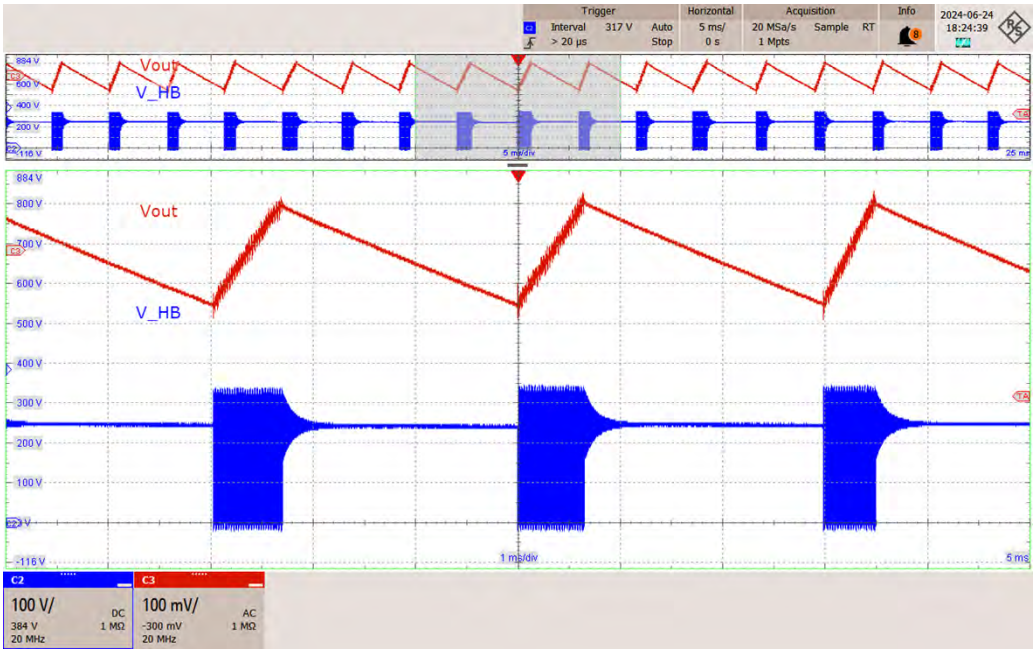


Figure 50 –Burst Operation During Light Load Condition (0.3A), 230 VAC
Time Division: 5 ms / div
Zoom Time Division: 5 us / div
Blue: V_{HB}, 100 V / div. Red: V_{OUT}, 100 mV / div.

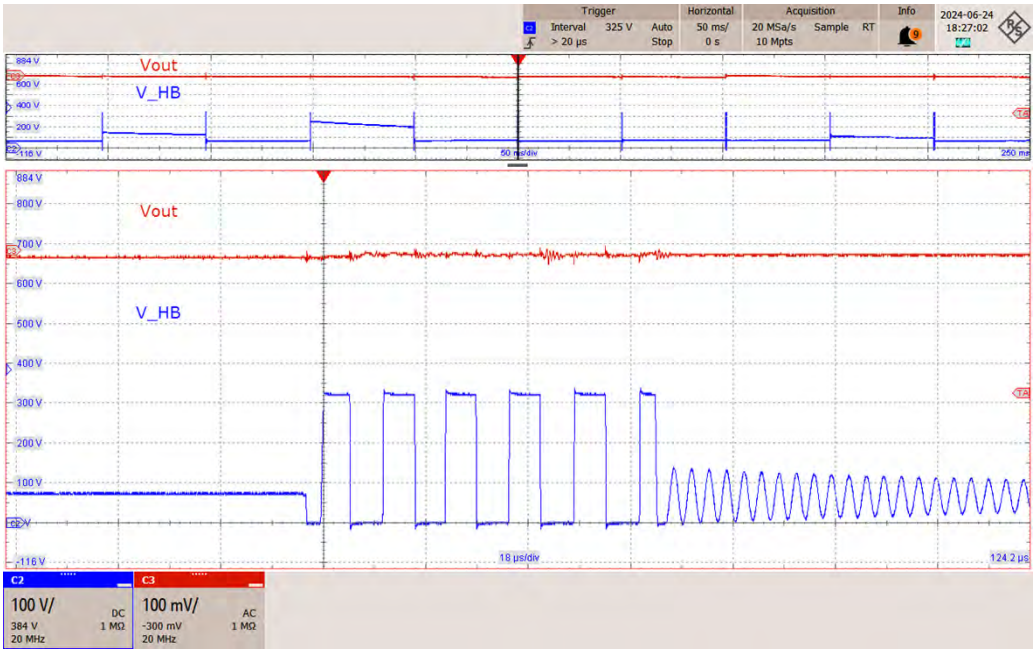


Figure 51 – Burst Operation During No Load Condition, 230 VAC
Time Division: 50 ms / div
Zoom Time Division: 18 us / div
Blue: V_{HB}, 100 V / div. Red: V_{OUT}, 100 mV / div.

12.7 *Dynamic Loading*

Figures below show the response of the LLC converter during a dynamic loading with very minimal change in voltage regulation. (Note: during no-load it is operating at burst mode that is why you can see a slightly higher regulation than loaded conditions.)

Electronic Load setting is as follows: Duty Cycle = 50%, Frequency = 100 Hz, Slew Rate = 800 mA/us.

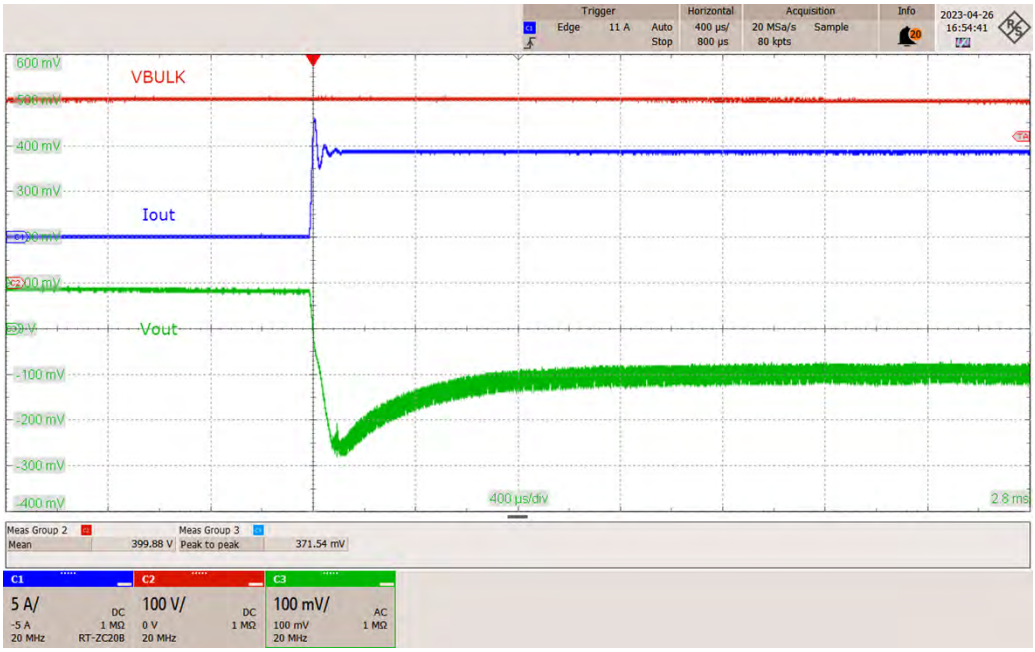


Figure 392 – Dynamic Loading. 115 VAC, 0-100% Load.
Time Division: 400 us / div, 1.55% Output Regulation Change.
Blue: I_{OUT}, 5 A / div Red: V_{BULK}, 100 V / div Green: V_{OUT}, 100 mV / div.

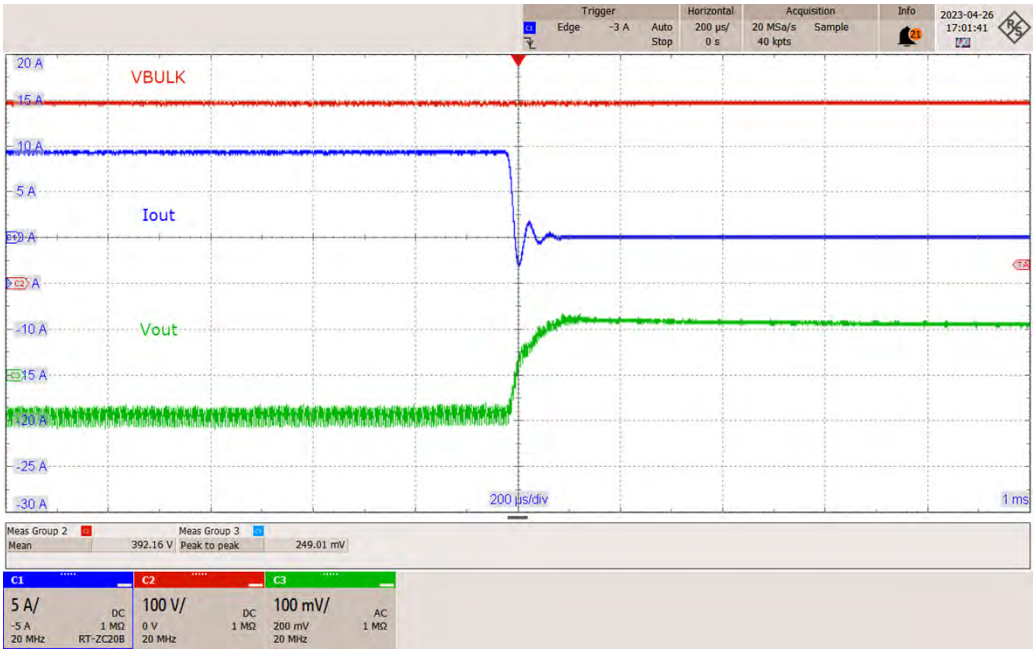


Figure 53 – Dynamic Loading. 115 VAC, 100-0% Load.
Time Division: 200 us / div, 1.04% Output Regulation Change.
Blue: I_{OUT}, 5 A / div Red: V_{BULK}, 100 V / div Green: V_{OUT}, 100 mV / div.

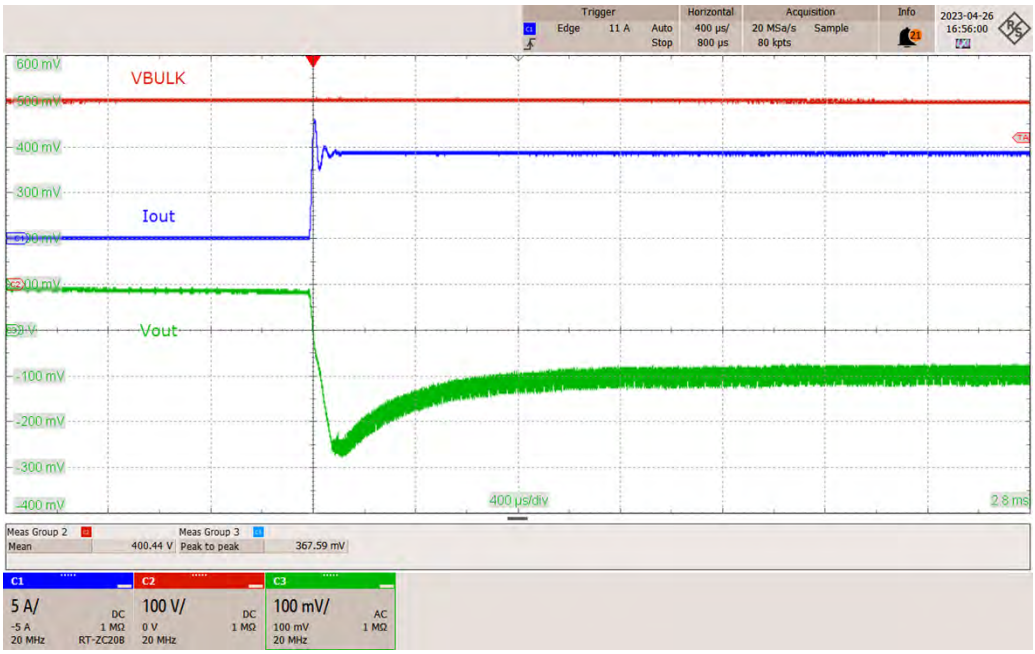


Figure 54 – Dynamic Loading. 230 VAC, 0-100% Load.
Time Division: 400 us / div, 1.53% Output Regulation Change.
Blue: I_{OUT}, 5 A / div Red: V_{BULK}, 100 V / div Green: V_{OUT}, 100 mV / div.

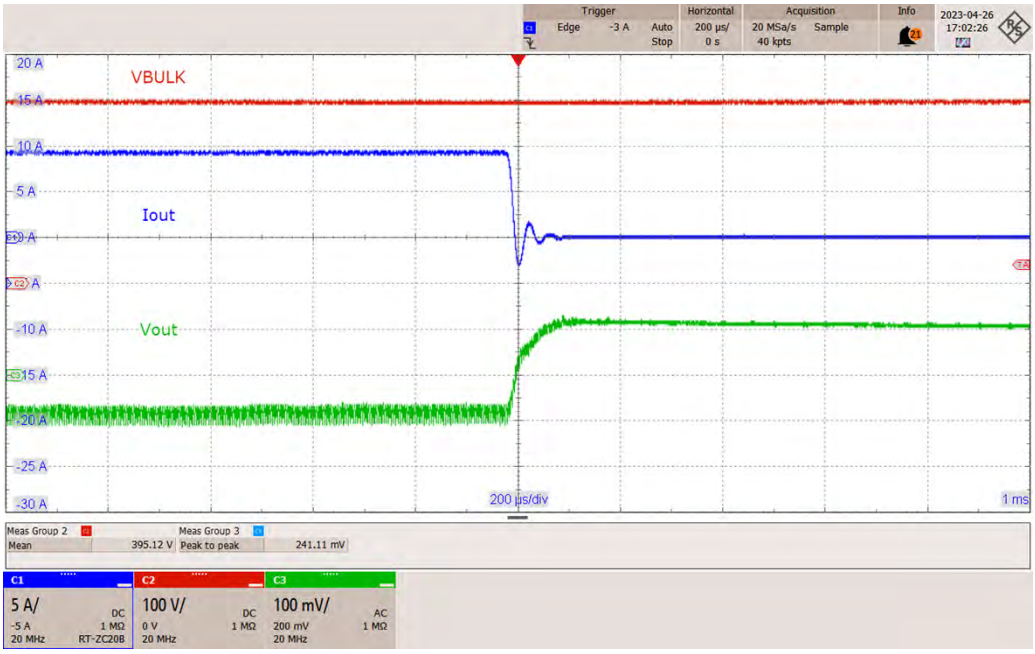


Figure 55 – Dynamic Loading. 230 VAC, 100-0% Load.
Time Division: 200 us / div, 1.00% Output Regulation Change.
Blue: I_{OUT}, 5 A / div Red: V_{BULK}, 100 V / div Green: V_{OUT}, 100 mV / div.

13 Output Ripple Measurements

13.1 ***Ripple Measurement Technique***

For DC output ripple measurements, a modified oscilloscope test probe is used to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. A 0.1 µF / 100 V ceramic capacitor and 47 µF / 100 V aluminum electrolytic capacitor were used. The aluminum electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

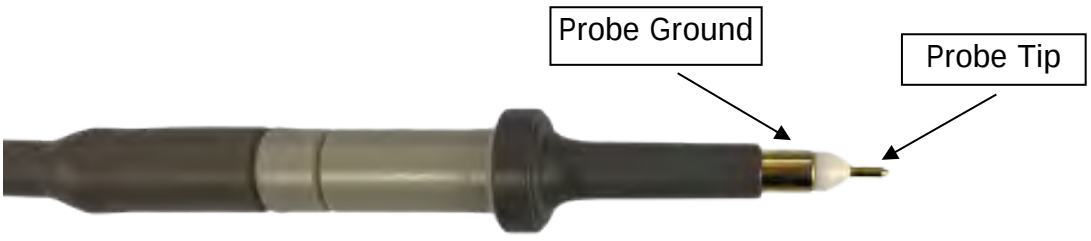


Figure 406 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

Figure 57 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

13.2 *Ripple Measurements*

The following pictures show the output voltage ripple measurement with electronic load configured to constant current (CCH) mode. Measurements were taken at 230VAC line voltage at full load, intermediate burst(IM) and light load burst (LL).

Note: Use 20MHz Bandwidth

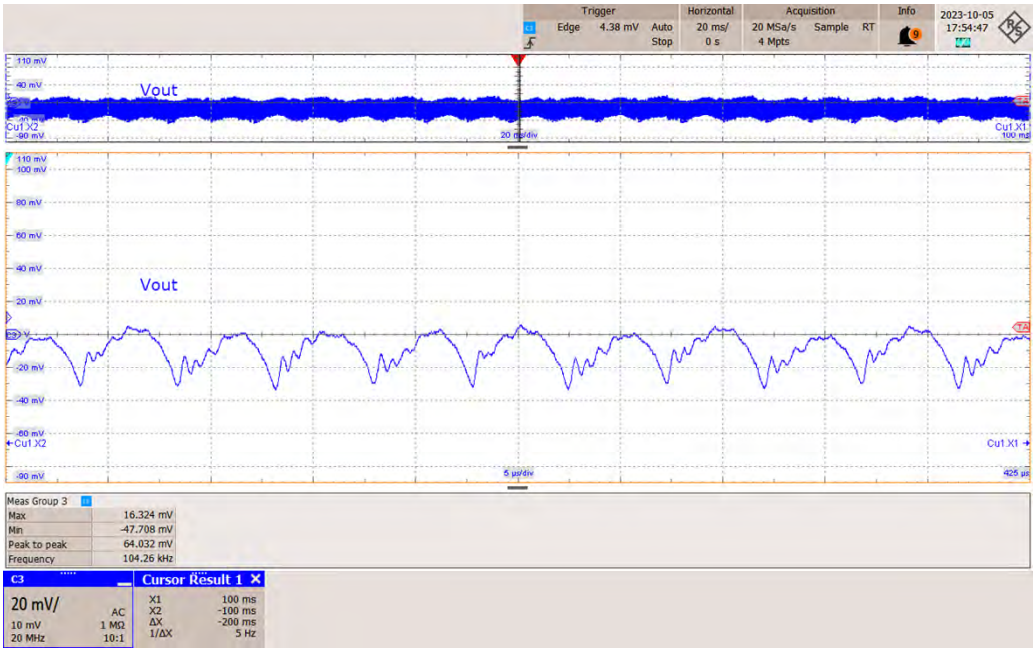


Figure 58– Output Ripple at Full Load (9.2 A), 230 VAC.
Time Division: 20 ms / div
Zoom Time Division: 5 us / div
Blue: V_{OUT}, 20 mV / div.

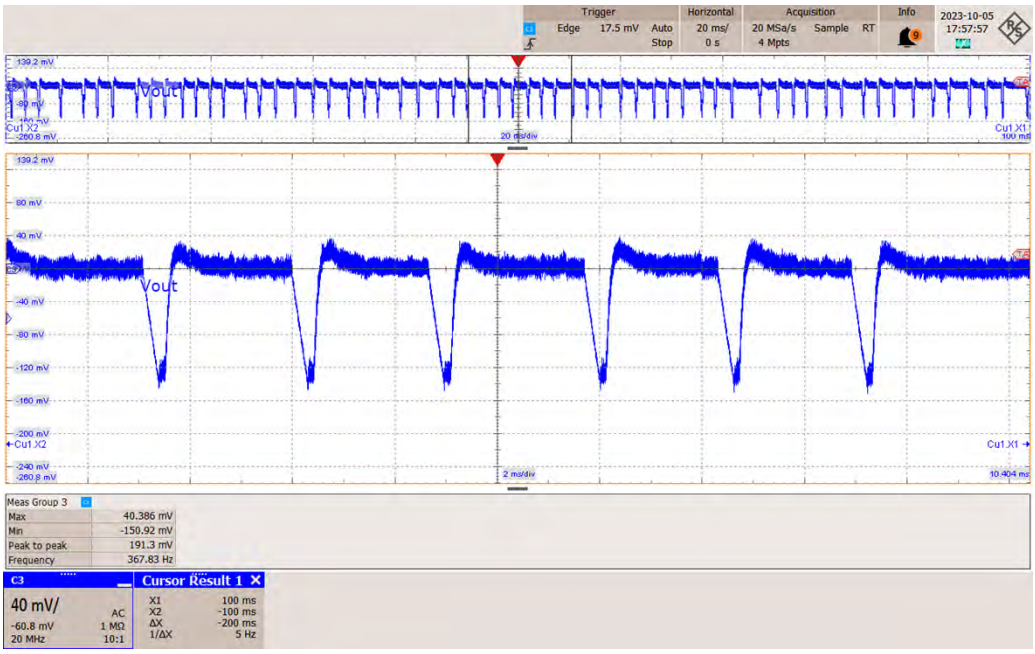


Figure 59– Output Ripple at Light Load Condition (2.0A), 230 VAC.
Time Division: 20 ms / div
Zoom Time Division: 2 ms / div
Blue: V_{OUT}, 40 mV / div.

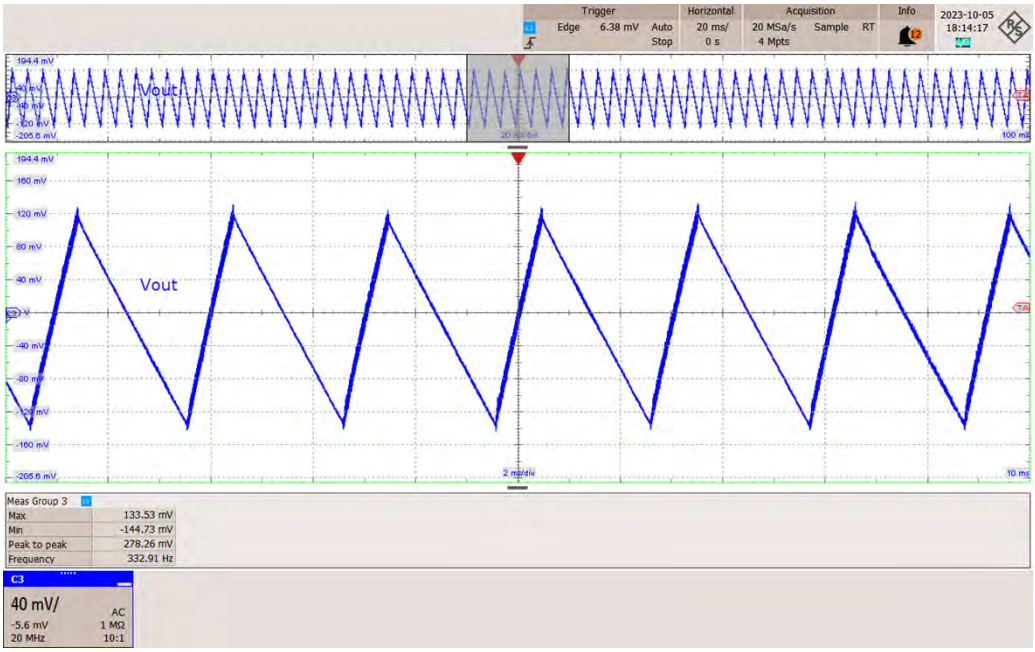


Figure 60– Output Ripple at Light Load Condition (0.5A), 230 VAC.
Time Division: 20 ms / div
Zoom Time Division: 2 ms / div
Blue: V_{OUT}, 40 mV / div.

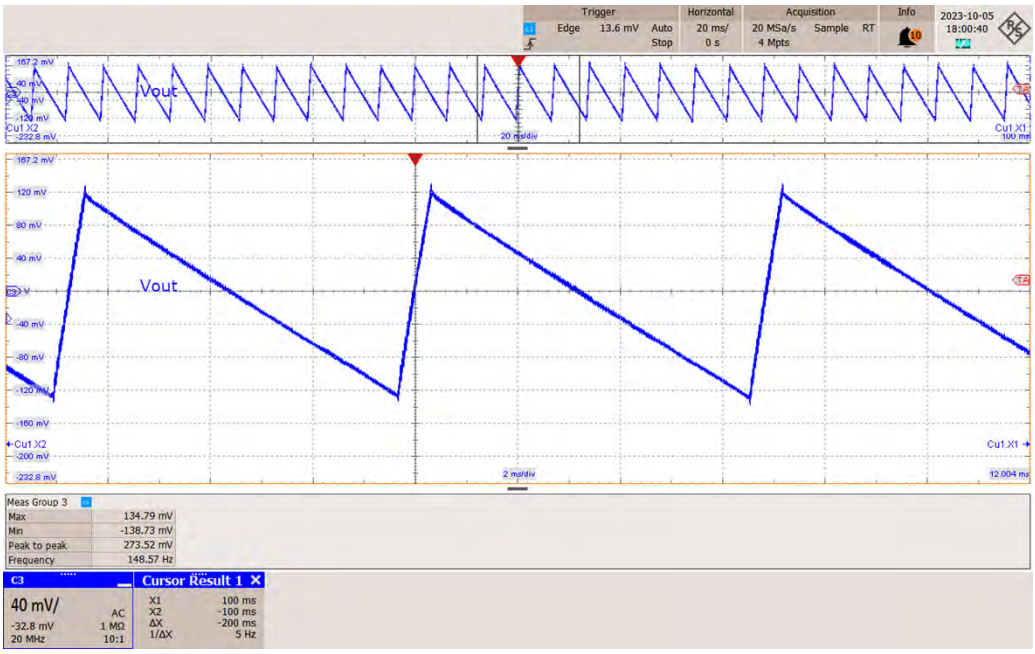


Figure 61– Output Ripple at Light Load Condition (0.3A), 230 VAC.
Time Division: 20 ms / div
Zoom Time Division: 2 ms / div
Blue: V_{OUT}, 40 mV / div.

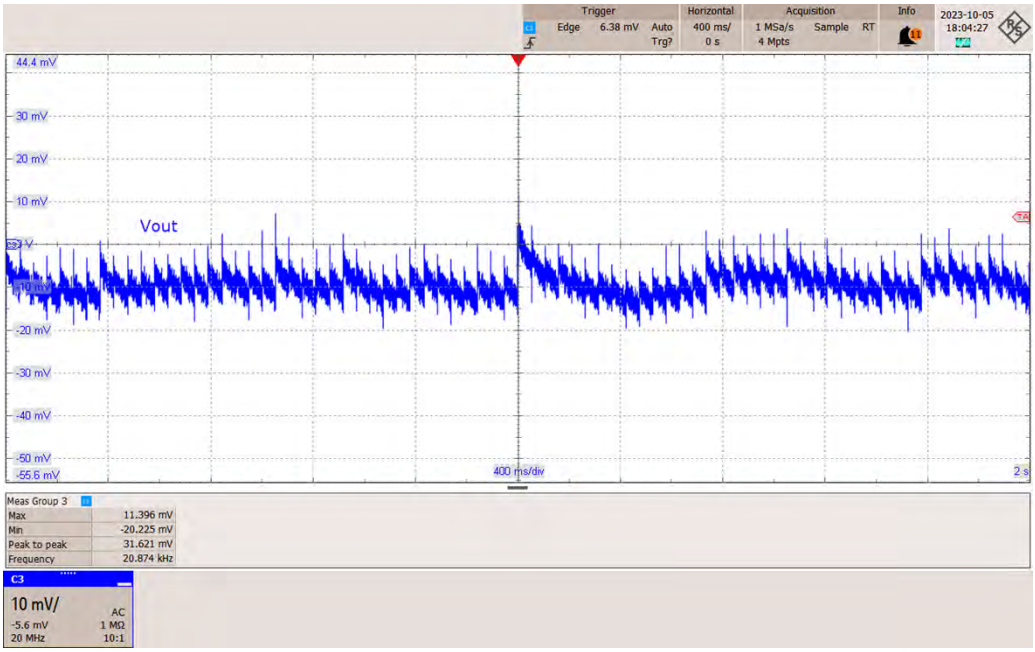


Figure 62– Output Ripple at No Load, 230 VAC.
Time Division: 400 ms / div
Blue: V_{OUT}, 10 mV / div.

14 Temperature Profiles

The board was placed in an enclosed acrylic box, with electronic load set at constant current mode with full load current of 9.2 A. For each test conditions, the UUT was soaked for 1 hour before measurement was made.

14.1 *90 VAC, 60 Hz, 220 W Output*

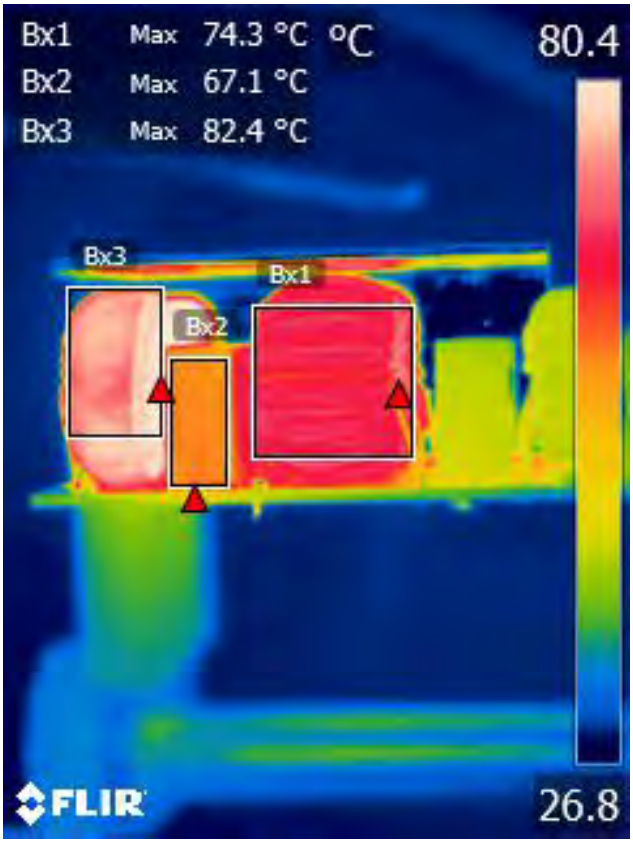


Figure 63– EMI Side Thermal Picture, 100% Load, 90 VAC.

Legend	Refdes	Description	Temperature (^{0}C)
BX1	L2	CMC	74.3
BX2	C1	XCAP	67.1
BX3	L4	DIFF CHK	82.4
		AMBIENT	32

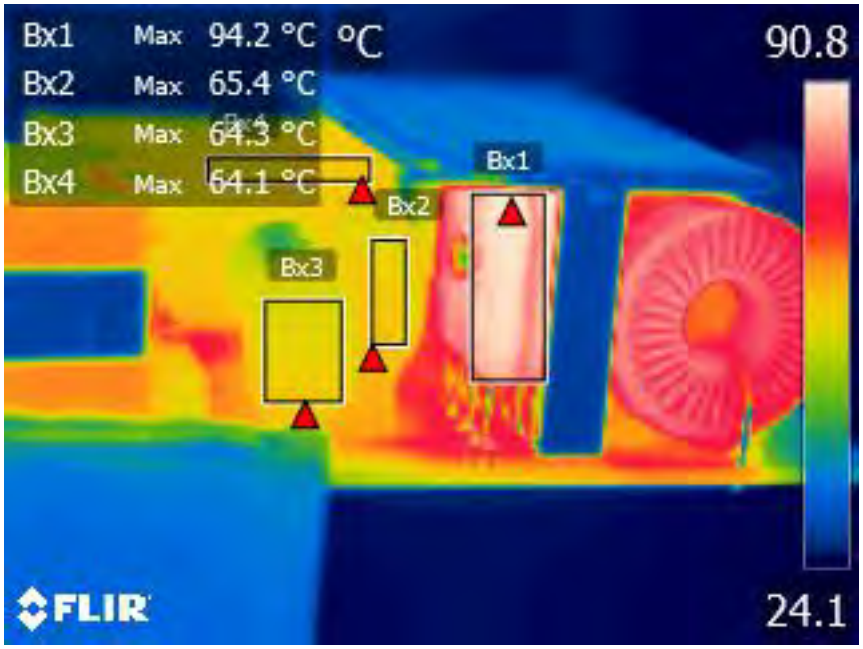


Figure 64– Bridge Rectifier Side Thermal Picture, 100% Load, 90 VAC.

Legend	Refdes	Description	Temperature (^{0}C)
BX1	BR1	BRIDGE DIODE	94.2
BX2	RT1	THERMISTOR	65.4
BX3	C3	XCAP	64.3
BX4	C10	BULK CAP	64.1
		AMBIENT	32

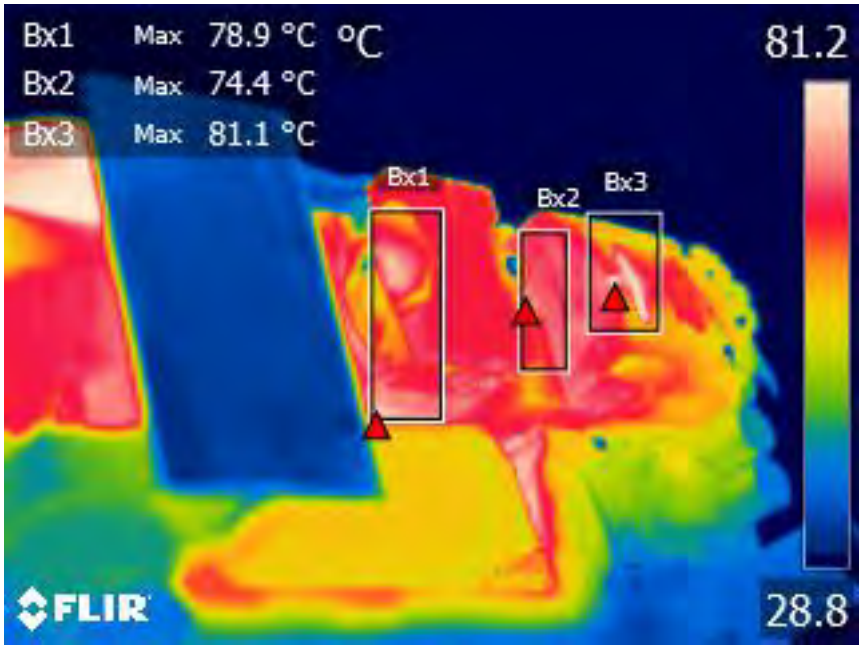


Figure 415 – Top Side Thermal Picture, 100% Load, 90 VAC.

Legend	Refdes	Description	Temperature (^{0}C)
BX1	T1	PFC CHK	78.9
BX2	T2	LLC TRF CORE	74.4
BX3	T2	LLC TRF WDG	81.1
		AMBIENT	32

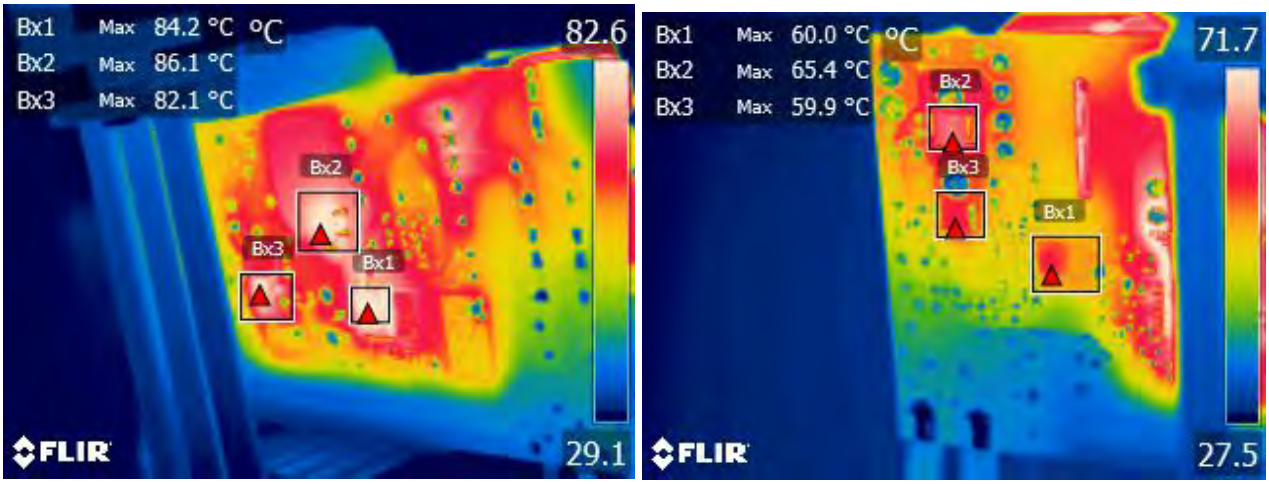


Figure 426 – Bottom Side Thermal Picture, 100% Load, 90 VAC.

Legend	Refdes	Description	Temperature (^{0}C)
BX1	U1	HIPERPFS-5	84.2
BX2	D3	BOOST DIODE	86.1
BX3	U2	HIPERLCS-2 HB	82.1
		AMBIENT	32

Legend	Refdes	Description	Temperature (^{0}C)
BX1	U3	HIPERLCS-2 SR	60.0
BX2	Q4	SR1	65.4
BX3	Q5	SR2	59.9
		AMBIENT	32

14.2 *265 VAC, 50 Hz, 220 W Output, Room Temperature*

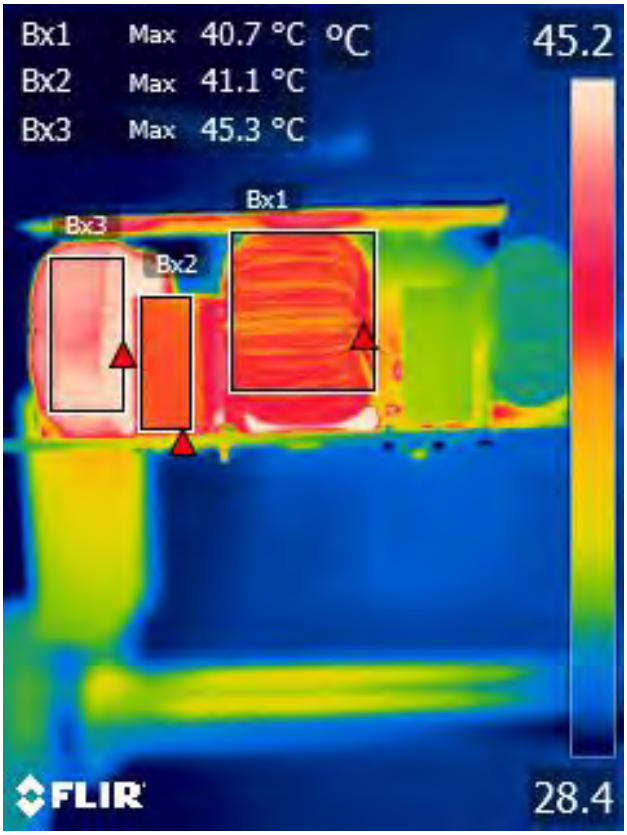


Figure 67– EMI Side Thermal Picture, 100% Load, 265 VAC.

Legend	Refdes	Description	Temperature (^{0}C)
BX1	L2	CMC	40.7
BX2	C1	XCAP	41.1
BX3	L4	DIFF CHK	45.3
		AMBIENT	28

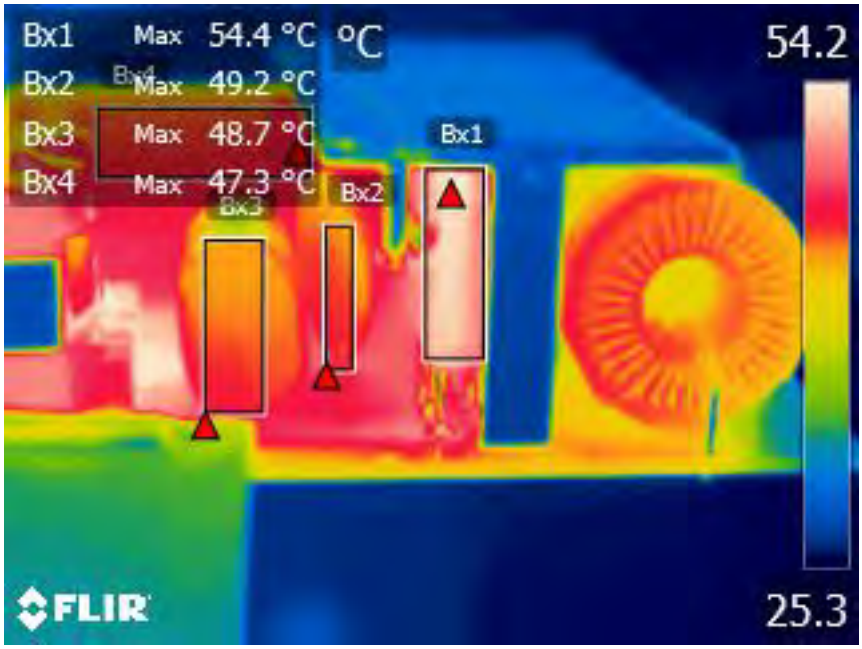


Figure 68 – Bridge Rectifier Side Thermal Picture, 100% Load, 265 VAC.

Legend	Refdes	Description	Temperature (^{0}C)
BX1	BR1	BRIDGE DIODE	54.4
BX2	RT1	THERMISTOR	49.2
BX3	C3	XCAP	48.7
BX4	C10	BULK CAP	47.3
		AMBIENT	28

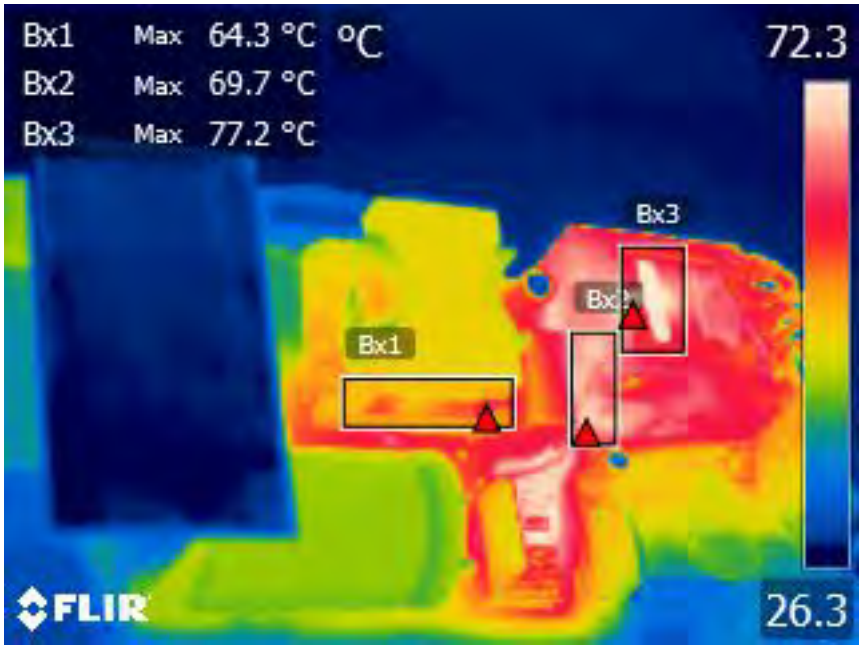


Figure 439– Top Side Thermal Picture, 100% Load, 265 VAC.

Legend	Refdes	Description	Temperature (^{0}C)
BX1	T1	PFC CHK	64.3
BX2	T2	LLC TRF CORE	69.7
BX3	T2	LLC TRF WDG	77.2
		AMBIENT	28

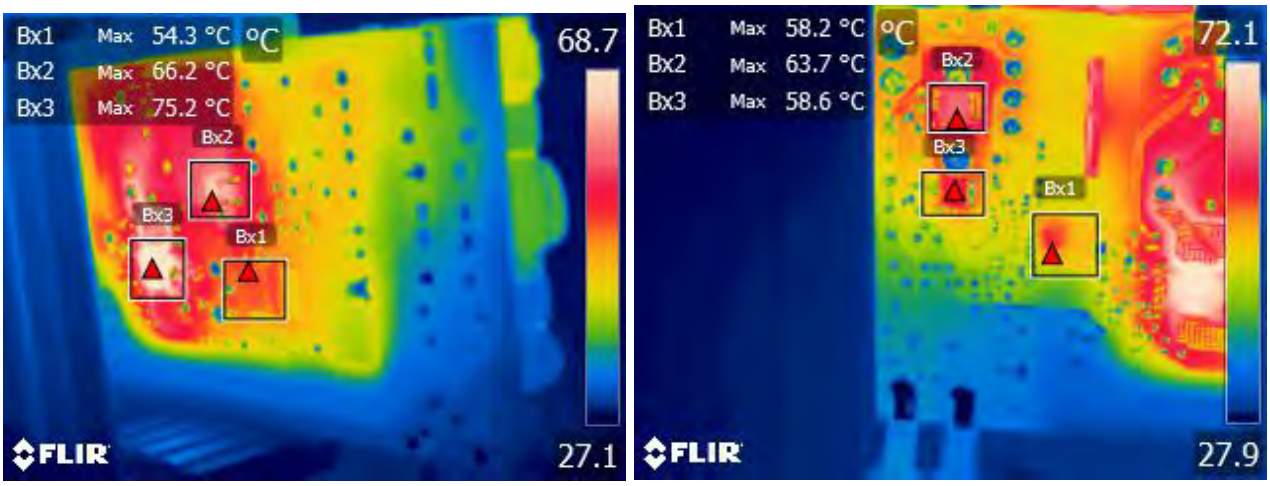


Figure 70– Bottom Side Thermal Picture, 100% Load, 265 VAC.

Legend	Refdes	Description	Temperature (^{0}C)
BX1	U1	HIPERPFS-5	54.3
BX2	D3	BOOST DIODE	66.2
BX3	U2	HIPERLCS-2 PRI	75.2
		AMBIENT	28

Legend	Refdes	Description	Temperature (^{0}C)
BX1	U3	HIPERLCS-2 SEC	58.2
BX2	Q4	SR1	63.7
BX3	Q5	SR2	58.6
		AMBIENT	32

15 Conducted EMI

Conducted EMI tests were performed at 115 VAC and 230 VAC at full load (24V, 9.2A). Measurements were taken with the LISN ground connected to the output ground.

15.1 ***Test Set-up and Equipment Used***

15.1.1 *Test Set-up*

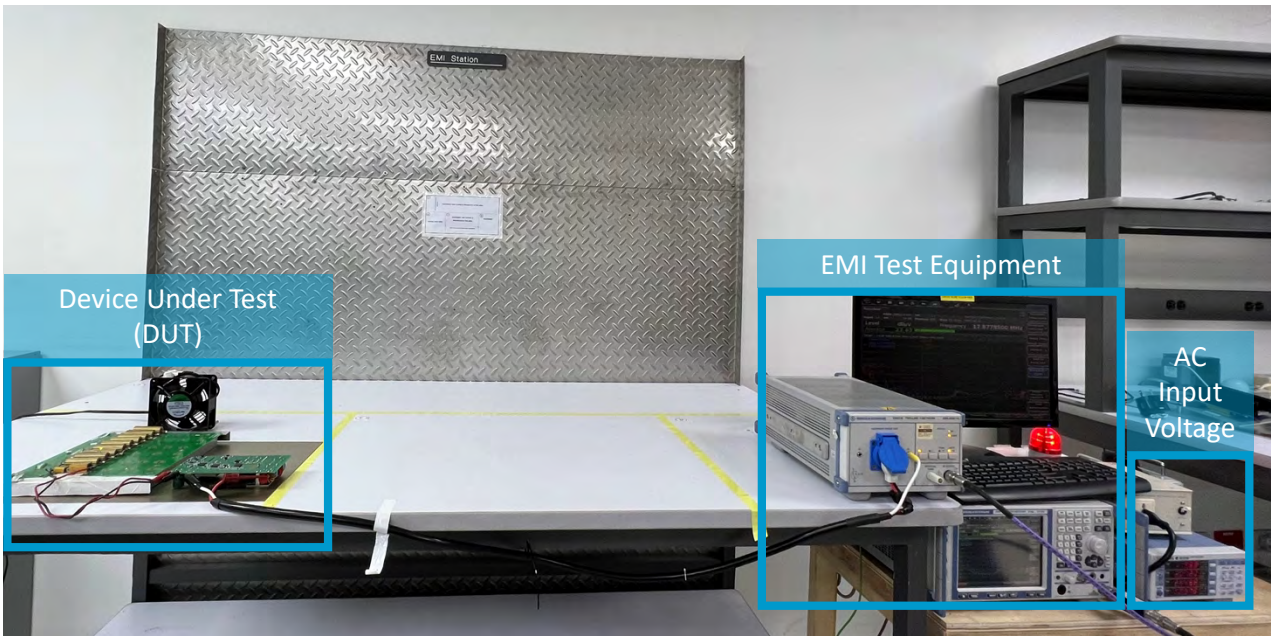


Figure 71 – EMI Test Set-up

15.1.2 *Equipment and Load Used*

1. Rohde and Schwarz ENV216 two-line V-network.
2. Rohde and Schwarz ESRP EMI Test Receiver.
3. Yokogawa WT310E Digital Power Meter
4. Chroma Measurement test fixture
5. Input Voltage set at 115 VAC and 230 VAC.
6. 2.6 ohms Resistor Load

15.2 *Test Results*

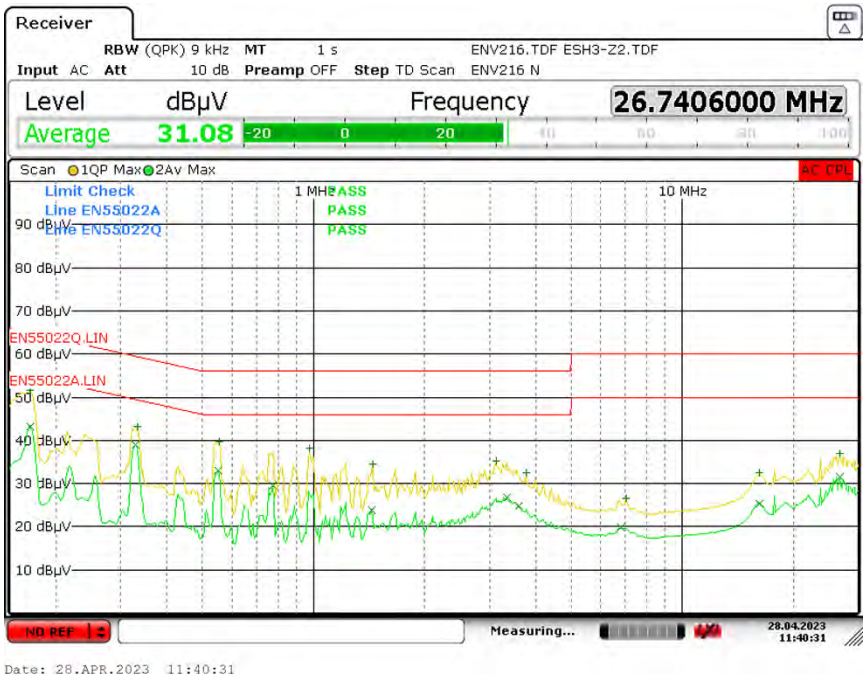


Figure 72 – Conducted EMI QP Scan at 24V 9.2A Load, 115 VAC, 60Hz, LISN ground.

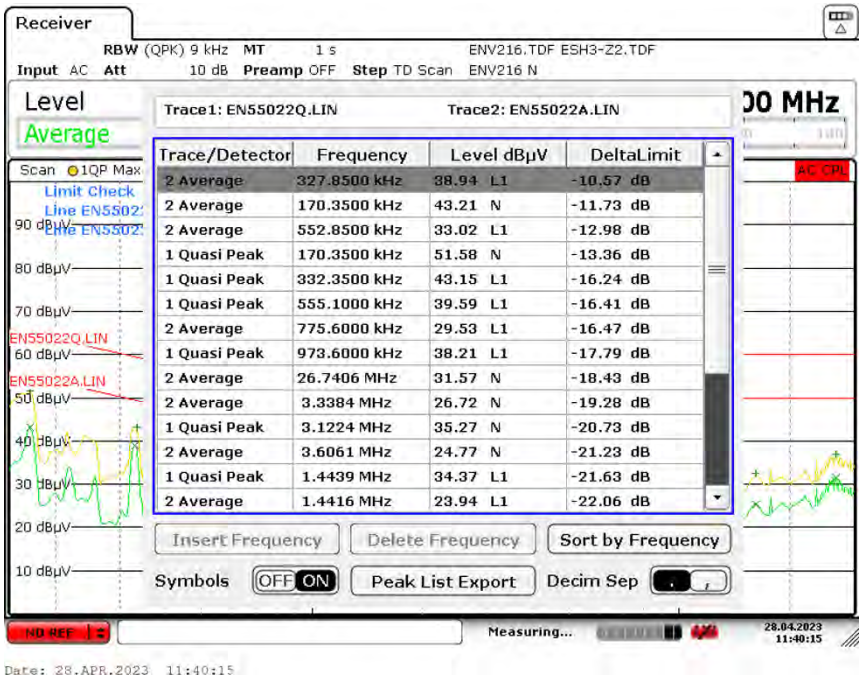


Figure 73 – Conducted EMI Data at 24V 9.2A Load, 115 VAC, 60Hz.

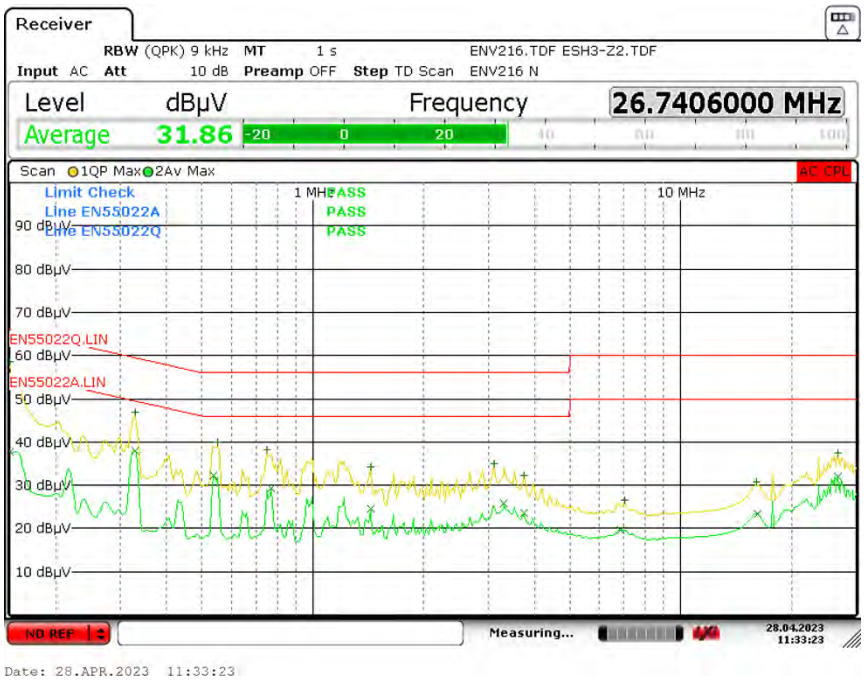


Figure 74 – Conducted EMI QP Scan at 24V 9.2A Load, 230 VAC, 60Hz, LISN ground.

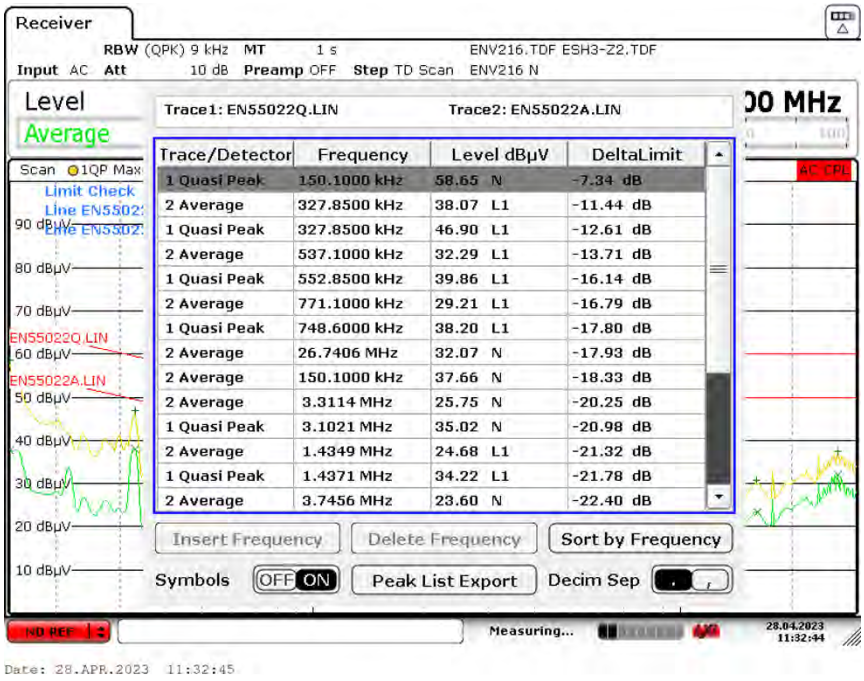


Figure 75 – Conducted EMI Data at 24V 9.2A Load, 230 VAC, 60Hz.

16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
16-Mar-22	MCDP	1.0	Initial Release	Apps & Mktg
18-Apr-24	ZK	1.1	Updates made to page 1 Application text and page 5 Introduction.	Mktg
05-Jul-24	AAM	1.2	New board revision to update EMI Section. Include conducted EMI test data	Apps & Mktg

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@power.com

CHINA (SHANGHAI)
Rm 2410, Charity Plaza, No. 88,
North Caoxi Road,
Shanghai, PRC 200030
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail:
chinasales@power.com

CHINA (SHENZHEN)
17/F, Hivac Building, No. 2, Keji Nan 8th Road, Nanshan District,
Shenzhen, China, 518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@power.com

GERMANY
(AC-DC/LED Sales)
Lindwurmstrasse 114
80337, Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@power.com

GERMANY
(IGBT Driver Sales)
HellwegForum 1
59469 Ense, Germany
Tel: +49-2938-64-39990
Email: igbt-
driver.sales@power.com

INDIA
#1, 14th Main Road
Vasanthanagar
Bangalore-560052
India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail:
indiasales@power.com

ITALY
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI)
Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@power.com

JAPAN
Kosei Dai-3 Building
2-12-11, Shin-Yokohama,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033
Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@power.com

KOREA
RM 602, 6FL
Korea City Air Terminal B/D,
159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728 Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@power.com

SINGAPORE
51 Newton Road,
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail:
singaporesales@power.com

TAIWAN
5F, No. 318, Nei Hu Rd.,
Sec. 1
Nei Hu District
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@power.com

UK
Cambridge Semiconductor,
a Power Integrations company
Westbrook Centre, Block 5, 2nd Floor
Milton Road
Cambridge CB4 1YG
Phone: +44 (0) 1223-446483
e-mail: eurosales@power.com