

Design Example Report

Title	<i>45 W USB PD 3.0 Power Supply with 3.3 V – 21 V PPS Output Using InnoSwitch™ 3-Pro INN3368C-H301 and VIA Labs VP302 Controller</i>
Specification	85 VAC – 265 VAC Input; 5 V / 5 A; 9 V / 3 A; 15 V / 3 A; 20 V / 2.25 A; or 3.3 V – 21 V PPS Output
Application	Mobile Phone Charger
Author	Applications Engineering Department
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Summary and Features

- InnoSwitch3-Pro - digitally controllable CV/CC QR flyback switcher IC with integrated high-voltage MOSFET, synchronous rectification and FluxLink™ feedback
 - I²C Interface enables low pin count USB PD Controller (8 pin)
 - Sophisticated telemetry and comprehensive protection features
- USB PD 3.0 with PPS using highly optimized, low pin count USB PD Controller VP302
 - APDO: 3.3V – 5.9V , 5A PPS (Requires e-Marked Cable)
- All the benefits of secondary-side control with the simplicity of primary-side regulation
 - Insensitive to transformer variation
- Meets DOE6 and CoC v5 2016 efficiency requirement (>1% efficiency margin)
- Micro stepping of voltages (20 mV) and CC thresholds (50 mA) in compliance with PPS protocol
- Output overvoltage and overcurrent protection
- Integrated thermal protection
- < 34 mW no-load input power

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PATENT INFORMATION

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Table of Contents

1	Introduction	7
2	Power Supply Specification	9
3	Schematic Diagram	11
4	Circuit Description	12
4.1	Input Rectifier and EMI Filter.....	12
4.2	InnoSwitch3-Pro IC Primary	12
4.3	InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller	13
4.4	USB Type-C and PD Interface.....	14
5	PCB Layout	15
6	Bill of Materials	16
7	Transformer (T1) Specification	18
7.1	Electrical Diagram.....	18
7.2	Electrical Specifications	18
7.3	Materials	18
7.4	Transformer Build Diagram	19
7.5	Winding Instructions.....	19
7.6	Winding Illustrations	20
8	Common Mode Choke Specifications.....	30
8.1	250 μ H Common Mode Choke (L2)	30
8.1.1	Electrical Diagram	30
8.1.2	Electrical Specifications.....	30
8.1.3	Material List.....	30
8.1.4	Winding Construction	31
8.2	16 mH Common Mode Choke (L1)	32
8.2.1	Electrical Diagram	32
8.2.2	Electrical Specifications.....	32
8.2.3	Materials List	32
8.2.4	Winding Instructions	32
9	Transformer Design Spreadsheet	33
10	Adapter Case Dimensions	38
10.1	Case Bottom Dimensions.....	38
10.2	Case Top Dimensions.....	38
10.3	Adapter Assembly Drawing.....	39
11	Heat Spreader Drawings.....	39
12	Heat Spreader Assembly Instructions	42
12.1	Materials	42
12.2	Assembly Instructions	42
13	PCB Assembly Instructions	48
13.1	Materials	48
13.2	Output capacitor and transformer assembly instructions	48
14	Performance Data	51

14.1	Efficiency vs. Load	51
14.1.1	Output: 3.3 V / 5 A	51
14.1.2	Output: 5 V / 5 A	52
14.1.3	Output: 9 V / 3 A	53
14.1.4	Output: 15 V / 3 A	54
14.1.5	Output: 16 V / 3 A	55
14.1.6	Output: 20 V / 2.25 A	56
14.1.7	Output: 21 V / 2.25 A	57
14.2	Efficiency vs. Line	58
14.3	Load Regulation	59
14.3.1	Output: 3.3 V / 5 A	59
14.3.2	Output: 5 V / 5 A	60
14.3.3	Output: 9 V / 3 A	61
14.3.4	Output: 15 V / 3 A	62
14.3.5	Output: 16 V / 3 A	63
14.3.6	Output: 20 V / 2.25 A	64
14.3.7	Output: 21 V / 2.25 A	65
14.4	Line Regulation	66
14.4.1	Output: 3.3 V / 5 A	66
14.4.2	Output: 5 V / 5 A	67
14.4.3	Output: 9 V / 3 A	68
14.4.4	Output: 15 V / 3 A	69
14.4.5	Output: 16 V / 3 A	70
14.4.6	Output: 20 V / 2.25 A	71
14.4.7	Output: 21 V / 2.25 A	72
14.5	No-Load Input Power at 5 V _{OUT}	73
14.6	Average and 10% Load Efficiency	74
14.6.1	Efficiency Requirements	74
14.6.2	Average and 10% Efficiency (On the Board)	74
14.7	CV/CC Operation	78
14.7.1	Output: 5.9 V / 3 A	78
14.7.2	Output: 5.9 V / 5 A	79
14.7.3	Output: 11 V / 3 A	80
14.7.4	Output: 16 V / 3 A	81
14.7.5	Output: 21 V / 2.25 A	82
15	Thermal Performance in Open Case	83
15.1	85 VAC Input 15 V / 3 A	83
15.2	265 VAC Input 15 V / 3 A	83
15.3	85 VAC Input 16 V / 3 A	84
15.4	265 VAC Input 16 V / 3 A	84
15.5	85 VAC Input 20 V / 2.25 A	85
15.6	265 VAC Input 20 V / 2.25 A	85



16	Thermal Performance with Enclosure	86
16.1	Room Temperature.....	86
16.1.1	85 VAC Input 15 V / 3 A.....	86
16.1.2	265 VAC Input 15 V / 3 A	87
16.1.3	85 VAC Input 20 V / 2.25 A	88
16.1.4	265 VAC Input 20 V / 2.25 A	89
16.2	High Temperature	90
16.2.1	85 VAC Input 15 V / 3 A.....	90
16.2.2	85 VAC Input 16 V / 3 A.....	91
16.2.3	85 VAC Input 20 V / 2.25 A	92
17	Output Voltage Ripple Measurements.....	93
17.1	Ripple Measurement Technique	93
17.2	Output Voltage Ripple Waveforms	94
17.2.1	Output: 3.3 V / 5 A	94
17.2.2	Output: 5 V / 5 A.....	94
17.2.3	Output: 9 V / 3 A	95
17.2.4	Output: 15 V / 3 A	95
17.2.5	Output: 16 V / 3 A	96
17.2.6	Output: 20V / 2.25 A.....	96
17.2.7	Output: 21V / 2.25 A.....	97
17.3	Output Voltage Ripple Amplitude vs. Load	98
17.3.1	Output: 3.3 V / 5 A	98
17.3.2	Output: 5 V / 5 A	99
17.3.3	Output: 9 V / 3 A	100
17.3.4	Output: 15 V / 3 A	101
17.3.5	Output: 16 V / 3 A	102
17.3.6	Output: 20 V / 2.25 A.....	103
17.3.7	Output: 21 V / 2.25 A.....	104
18	Waveforms.....	105
18.1	Transient Response (On the Board)	105
18.1.1	Output: 3.3 V	105
18.1.2	Output: 5 V	108
18.1.3	Output: 9 V	110
18.1.4	Output: 15 V	112
18.1.5	Output: 20 V	114
18.2	Drain Voltage and Current.....	116
18.3	Drain Voltage and Current at Start-up.....	119
18.4	SR FET Voltage.....	120
18.5	Output Voltage and Current at Start-up (On the Board)	124
19	Voltage and Current Step Test using Quadramax and Total Phase Analyzer	125
19.1	Voltage Step Test (VST).....	125
19.2	Current Limit Test (CLT)	125

20	Conducted EMI	126
20.1	Floating Output	126
20.1.1	Output: 5 V / 5 A	126
20.1.2	Output: 9 V / 3 A	128
20.1.3	Output: 15 V / 3 A	130
20.1.4	Output: 20 V / 2.25 A.....	132
20.2	Artificial Hand.....	134
20.2.1	Output: 5 V / 5 A	134
20.2.2	Output: 9 V / 3 A	136
20.2.3	Output: 15 V / 3 A	138
20.2.4	Output: 20 V / 2.25 A.....	140
20.3	Earth Ground.....	142
20.3.1	Output: 5 V / 5 A	142
20.3.2	Output: 9 V / 3 A	144
20.3.3	Output: 15 V / 3 A	146
20.3.4	Output: 20 V / 2.25 A.....	148
21	Line Surge	150
21.1	Differential Surge.....	150
21.2	Common Mode Surge.....	150
22	Electrostatic Discharge	151
22.1	Air Discharge: End of Cable	151
22.2	Air Discharge: On-board USB Receptacle.....	151
22.3	Contact Discharge: End of Cable.....	151
23	Revision History	152

Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This document is an engineering report describing a 45 W USB PD power supply with 5 V / 5 A, 9 V / 3 A, 15 V / 3 A, 20 V / 2.25 A or 3.3 V – 21 V Programmable Power Supply (PPS) output using InnoSwitch3-Pro INN3368-H301 IC and VIA Labs VP302 USB PD controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-Pro controller providing exceptional performance.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, transformer documentation, and performance data.

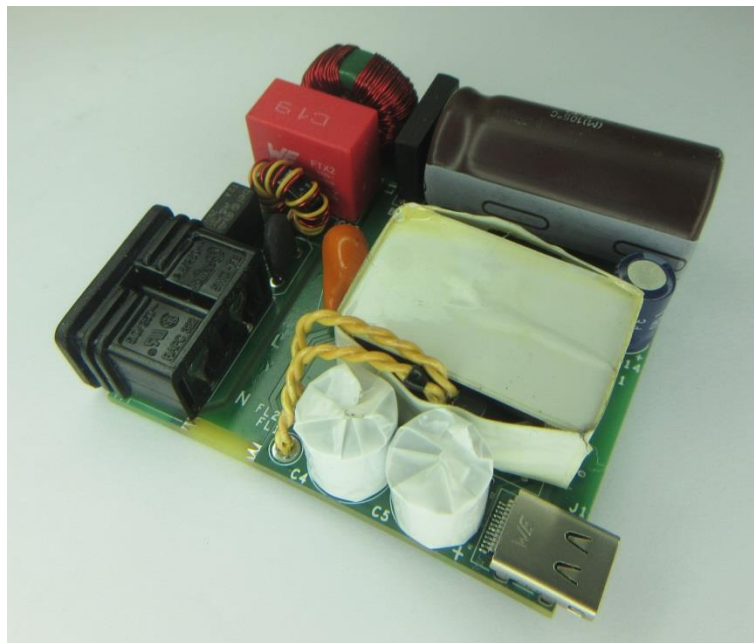


Figure 1 – Populated Circuit Board Photograph, Entire Assembly.

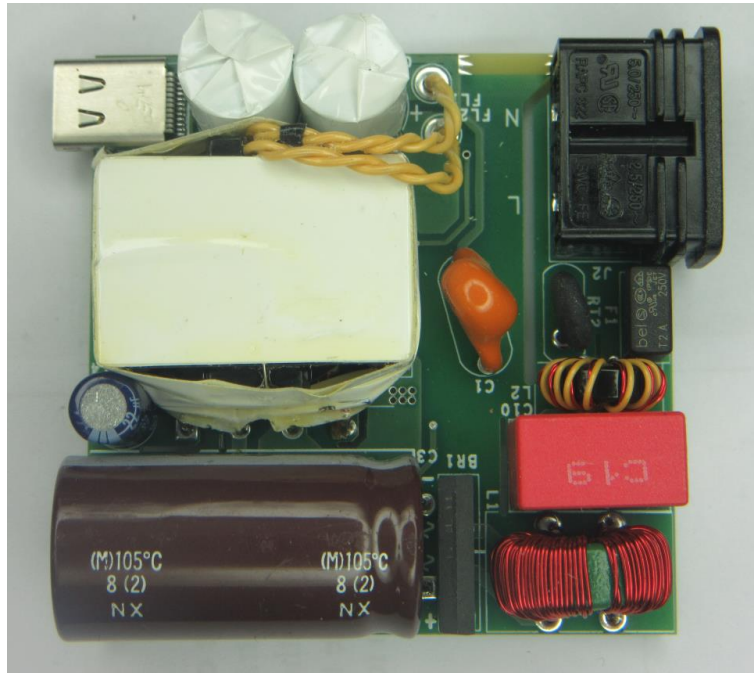


Figure 2 – Populated Circuit Board Photograph, Top.

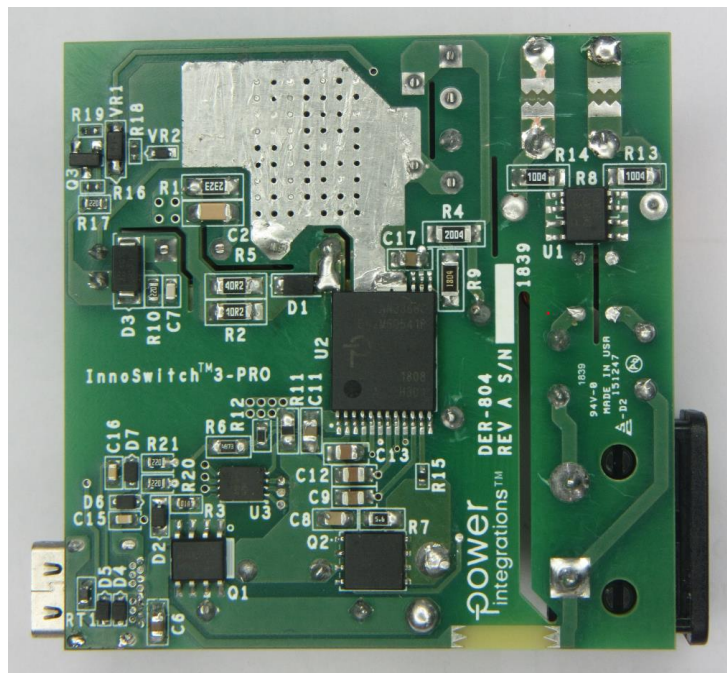


Figure 3 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance for the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power			36		mW	Measured at 265 VAC.
5 V Setting						
Output Voltage	$V_{OUT,5V}$		5.0		V	±5%
Output Voltage Ripple	$V_{RIPPLE,5V}$			150	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT,5V}$			5	A	±3%
Average Efficiency	η_{5V}		88.87		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT,5V}$			25	W	
9 V Setting						
Output Voltage	$V_{OUT,9V}$		9.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE,9V}$			150	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT,9V}$			3	A	±3%
Average Efficiency	η_{9V}		91.10		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT,9V}$			27	W	
15 V Setting						
Output Voltage	$V_{OUT,15V}$		15.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE,15V}$			150	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT,15V}$			3	A	±3%
Average Efficiency	η_{15V}		91.23		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT,15V}$			45	W	
20 V Setting						
Output Voltage	$V_{OUT,20V}$		20.0		V	±3%
Output Voltage Ripple	$V_{RIPPLE,20V}$			150	mV	Measured at End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT,20V}$			2.25	A	±3%
Average Efficiency	η_{20V}		91.03		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Continuous Output Power	$P_{OUT,20V}$			45	W	
3.3 V – 21 V PPS Setting						
Output Voltage	$V_{OUT,PPS}$	3.3		21	V	±3%
Output Voltage Ripple	$V_{RIPPLE,PPS}$			150	mV	Measured at the End of 100 mΩ Cable (20 MHz Bandwidth).
Output Current	$I_{OUT,PPS}$			3	A	±3%
PPS Voltage Step	$V_{STEP,PPS}$		20		mV	PPS Output Voltage Step Size.
PPS Current Step	$I_{STEP,PPS}$		50		mA	PPS Operating Current Step Size.
Average Efficiency (3.3 V)	$\eta_{3.3 V}$		86.34		%	Measured at 115 VAC from AC Receptacle to Type-C Receptacle on the Board.
Average Efficiency (21 V)	$\eta_{21 V}$		91.09		%	
Continuous Output Power	$P_{OUT,PPS}$			45	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.

Note: To use this design for a charger/adapter, the circuit board may need to be modified to match the shape and form factor of the housing. ESD and line surge performance would need to be evaluated and layout adjusted as appropriate for the revised design.



3 Schematic Diagram

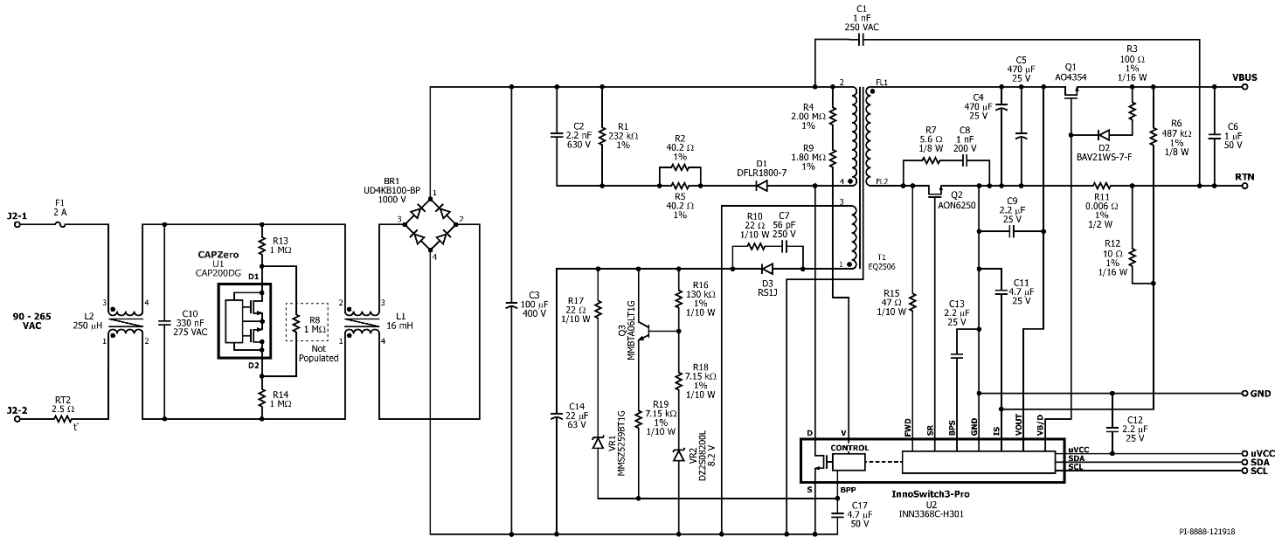


Figure 4 – Schematic Diagram 1.

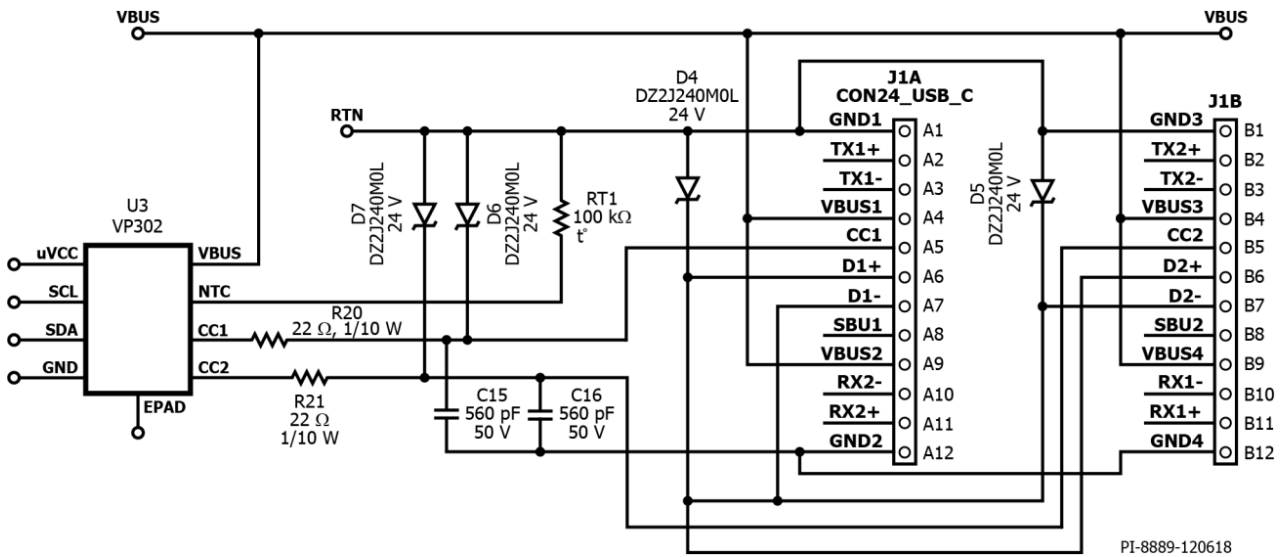


Figure 5 – Schematic Diagram 2.



4 Circuit Description

4.1 *Input Rectifier and EMI Filter*

Fuse F1 isolates the circuit and provides protection from component failure, and the common mode choke L2 with capacitor C1 and C10 provides attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across C3. Thermistor RT2 limits the inrush current when the power supply is connected to the input AC supply.

Resistors R13 and R14 along with CapZero-2 IC U1 discharges capacitor C1 when the power supply is disconnected from AC mains.

4.2 *InnoSwitch3-Pro IC Primary*

One end of the transformer primary is connected to the rectified DC bus and the other end is connected to the drain terminal of the MOSFET inside the InnoSwitch3-Pro IC U2. Resistors R4 and R9 provide input voltage sensing for protection in case of AC input undervoltage or overvoltage.

A low-cost RCD clamp formed by diode D1, resistors R1, R2, R5 and capacitor C2 limits the peak drain-source voltage of U2 at the instant the MOSFET inside U2 turns off. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor C17 when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. The output of the auxiliary (or bias) winding is rectified using diode D3 and filtered using capacitor C14. Resistor R19 limits the current being supplied to the BPP pin of the InnoSwitch3-Pro IC U2. A linear regulator comprising resistor R16, R18, BJT Q3 and Zener diode VR2 ensures sufficient current flows through R19 such that the internal current source of U2 is not required to charge C17 during normal operation. The RC network comprising of resistor R10 and capacitor C7 offers damping of the high frequency ringing in the voltage across diode D3 to reduce radiated EMI.

Zener diode VR1 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes excess current to flow into the BPP pin of InnoSwitch3-Pro IC U2. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-Pro controller will latch off and prevent any further increase in output voltage. Resistor R17 limits the current injected to BPP pin.



4.3 ***InnoSwitch3-Pro IC Secondary and USB Power Delivery Controller***

The secondary-side of the InnoSwitch3-Pro IC provides output voltage and current sensing and a gate drive to a MOSFET for synchronous rectification. The voltage across the transformer secondary winding is rectified by the secondary-side MOSFET (or SR FET) Q2 and filtered by capacitors C4 and C5. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RC snubber, R7 and C8.

The gate of Q2 is turned on by secondary-side controller inside IC U2, based on the secondary winding voltage sensed via resistor R15 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the SR FET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the SR FET is turned off when the magnitude of the voltage drop across the SR FET falls below a threshold of approximately $V_{SR(TH)}$. Secondary-side control of the primary-side power MOSFET avoids any possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectifier operation.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C13 connected to the BPS pin of InnoSwitch3-Pro IC U2 provides decoupling for the internal circuitry.

The output current is sensed by monitoring the voltage drop across resistor R11. Resistors R6 and R12 add an offset to the sensed output current to provide a positive slope to the CC characteristic. The resulting current measurement is filtered with decoupling capacitor C11 and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold which is configured via the I²C interface up to approximately 32 mV is used to reduce losses. Once the threshold is exceeded, the InnoSwitch3-Pro IC U2 regulates the number of switch pulses to maintain a fixed output current.

During constant current (CC) operation, when the output voltage falls, the secondary side controller inside InnoSwitch3-Pro IC U2 will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C13 via resistor R15 and an internal regulator. This allows output current regulation to be maintained down to the minimum UV threshold. Below this level the unit enters auto-restart until the output load is reduced.

When the output current is below the CC threshold, the converter operates in constant voltage mode. The output voltage is monitored by the VOUT pin of the InnoSwitch3-Pro IC. Similar with current regulation, the output voltage is also compared to an internal

voltage threshold that is set via the I²C interface and the controller inside IC U2 regulates the output voltage by controlling the number of switch pulses. Capacitor C9 is needed between the VOUT pin and the SECONDARY GROUND pin for ESD protection of the VOUT pin.

N-MOSFET Q1 functions as the bus switch which connects or disconnects the output of the flyback converter from the USB Type-C receptacle. Q1 is controlled by the VB/D pin on the InnoSwitch3-Pro IC. Resistor R3 and diode D2 are connected across the Source and Gate terminals of the Q1 to provide a discharge path for the bus voltage when the Q1 is turned off. Capacitor C6 is needed at the output for ESD protection.

4.4 ***USB Type-C and PD Interface***

In this design, VP302 (U3) is the USB Power Delivery (USB PD) controller. It is powered by the InnoSwitch3-Pro IC through the μ VCC pin. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

VP302 communicates with InnoSwitch3-Pro IC through the I²C interface using the SCL and SDA lines in which it sets the CV, CC, V_{kp} , OVA and UVA parameters. These parameters correspond to the output voltage, constant output current, constant output power voltage threshold, output overvoltage threshold, and output undervoltage threshold registers of the InnoSwitch3-Pro IC, respectively. The status of the InnoSwitch3-Pro IC is read by the VP302 IC from the telemetry registers also using the I²C interface.

Capacitor C12 provides decoupling to VCC of the VP302 IC. Capacitors C15 and C16; resistors R20, and R21; TVS D4, D5, D6, and D7 provide protection from ESD to pins CC1, CC2, D1 and D2.

Thermistor RT1 is connected to the NTC pin of the VP302 IC to provide temperature detection of the USB Type-C receptacle. The VBUS pin of the VP302 IC is used to sense the output voltage at the USB Type-C receptacle, which is the voltage after the bus switch Q1.



5 PCB Layout

PCB copper thickness is 2.0 oz.

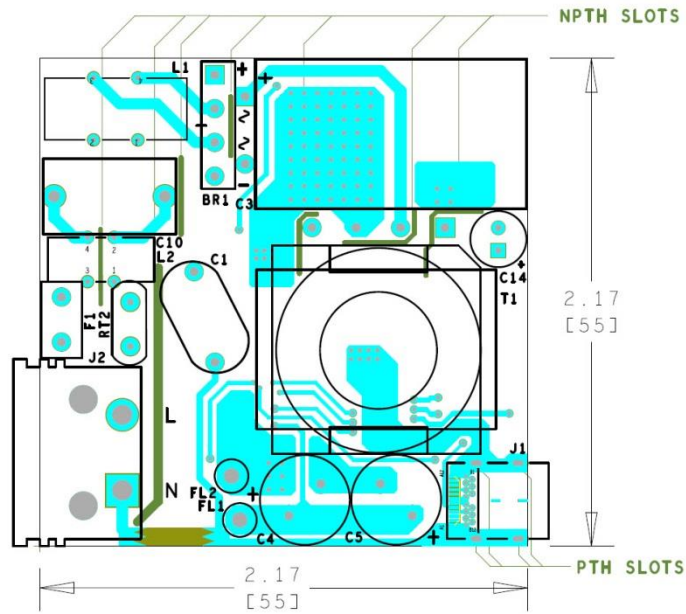


Figure 6 – Printed Circuit Layout, Top.

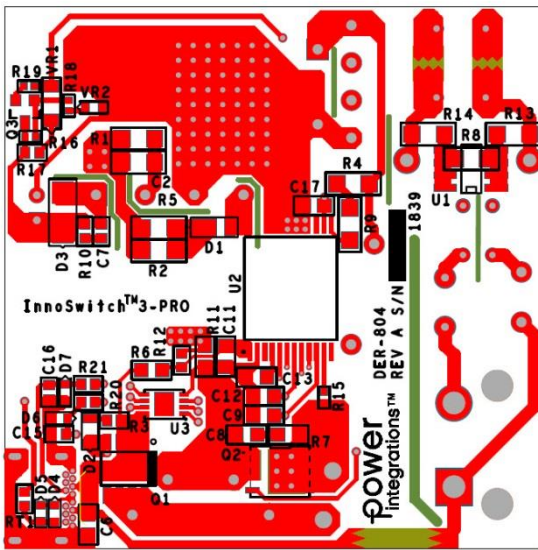


Figure 7 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	Bridge Rectifier, 1000 V, 4 A, 4-ESIP, D3K, -55°C ~ 150°C (TJ), Vf=1V @ 7.5A	UD4KB100-BP	Micro Commercial Co
2	1	C1	1 nF, Ceramic, Y1	440LD10-R	Vishay
3	1	C2	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
4	1	C3	100 µF, 400 V, Electrolytic, Low ESR, (16 x 30)	EPAG401ELL101ML30S	Nippon Chemi-Con
5	1	C4	470 µF, 25 V, ±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mΩ, 2000 Hrs @ 105°C	A750MS477M1EAAE015	KEMET
6	1	C5	470 µF, 25 V, ±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mΩ, 2000 Hrs @ 105°C	A750MS477M1EAAE015	KEMET
7	1	C6	1 µF, ±20%, 50 V, Ceramic, X7R, AEC-Q200, Automotive, Boardflex Sensitive, 0805	CGA4J3X7R1H105M125AE	TDK
8	1	C7	56 pF, 250 V, Ceramic, NPO, 0603	GQM1875C2E560JB12D	Murata
9	1	C8	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
10	1	C9	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
11	1	C10	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00mm x 8.50mm	890324024003CS	Würth
12	1	C11	4.7 µF ±10%, 25V, X7R, 0805, -55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
13	1	C12	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
14	1	C13	2.2 µF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
15	1	C14	22 µF, 63, Electrolytic, Low ESR, 1000 mΩ, (6.3 x 11.5)	ELXZ630ELL220MFB5D	Nippon Chemi-Con
16	1	C15	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60mm x 0.80mm)	CL10B561KB8NNNC	Samsung
17	1	C16	560 pF, 50 V, Ceramic, X7R, 0603, 0.063" L x 0.031" W (1.60mm x 0.80mm)	CL10B561KB8NNNC	Samsung
18	1	C17	4.7 µF, 50 V, Ceramic, X5R, 0805	CL21A475KBQNNNE	Samsung
19	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc.
20	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
21	1	D3	600 V, 1 A, Fast Recovery, 250 ns, SMA	RS1J-13-F	Diodes, Inc.
22	1	D4	DIODE, ZENER, 24 V, 200 MW, SMINI2	DZ2J240MOL	Panasonic
23	1	D5	DIODE, ZENER, 24 V, 200 MW, SMINI2	DZ2J240MOL	Panasonic
24	1	D6	DIODE, ZENER, 24 V, 200 MW, SMINI2	DZ2J240MOL	Panasonic
25	1	D7	DIODE, ZENER, 24 V, 200 MW, SMINI2	DZ2J240MOL	Panasonic
26	1	F1	2 A, 250 V, Slow, Long Time Lag, RST	RST 2	Belfuse
27	1	J1	Connector, "Certified", USB - C, USB 3.1, For 0.062" PCB Material!, Superspeed+, Receptacle Connector, 24 Position, Surface Mount, Right Angle, Through Hole	632723300011	Würth
28	1	J2	Power Entry Connector Receptacle, Male Pins, IEC 320-C8, Non-Polarized, Panel Mount, Snap-In; Through Hole, Right Angle	RAPC322X	Switchcraft
29	1	L1	CMC, 16 mH @ 100 kHz, ±25%, Toroidal, wound on 32-00286-00 toroidal core, with 75-00082-00 cable tie divider, using #28 AWG Heavy Nyleze wire	30-00463-00	Power Integrations
30	1	L2	250 µH, Toroidal Common Mode Choke, custom, wound on 32-00275-00 core.	32-00367-00	Power Integrations
31	1	Q1	MOSFET, N-CH, 30 V, 23 A (Ta), 3.1W (Ta), 3.7 mΩ (@ 20A, 10V), 8SOIC	AO4354	Alpha & Omega Semi
32	1	Q2	MOSFET, N-CH, 150V, 52A, 8DFN	AON6250	Alpha & Omega Semi
33	1	Q3	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
34	1	R1	RES, 232 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2323V	Panasonic
35	1	R2	RES, 40.2 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF40R2V	Panasonic
36	1	R3	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic

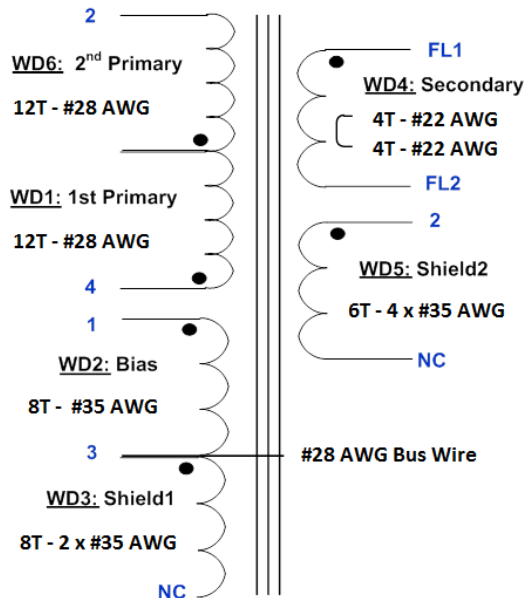


37	1	R4	RES, 2.00 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
38	1	R5	RES, 40.2 Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF40R2V	Panasonic
39	1	R6	RES, 487 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4873V	Panasonic
40	1	R7	RES, 5.6 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ5R6V	Panasonic
41	1	R8	RES, 1 M Ω , 5%, 1/4 W, Thick Film, 1206 (Not Populated)	ERJ-8GEYJ105V	Panasonic
42	1	R9	RES, 1.80 M Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
43	1	R10	RES, 22 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
44	1	R11	RES, 0.006 Ω , \pm 1%, 0.5W, 1/2W, 0805, Current Sense, Thick Film, \pm 300ppm/ $^{\circ}$ C, -55 $^{\circ}$ C ~ 155 $^{\circ}$ C	ERJ-6LWFR006V	Panasonic
45	1	R12	RES, 10 Ω , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
46	1	R13	RES, 1 M Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
47	1	R14	RES, 1 M Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
48	1	R15	RES, 47 Ω , 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ470X	Panasonic
49	1	R16	RES, 130.0 k Ω , 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1303X	Panasonic
50	1	R17	RES, 22 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
51	1	R18	RES, 7.15 k Ω , 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF7151X	Panasonic
52	1	R19	RES, 7.15 k Ω , 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF7151X	Panasonic
53	1	R20	RES, 22 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
54	1	R21	RES, 22 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
55	1	RT1	NTC Thermistor, 100 k, 3%, 0603	NCP18WF104E03RB	Murata
56	1	RT2	NTC Thermistor, 2.5 Ohms, 3 A	SL08 2R503	Ametherm
57	1	T1	Bobbin, EQ25, 4 pins, 4pri, 0sec	EQ-2506	Shen Zhen Xin Yu Jia
58	1	U1	CAPZero-2, SO-8C	CAP200DG	Power Integrations
59	1	U2	InnoSwitch3-Pro, InSOP24D	INN3368C-H301	Power Integrations
60	1	U3	IC, USB PD Type-C Controller for SMPS	VP302	VIA Labs
61	1	VR1	DIODE ZENER 39 V 500 MW SOD123	MMSZ5259BT1G	ON Semi
62	1	VR2	8.2 V, 5%, 150 mW, SSMINI-2	DZ2S08200L	Panasonic



7 Transformer (T1) Specification

7.1 Electrical Diagram



7.2 Electrical Specifications

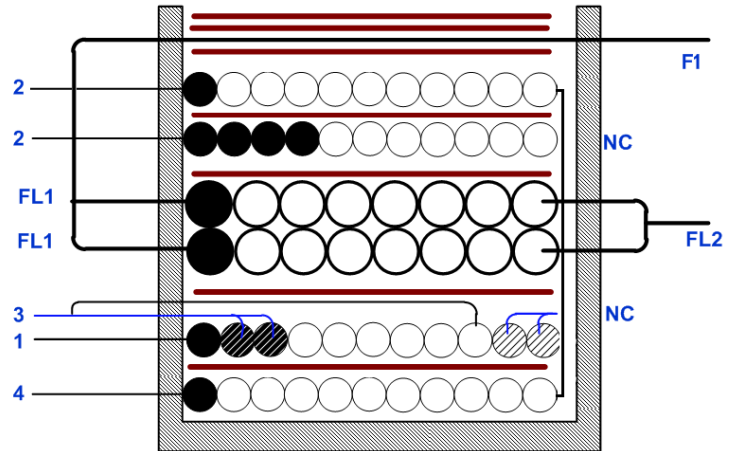
Electrical Strength	60 second, 60 Hz, from Pins 1, 2, 3, 4 to FL1-FL2.	3000 VAC
Nominal Primary Inductance	Measured at 1 V pk-pk, 100 kHz switching frequency, between pin 2 and 4, with all other windings open.	440 μ H \pm 5%
Resonant Frequency	Between pin 2 and 4, other windings open.	1200 kHz (min)
Primary Leakage Inductance	Between pin 2 and 4, with pins: FL1-FL2 shorted.	11.35 μ H

7.3 Materials

Item	Description
[1]	Core: EQ27
[2]	Bobbin: EQ2506-Vertical - 4pins (4/0), PI#: 25-01095-00.
[3]	Magnet wire: #28 AWG, double coated.
[4]	Magnet wire: #35 AWG, double coated.
[5]	Magnet wire: #22 AWG, Triple Insulated Wire.
[6]	Bus wire: #28AWG, Alpha wire, tinned copper, 40.0mm length.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 4.5 mm width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 18 mm width
[9]	Tape: 3M 13450-F, Polyester Film, 1 mil thickness, 12.4 mm width
[10]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

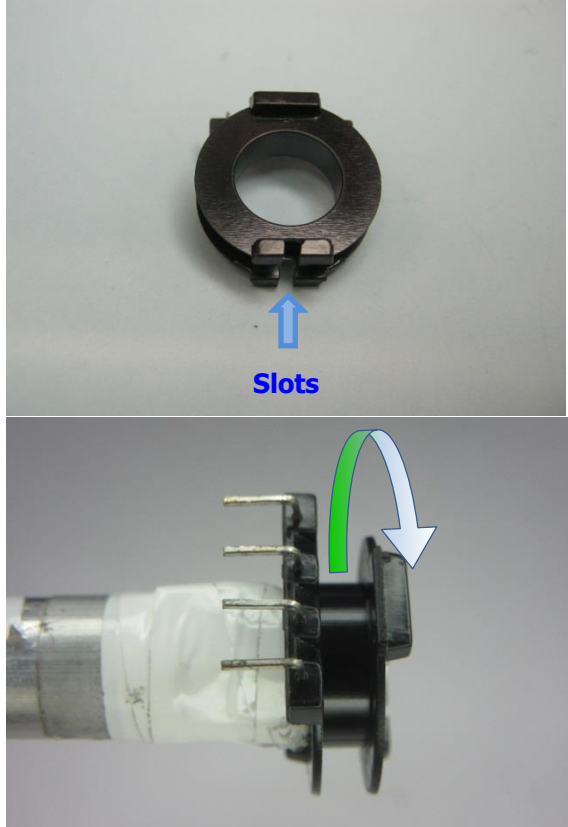
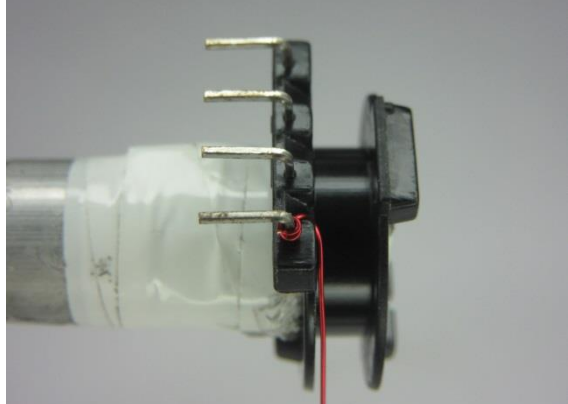
<u>WD6</u> : 2nd Primary	12T - #28 AWG
<u>WD5</u> : Shield 2	6T - 4 x #35 AWG
<u>WD4</u> : Secondary	4T - #22 AWG_TIW
<u>WD3</u> : Shield 1 (Wound Interleave with..)	8T - 2 x #35 AWG
<u>WD2</u> : Bias	8T - #35 AWG
<u>WD1</u> : 1st Primary	12T - #28 AWG


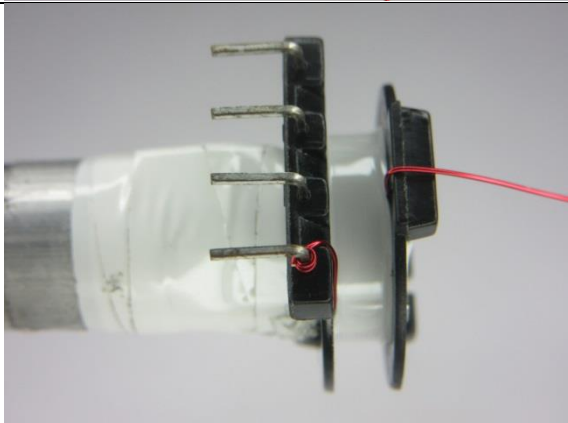
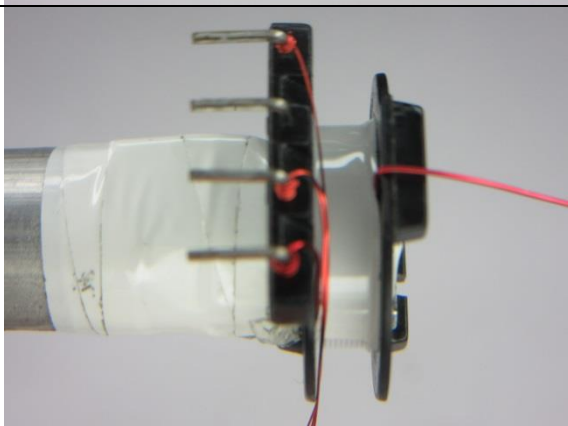


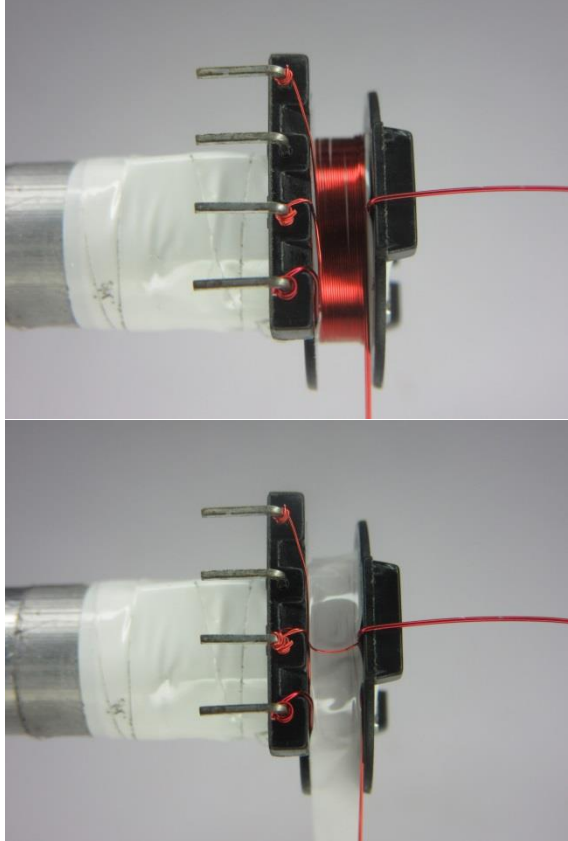
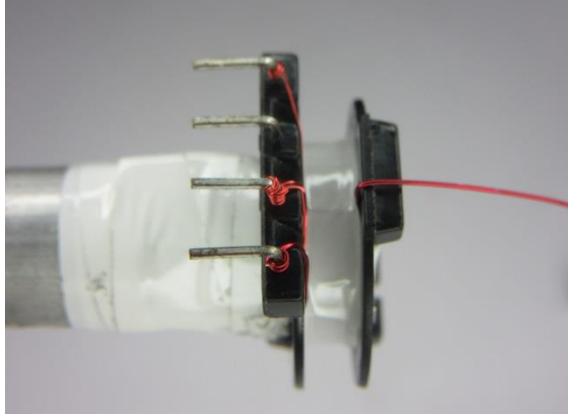
7.5 Winding Instructions

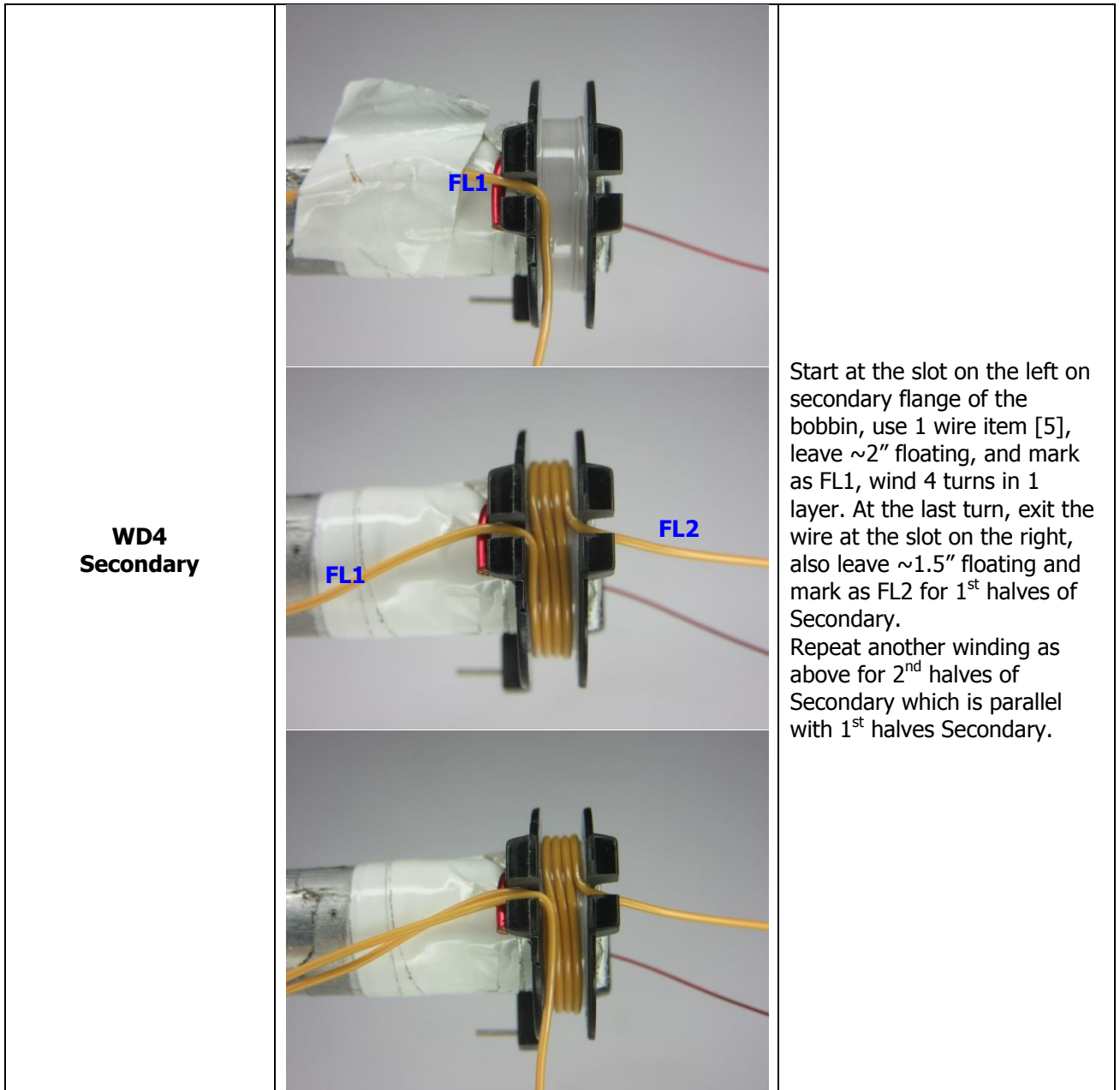
Winding Preparation	Use a "needle file" to grind and make the slots on both sides of secondary flange. A rotary tool (Dremel) with a grinding head T type can also be used to create the slots. Position the bobbin item [2] on the mandrel such that the pin side of the bobbin is on the left side. Winding direction is clock-wise direction.
WD1 1st Primary	Start at pin 4, wind 12 turns of wire item [3] in 1 layer, from left to right, and place 1 layer of tape item [7]. Leave ~3 ft. long for 2nd half primary winding
Insulation	1 layer of tape item [7].
WD2 & WD3 Bias & Shield 1	Start at pin 1, with 1 wire item [4] for WD2 and start pin 3 with 2 wires also item [4] for WD3. Wind all 3 wires 8 turns in parallel, at the last turn, finish 1 wire for WD2 at pin 3, cut short 2 wires for WD3 as No-Connect.
Insulation	1 layer of tape item [7].
WD4 Secondary	Start at the slot on the left on secondary flange of the bobbin, use 1 wire item [5], leave ~2" floating, and mark as FL1, wind 4 turns in 1 layer. At the last turn, exit the wire at the slot on the right, also leave ~1.5" floating and mark as FL2 for 1 st halves of Secondary. Repeat another winding as above for 2 nd halves of Secondary which is parallel with 1 st halves Secondary.
Insulation	1 layers of tape item [7].
WD5 Shield 2	Start at pin 2, wind 6 turns quad-filar turns of wire item [4]. At the last turn cut short the wires as No-Connect.
Insulation	1 layer of tape item [7].
WD6 2nd Primary	Use wire hanging from WD1 and Continue winding 12 turns from right to left. At the last turn, finish winding at pin2.
Insulation	1 layers of tape item [7] and bring the secondary wires FL1 to the right , then add another 2 layers of tape Item [7]. (total of 3 Layers)
Finish	Gap cores to get 440 uH, solder bus wire item [6] to pin 3 which leans along with core halves, and secure with tape. Wrap the body of transformer vertically with 3 layers of tape item [8], and also wrap the transformer horizontally with 3 layers of tape item [9] . Varnish using item [10].

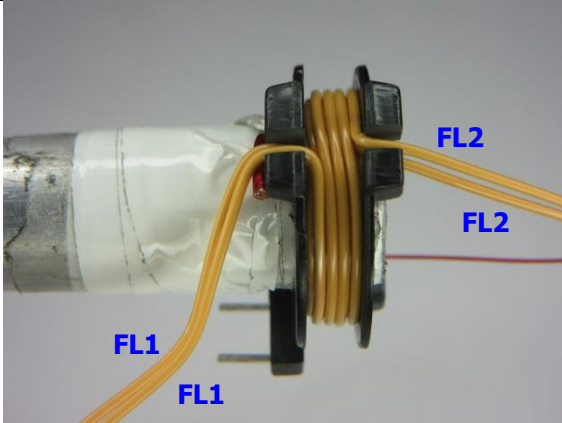
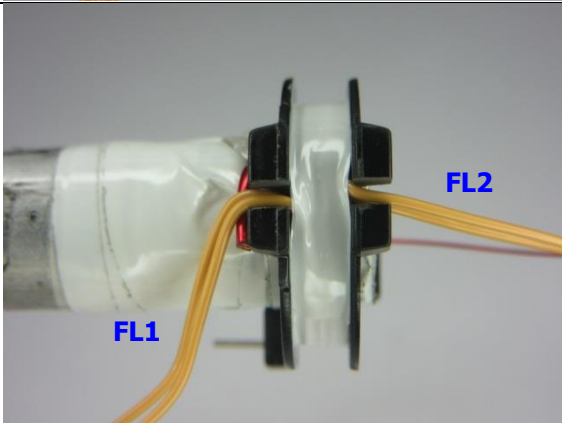
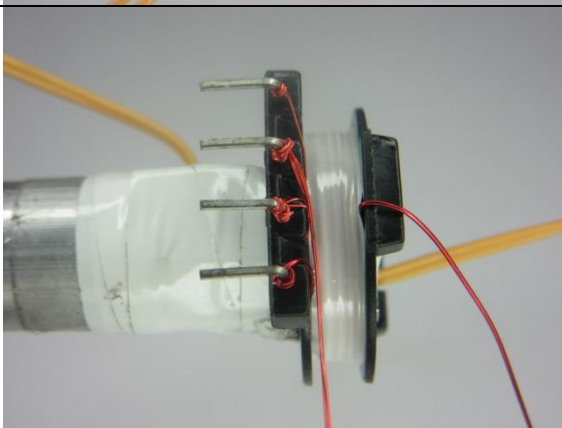
7.6 **Winding Illustrations**

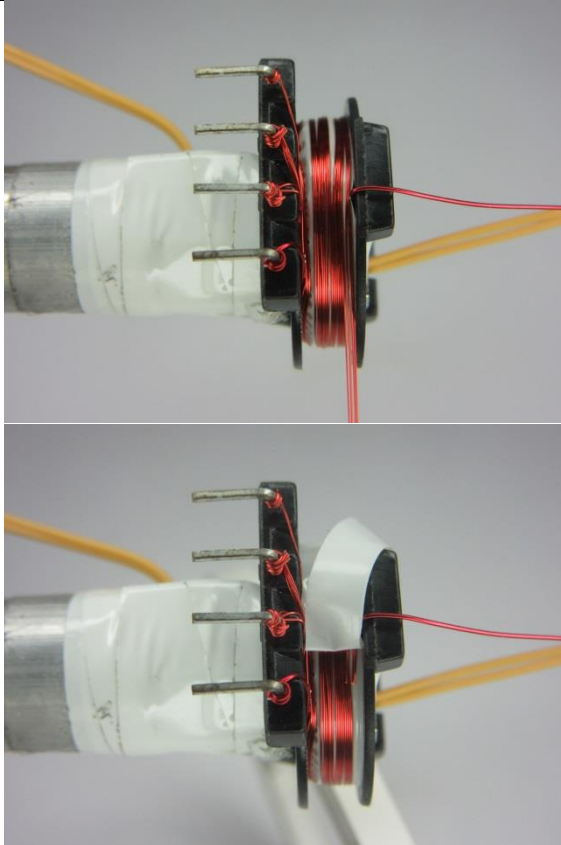
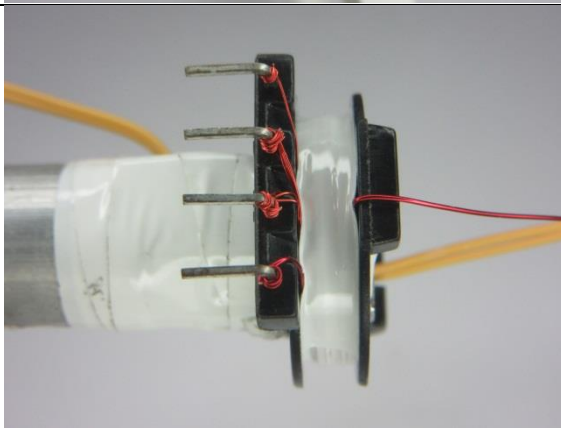
<p>Winding Preparation</p>		<p>Use a "needle file" to grind and make the slots on both sides of secondary flange.</p> <p>A rotary tool (Dremel) with a grinding head T type can also be used to create the slots.</p> <p>Position the bobbin item [2] on the mandrel such that the pin side of the bobbin is on the left side. Winding direction is clock-wise direction.</p>
<p>WD1 1st Primary</p>		<p>Start at pin 4, wind 12 turns of wire item [3] in 1 layer, from left to right, and place 1 layer of tape item [7]. Leave ~3 ft. long for 2nd half primary winding</p>

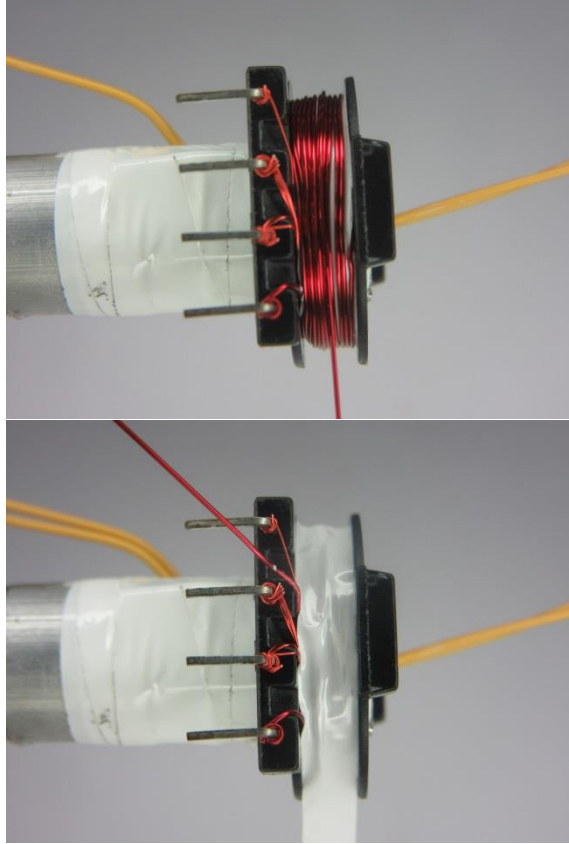
		
<p>Insulation</p>		<p>1 layer of tape item [7].</p>
<p>WD2 & WD3 Bias & Shield 1</p>		<p>Start at pin 1, with 1 wire item [4] for WD2 and start pin 3 with 2 wires also item [4] for WD3. Wind all 3 wires 8 turns in parallel, at the last turn, finish 1 wire for WD2 at pin 3, cut short 2 wires for WD3 as No-Connect.</p>

		
<p>Insulation</p>		<p>1 layer of tape item [7].</p>

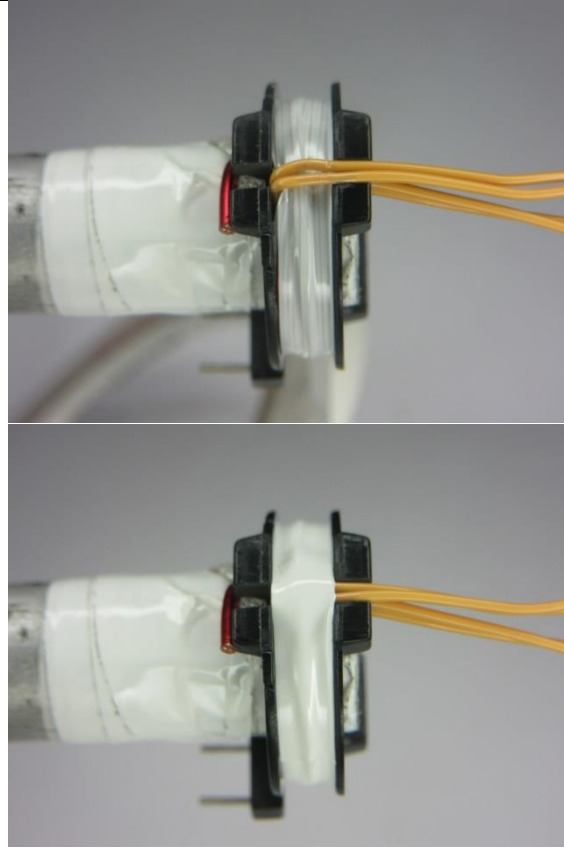


		
<p>Insulation</p>		<p>1 layers of tape item [7].</p>
<p>WD5 Shield 2</p>		<p>Start at pin 2, wind 6 turns quad-filar turns of wire item [4]. At the last turn cut short the wires as No-Connect.</p>

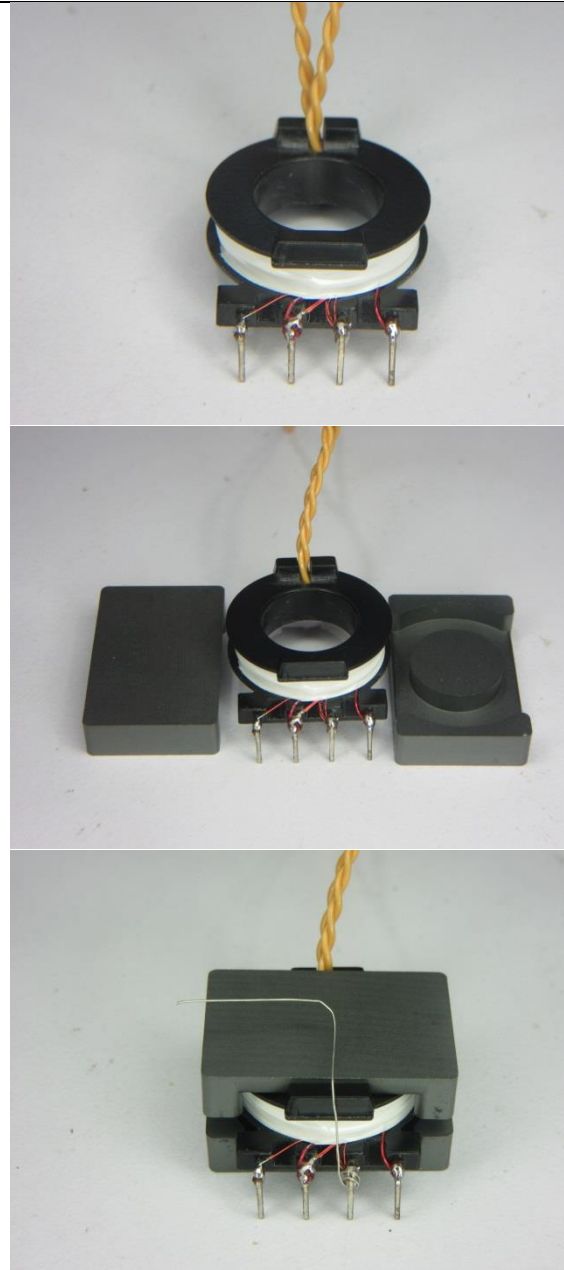
		
<p>Insulation</p>		<p>1 layer of tape item [7].</p>

<p>WD6 2nd Primary</p>		<p>Use wire hanging from WD1 and Continue winding 12 turns from right to left. At the last turn, finish winding at pin2.</p>
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Insulation



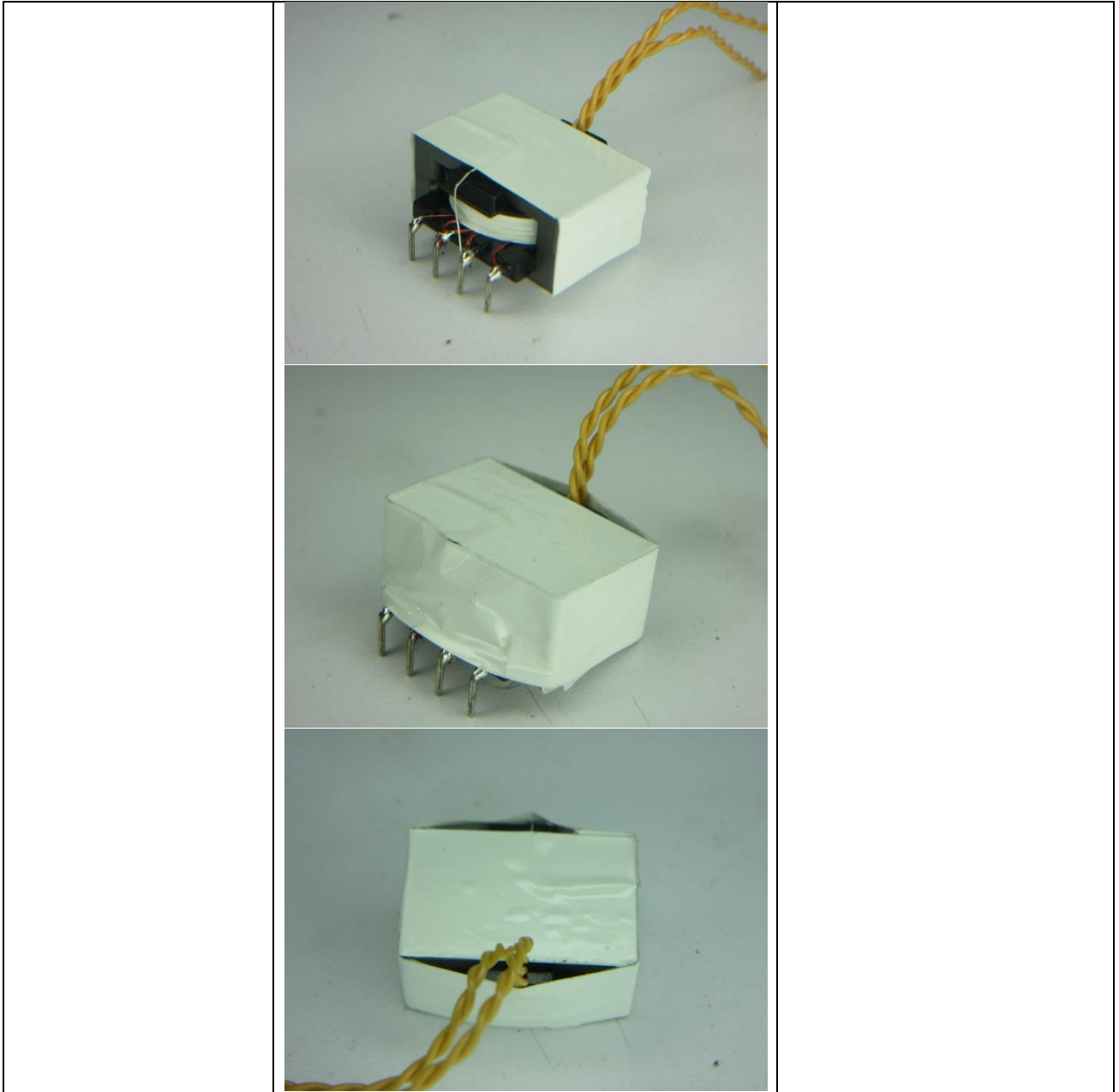
1 layers of tape item [7] and bring the secondary wires FL1 to the right, then add another 2 layers of tape Item [7]. (total of 3 Layers)

Finish

Gap cores to get 440 uH, solder bus wire item [6] to pin 3 which leans along with core halves, and secure with tape.

Wrap the body of transformer vertically with 3 layers of tape item [8], and also wrap the transformer horizontally with 3 layers of tape item [9].

Varnish using item [10].



8 Common Mode Choke Specifications

8.1 250 μH Common Mode Choke (L2)

8.1.1 Electrical Diagram

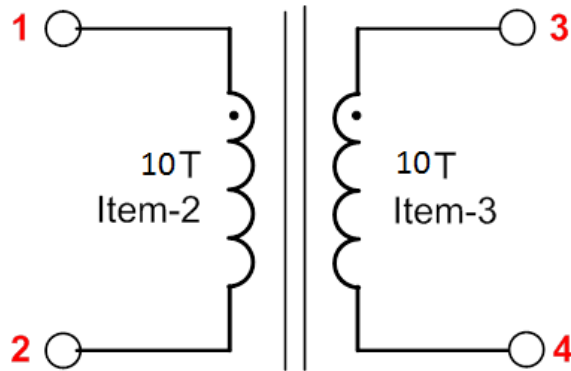


Figure 8 – Inductor Electrical Diagram.

8.1.2 Electrical Specifications

Inductance	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	250 μH ± 10%
Leakage Inductance	Pins 1-2, with 3-4 shorted.	0.5 μH ± 10%

8.1.3 Material List

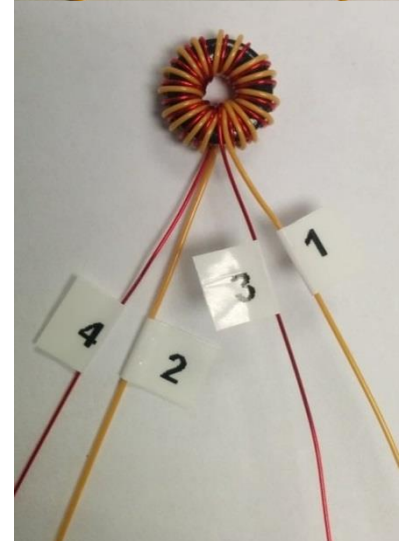
Item	Description
[1]	Toroid: Ferrite Inductor Toroid.415" OD; Mfg Part Number: 35T0375-10H. Dim: 9.53 mm, O.D. x 4.75 mm, I.D. x 3.18 mm L.
[2]	Magnet Wire: #27 AWG, Triple Insulated Wire.
[3]	Magnet Wire: #27 AWG, Double Coated.

8.1.4 Winding Construction

Mark the start of the winding as 1 and wind 10 turns of Item [2] on Item [1]. Mark the end of this winding as 2



Repeat the same procedure as above for the other winding using Item [3], making sure that the start/end and the direction of winding is the same as the first winding. Mark the start of this winding as 3 and the end as 4.



8.2 16 mH Common Mode Choke (L1)

8.2.1 Electrical Diagram

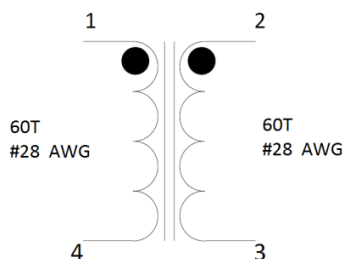


Figure 9 – Inductor Electrical Diagram.

8.2.2 Electrical Specifications

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS.	~16 mH ±25%
Core effective Inductance		5500 nH/N ²
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted.	~80 μH

8.2.3 Materials List

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID T14 x 8 x 5.5. PI Part number: #32-00286-00.
[2]	Divider: Cable-tie, Panduit, PLT.7M-M, 75-00082-00
[3]	Magnet Wire: #28 AWG Heavy Nyleze.
[4]	Epoxy: Devcon, 14270, 5 min Epoxy; or Equivalent.

8.2.4 Winding Instructions

- Place 2 pieces of cable tie item [2] onto toroid item [1] to divide 2 equal sections.
- Use 4 ft of wire item [3], start as pin 1 wind 60 turns in 2 layers in 1 section of toroid, and end at pin 4.
- Do the same for another section of toroid, start at pin 2 then end at pin 3 Symmetrically with last winding
- Apply Epoxy item [4] where leads floating. (see figure)

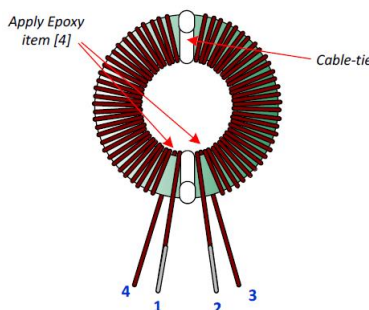


Figure 10 – Inductor Illustration.

9 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-Pro_Flyback_081518; Rev.1.1; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-Pro Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VAC_MIN			85	V	Minimum AC line voltage
4	VAC_MAX			265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	100.0		100.0	uF	Input capacitance
9	SETPOINT 1					
10	VOUT1	21.00		21.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	2.250		2.250	A	Output current 1
12	POUT1			47.25	W	Output power 1
13	EFFICIENCY1	0.89		0.89		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	SETPOINT 2					
17	VOUT2	20.00		20.00	V	Output voltage 2
18	IOUT2	2.250		2.250	A	Output current 2
19	POUT2			45.00	W	Output power 2
20	EFFICIENCY2	0.89		0.89		Converter efficiency for output 2
21	Z_FACTOR2	0.50		0.50		Z-factor for output 2
23	SETPOINT 3					
24	VOUT3	16.00		16.00	V	Output voltage 3
25	IOUT3	3.000		3.000	A	Output current 3
26	POUT3			48.00	W	Output power 3
27	EFFICIENCY3	0.91		0.91		Converter efficiency for output 3
28	Z_FACTOR3	0.50		0.50		Z-factor for output 3
29						
30	SETPOINT 4					
31	VOUT4	15.00		15.00	V	Output voltage 4
32	IOUT4	3.000		3.000	A	Output current 4
33	POUT4			45.00	W	Output power 4
34	EFFICIENCY4	0.91		0.91		Converter efficiency for output 4
35	Z_FACTOR4	0.50		0.50		Z-factor for output 4
36						
37	SETPOINT 5					
38	VOUT5	11.00		11.00	V	Output voltage 5
39	IOUT5	3.000		3.000	A	Output current 5
40	POUT5			33.00	W	Output power 5
41	EFFICIENCY5	0.90		0.90		Converter efficiency for output 5
42	Z_FACTOR5	0.50		0.50		Z-factor for output 5
43						
44	SETPOINT 6					
45	VOUT6	9.00		9.00	V	Output voltage 6
46	IOUT6	3.000		3.000	A	Output current 6
47	POUT6			27.00	W	Output power 6
48	EFFICIENCY6	0.89		0.89		Converter efficiency for output 6
49	Z_FACTOR6	0.50		0.50		Z-factor for output 6
50						
51	SETPOINT 7					
52	VOUT7	5.90		5.90	V	Output voltage 7
53	IOUT7	5.000		5.000	A	Output current 7
54	POUT7			29.50	W	Output power 7
55	EFFICIENCY7	0.88		0.88		Converter efficiency for output 7
56	Z_FACTOR7	0.50		0.50		Z-factor for output 7



57						
58	SETPOINT 8					
59	VOUT8	5.00		5.00	V	Output voltage 8
60	IOUT8	5.000		5.000	A	Output current 8
61	POUT8			25.00	W	Output power 8
62	EFFICIENCY8	0.88		0.88		Converter efficiency for output 8
63	Z_FACTOR8	0.50		0.50		Z-factor for output 8
64						
65	SETPOINT 9					
66	VOUT9	3.30		3.30	V	Output voltage 9
67	IOUT9	5.000		5.000	A	Output current 9
68	POUT9			16.50	W	Output power 9
69	EFFICIENCY9	0.86		0.86		Converter efficiency for output 9
70	Z_FACTOR9	0.50		0.50		Z-factor for output 9
72	VOLTAGE_CDC	0.000		0.000		Percentage (of output voltage) cable drop compensation desired at full load
76	PRIMARY CONTROLLER SELECTION					
77	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
78	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
79	VDRAIN_BREAKDOWN	650		650	V	Device breakdown voltage
80	DEVICE_GENERIC	AUTO		INN33X8		Device selection
81	DEVICE_CODE			INN3368C		Device code
82	PDEVICE_MAX			50	W	Device maximum power capability
83	RDSON_25DEG			0.99	Ω	Primary MOSFET on-time resistance at 25°C
84	RDSON_100DEG			1.54	Ω	Primary MOSFET on-time resistance at 100°C
85	ILIMIT_MIN			1.683	A	Primary MOSFET minimum current limit
86	ILIMIT_TYP			1.850	A	Primary MOSFET typical current limit
87	ILIMIT_MAX			2.017	A	Primary MOSFET maximum current limit
88	VDRAIN_ON_MOSFET			0.89	V	Primary MOSFET on-time voltage drop
89	VDRAIN_OFF_MOSFET			567.31	V	Peak drain voltage on the primary MOSFET during turn-off
93	WORST CASE ELECTRICAL PARAMETERS					
94	FSWITCHING_MAX	95722		95722	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
95	VOR	124.0		124.0	V	Voltage reflected to the primary winding (corresponding to setpoint 1) when the primary MOSFET turns off
96	VMIN			87.96	V	Valley of the rectified minimum input AC voltage at full load
97	KP			0.499		Measure of continuous/discontinuous mode of operation
98	MODE_OPERATION			CCM		Mode of operation
99	DUTYCYCLE			0.587		Primary MOSFET duty cycle
100	TIME_ON			9.84	us	Primary MOSFET on-time
101	TIME_OFF			4.61	us	Primary MOSFET off-time
102	LPRIMARY_MIN			418.4	uH	Minimum primary magnetizing inductance
103	LPRIMARY_TYP			440.4	uH	Typical primary magnetizing inductance
104	LPRIMARY_TOL	5.0		5.0	%	Primary magnetizing inductance tolerance
105	LPRIMARY_MAX			462.4	uH	Maximum primary magnetizing inductance
107	PRIMARY CURRENT					
108	I AVG_PRIMARY			0.577	A	Primary MOSFET average current
109	I PEAK_PRIMARY			1.922	A	Primary MOSFET peak current
110	I PEDESTAL_PRIMARY			0.809	A	Primary MOSFET current pedestal
111	I RIPPLE_PRIMARY			1.904	A	Primary MOSFET ripple current



112	IRMS_PRIMARY			0.869	A	Primary MOSFET RMS current
114	SECONDARY CURRENT					
115	IPEAK_SECONDARY			11.531	A	Secondary MOSFET peak current
116	IPEDESTAL_SECONDARY			4.855	A	Secondary MOSFET pedestal current
117	IRMS_SECONDARY			6.507	A	Secondary MOSFET RMS current
118	IRIPPLE_CAP_OUT			4.165	A	Output capacitor ripple current
122	TRANSFORMER CONSTRUCTION PARAMETERS					
123	CORE SELECTION					
124	CORE	CUSTOM	Info	CUSTOM		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
125	CORE NAME	EQ27		EQ27		Core code
126	AE	108.0		108.0	mm ²	Core cross sectional area
127	LE	36.3		36.3	mm	Core magnetic path length
128	AL	7700		7700	nH	Ungapped core effective inductance per turns squared
129	VE	3920		3920	mm ³	Core volume
130	BOBBIN NAME	EQ2506		EQ2506		Bobbin name
131	AW	10.0		10.0	mm ²	Bobbin window area
132	BW	4.25		4.25	mm	Bobbin width
133	MARGIN			0.0	mm	Bobbin safety margin
135	PRIMARY WINDING					
136	NPRIMARY			24		Primary winding number of turns
137	BPEAK			3683	Gauss	Peak flux density
138	BMAX			3390	Gauss	Maximum flux density
139	BAC			1672	Gauss	AC flux density (0.5 x Peak to Peak)
140	ALG			765	nH	Typical gapped core effective inductance per turns squared
141	LG			0.160	mm	Core gap length
142	LAYERS_PRIMARY	2		2		Primary winding number of layers
143	AWG_PRIMARY	28		28		Primary wire gauge
144	OD_PRIMARY_INSULATED			0.375	mm	Primary wire insulated outer diameter
145	OD_PRIMARY_BARE			0.321	mm	Primary wire bare outer diameter
146	CMA_PRIMARY		Warning	183.9	Cmils/A	The primary winding wire CMA is less than 200 mil ² /Amperes: Increase the primary layers or wire thickness
148	SECONDARY WINDING					
149	NSECONDARY	4		4		Secondary winding number of turns
150	AWG_SECONDARY	19		19		Secondary wire gauge
151	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
152	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
153	CMA_SECONDARY		Warning	198.0	Cmils/A	The secondary winding wire CMA is less than 200 mil ² /Amperes: Increase the wire thickness
155	BIAS WINDING					
156	NBIAS			8		Bias winding number of turns
160	PRIMARY COMPONENTS SELECTION					
161	LINE UNDERVOLTAGE					
162	BROWN-IN REQUIRED	76.00		76.00	V	Required line brown-in threshold
163	RLS			3.82	MΩ	Connect two 1.91 MOhm resistors to the V-pin for the required UV/OV threshold
164	BROWN-IN ACTUAL			76.58	V	Actual brown-in threshold using standard resistors
165	BROWN-OUT ACTUAL			69.26	V	Actual brown-out threshold using standard resistors
166						
167	LINE OVERVOLTAGE					
168	OVERVOLTAGE_LINE		Warning	319.20	V	The device voltage stress will be higher than 90% of the breakdown voltage

						when overvoltage is triggered
170	BIAS WINDING					
171	VBIAS	6.00	Info	6.00	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 9V
172	VF_BIAS			0.70	V	Bias winding diode forward drop
173	VREVERSE_BIASDIODE			130.44	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
174	CBIAS			22	uF	Bias winding rectification capacitor
175	CBPP			4.70	uF	BPP pin capacitor
179	SECONDARY COMPONENTS SELECTION					
180	RECTIFIER					
181	VDRAIN_OFF_SRFET			83.22	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
182	SRFET	AUTO		AON7254		Secondary rectifier (Logic MOSFET)
183	VBREAKDOWN_SRFET			150	V	Secondary rectifier breakdown voltage
184	RDSON_SRFET			66.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
188	SETPOINTS ANALYSIS					
189	TOLERANCE CORNER					
190	USER_VAC	85		85	V	Input AC RMS voltage corner to be evaluated
191	USER_ILIMIT	TYP		1.850	A	Current limit corner to be evaluated
192	USER_LPRIMARY	TYP		440.4	uH	Primary inductance corner to be evaluated
194	SETPOINT SELECTION					
195	SETPOINT	1		1		Select the setpoint which needs to be evaluated
196	FSWITCHING			72383.2	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
197	VOR			124.0	V	Voltage reflected to the primary winding when the primary MOSFET turns off
198	VMIN			87.96	V	Valley of the minimum input AC voltage
199	KP			0.900		Measure of continuous/discontinuous mode of operation
200	MODE_OPERATION			CCM		Mode of operation
201	DUTYCYCLE			0.587		Primary MOSFET duty cycle
202	TIME_ON			8.60	us	Primary MOSFET on-time
203	TIME_OFF			5.70	us	Primary MOSFET off-time
205	PRIMARY CURRENT					
206	I AVG_PRIMARY			0.576	A	Primary MOSFET average current
207	IPEAK_PRIMARY			1.783	A	Primary MOSFET peak current
208	IPEDESTAL_PRIMARY			0.179	A	Primary MOSFET current pedestal
209	IRIPPLE_PRIMARY			1.605	A	Primary MOSFET ripple current
210	IRMS_PRIMARY			0.831	A	Primary MOSFET RMS current
212	SECONDARY CURRENT					
213	IPEAK_SECONDARY			10.698	A	Secondary MOSFET peak current
214	IPEDESTAL_SECONDARY			1.071	A	Secondary MOSFET pedestal current
215	IRMS_SECONDARY			4.180	A	Secondary MOSFET RMS current
216	IRIPPLE_CAP_OUT			3.523	A	Output capacitor ripple current
218	MAGNETIC FLUX DENSITY					
219	BPEAK			3217	Gauss	Peak flux density
220	BMAX			3030	Gauss	Maximum flux density
221	BAC			1363	Gauss	AC flux density (0.5 x Peak to Peak)

Note: Although the spreadsheet shows a warning indicating that device voltage stress likely exceeding 90% of the device rating, this voltage will still be safely below the specified voltage breakdown rating of



the device and is acceptable since line OV is an abnormal operating condition and hence not expected to be a continuous operating condition.

The warnings on the primary and secondary winding wire CMA are also acceptable since both are relatively close to 200 mil²/Amperes. The thermal performance for all of the operating conditions is within acceptable limits.



10 Adapter Case Dimensions

10.1 Case Bottom Dimensions

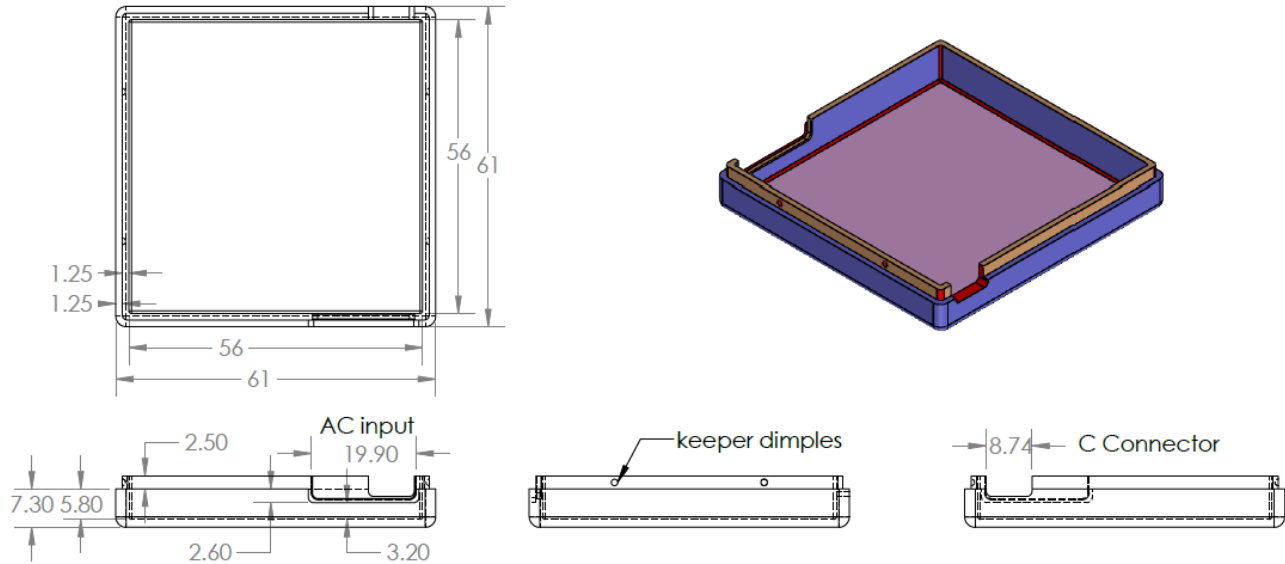


Figure 11 – DER 804 Adapter Case Bottom.

10.2 Case Top Dimensions

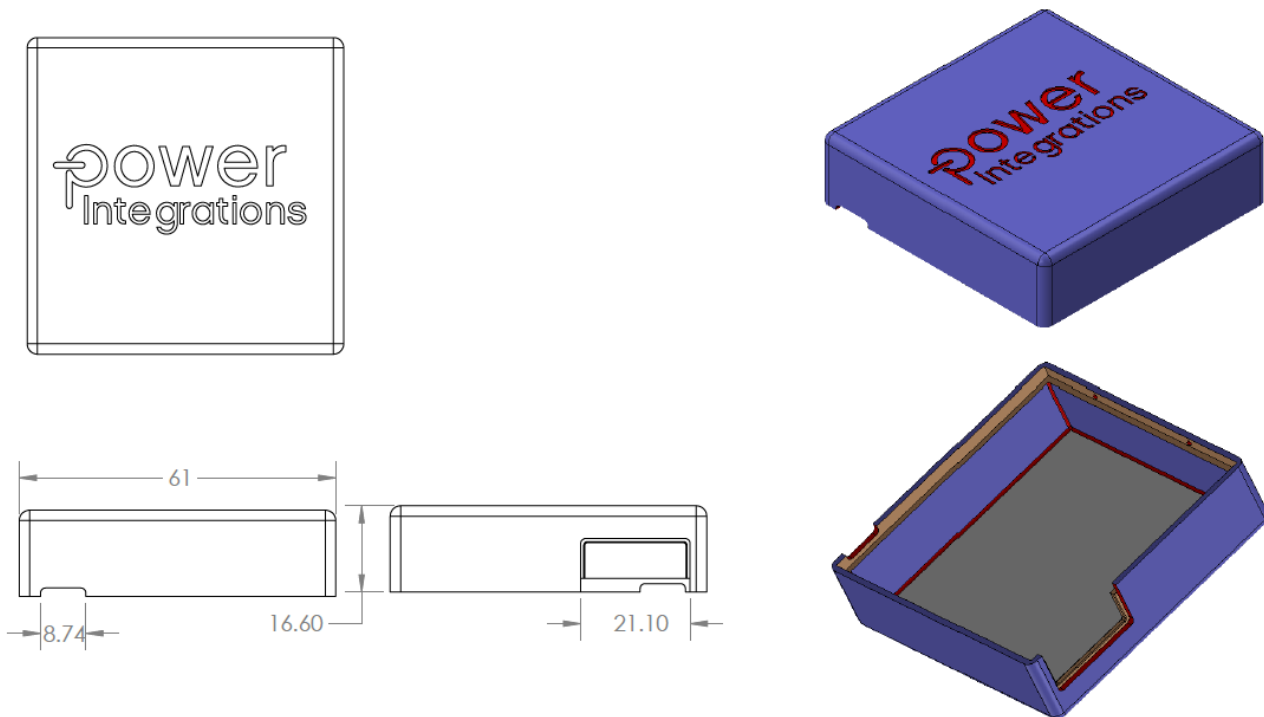


Figure 12 – DER-804 Adapter Case Top.

10.3 Adapter Assembly Drawing

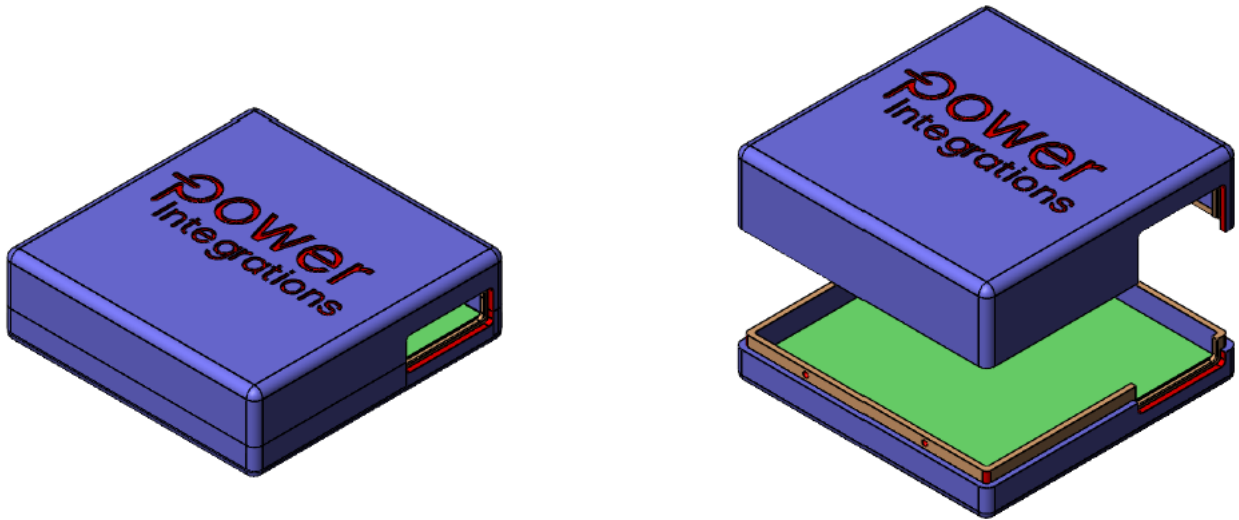
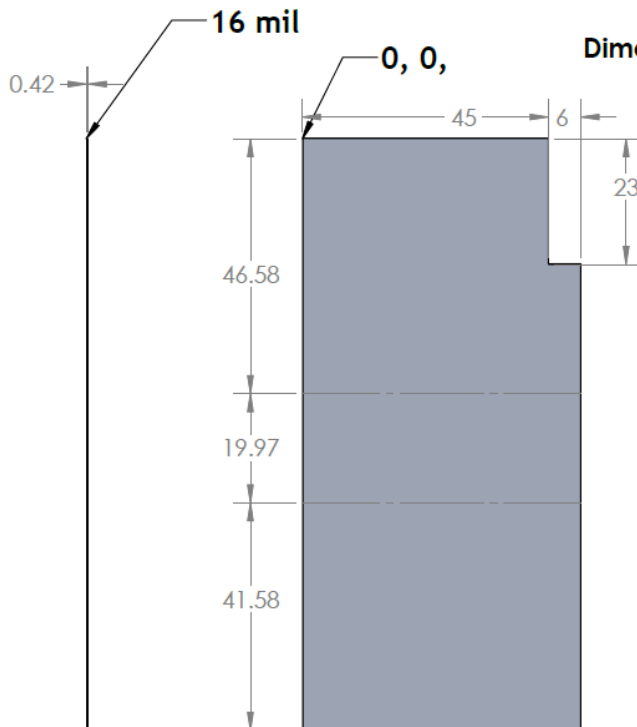


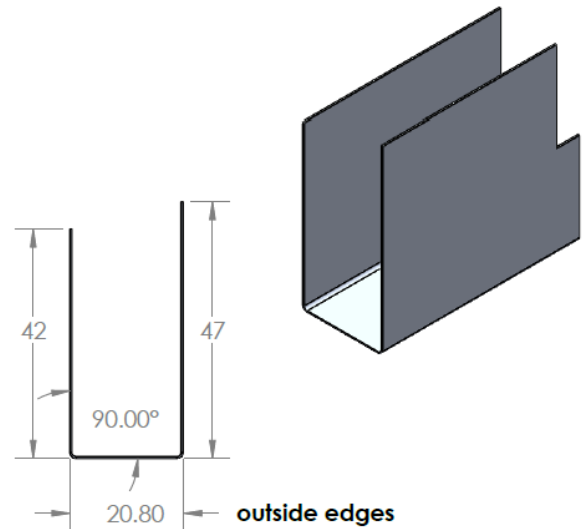
Figure 13 – DER-804 Adapter Assembly Drawing.

11 Heat Spreader Drawings

Notes:

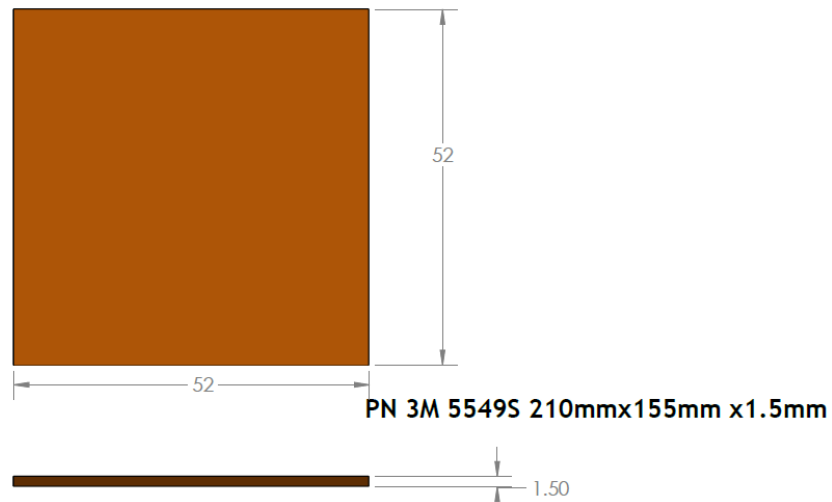


Heat Spreader
PN 61-00235-00
Dimensions: mm Scale: 1:1

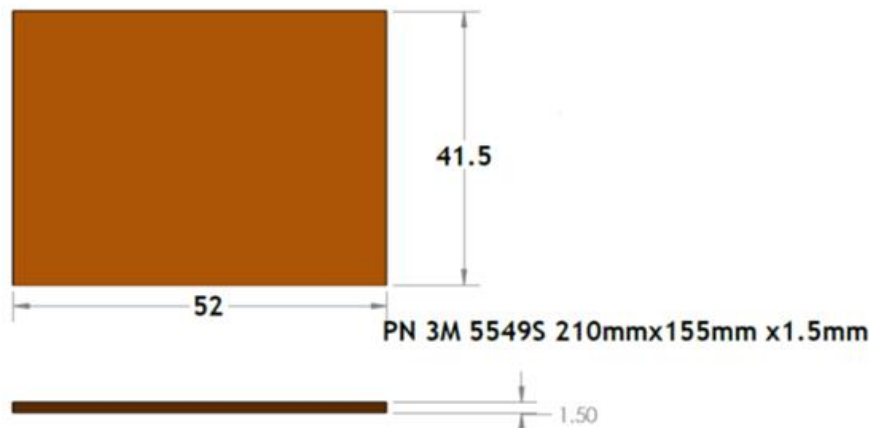


Notes:

PN 61-00236-01
Square Shape Thermal Pad
Dimensions: mm Scale: 3:2



Thermal Pad
Dimensions: mm Scale: 3:2



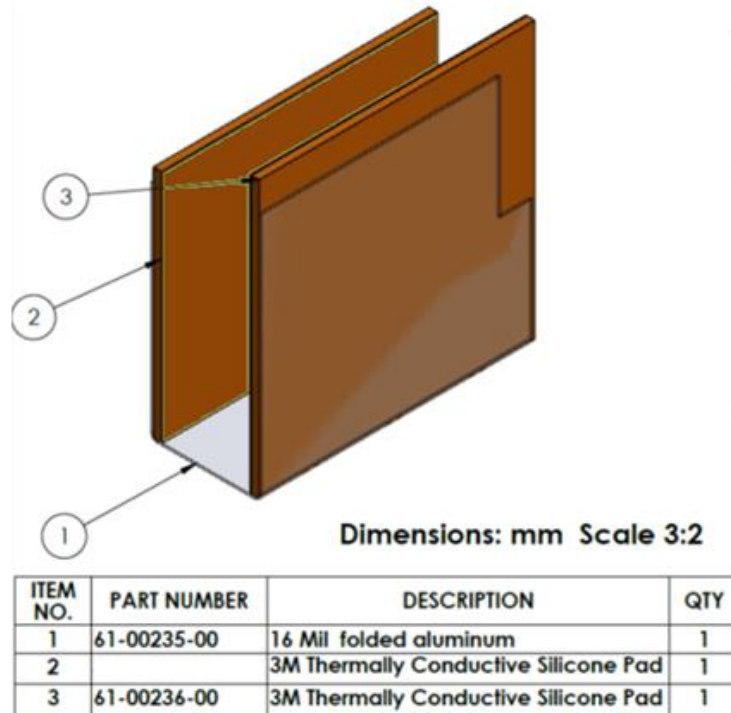


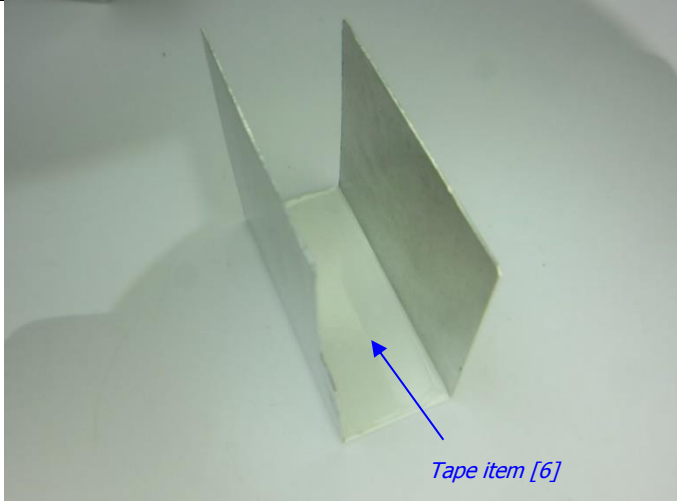
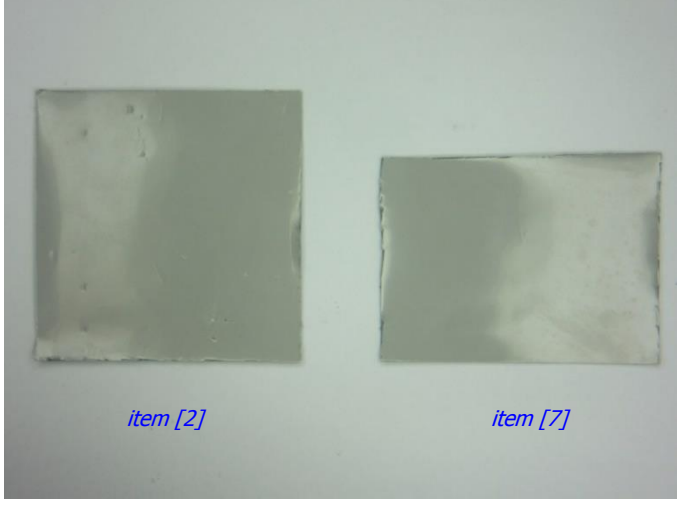
Figure 14 – Heat Spreader, Thermal Pad Drawings and Assembly.

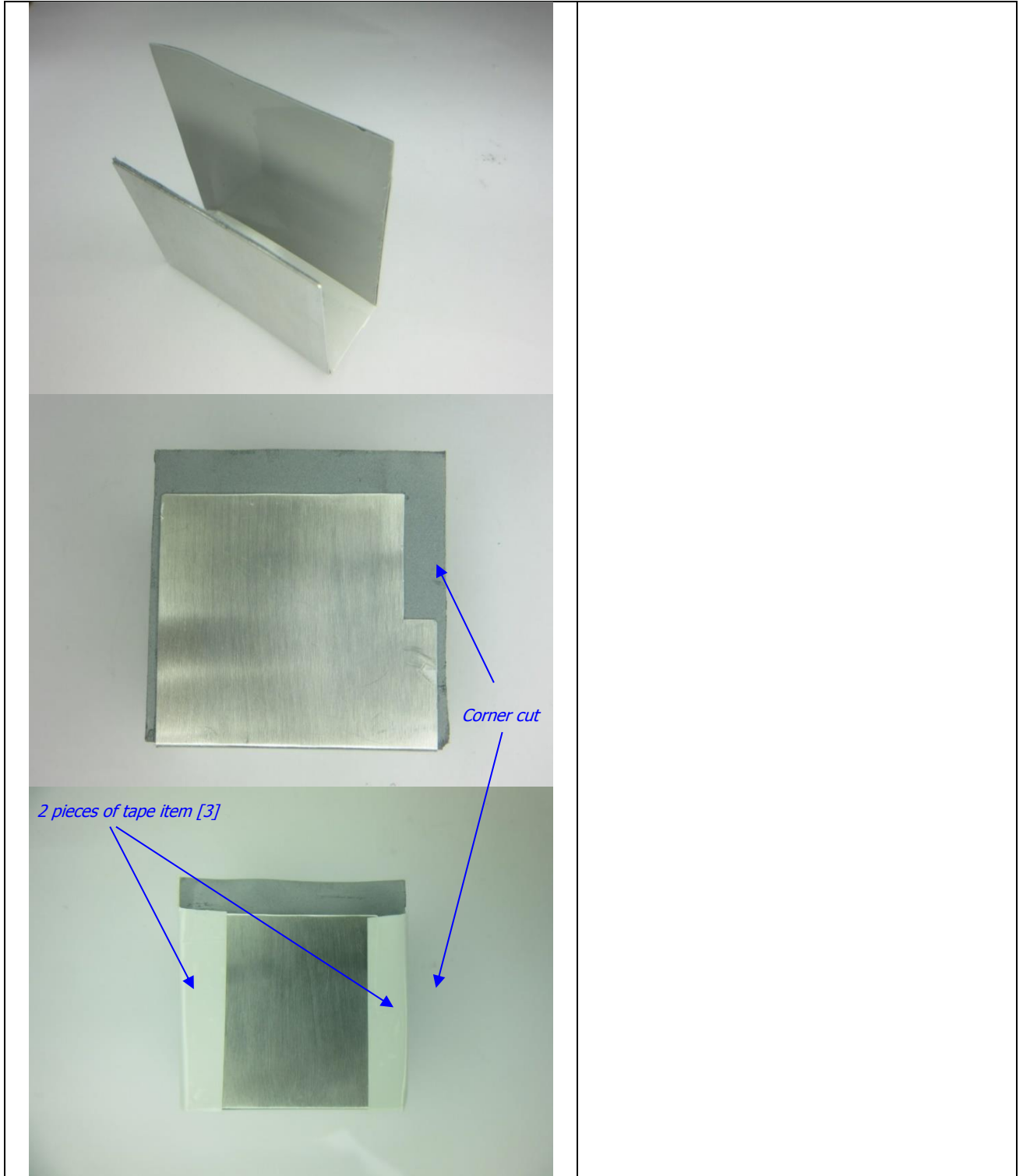
12 Heat Spreader Assembly Instructions

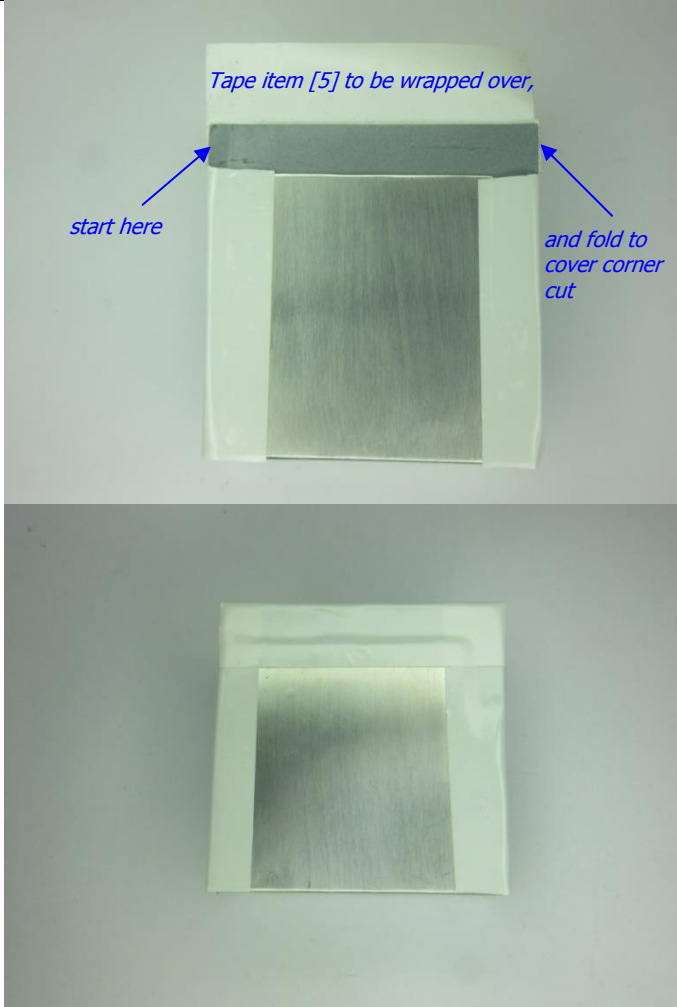
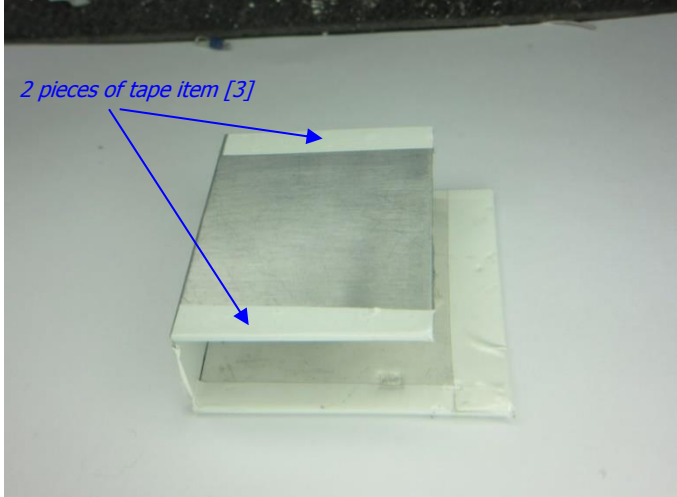
12.1 Materials

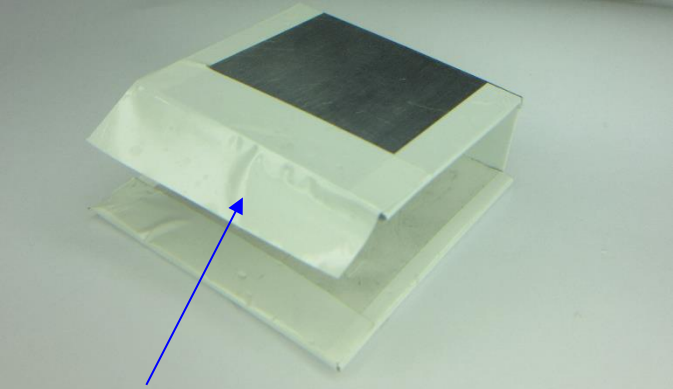
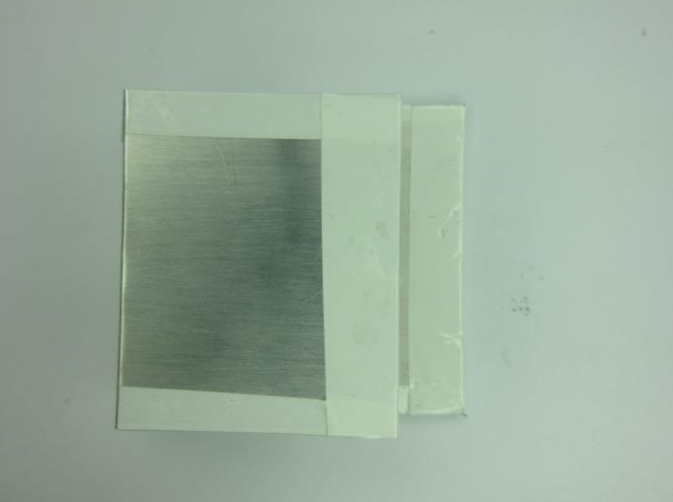
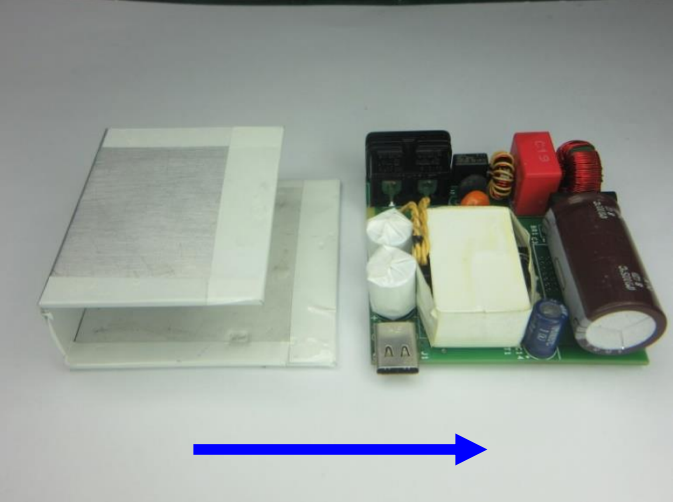
Item	Description
[1]	Heat Spreader; PI#: 61-00235-00.
[2]	Thermal Pad (thick, square); PI#: 61-00236-00.
[3]	Tape: 3M 1298 Polyester Film, 1 mil thick, 15.0mm wide, 51mm long.
[4]	Tape: 3M 1298 Polyester Film, 1 mil thick, 20.0mm wide, 51mm long.
[5]	Tape: 3M 1298 Polyester Film, 2 mil thick, 24.0mm wide, 60mm long.
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 24.0mm wide, 60mm long.
[7]	Thermal Pad (thick, rectangle).

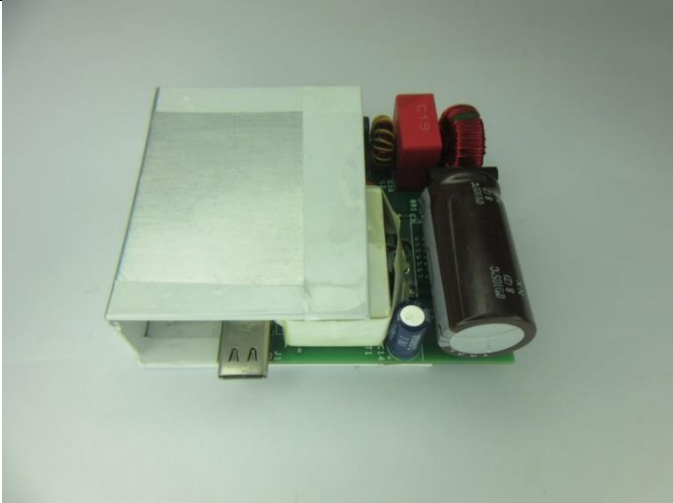
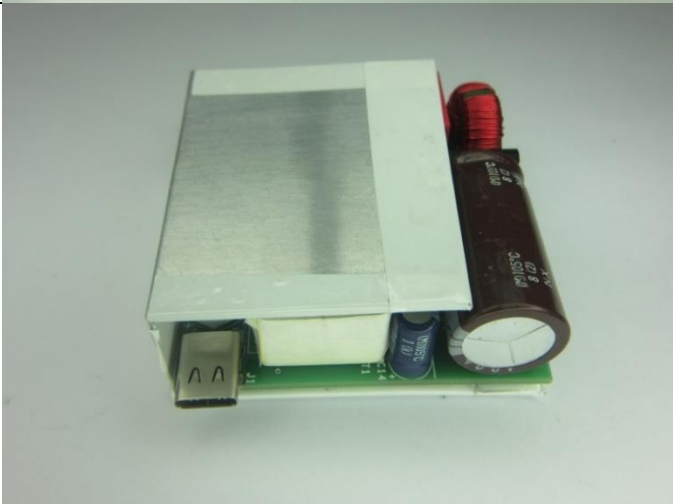
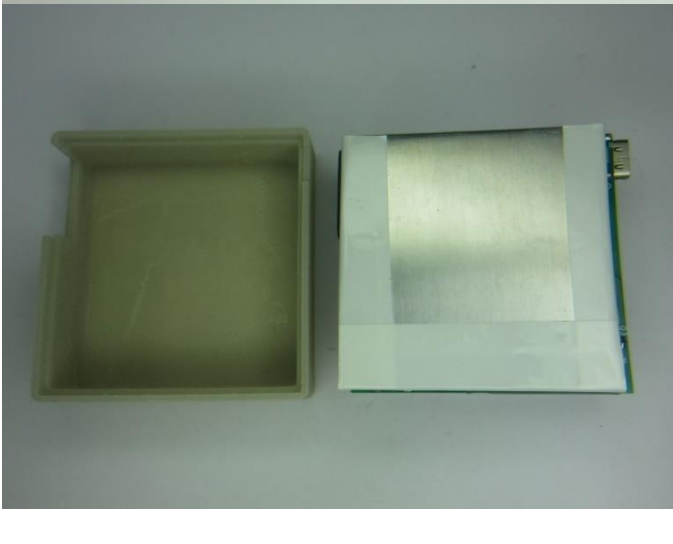
12.2 Assembly Instructions

	<p>Place 1 layer of tape item [4] at inner edge of heat spreader item [1].</p>
	<p>Prepare thermal pads item [2] (square) and item [7] (rectangle). Place the thermal pads inside the heat spreader item [1].</p> <p>Wrap 2 pieces of tape item [3] on side edges and 1 pieces of item [5] to front edge of bottom side of heat spreader which has corner cut.</p>



	
	<p>Wrap 2 pieces of tape item [3] on side edges of top side of heat spreader and 1 pieces of item [5] to front edge of top side of heat spreader</p>

 <p><i>Tape item [5] to be wrapped over</i></p>	
	<p>Complete assembly of heat spreader and thermal pads.</p>
	<p>Side by side picture showing how to insert board into heat spreader assembly</p>

	
	
	<p>Insert the board with heat spreader into the case and finish the assembly.</p>

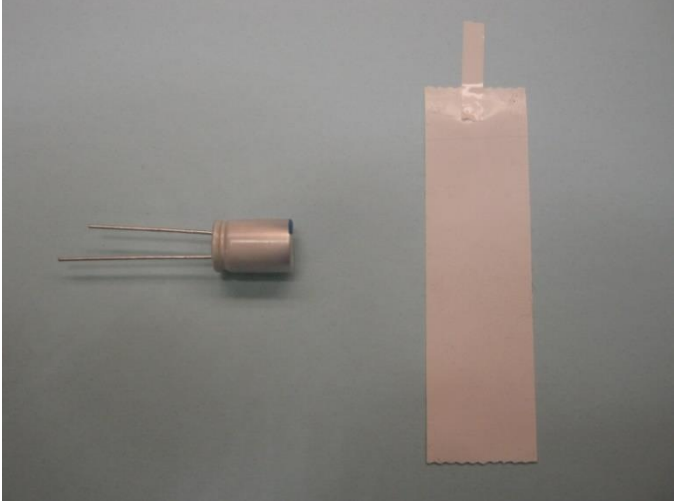
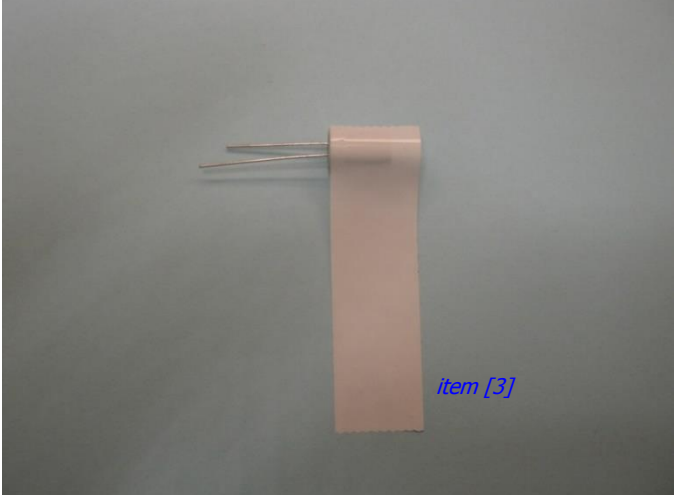


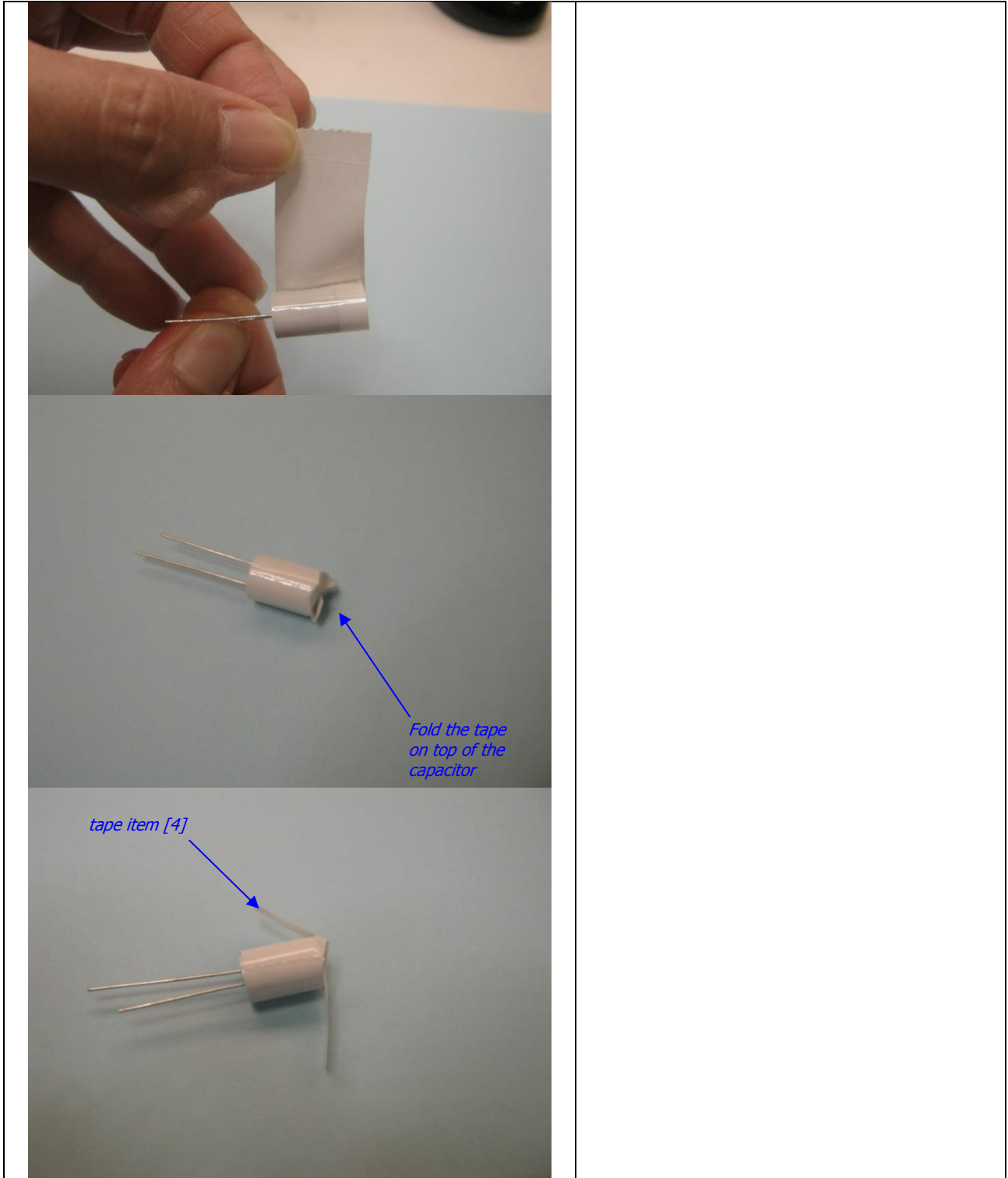
13 PCB Assembly Instructions

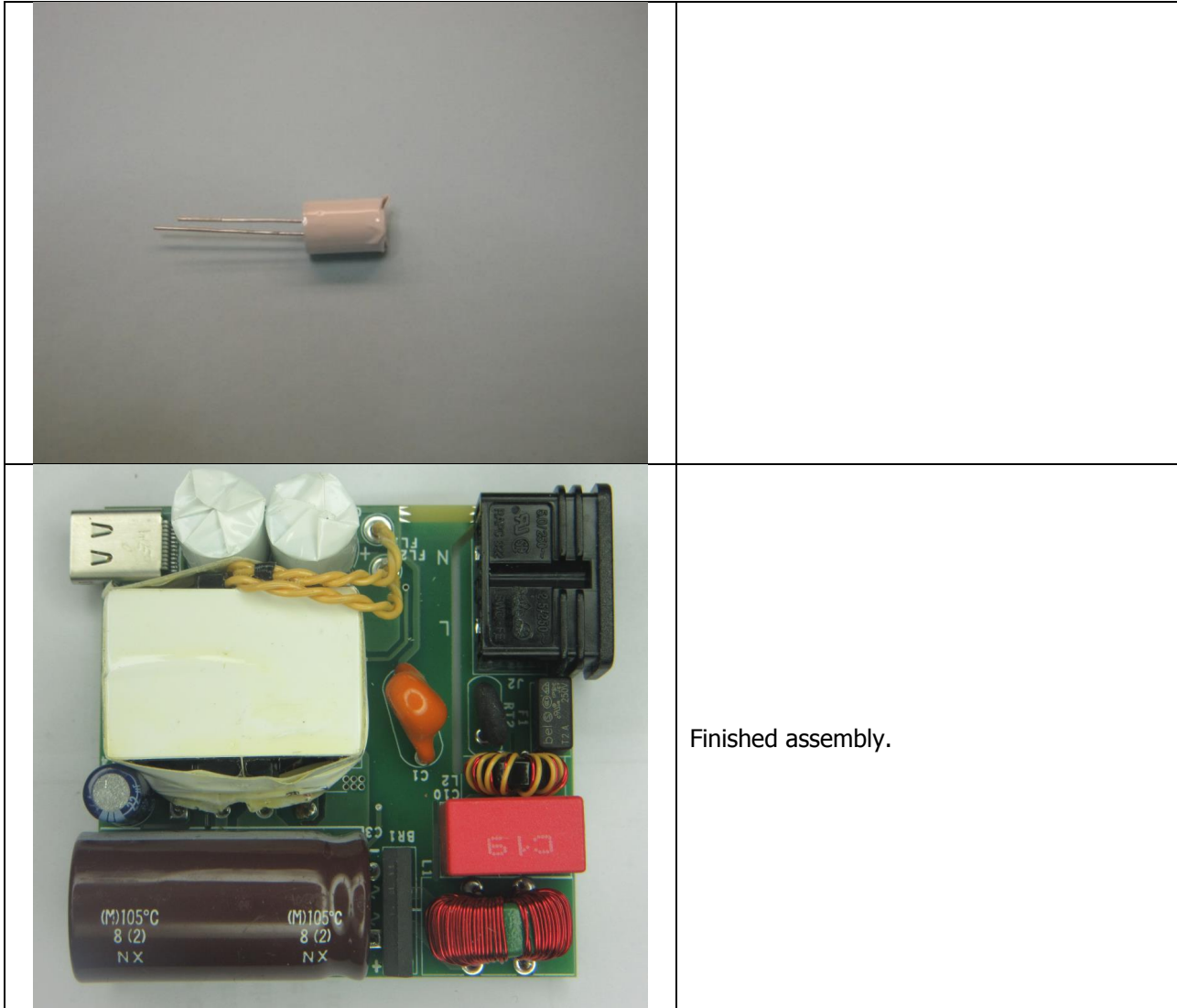
13.1 Materials

Item	Description
[1]	Capacitor C4 on DER-804 Schematic
[2]	Capacitor C5 on DER-804 Schematic
[3]	Tape: 3M 1298 Polyester Film, 1 mil thick, 16.4mm wide, 25mm long.
[4]	Tape: 3M 1298 Polyester Film, 1 mil thick, 5.0mm wide, 15mm long.

13.2 Output capacitor and transformer assembly instructions

	<p>Prepare ~2 Inches tape item [3].</p>
	<p>Wrap C4 and C5 with tape item [3] to insulate the capacitor from transformer core.</p> <p>Fold the tape on top to fully cover the capacitor.</p> <p>Use the tape item [4] to secure the cover.</p>





Finished assembly.

Note: cut all the TH (PTH and NPTH) pins to <math><0.5\text{ mm}</math> on the bottom side of the board after completing the assembly.

14 Performance Data

Note 1: Output voltages measured at PCB end
2: Measurements taken at room temperature

14.1 Efficiency vs. Load

14.1.1 Output: 3.3 V / 5 A

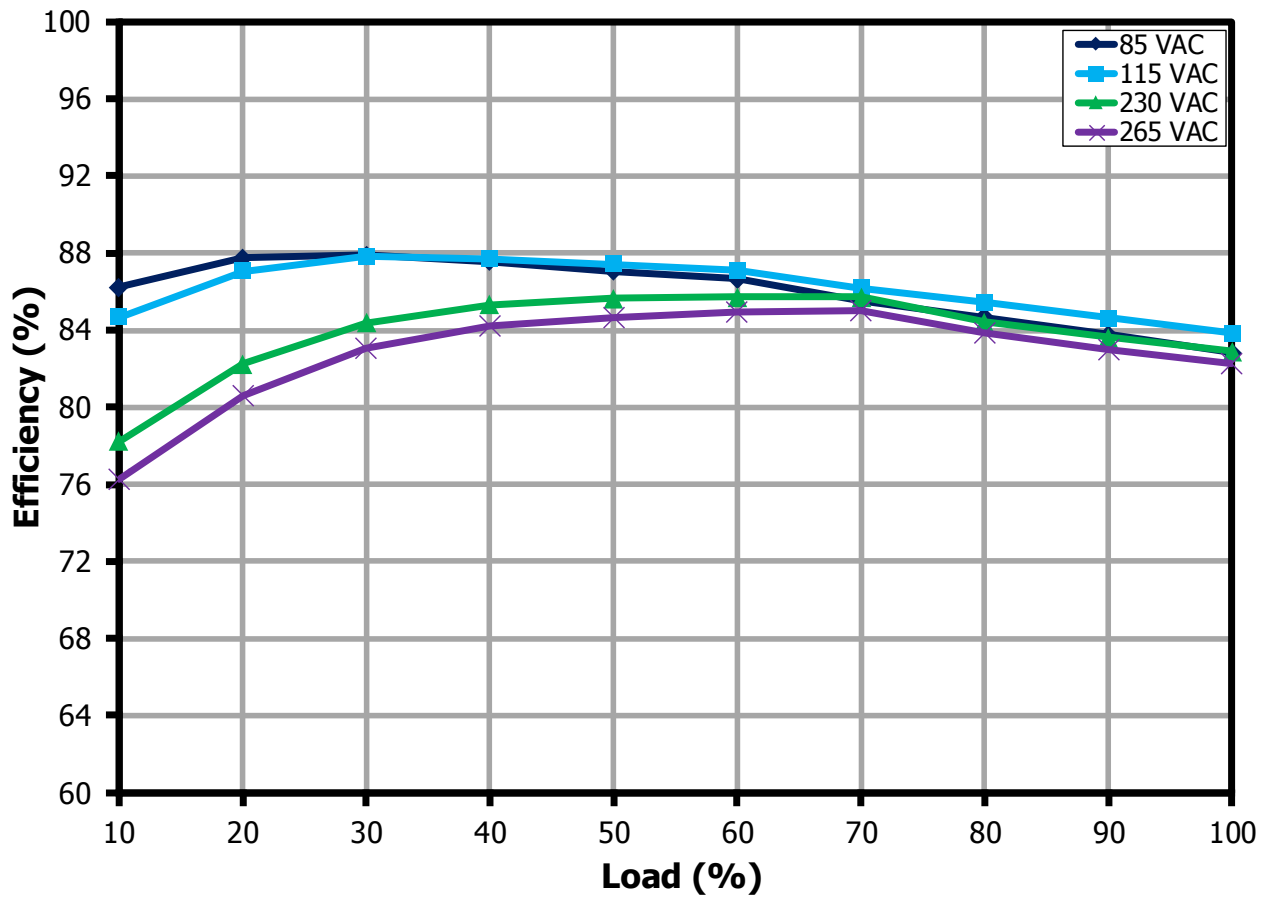


Figure 15 – 3.3 V Output Efficiency vs. Load.



14.1.2 Output: 5 V / 5 A

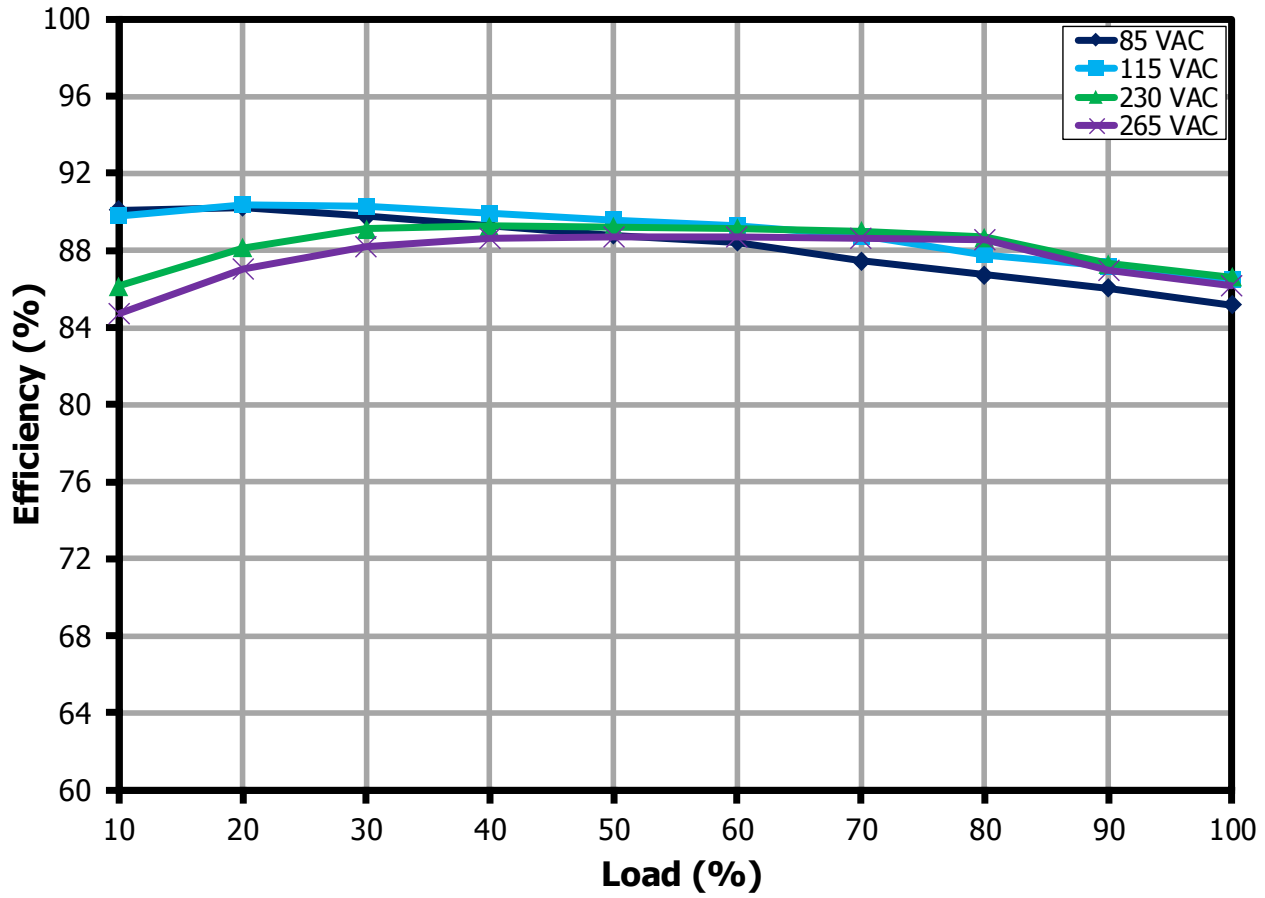


Figure 16 – 5 V Output Efficiency vs. Load.



14.1.3 Output: 9 V / 3 A

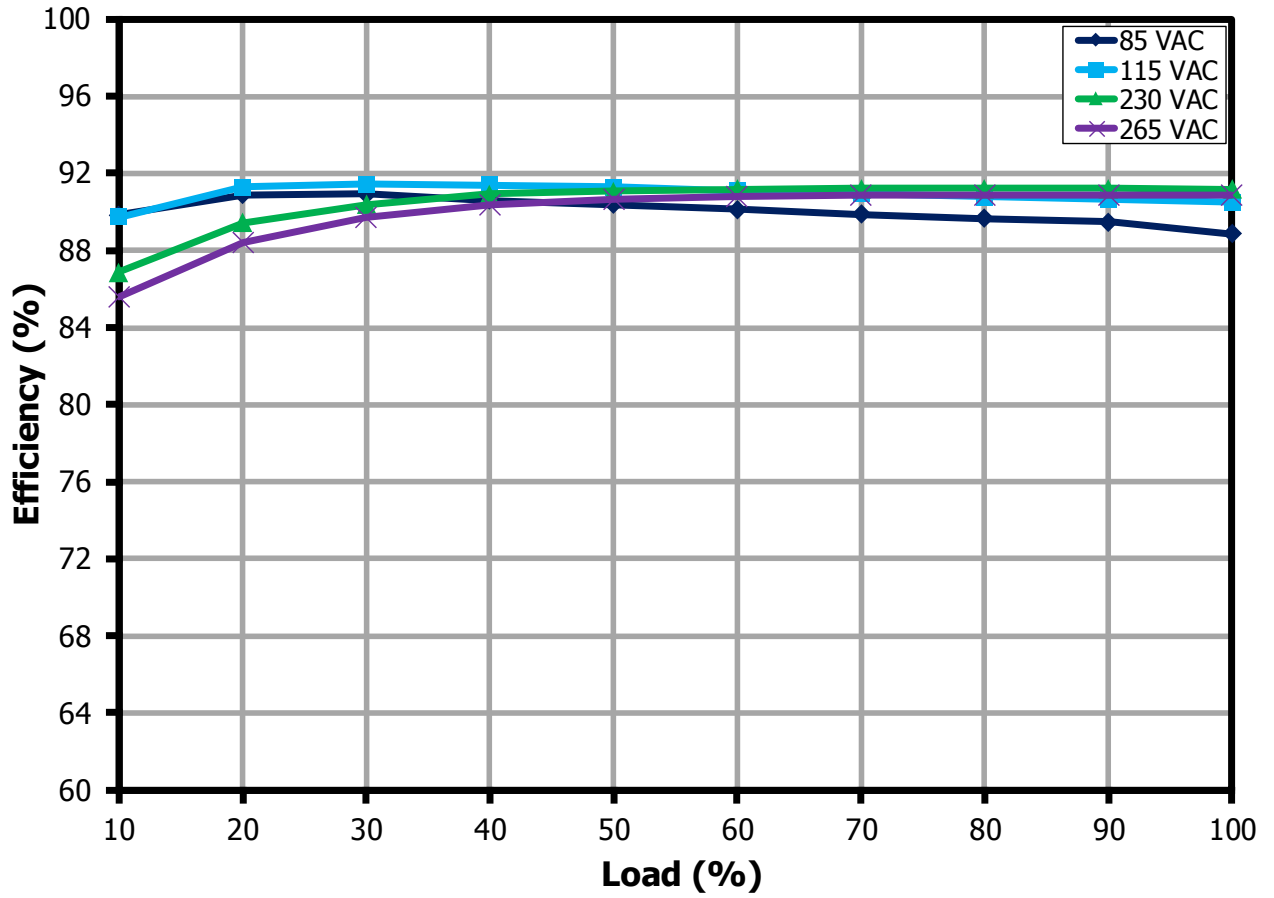


Figure 17 – 9 V Output Efficiency vs. Load.



14.1.4 Output: 15 V / 3 A

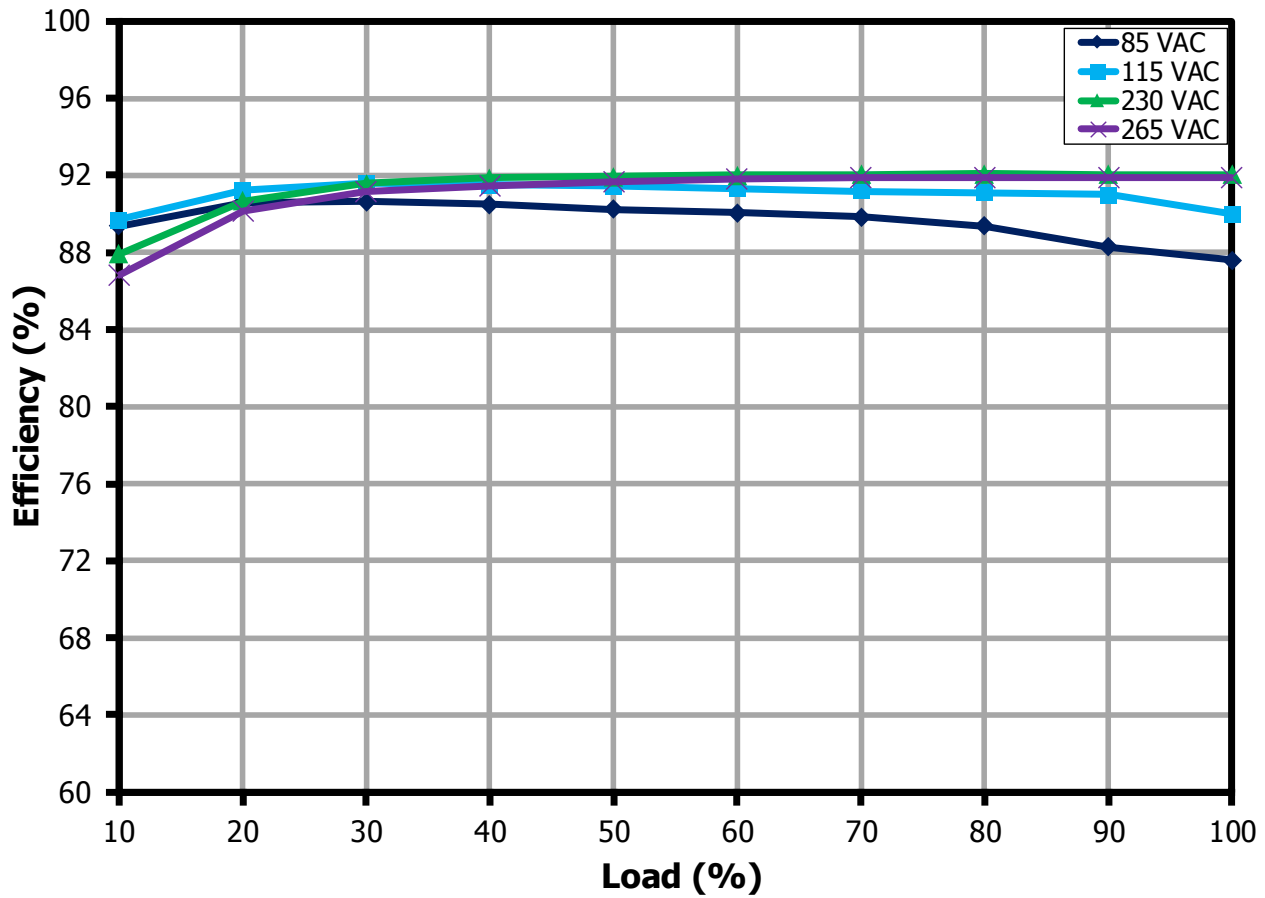


Figure 18 – 15 V Output Efficiency vs. Load.

14.1.5 Output: 16 V / 3 A

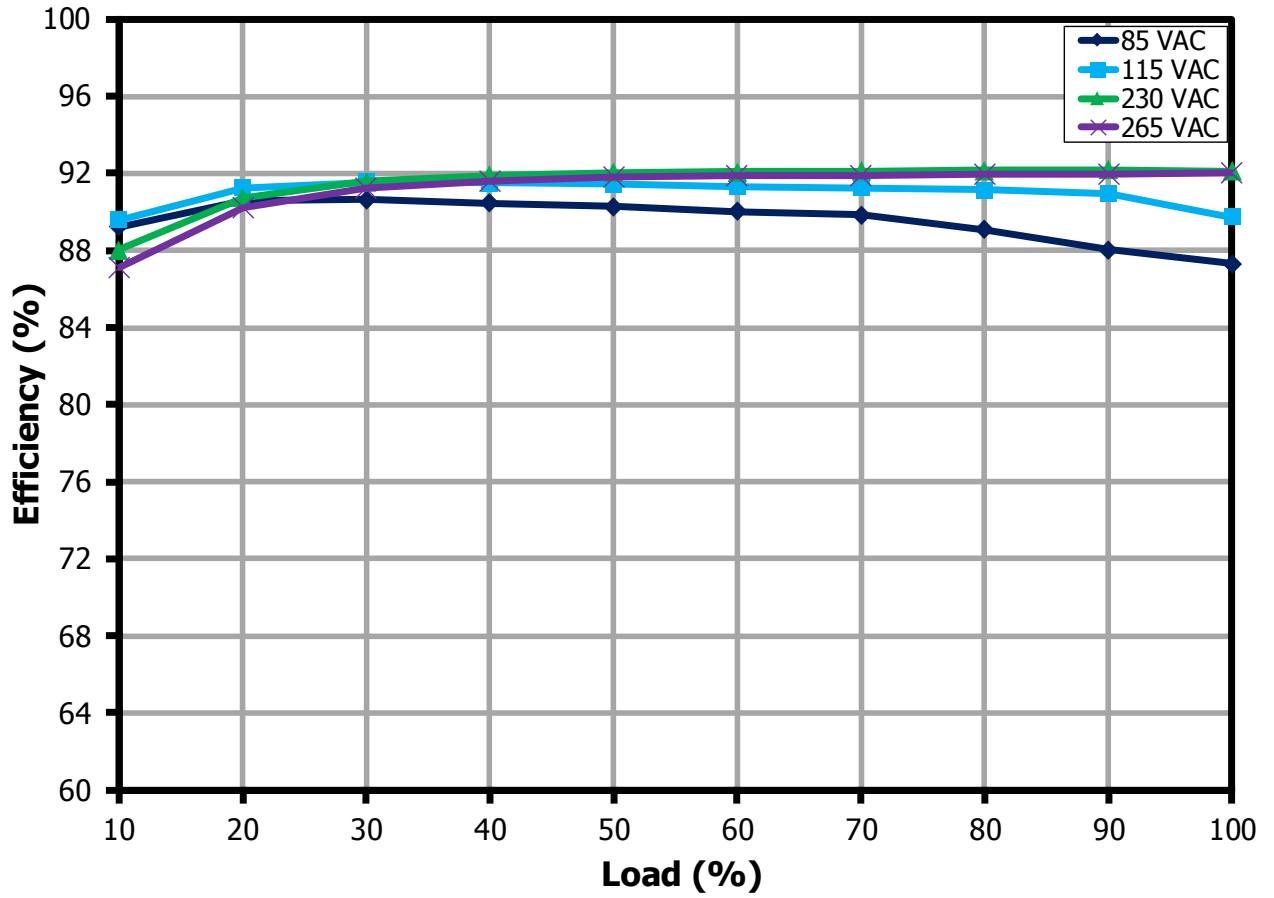


Figure 19 – 16 V Output Efficiency vs. Load.



14.1.6 Output: 20 V / 2.25 A

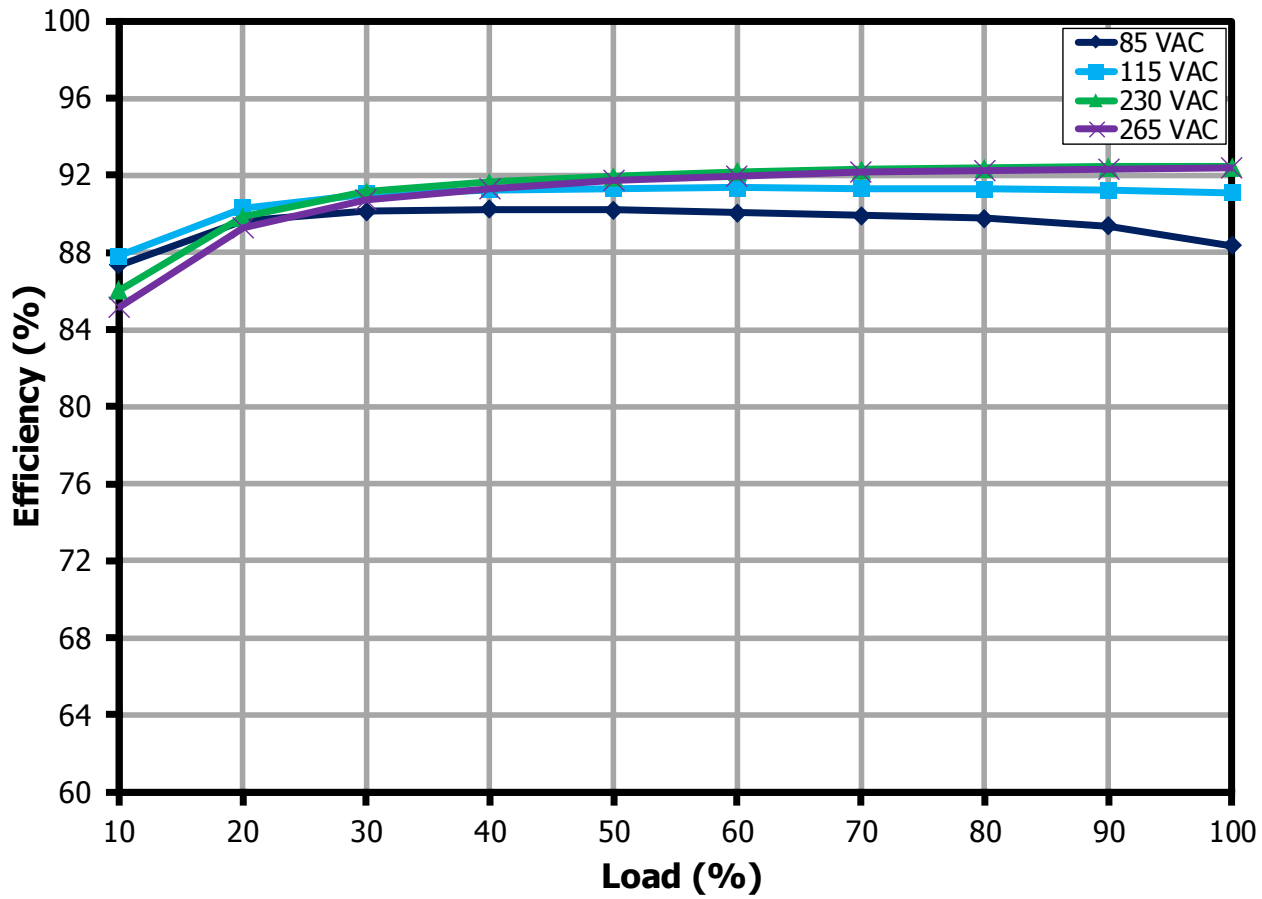


Figure 20 – 20 V Output Efficiency vs. Load.

14.1.7 Output: 21 V / 2.25 A

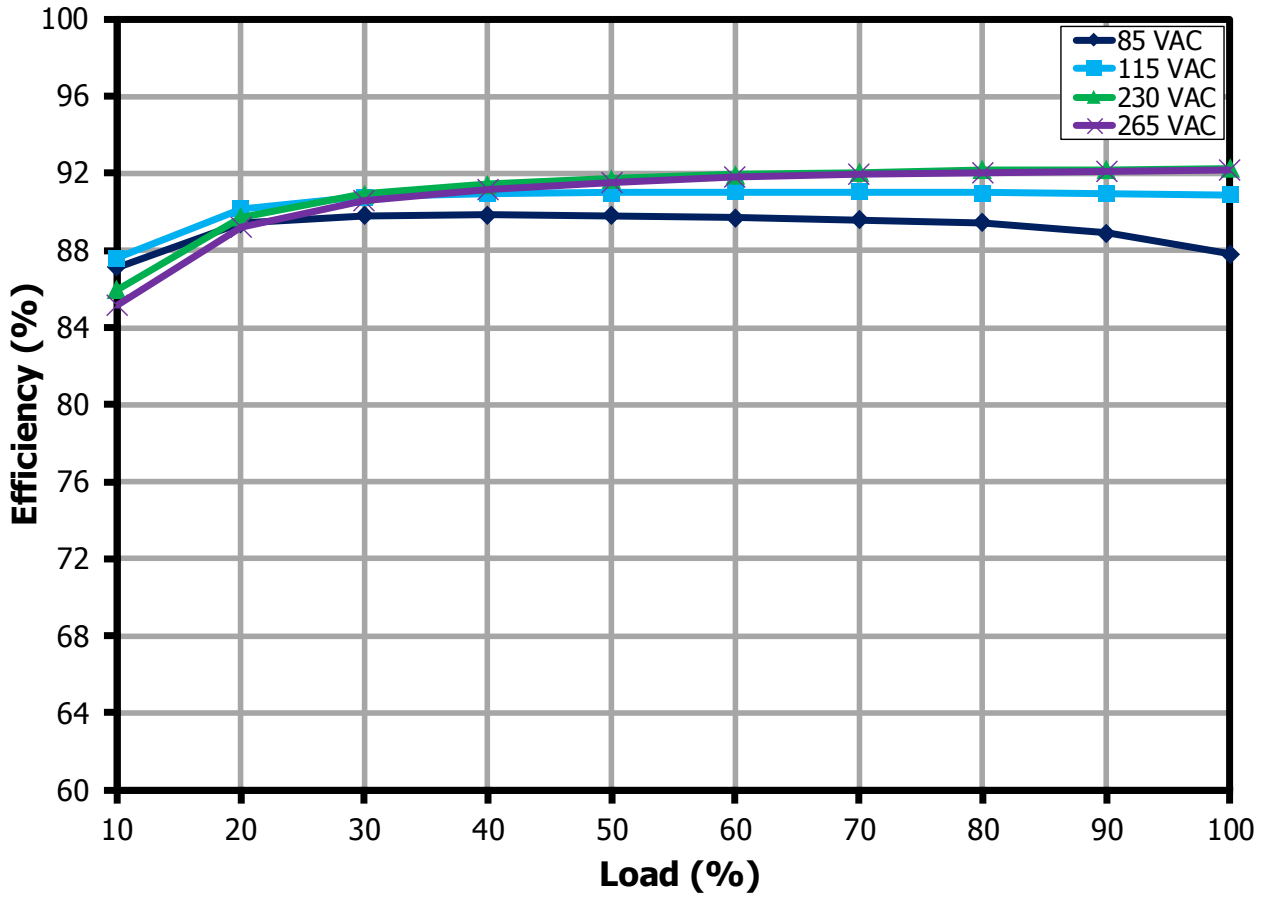


Figure 21 – 21 V Output Efficiency vs. Load.



14.2 Efficiency vs. Line

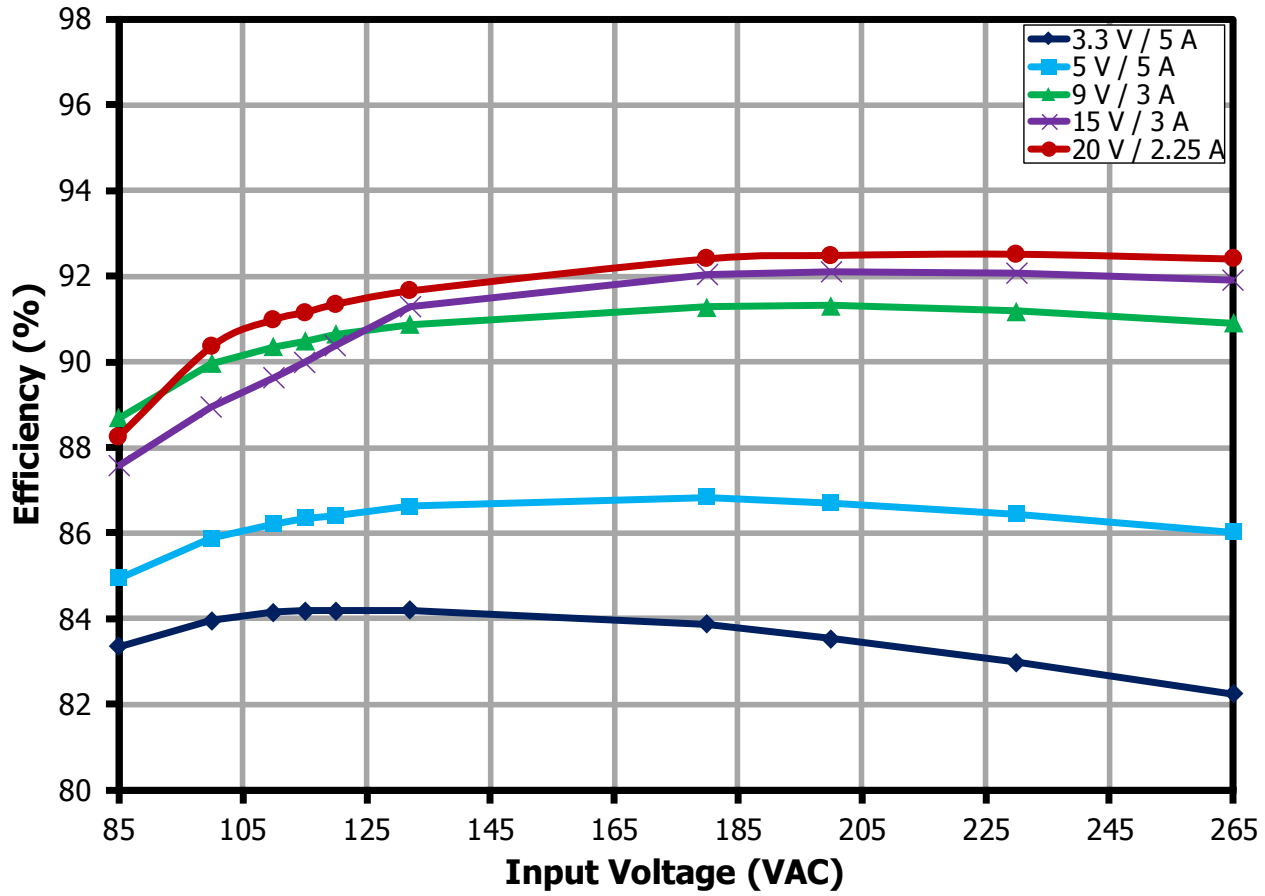


Figure 22 – Efficiency vs. Line.

14.3 Load Regulation

14.3.1 Output: 3.3 V / 5 A

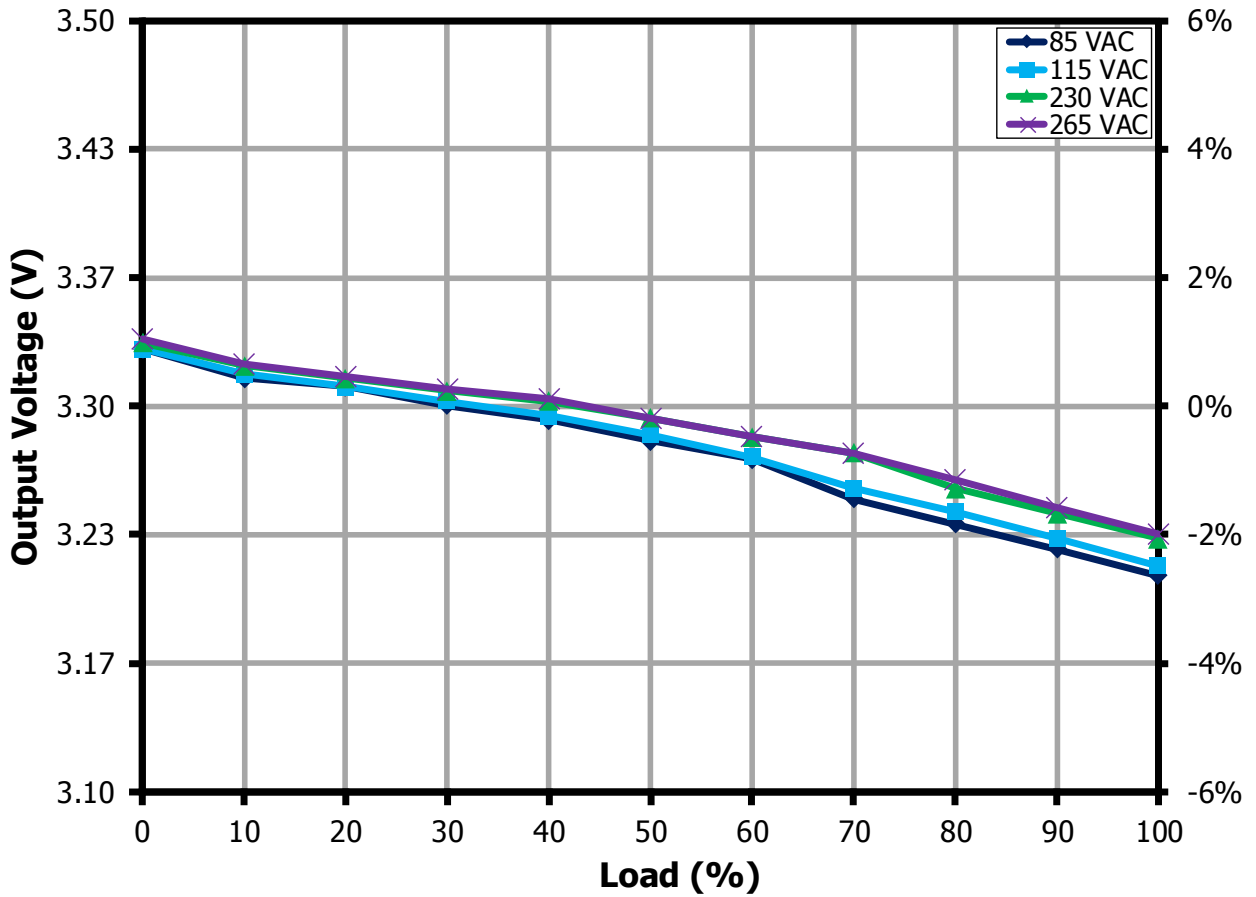


Figure 23 – 3.3 V Output Regulation vs. Percent Load.



14.3.2 Output: 5 V / 5 A

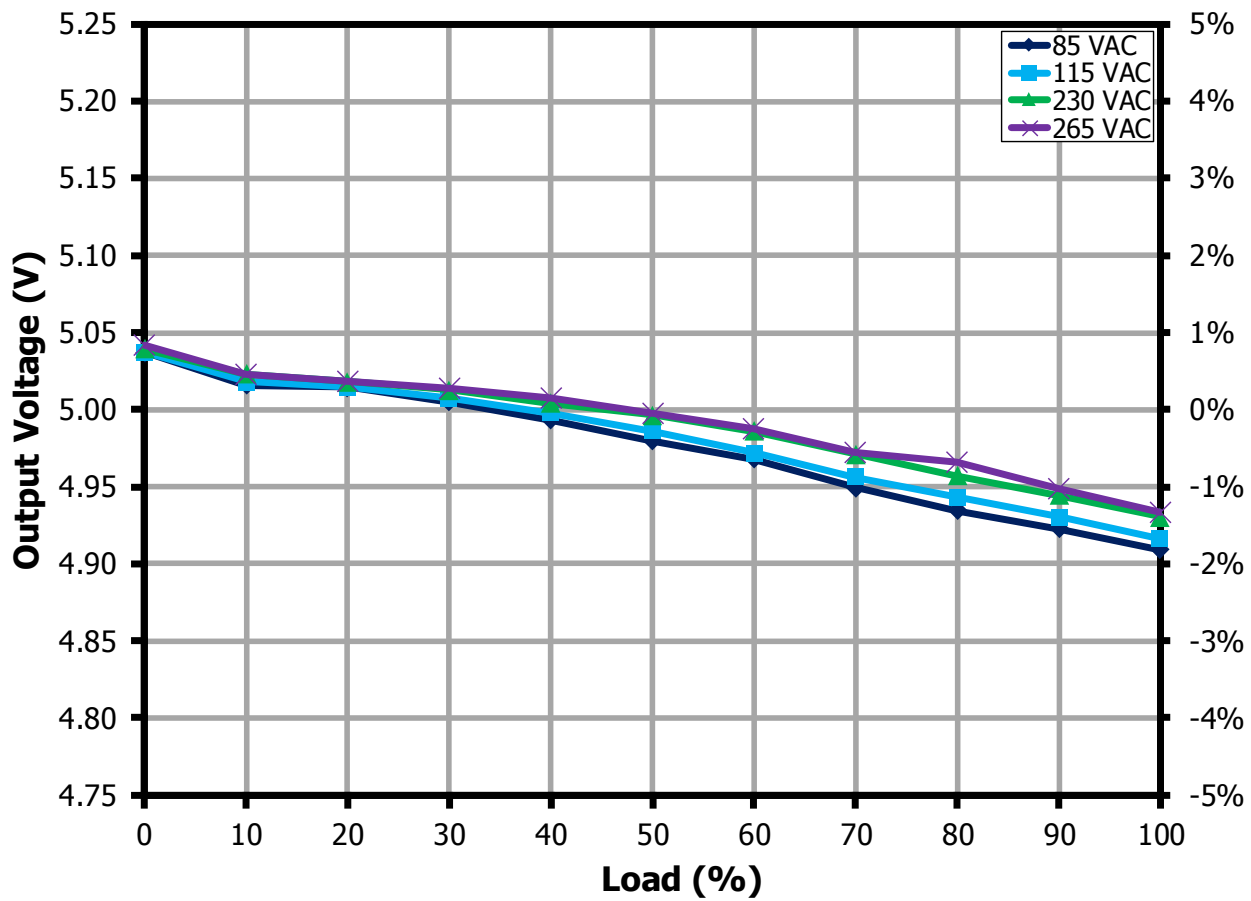


Figure 24 – 5 V Output Regulation vs. Percent Load.



14.3.3 Output: 9 V / 3 A

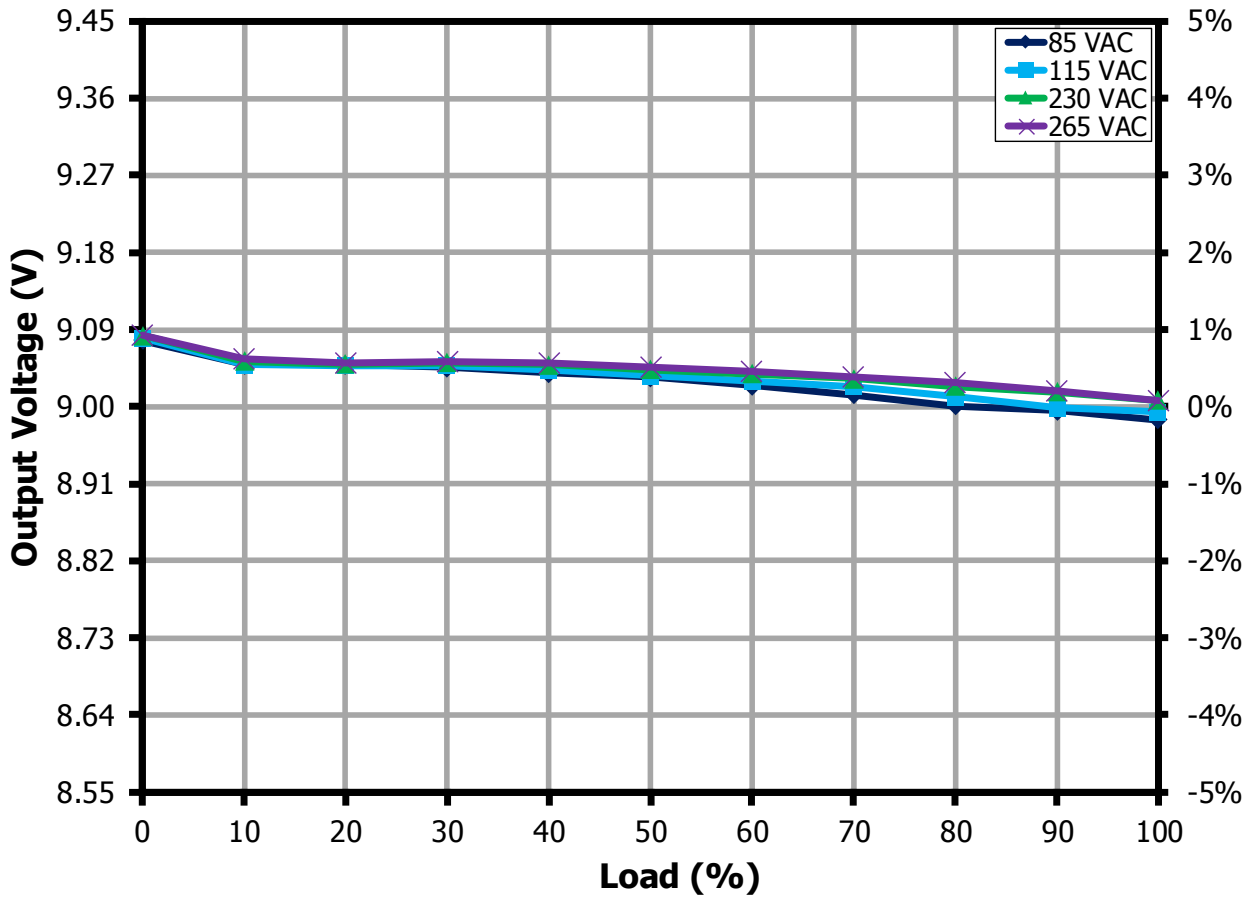


Figure 25 – 9 V Output Regulation vs. Percent Load.



14.3.4 Output: 15 V / 3 A

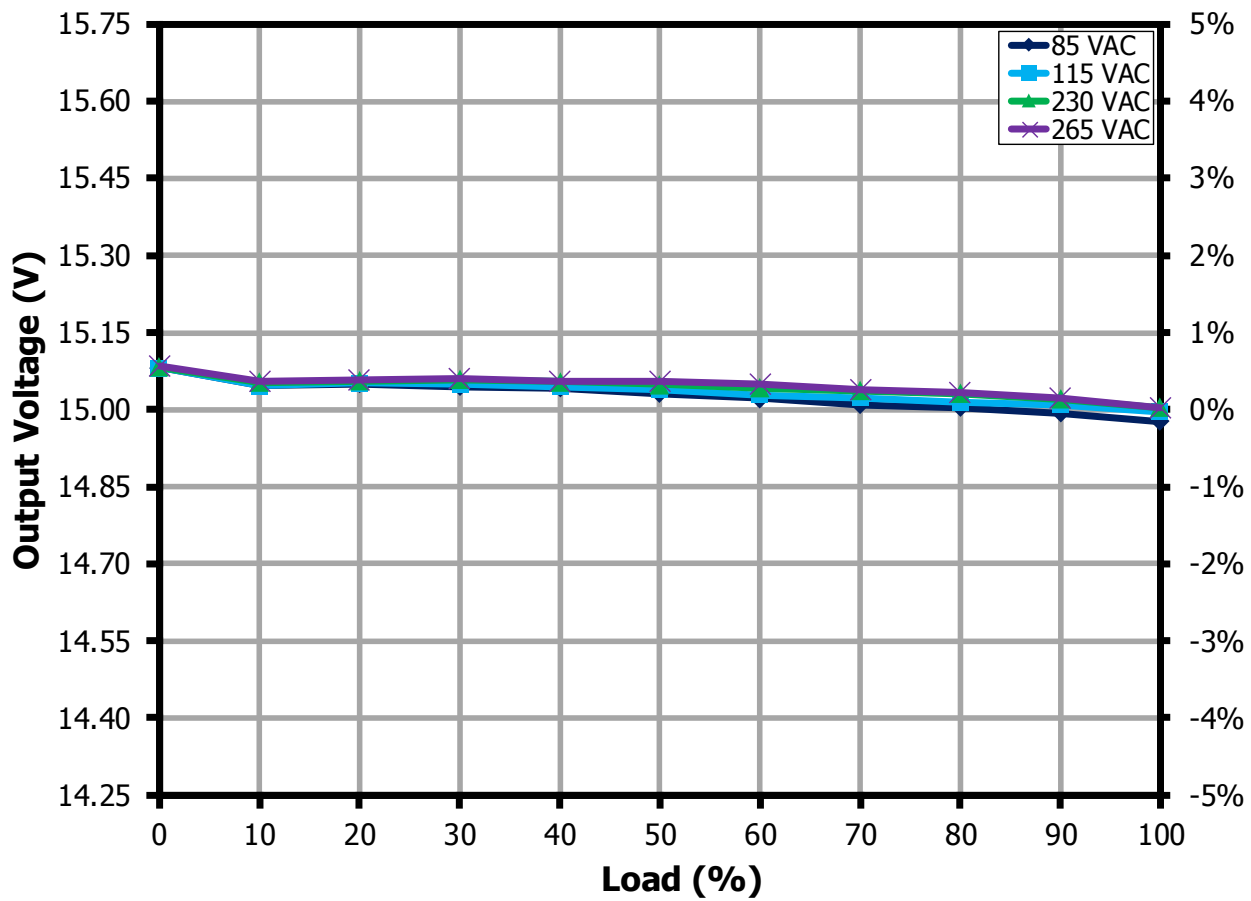


Figure 26 – 15 V Output Regulation vs. Percent Load.

14.3.5 Output: 16 V / 3 A

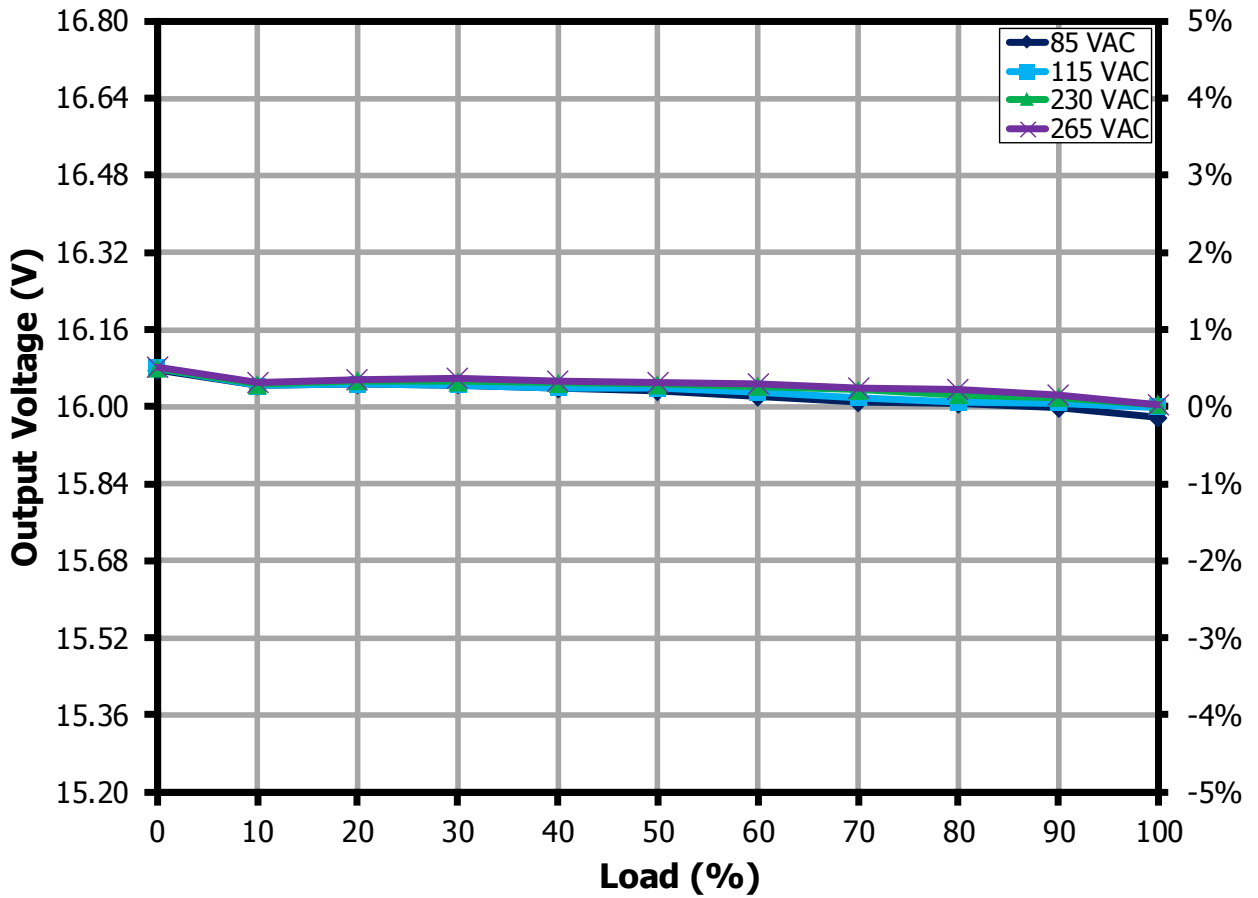


Figure 27 – 16 V Output Regulation vs. Percent Load.



14.3.6 Output: 20 V / 2.25 A

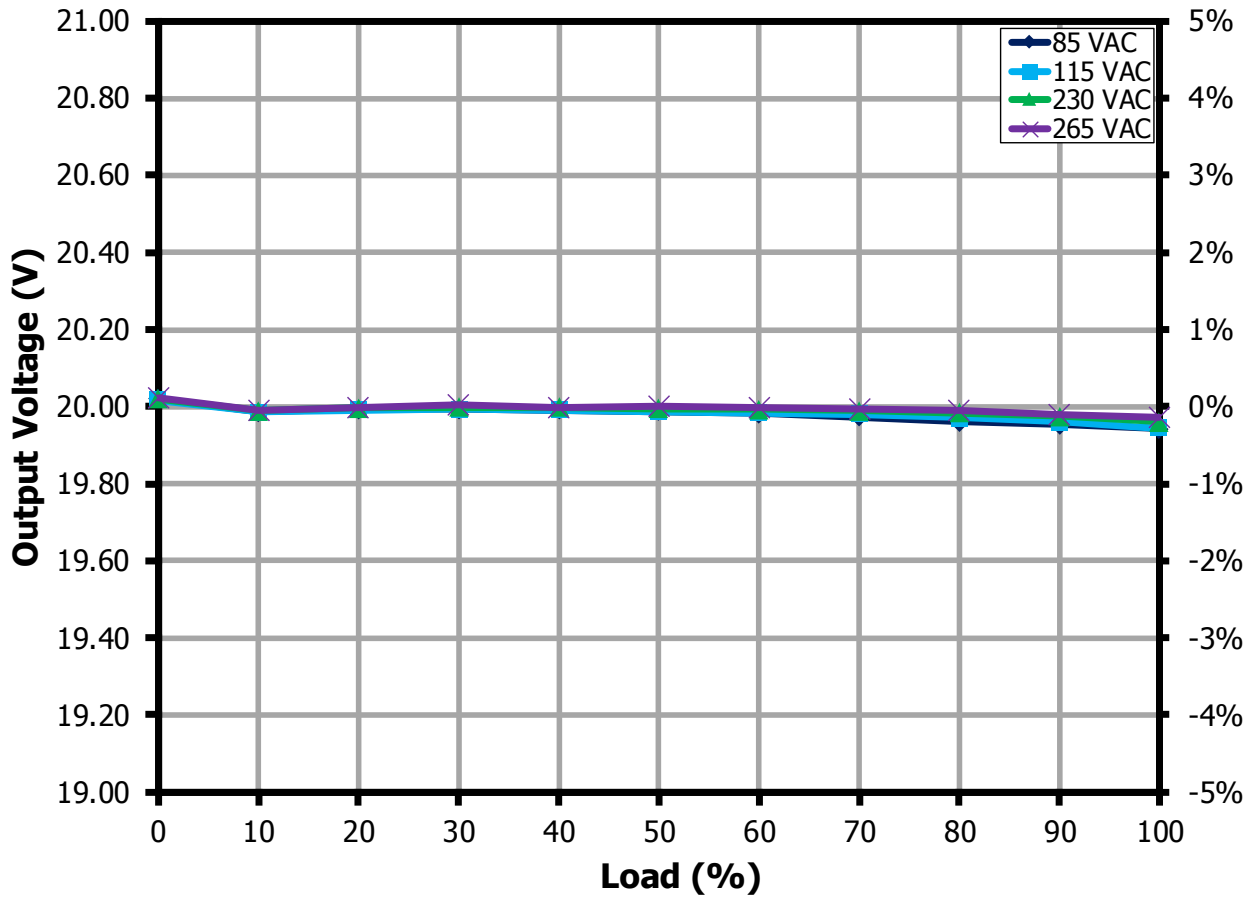


Figure 28 – 20 V Output Regulation vs. Percent Load.



14.3.7 Output: 21 V / 2.25 A

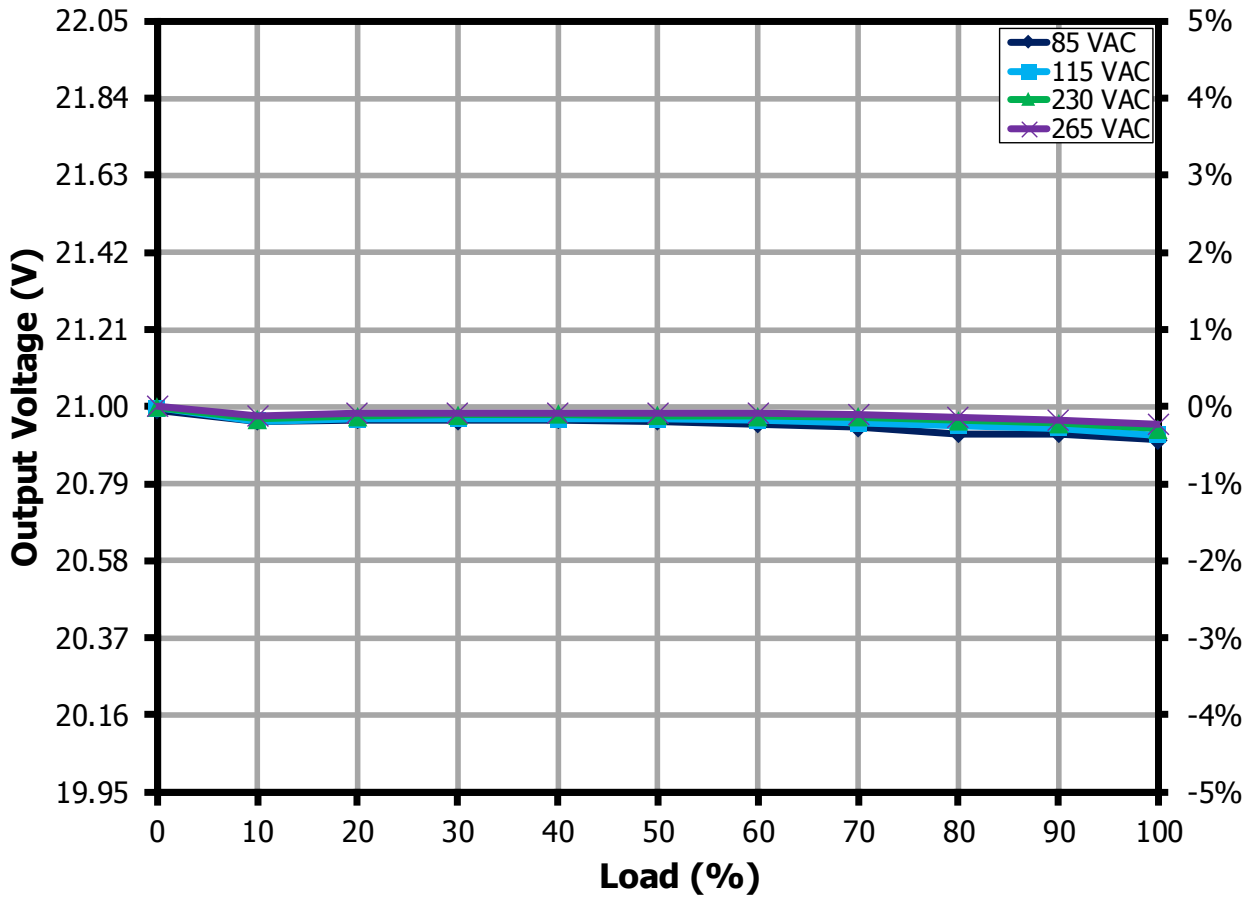


Figure 29 – 20 V Output Regulation vs. Percent Load.



14.4 Line Regulation

14.4.1 Output: 3.3 V / 5 A

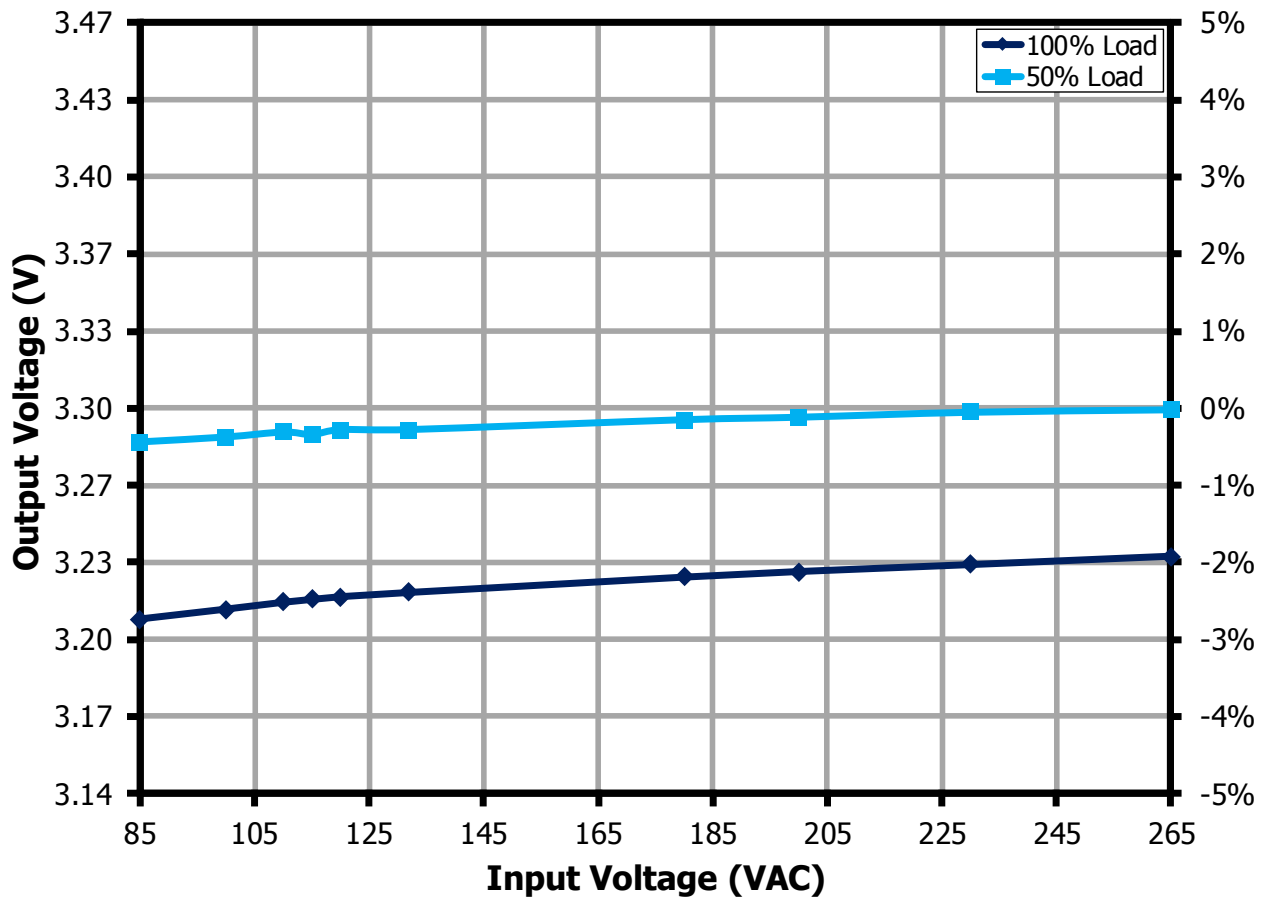


Figure 30 – 3.3 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.

14.4.2 Output: 5 V / 5 A

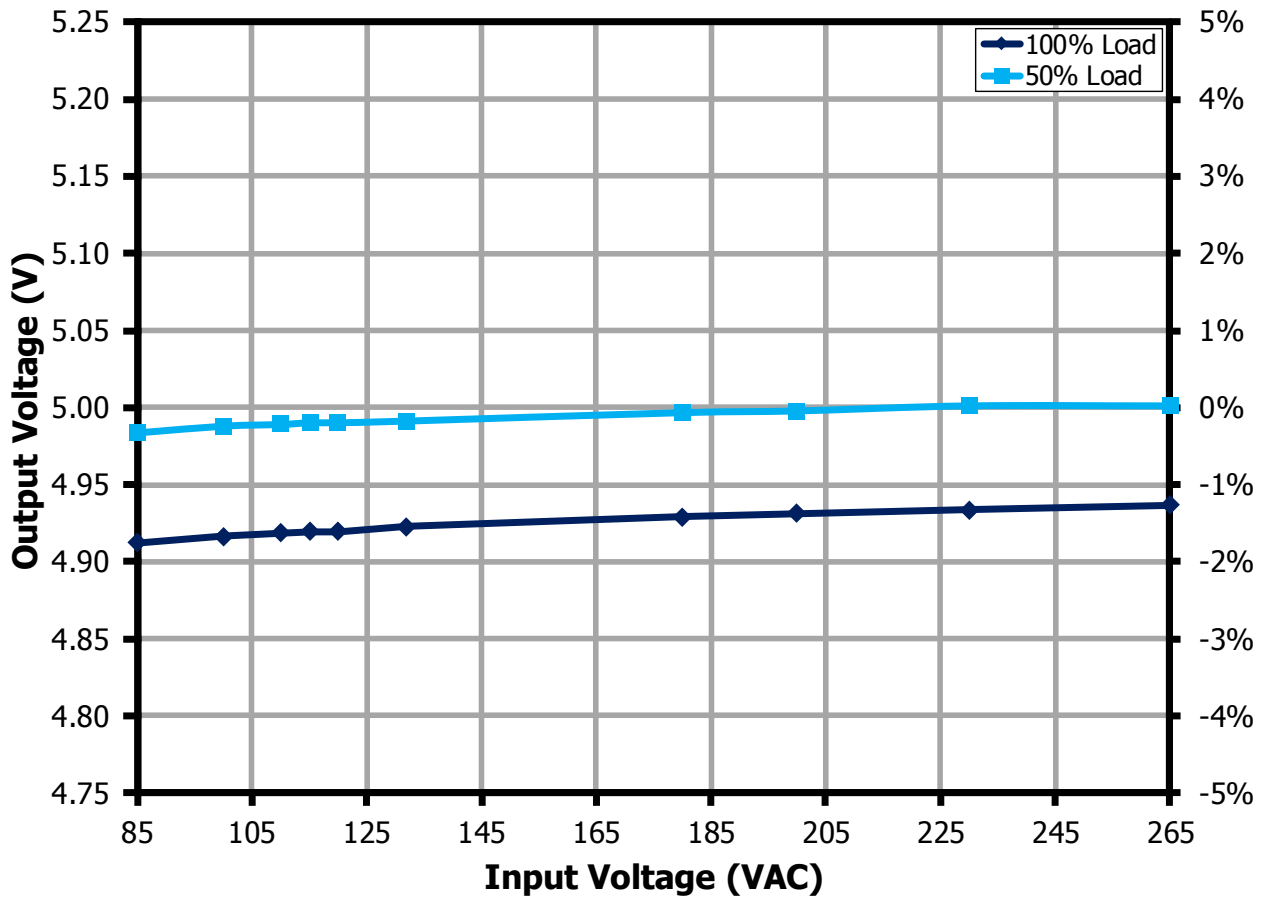


Figure 31 – 5 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.



14.4.3 Output: 9 V / 3 A

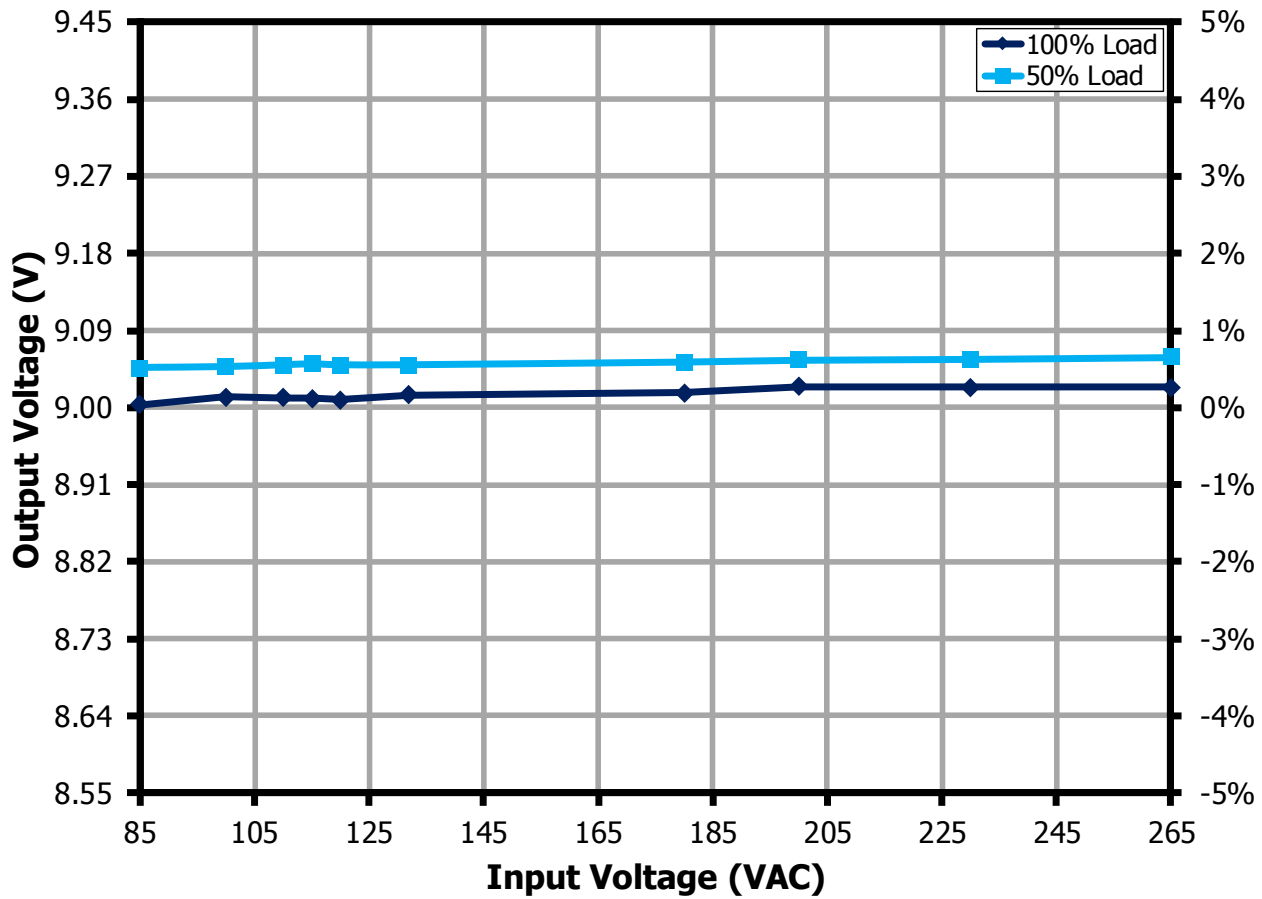


Figure 32 – 9 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.



14.4.4 Output: 15 V / 3 A

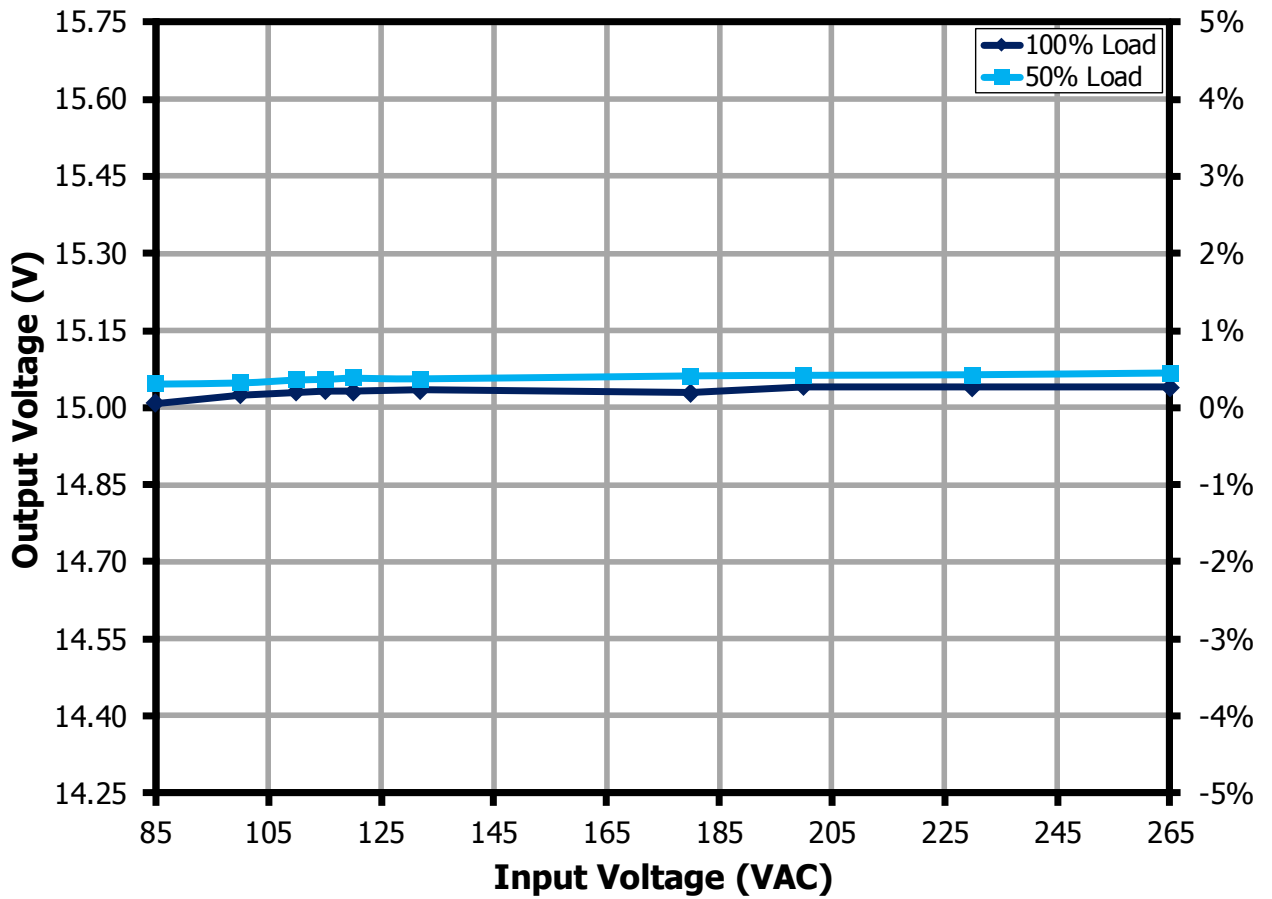


Figure 33 – 15 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.



14.4.5 Output: 16 V / 3 A

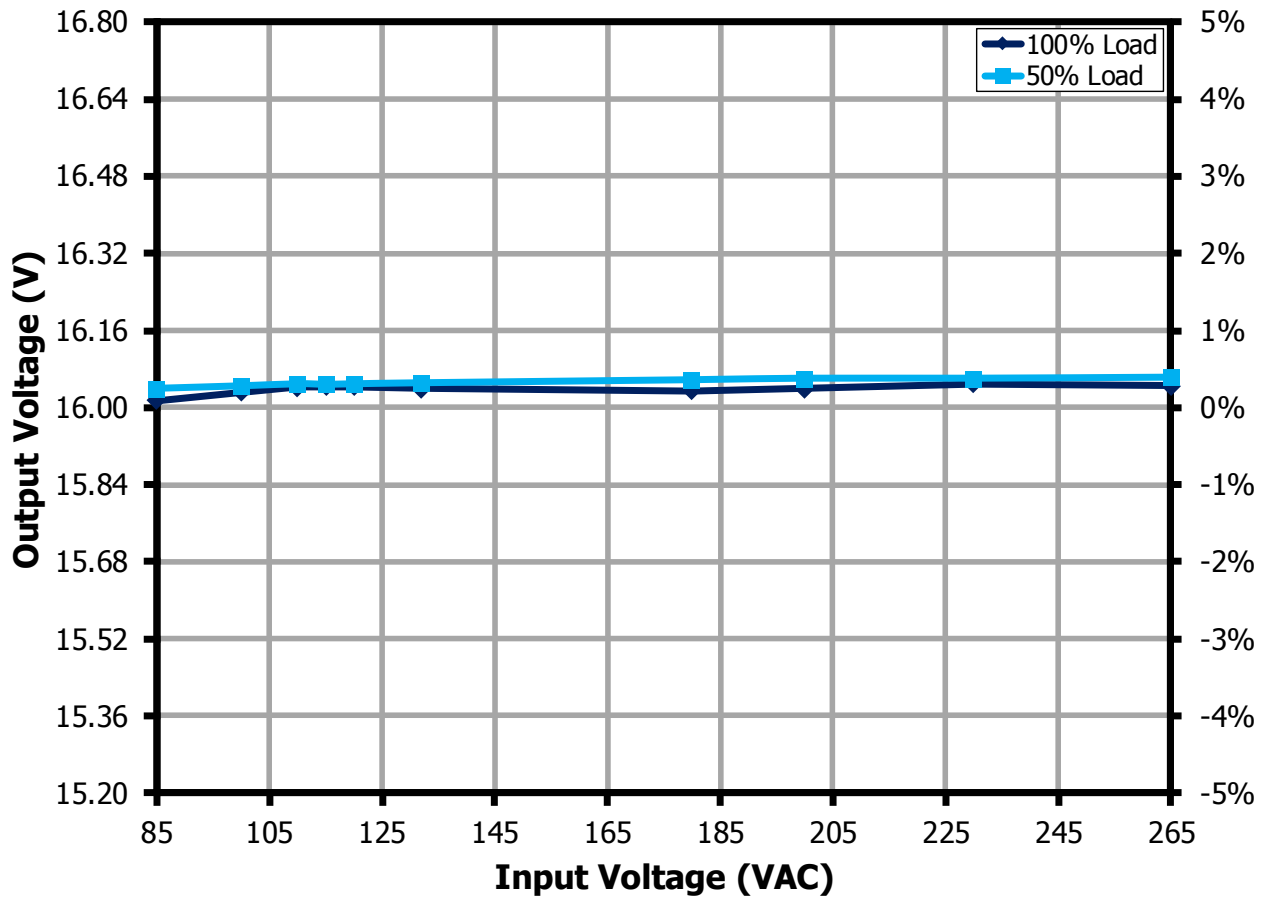


Figure 34 – 15 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.



14.4.6 Output: 20 V / 2.25 A

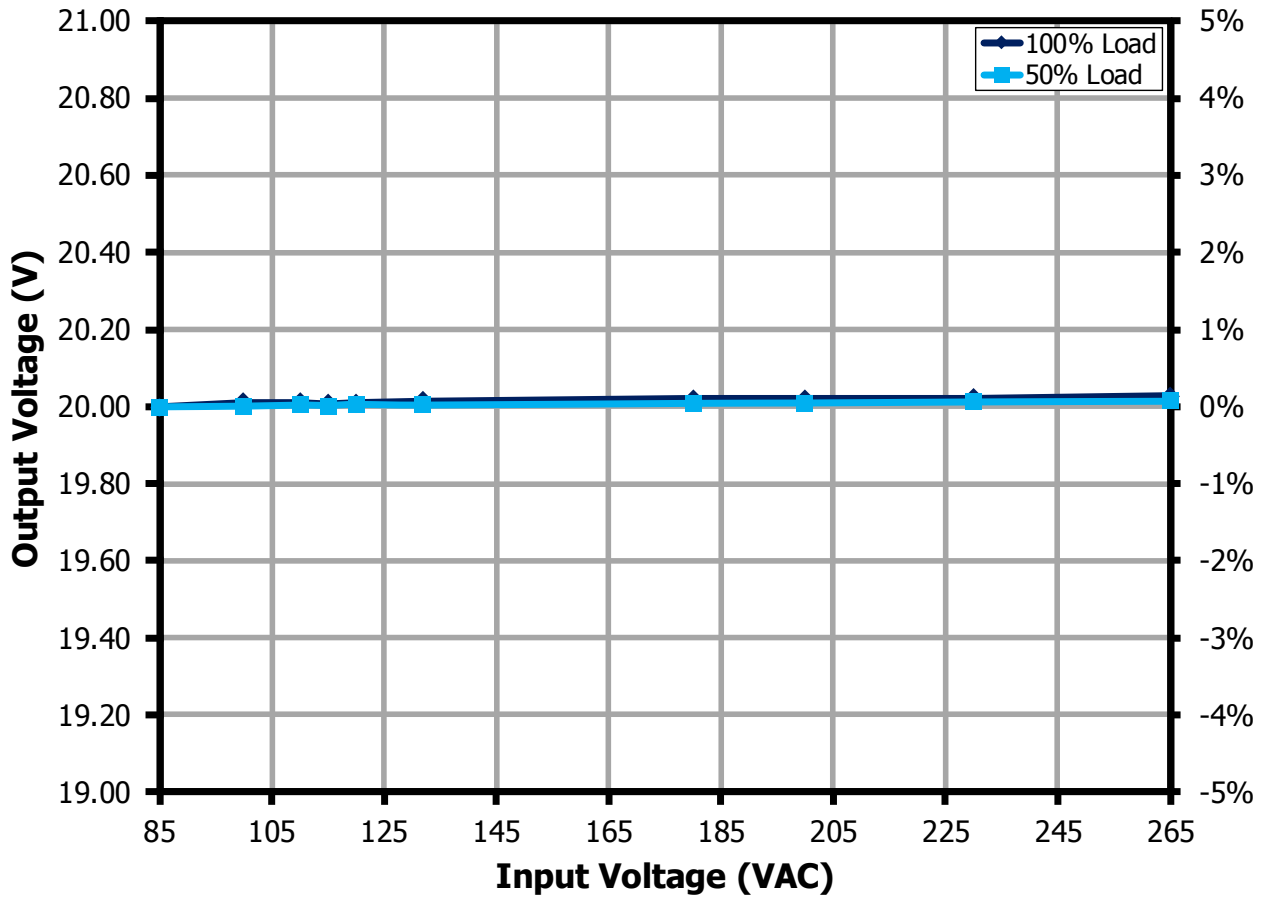


Figure 35 – 20 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.



14.4.7 Output: 21 V / 2.25 A

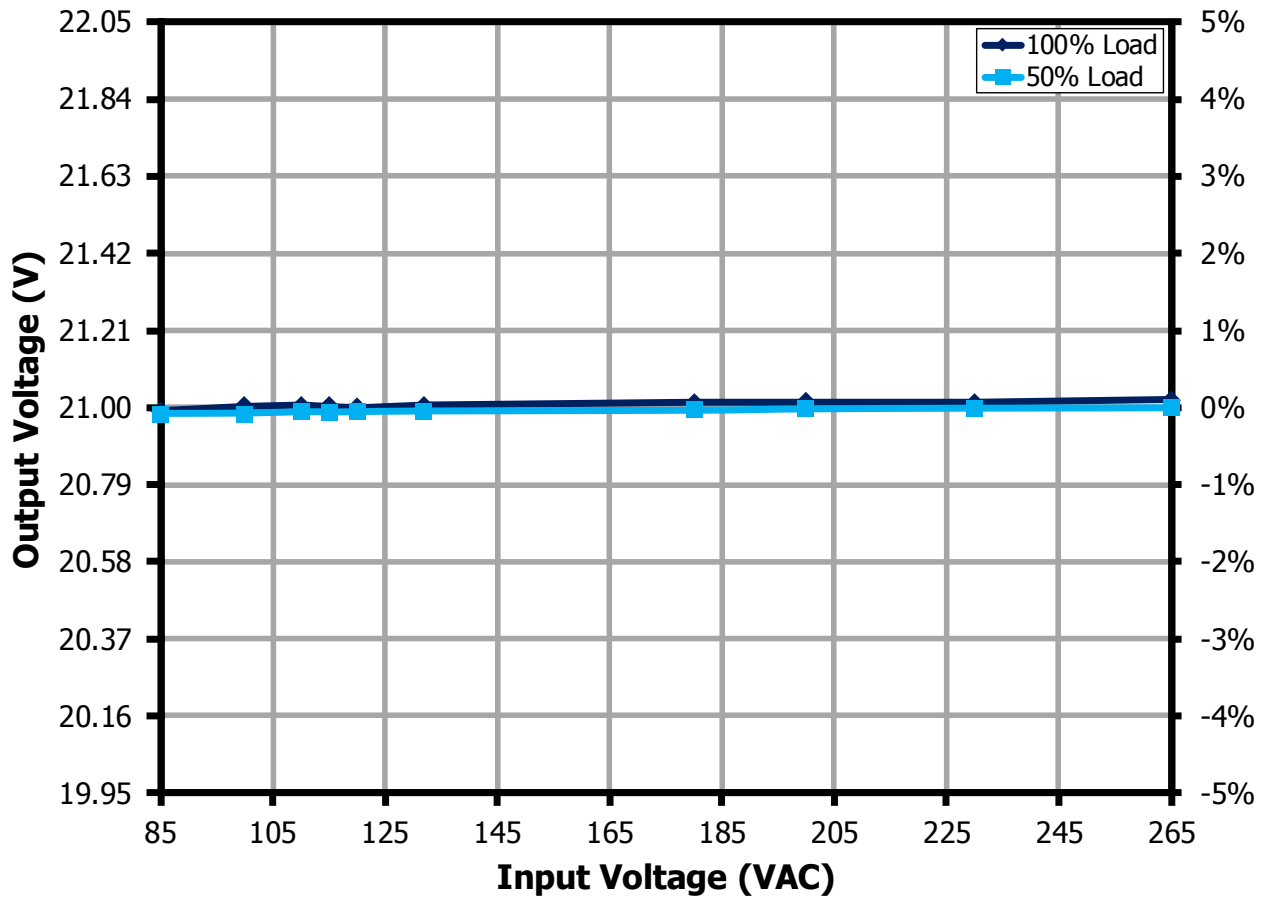


Figure 36 – 20 V Output Regulation vs. Input Line Voltage at 50% and 100% Load.

14.5 **No-Load Input Power at 5 VOUT**

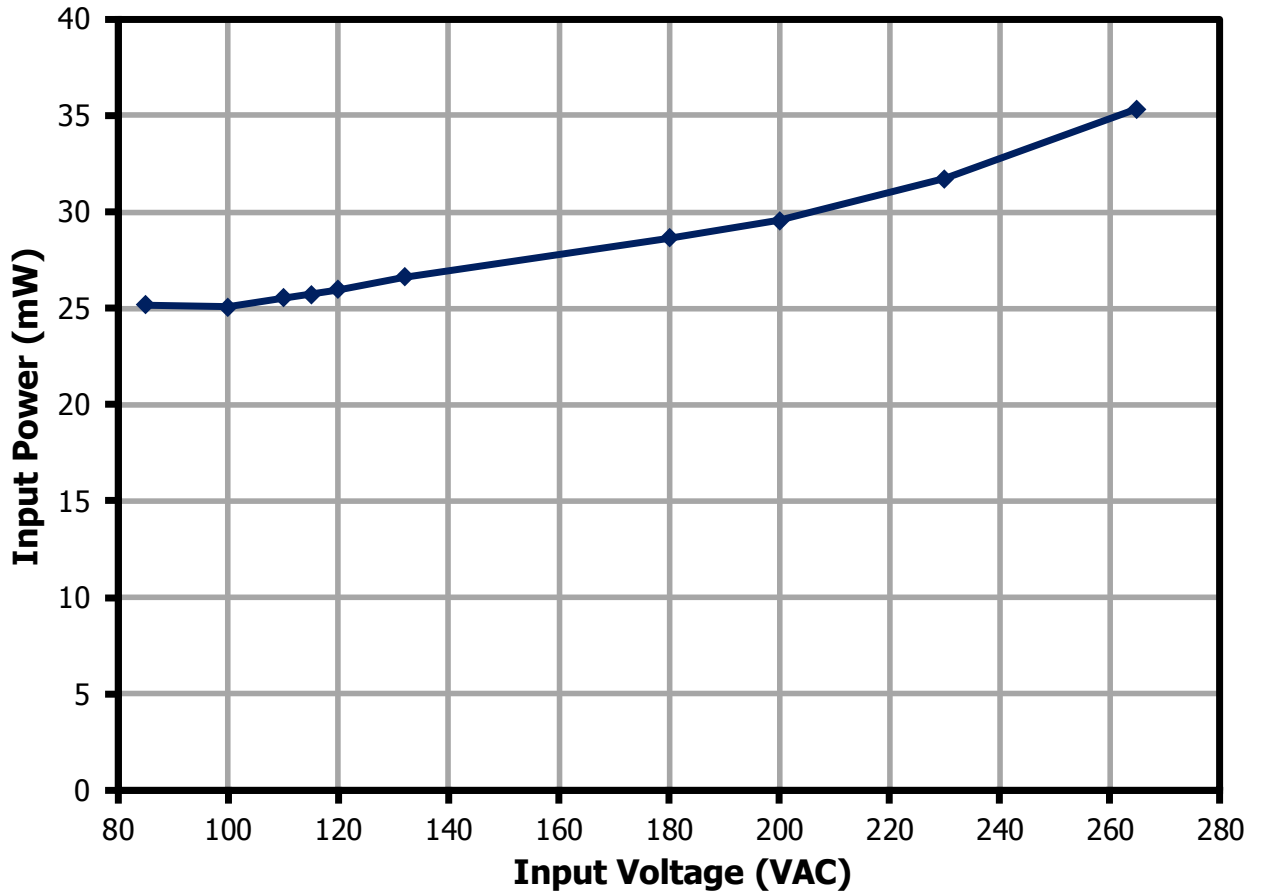


Figure 37 – No-Load Input Power vs. Input Line Voltage.



14.6 Average and 10% Load Efficiency

14.6.1 Efficiency Requirements

		Test Effective	Average 2016 New EISA2007	Average Jan-16 CoC v5 Tier 2	10% Load Jan-16 CoC v5 Tier 2
Output voltage	Model	Power (W)			
3.3 V	<6 V	16.5	81.97%	82.47%	73.08%
5 V	<6 V	25	84.25%	85.00%	75.47%
9 V	>6 V	27	88.00%	87.30%	77.30%
15 V	>6 V	45	88.00%	88.85%	78.85%
20 V	>6 V	45	88.00%	88.85%	78.85%

14.6.2 Average and 10% Efficiency (On the Board)

14.6.2.1 Output: 3.3 V / 5 A

Input (VAC)	Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Limit (%)	CoC v5 Tier 2 (%)
115	100	15.77	84.27	86.34	81.97	82.47
	75	11.95	86.04			
	50	8.04	87.51			
	25	4.05	87.53			
	10	1.62	85.18			
230	100	15.82	83.23	84.41	81.97	82.47
	75	11.98	85.37			
	50	8.06	85.54			
	25	4.05	83.51			
	10	1.62	79.38			

14.6.2.2 Output: 5 V / 5 A

Input (VAC)	Load (%)	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	24.32	86.88	88.87	84.25	85.00
	75	18.36	88.39			
	50	12.32	89.74			
	25	6.19	90.48			
	10	2.48	90.12			
230	100	24.39	86.94	88.50	84.25	85.00
	75	18.41	89.12			
	50	12.34	89.25			
	25	6.19	88.70			



	10	2.48	86.91			75.47
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14.6.2.3 Output: 9 V / 3 A

Input (VAC)	% Load	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	26.68	90.59	91.10	86.62	87.30
	75	20.06	91.00			
	50	13.40	91.34			
	25	6.70	91.47			
	10	2.68	90.09			
230	100	26.72	91.21	90.87	86.62	87.30
	75	20.08	91.22			
	50	13.40	91.12			
	25	6.70	89.94			
	10	2.68	87.21			

14.6.2.4 Output: 15 V / 3 A

Input (VAC)	% Load	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	44.61	90.57	91.23	87.73	88.85
	75	33.51	91.28			
	50	22.37	91.53			
	25	11.19	91.54			
	10	4.46	89.84			
230	100	44.62	92.08	91.80	87.73	88.85
	75	33.53	92.10			
	50	22.38	91.97			
	25	11.18	91.06			
	10	4.46	87.84			

14.6.2.5 Output: 16 V / 3 A

Input (VAC)	% Load	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	47.58	90.22	91.13	87.77	88.97
	75	35.73	91.28			
	50	23.85	91.52			
	25	11.93	91.49			
	10	4.76	89.67			
230	100	47.61	92.15	91.85	87.77	88.97
	75	35.75	92.13			
	50	23.86	92.03			
	25	11.93	91.11			
	10	4.76	87.91			

14.6.2.6 Output: 20 V / 2.25 A

Input (VAC)	% Load	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	44.64	90.93	91.03	87.73	88.85
	75	33.50	91.16			
	50	22.34	91.26			
	25	11.16	90.76			
	10	4.44	87.63			
230	100	44.67	92.16	91.63	87.73	88.85
	75	33.52	92.10			
	50	22.36	91.88			
	25	11.15	90.37			
	10	4.44	86.13			



14.6.2.7 Output: 21 V / 2.25 A

Input (VAC)	% Load	P _{OUT} (W)	Efficiency (%)	Average Efficiency (%)	DOE6 Requirement (%)	CoC v5 Tier 2 Requirement (%)
115	100	46.80	91.10	91.09	87.76	88.94
	75	35.13	91.25			
	50	23.44	91.33			
	25	11.71	90.69			
	10	4.66	87.59			
230	100	46.85	92.18	91.64	87.76	88.94
	75	35.15	92.07			
	50	23.45	91.80			
	25	11.71	90.49			
	10	4.66	86.14			

14.7 CV/CC Operation

Note: Positive slope in CC region is per the guidelines of USB PD 3.0 PPS specification.

14.7.1 Output: 5.9 V / 3 A

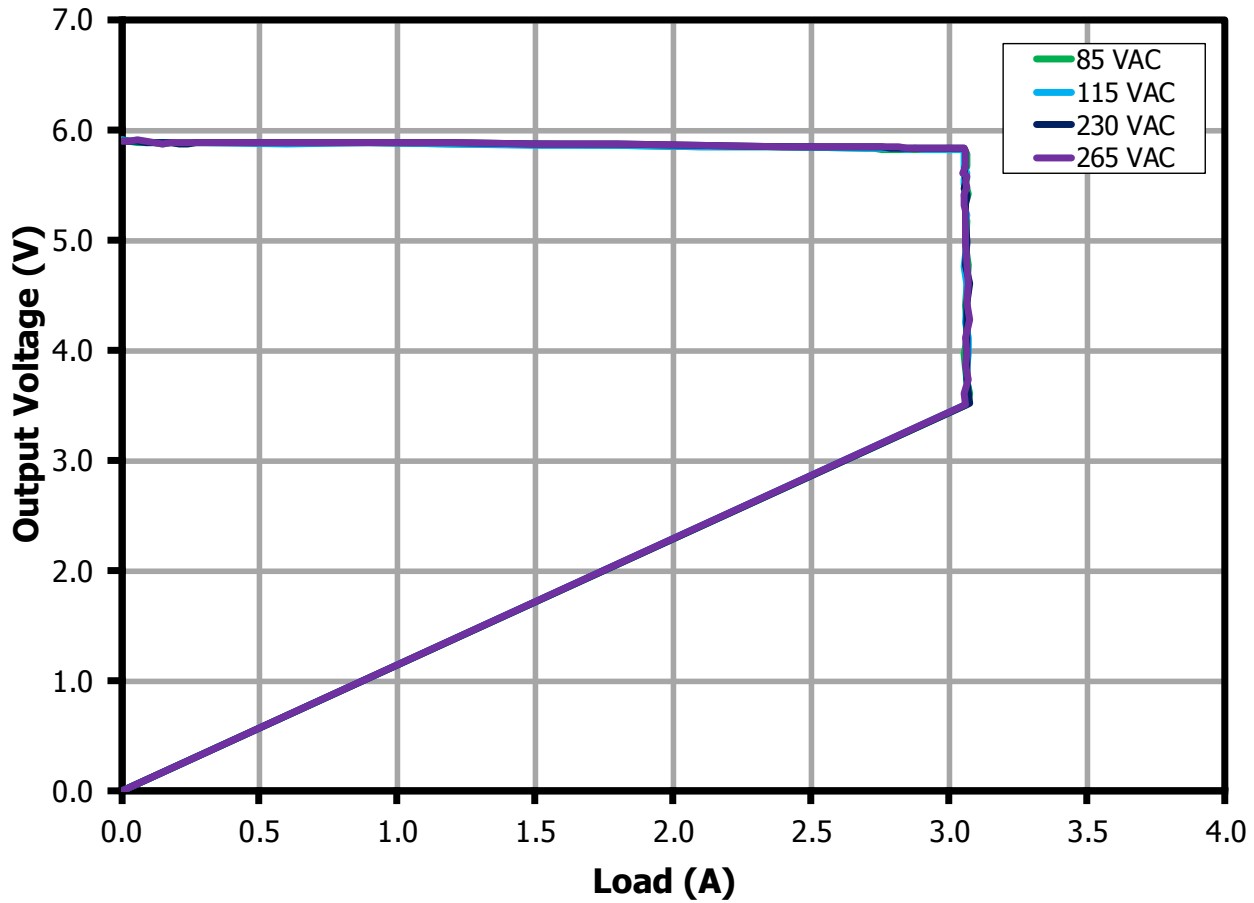


Figure 38 – Output Voltage vs. Output Current, Room Temperature.

14.7.2 Output: 5.9 V / 5 A

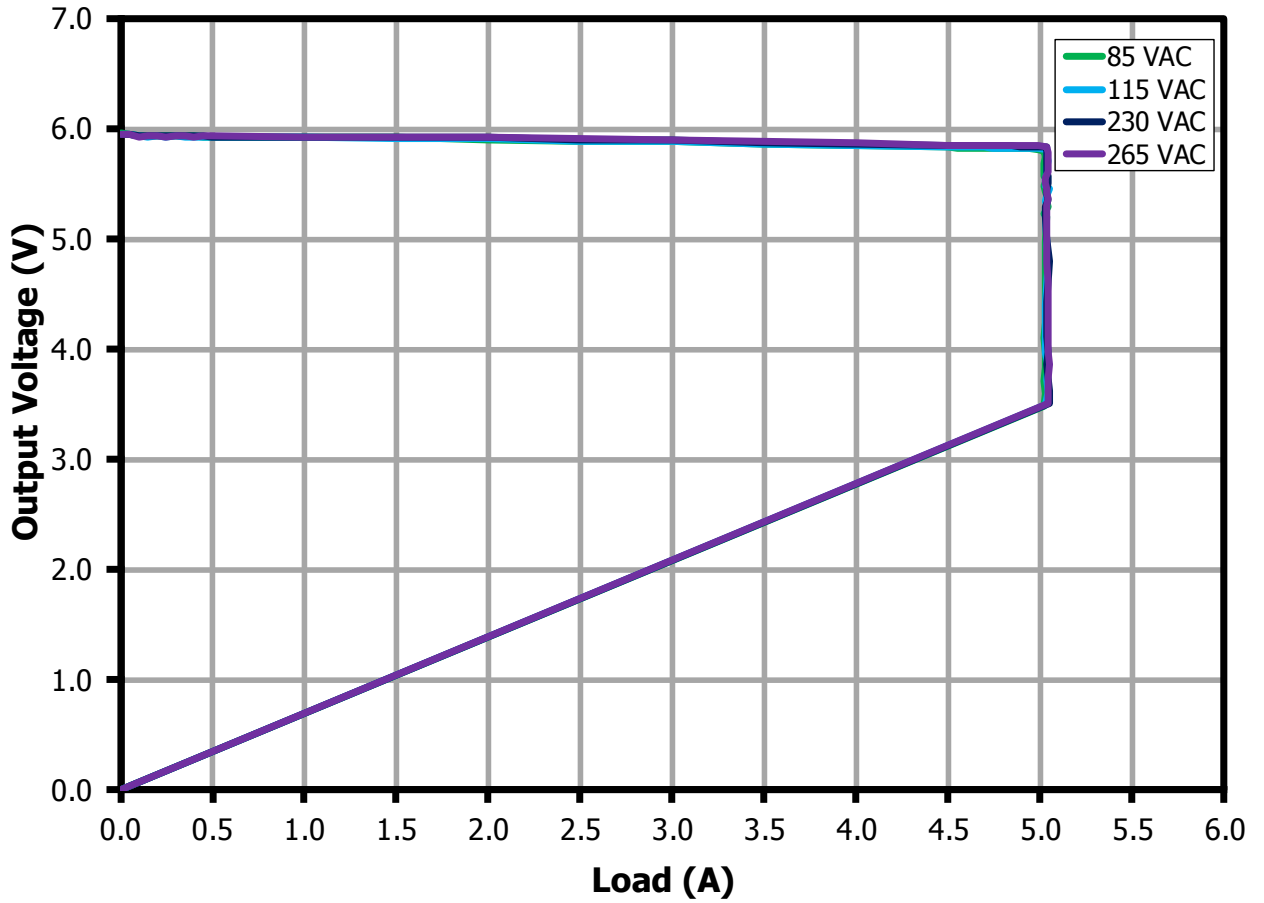


Figure 39 – Output Voltage vs. Output Current, Room Temperature.



14.7.3 Output: 11 V / 3 A

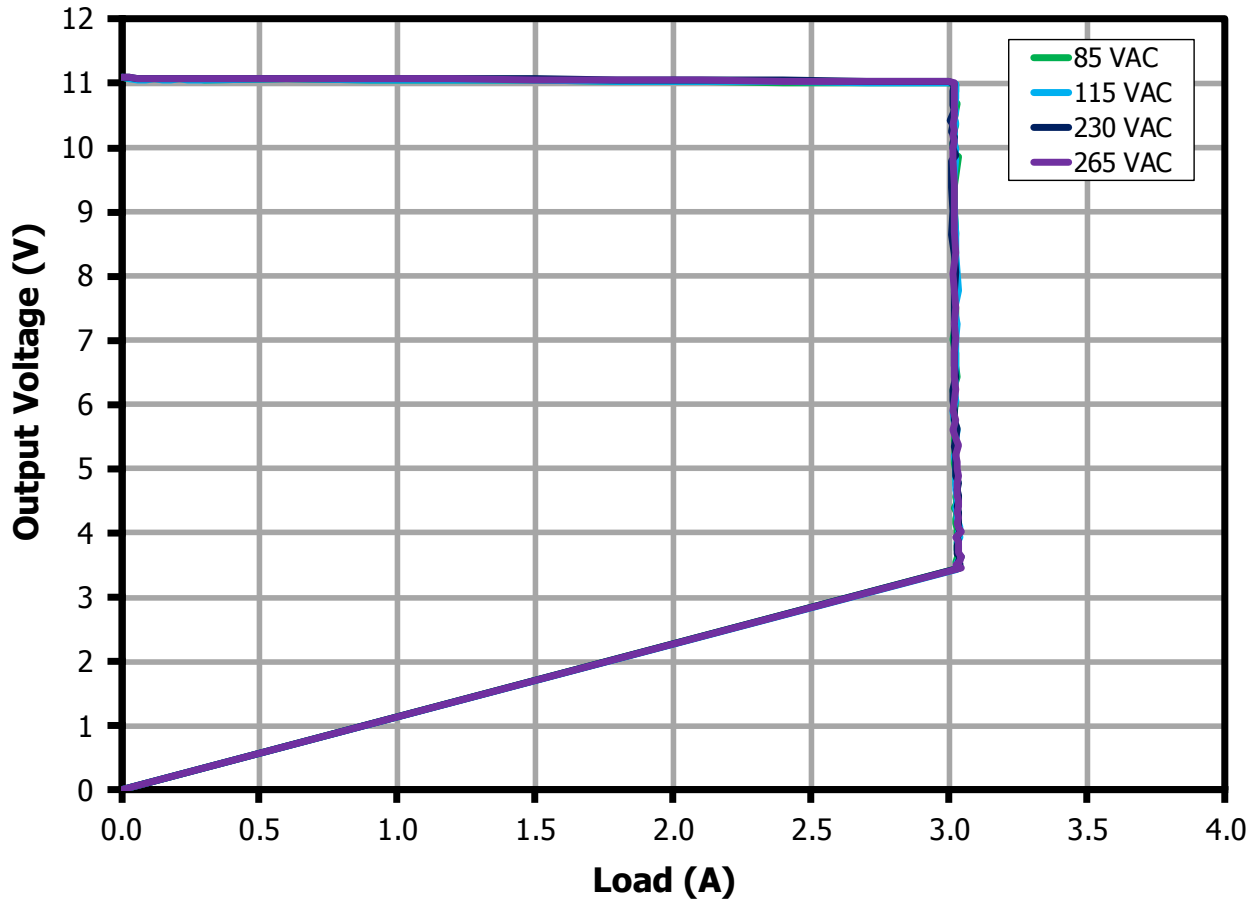


Figure 40 – Output Voltage vs. Output Current, Room Temperature.

14.7.4 Output: 16 V / 3 A

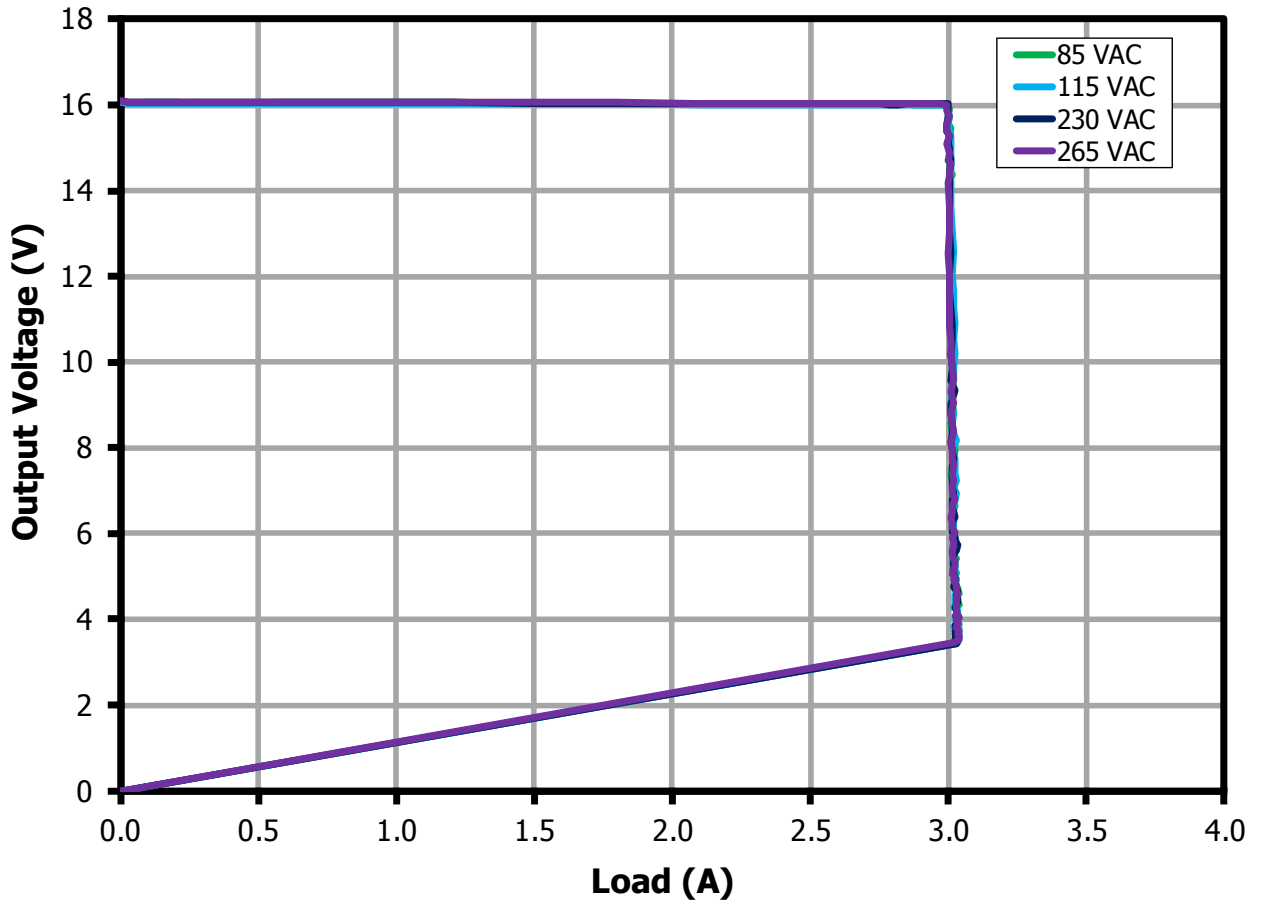


Figure 41 – Output Voltage vs. Output Current, Room Temperature.



14.7.5 Output: 21 V / 2.25 A

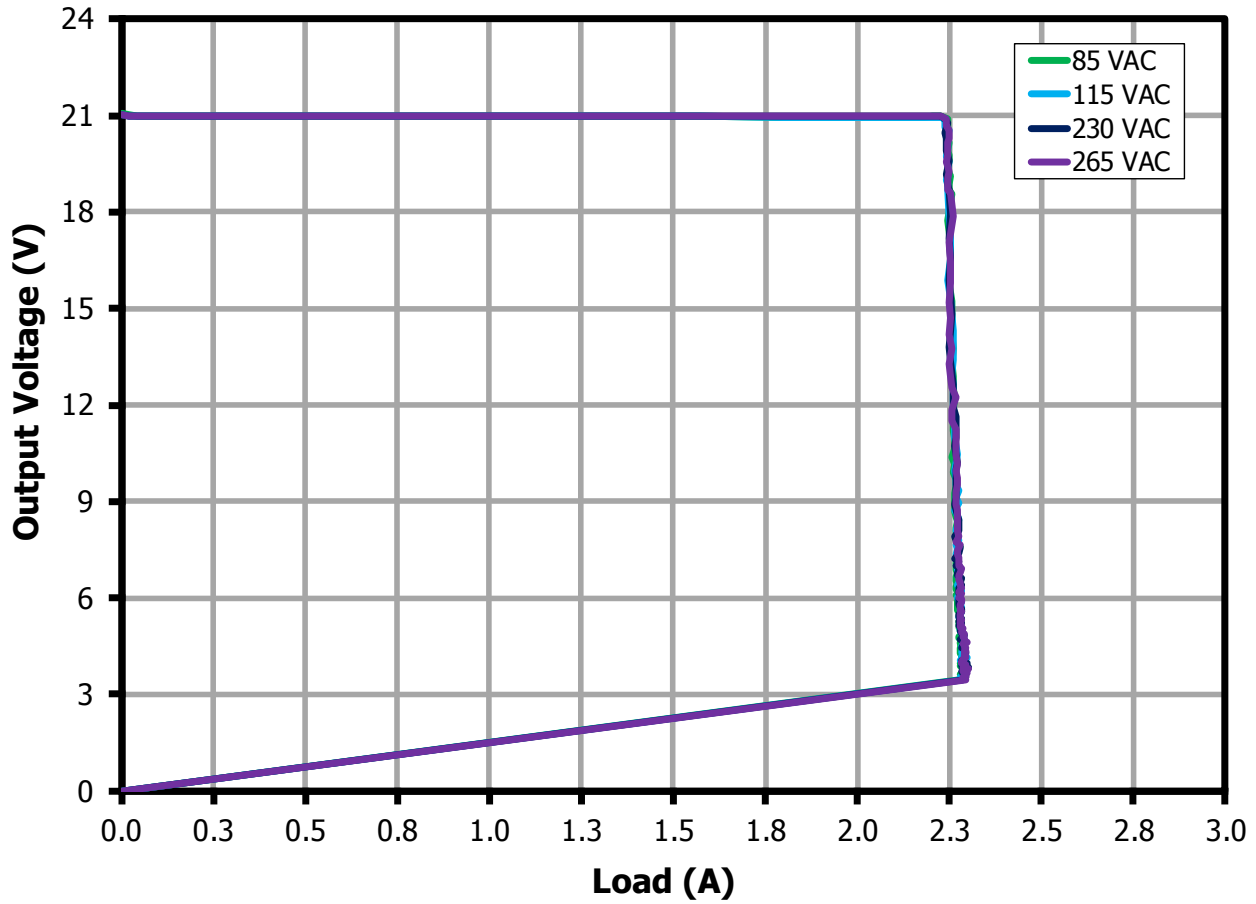


Figure 42 – Output Voltage vs. Output Current, Room Temperature.

15 Thermal Performance in Open Case

Note: Tested at approximately 25 °C ambient temperature.

15.1 85 VAC Input 15 V / 3 A

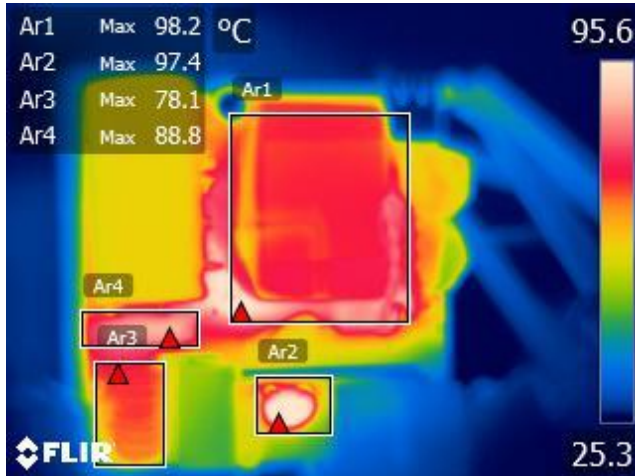


Figure 43 – Top Side Thermal Image.

Ar1: Transformer T1 = 98.2 °C.
 Ar2: Thermistor RT2 = 97.4 °C.
 Ar3: CMC L1 = 78.1 °C.
 Ar4: Bridge Rectifier BR1 = 88.8 °C.

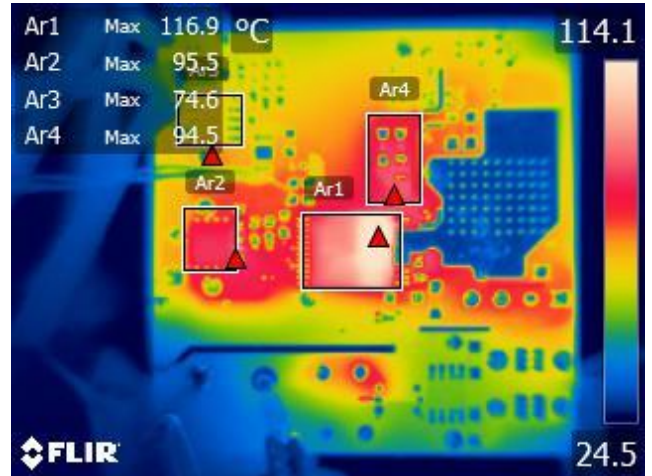


Figure 44 – Bottom Side Thermal Image.

Ar1: InnoSwitch3-Pro U2 = 116.9 °C.
 Ar2: SR FET Q2 = 95.5 °C.
 Ar3: VBUS FET Q1 = 74.6 °C.
 Ar4: Primary Snubber = 94.5 °C.

15.2 265 VAC Input 15 V / 3 A

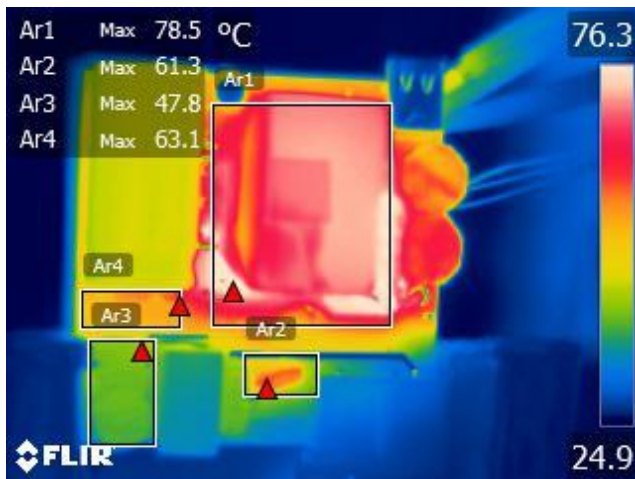


Figure 45 – Top Side Thermal Image.

Ar1: Transformer T1 = 78.5 °C.
 Ar2: Thermistor RT2 = 61.3 °C.
 Ar3: CMC L1 = 47.8 °C.
 Ar4: Bridge Rectifier BR1 = 63.1 °C.



Figure 46 – Bottom Side Thermal Image.

Ar1: InnoSwitch3-Pro U2 = 88.9 °C.
 Ar2: SR FET Q2 = 82.8 °C.
 Ar3: VBUS FET Q1 = 67.9 °C.
 Ar4: Primary Snubber = 75.2 °C.

15.3 **85 VAC Input 16 V / 3 A**

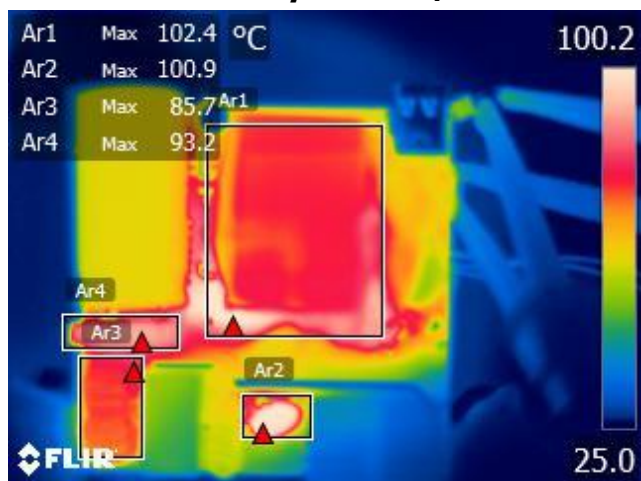


Figure 47 – Top Side Thermal Image.
 Ar1: Transformer T1 = 102.4 °C.
 Ar2: Thermistor RT2 = 100.9 °C.
 Ar3: CMC L1 = 85.7 °C.
 Ar4: Bridge Rectifier BR1 = 93.2 °C.

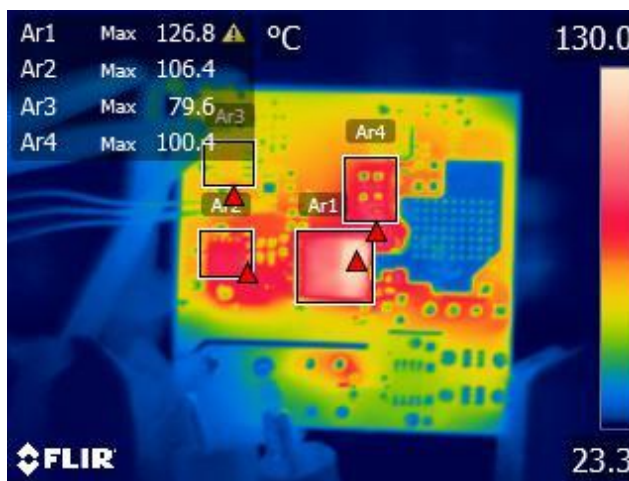


Figure 48 – Bottom Side Thermal Image.
 Ar1: InnoSwitch3-Pro U2 = 126.8 °C.
 Ar2: SR FET Q2 = 106.4 °C.
 Ar3: VBUS FET Q1 = 79.6 °C.
 Ar4: Primary Snubber = 100.4 °C.

15.4 **265 VAC Input 16 V / 3 A**

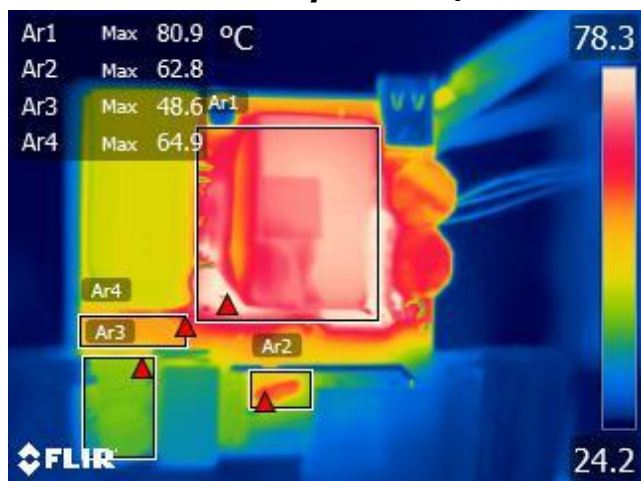


Figure 49 – Top Side Thermal Image.
 Ar1: Transformer T1 = 80.9 °C.
 Ar2: Thermistor RT2 = 62.8 °C.
 Ar3: CMC L1 = 48.6 °C.
 Ar4: Bridge Rectifier BR1 = 64.9 °C.

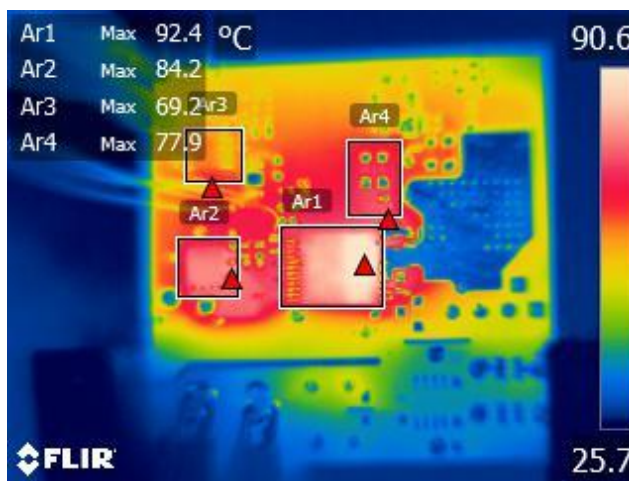


Figure 50 – Bottom Side Thermal Image.
 Ar1: InnoSwitch3-Pro U2 = 92.4 °C.
 Ar2: SR FET Q2 = 84.2 °C.
 Ar3: VBUS FET Q1 = 69.2 °C.
 Ar4: Primary Snubber = 77.9 °C.

15.5 **85 VAC Input 20 V / 2.25 A**

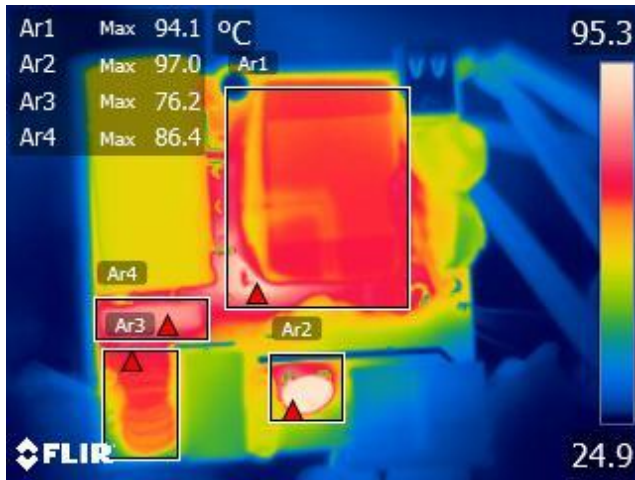


Figure 51 – Top Side Thermal Image.
 Ar1: Transformer T1 = 94.1 °C.
 Ar2: Thermistor RT2 = 97.0 °C.
 Ar3: CMC L1 = 76.2 °C.
 Ar4: Bridge Rectifier BR1 = 86.4 °C.

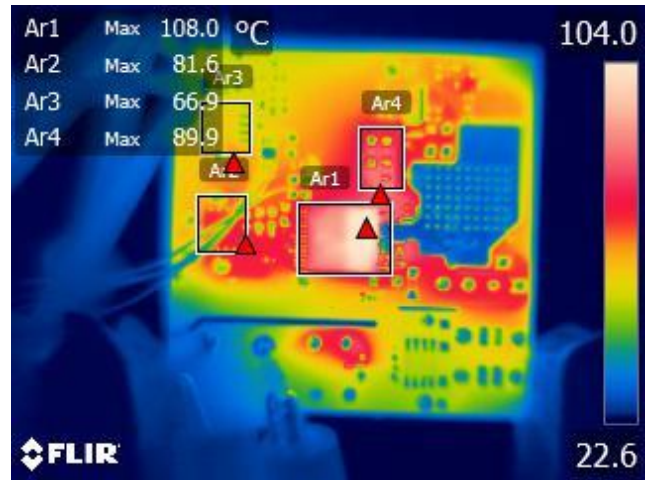


Figure 52 – Bottom Side Thermal Image.
 Ar1: InnoSwitch3-Pro U2 = 108.0 °C.
 Ar2: SR FET Q2 = 81.6 °C.
 Ar3: VBUS FET Q1 = 66.9 °C.
 Ar4: Primary Snubber = 89.9 °C.

15.6 **265 VAC Input 20 V / 2.25 A**

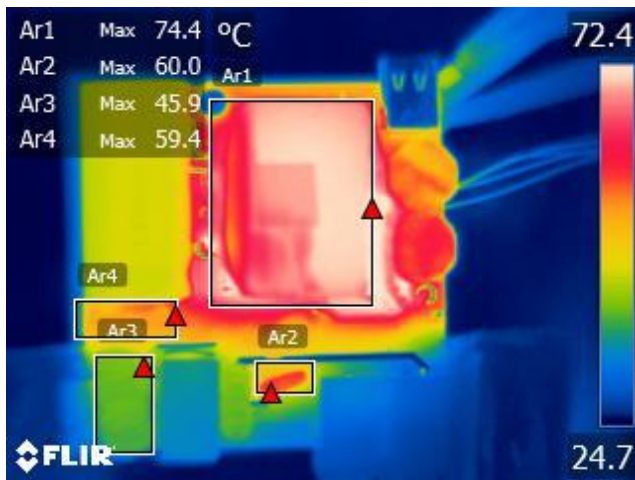


Figure 53 – Top Side Thermal Image.
 Ar1: Transformer T1 = 74.4 °C.
 Ar2: Thermistor RT2 = 60.0 °C.
 Ar3: CMC L1 = 45.9 °C.
 Ar4: Bridge Rectifier BR1 = 59.4 °C.

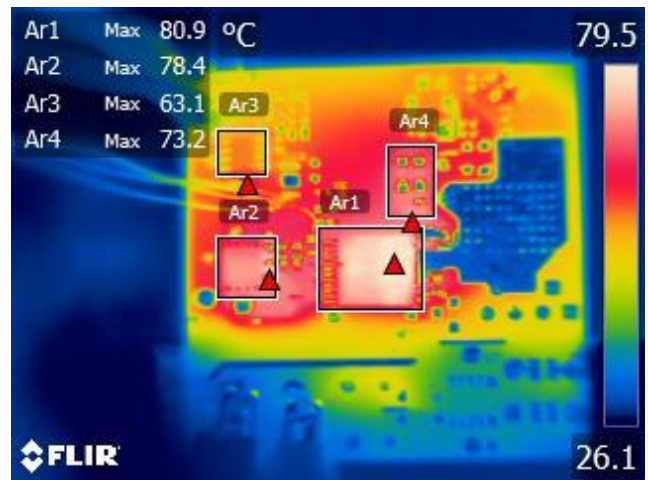


Figure 54 – Bottom Side Thermal Image.
 Ar1: InnoSwitch3-Pro U2 = 80.9 °C.
 Ar2: SR FET Q2 = 78.4 °C.
 Ar3: VBUS FET Q1 = 63.1 °C.
 Ar4: Primary Snubber = 73.2 °C.

16 Thermal Performance with Enclosure

16.1 Room Temperature

16.1.1 85 VAC Input 15 V / 3 A

Ambient	INN3368C (U2)	SR FET (Q2)	VBUS FET (Q1)	Transformer (T1)	Thermistor (RT2)	Bridge (BR1)	Output Capacitor (C4)	CMC (L2)	Bulk Capacitor (C3)
23.3	76.7	76.7	62.5	75	99.2	85.3	68.9	81.5	63.8

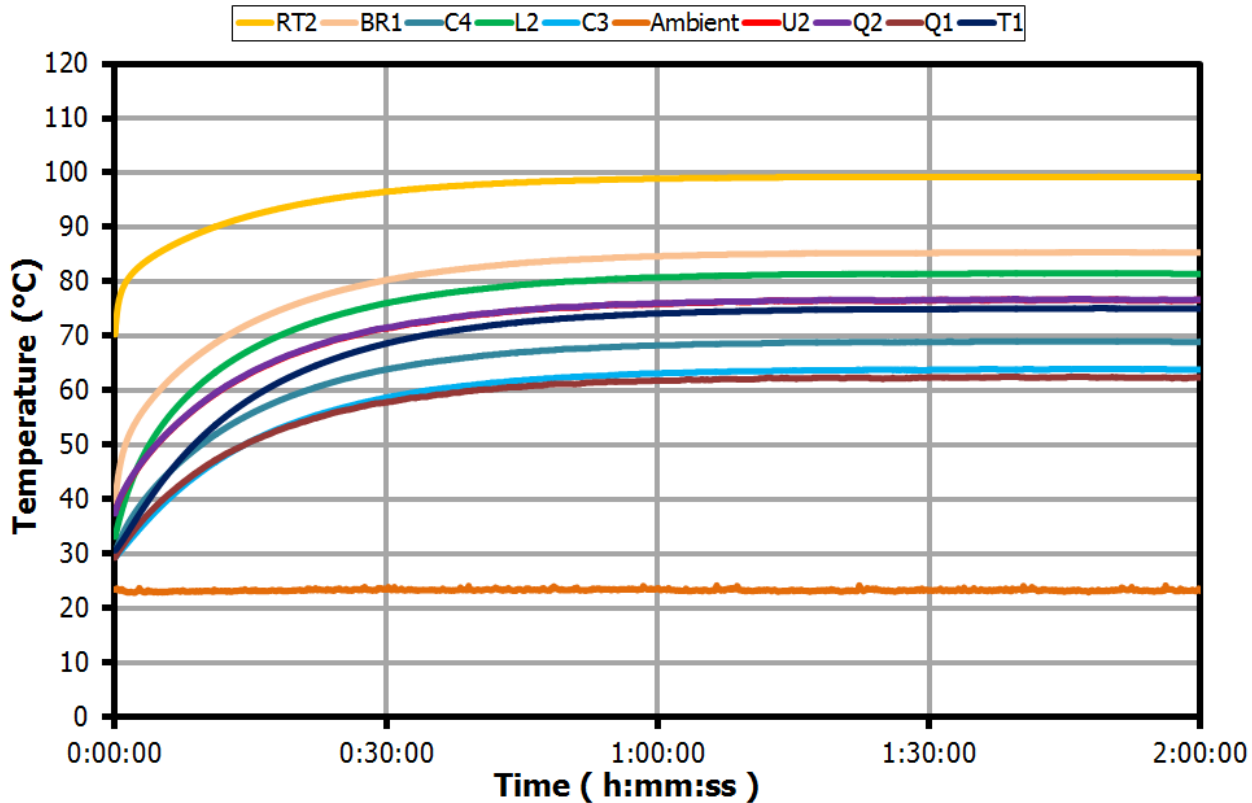


Figure 55 – Temperature vs. Time, at 23 °C Ambient.

16.1.2 265 VAC Input 15 V / 3 A

Ambient	INN3368C (U2)	SR FET (Q2)	VBUS FET (Q1)	Transformer (T1)	Thermistor (RT2)	Bridge (BR1)	Output Capacitor (C4)	CMC (L2))	Bulk Capacitor (C3)
23.4	58.9	61.9	51	64.6	66.5	55.7	56.8	50.5	49.8

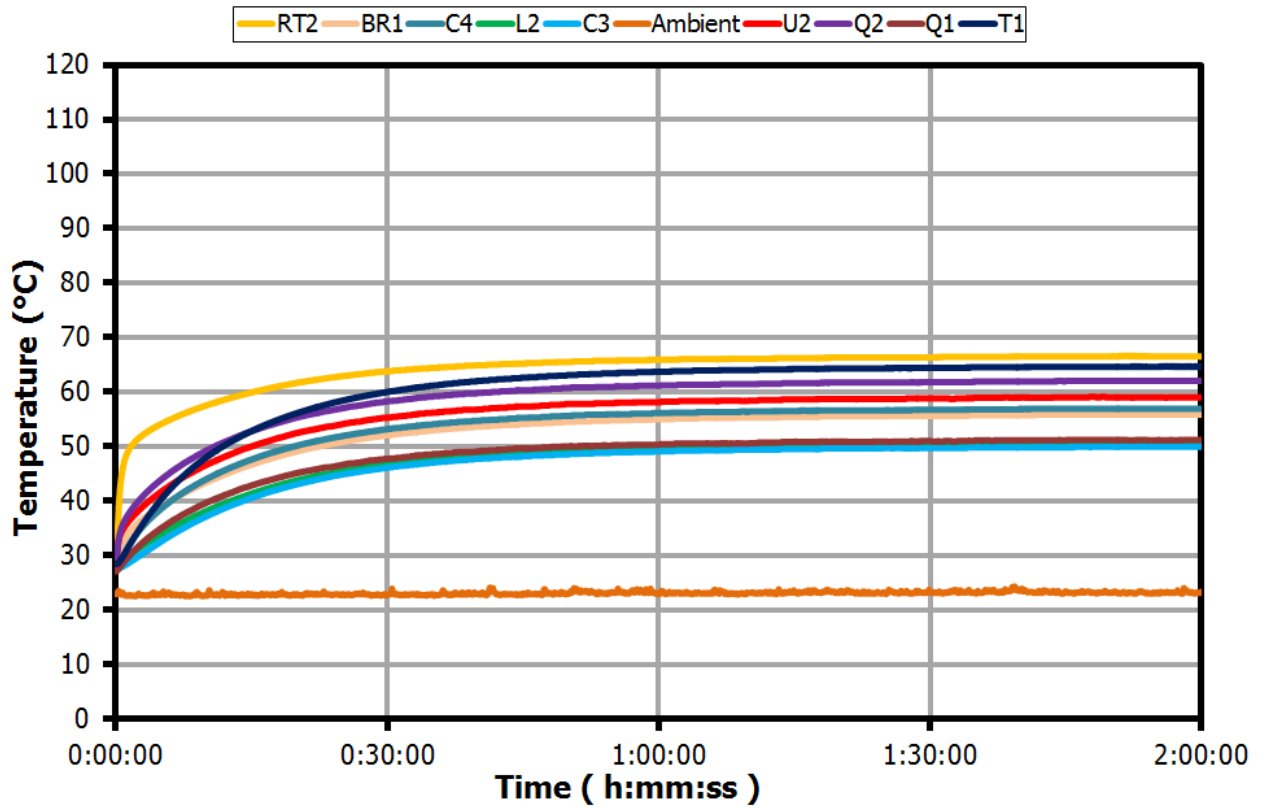


Figure 56 – Temperature vs. Time, at 23 °C Ambient.



16.1.3 85 VAC Input 20 V / 2.25 A

Ambient	INN3368C (U2)	SR FET (Q2)	VBUS FET (Q1)	Transformer (T1)	Thermistor (RT2)	Bridge (BR1)	Output Capacitor (C4)	CMC (L2)	Bulk Capacitor (C3)
25.9	76.1	72.1	61.6	74.6	99	85.5	66.7	82	64.2

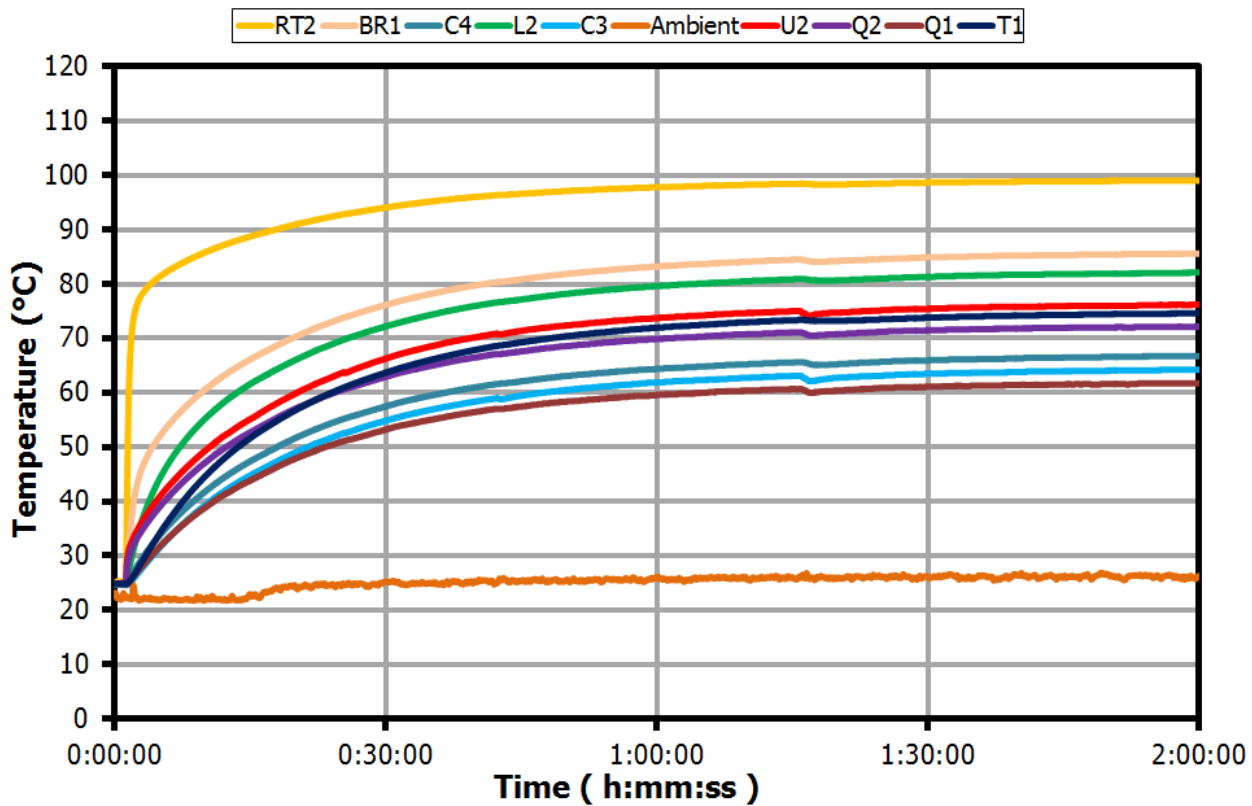


Figure 57 – Temperature vs. Time, at 26 °C Ambient.

16.1.4 265 VAC Input 20 V / 2.25 A

Ambient	INN3368C (U2)	SR FET (Q2)	VBUS FET (Q1)	Transformer (T1)	Thermistor (RT2)	Bridge (BR1)	Output Capacitor (C4)	CMC (L2)	Bulk Capacitor (C3)
24.1	59.7	61.3	51.7	65.8	67.5	57	57	51.9	51.1

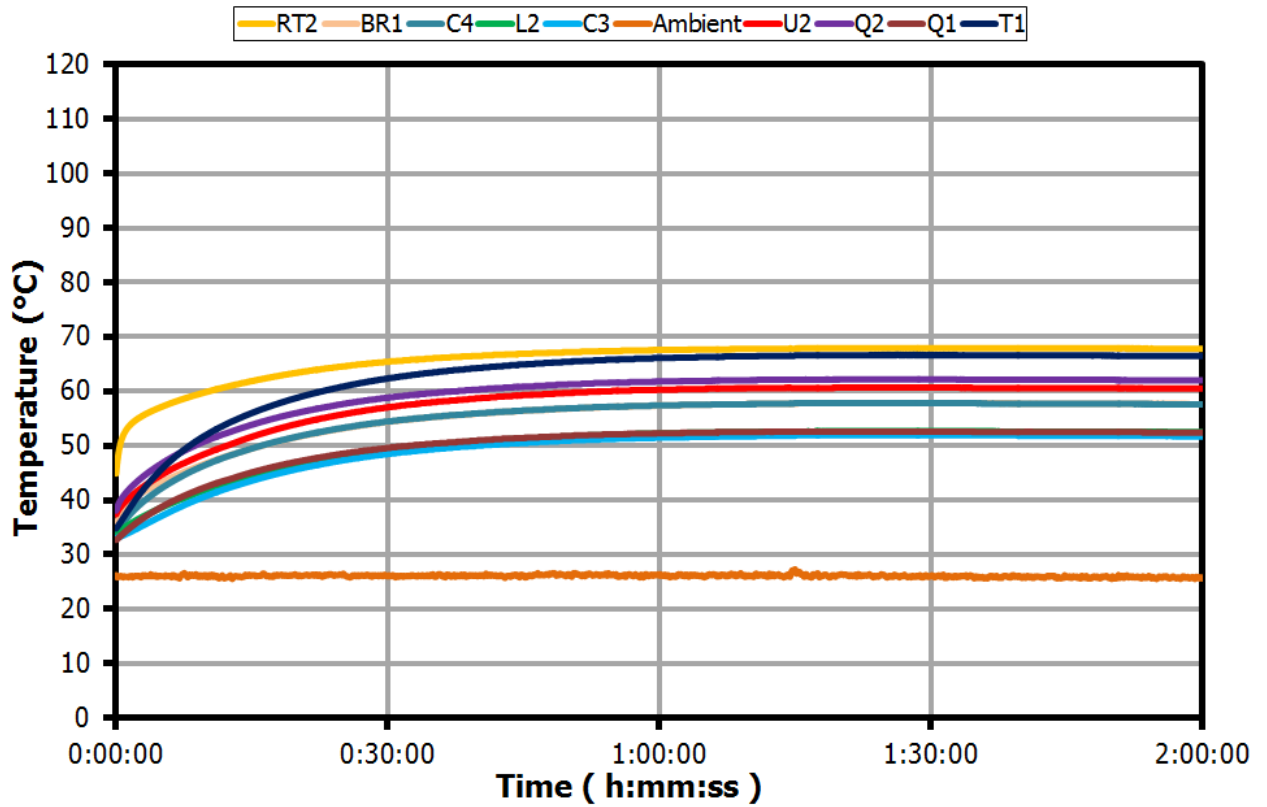


Figure 58 – Temperature vs. Time, at 24 °C Ambient.



16.2 High Temperature

16.2.1 85 VAC Input 15 V / 3 A

Ambient	INN3368C (U2)	SR FET (Q2)	VBUS FET (Q1)	Transformer (T1)	Thermistor (RT2)	Bridge (BR1)	Output Capacitor (C4)	CMC (L2)	Bulk Capacitor (C3)
47.2	81.1	82	67.4	81	103.3	91.3	75.2	88	70.7

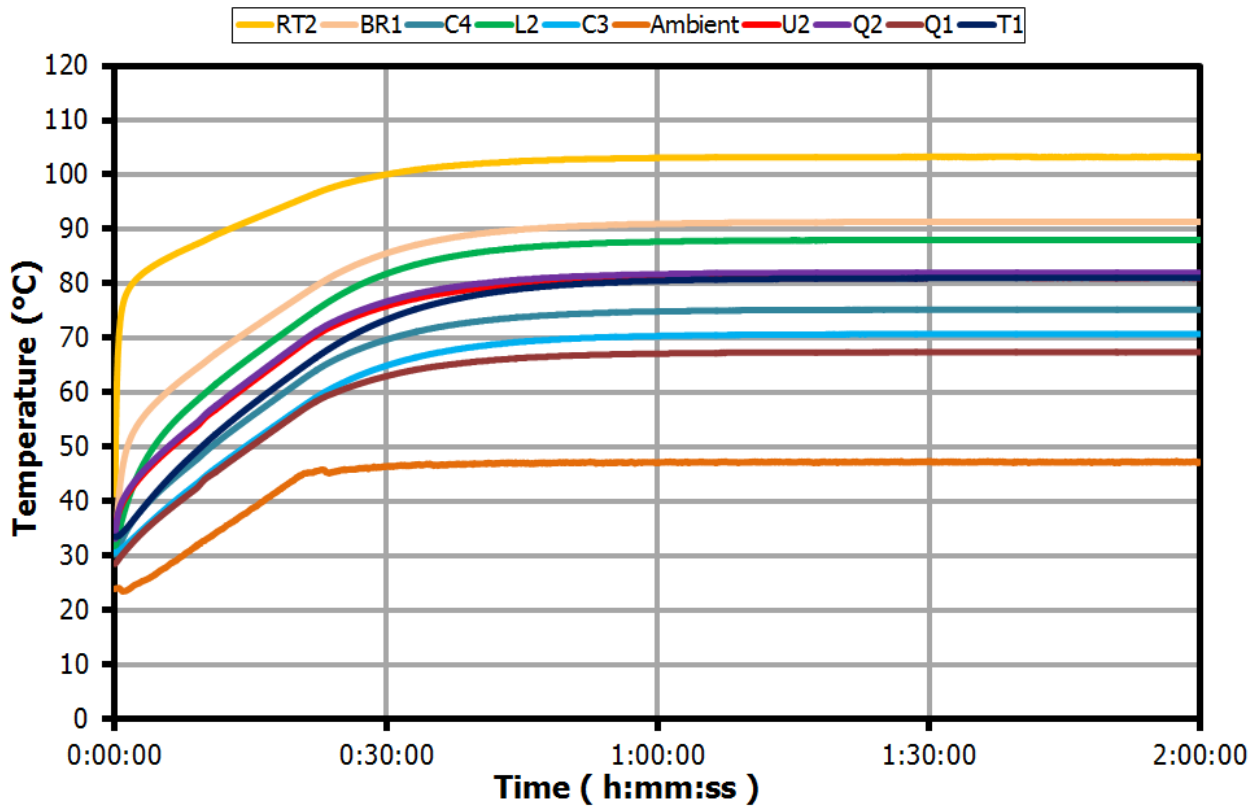


Figure 59 – Temperature vs. Time, at 47 °C Ambient.

16.2.2 85 VAC Input 16 V / 3 A

Ambient	INN3368C (U2)	SR FET (Q2)	VBUS FET (Q1)	Transformer (T1)	Thermistor (RT2)	Bridge (BR1)	Output Capacitor (C4)	CMC (L2)	Bulk Capacitor (C3)
40.8	83.8	84.6	67.8	84.2	106.6	95.3	77.2	92.7	72.6

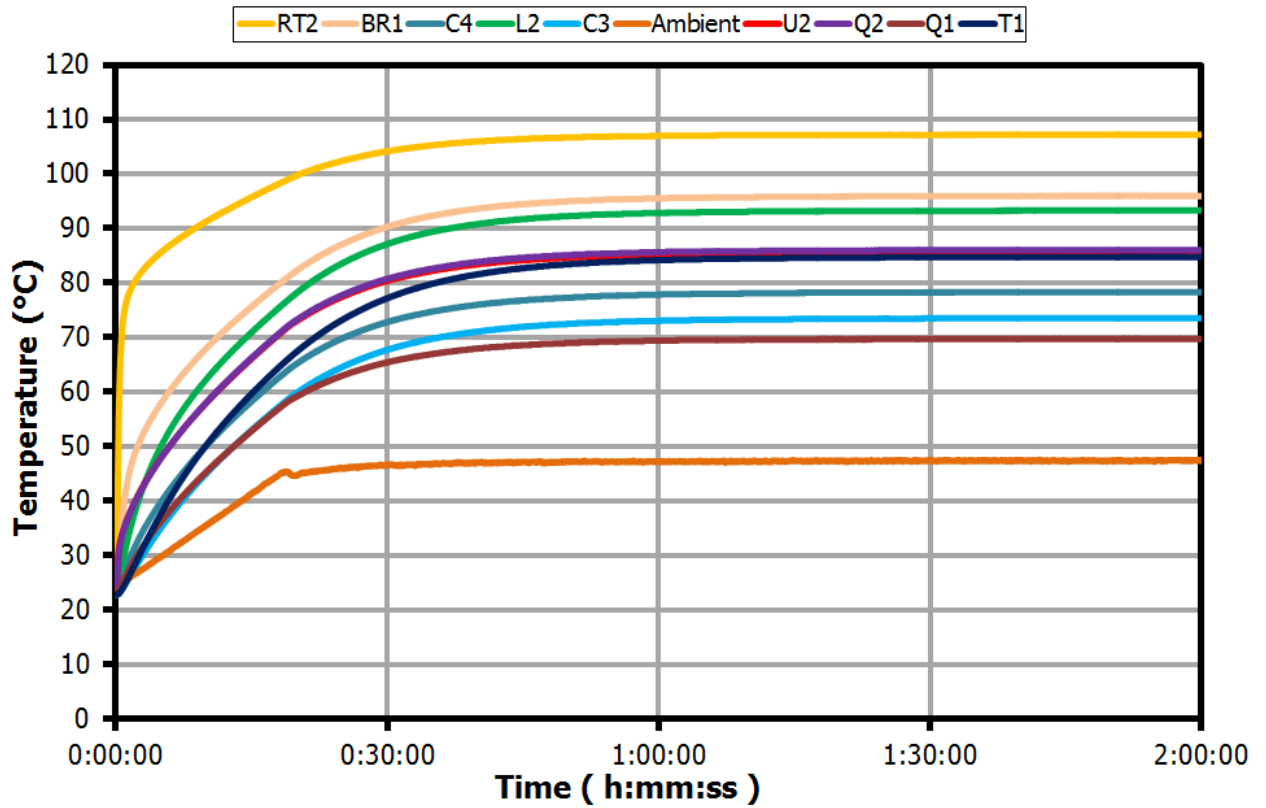


Figure 60 – Temperature vs. Time, at 41 °C Ambient.



16.2.3 85 VAC Input 20 V / 2.25 A

Ambient	INN3368C (U2)	SR FET (Q2)	VBUS FET (Q1)	Transformer (T1)	Thermistor (RT2)	Bridge (BR1)	Output Capacitor (C4)	CMC (L2)	Bulk Capacitor (C3)
46.5	78.8	75.7	64.9	78.8	102	89.8	71.1	86.5	69.1

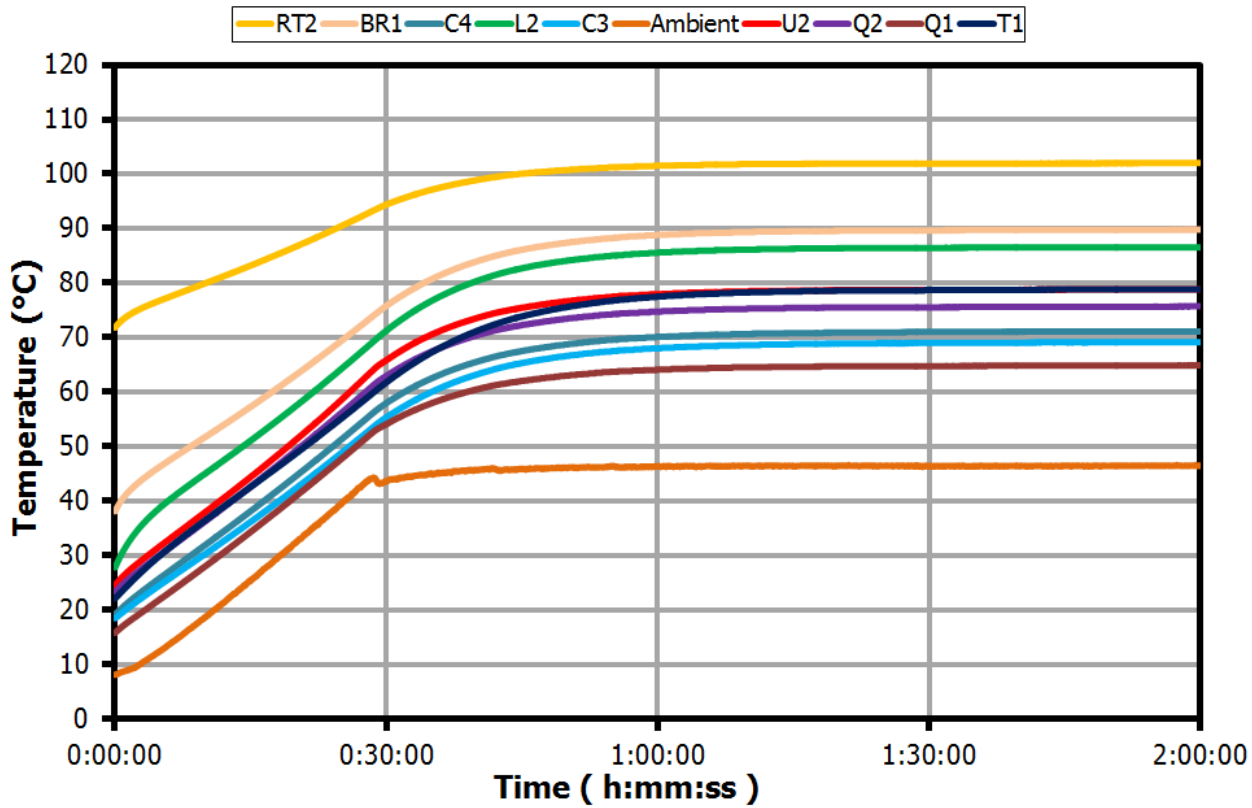


Figure 61 – Temperature vs. Time, at 46 °C Ambient.

17 Output Voltage Ripple Measurements

17.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF /50 V ceramic type and one (1) 47 μF /50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

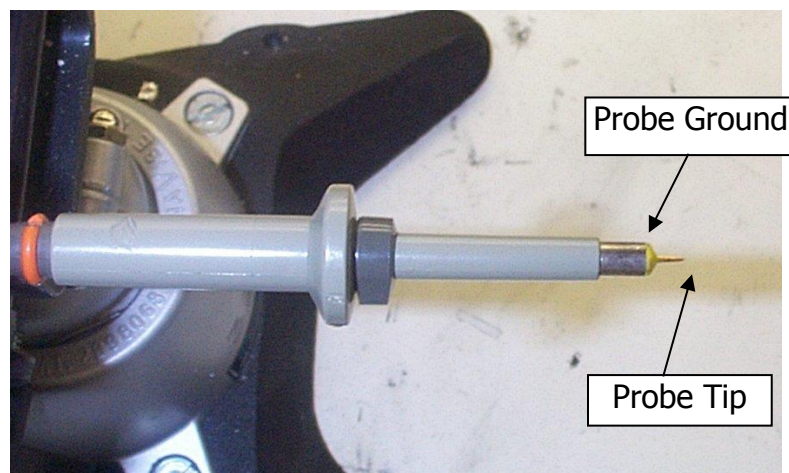


Figure 62 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



Figure 63 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

17.2 Output Voltage Ripple Waveforms

Note: Measurements are taken at the end of 100 mΩ cable

17.2.1 Output: 3.3 V / 5 A

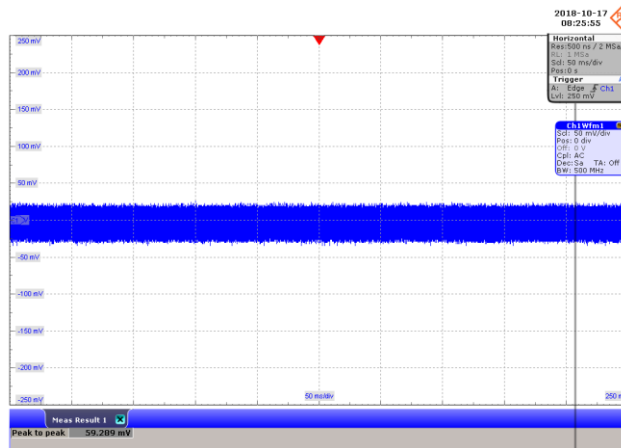
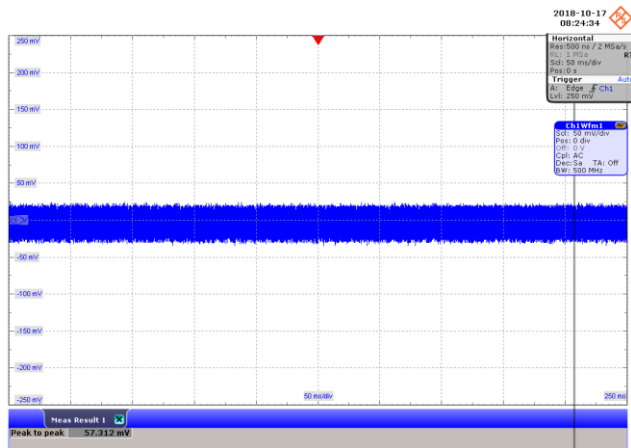


Figure 64 – Output Ripple (57 mV_{PK-PK}).
85 VAC Input 3.3 V, 5 A Load.
V_{OUT}, 50 mV / div., 50 ms / div.

Figure 65 – Output Ripple (59 mV_{PK-PK}).
265 VAC Input 3.3 V, 5 A Load.
V_{OUT}, 50 mV / div., 50 ms / div.

17.2.2 Output: 5 V / 5 A

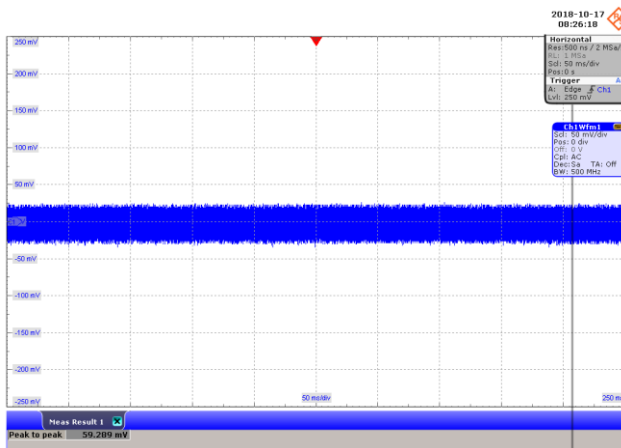
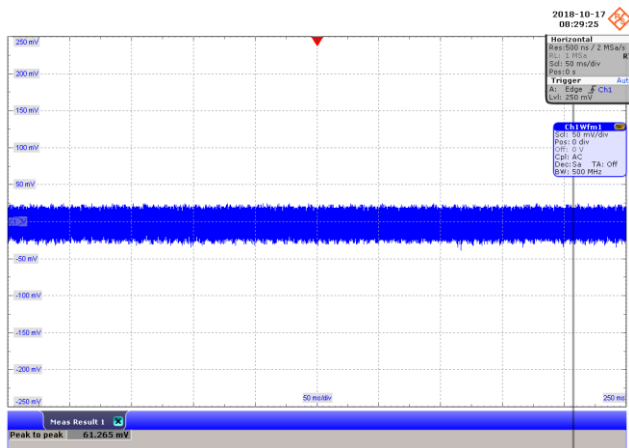


Figure 66 – Output Ripple (61 mV_{PK-PK}).
85 VAC Input 5.0 V, 5 A Load.
V_{OUT}, 50 mV / div., 50 ms / div.

Figure 67 – Output Ripple (59 mV_{PK-PK}).
265 VAC Input 5.0 V, 5 A Load.
V_{OUT}, 50 mV / div., 50 ms / div.



17.2.3 Output: 9 V / 3 A

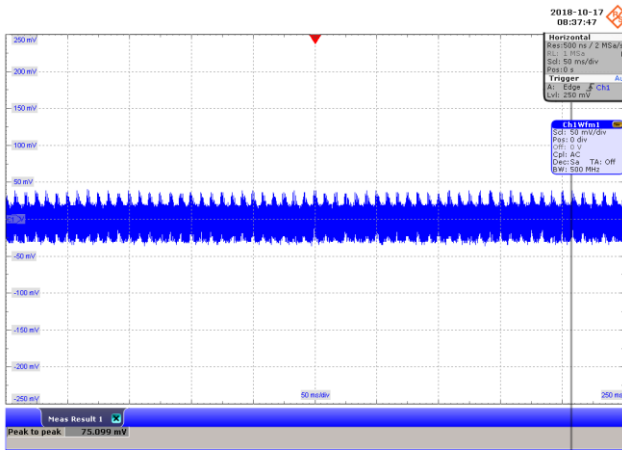


Figure 68 – Output Ripple (75 mV_{PK-PK}).
85 VAC Input 9.0 V, 3 A Load.
V_{OUT}, 50 mV / div., 50 ms / div.

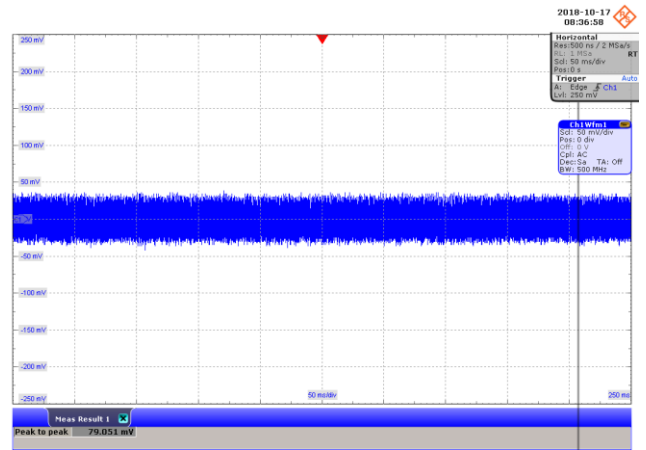


Figure 69 – Output Ripple (79 mV_{PK-PK}).
265 VAC Input 9.0 V, 3 A Load.
V_{OUT}, 50 mV / div., 50 ms / div.

17.2.4 Output: 15 V / 3 A

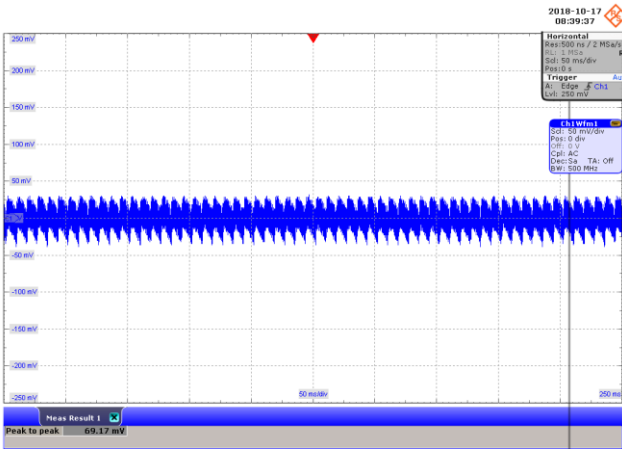


Figure 70 – Output Ripple (69 mV_{PK-PK}).
85 VAC Input 15.0 V, 3 A Load.
V_{OUT}, 50 mV / div., 50 ms / div.

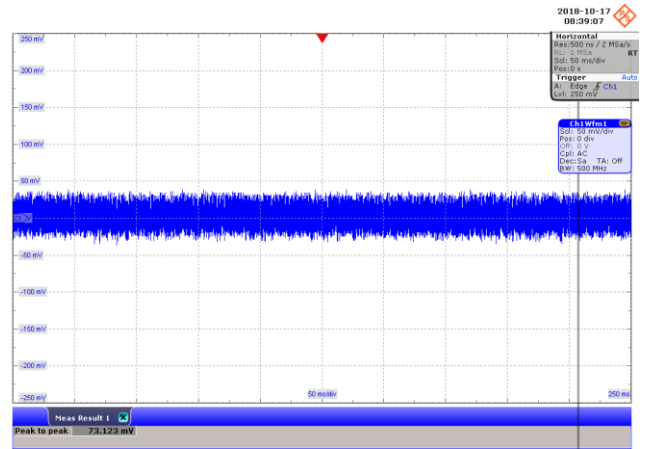


Figure 71 – Output Ripple (73 mV_{PK-PK}).
265 VAC Input 15.0 V, 3 A Load.
V_{OUT}, 50 mV / div., 50 ms / div.



17.2.5 Output: 16 V / 3 A

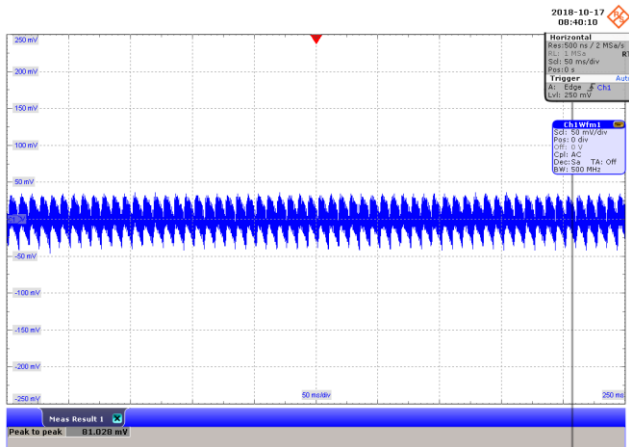


Figure 72 – Output Ripple (81 mV_{PK-PK}).
85 VAC Input 16.0 V, 3 A Load.
V_{OUT}, 50 mV / div., 50 ns / div.

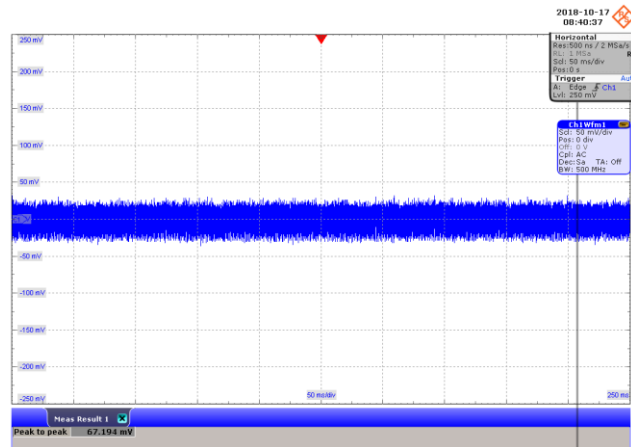


Figure 73 – Output Ripple (67 mV_{PK-PK}).
265 VAC Input 16.0 V, 3 A Load.
V_{OUT}, 50 mV / div., 50 ns / div.

17.2.6 Output: 20V / 2.25 A

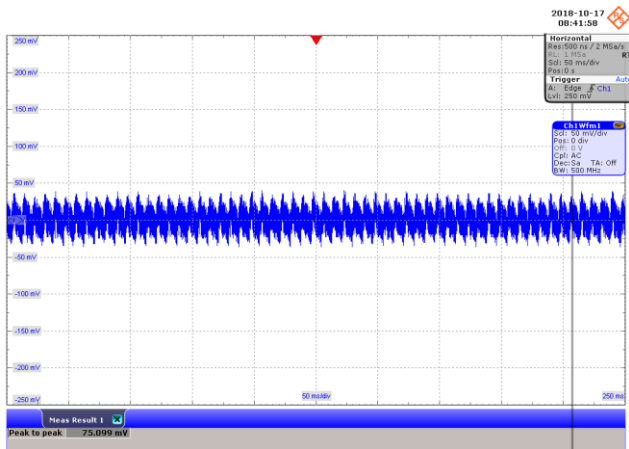


Figure 74 – Output Ripple (75 mV_{PK-PK}).
265 VAC Input 20.0 V, 2.25 A Load.
V_{OUT}, 50 mV / div., 50 ns / div.

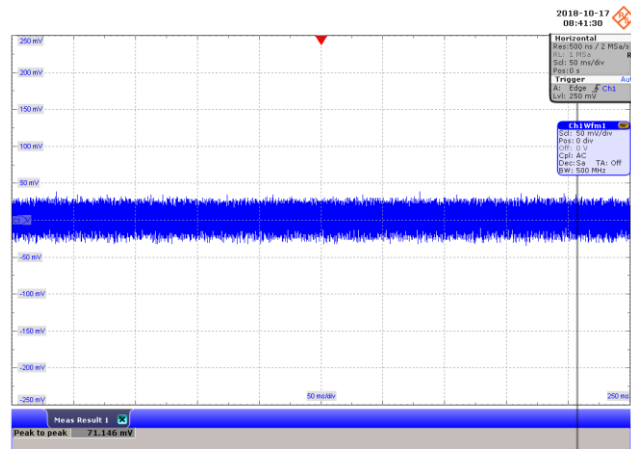


Figure 75 – Output Ripple (71 mV_{PK-PK}).
265 VAC Input 20.0 V, 2.25 A Load.
V_{OUT}, 50 mV / div., 50 ns / div.

17.2.7 Output: 21V / 2.25 A

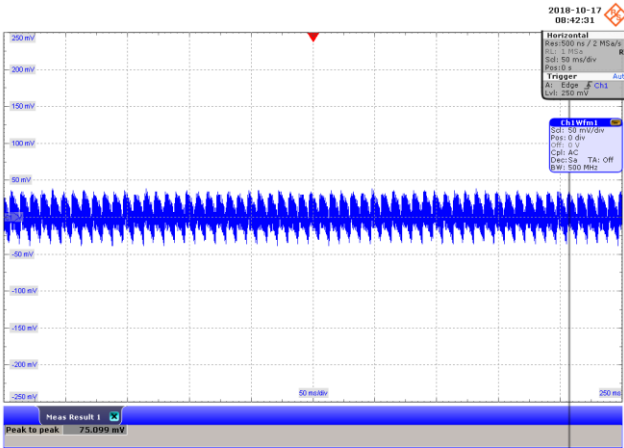


Figure 76 – Output Ripple (75 mV_{PK-PK}).
 265 VAC Input 21.0 V, 2.25 A Load.
 V_{OUT}, 50 mV / div., 50 ms / div.

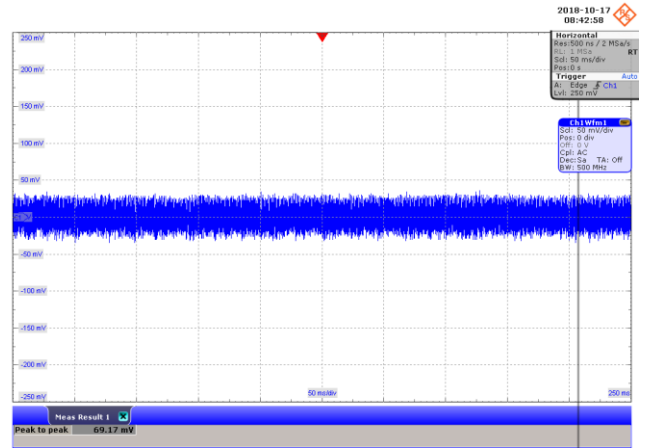


Figure 77 – Output Ripple (69 mV_{PK-PK}).
 265 VAC Input 21.0 V, 2.25 A Load.
 V_{OUT}, 50 mV / div., 50 ms / div.



17.3 Output Voltage Ripple Amplitude vs. Load

17.3.1 Output: 3.3 V / 5 A

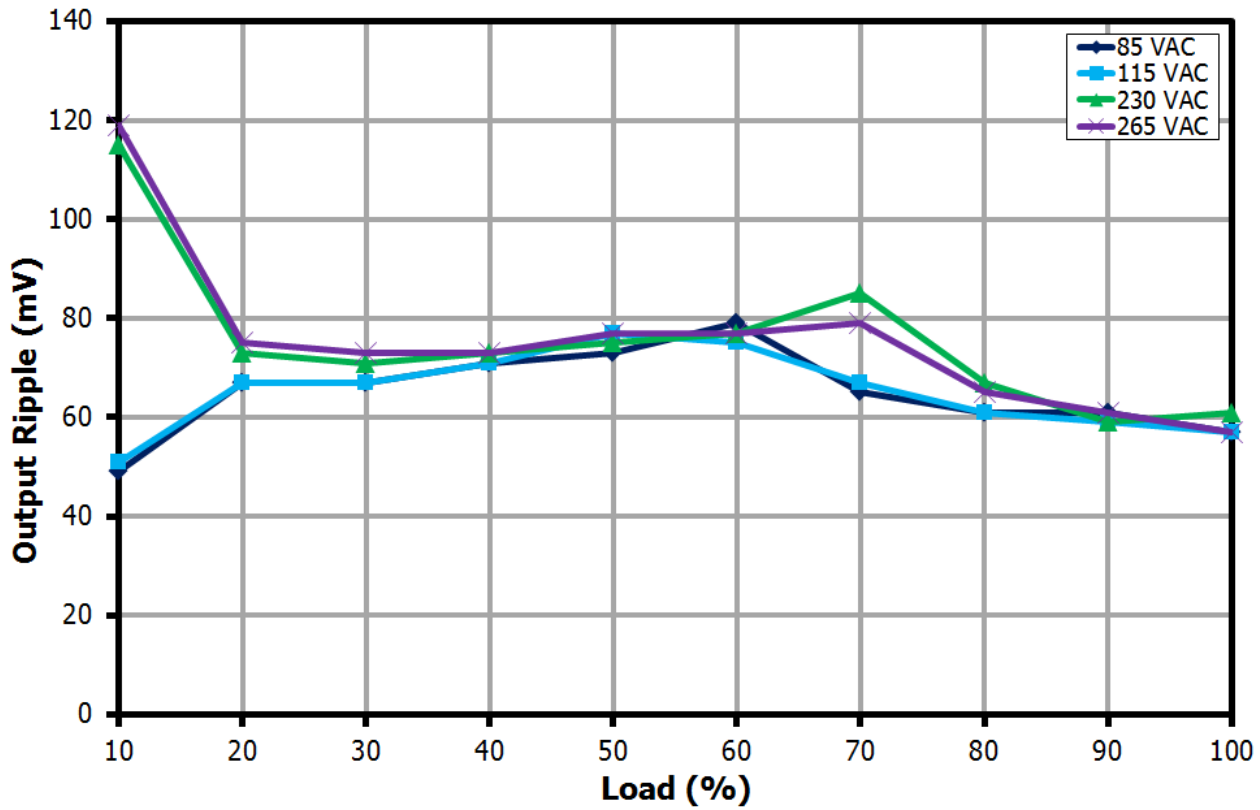


Figure 78 – 3.3 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

17.3.2 Output: 5 V / 5 A

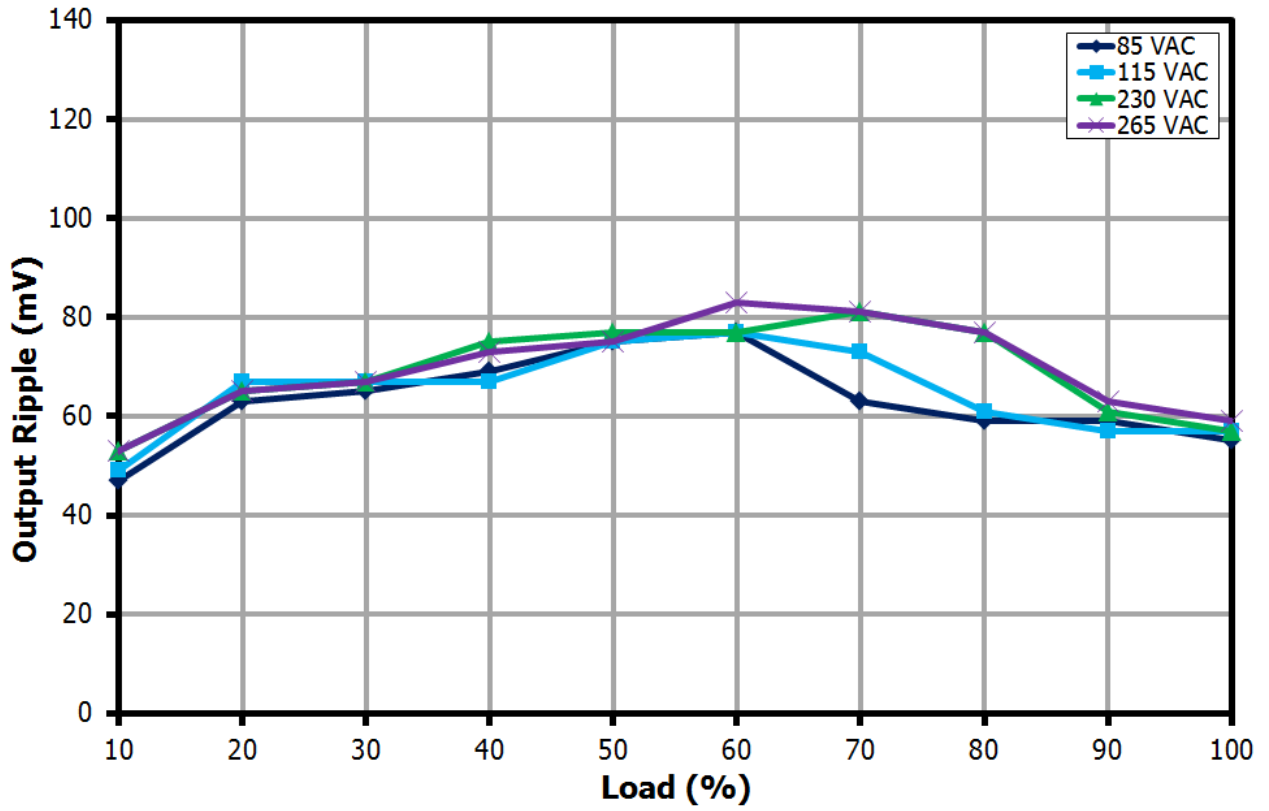


Figure 79 – 5 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.



17.3.3 Output: 9 V / 3 A

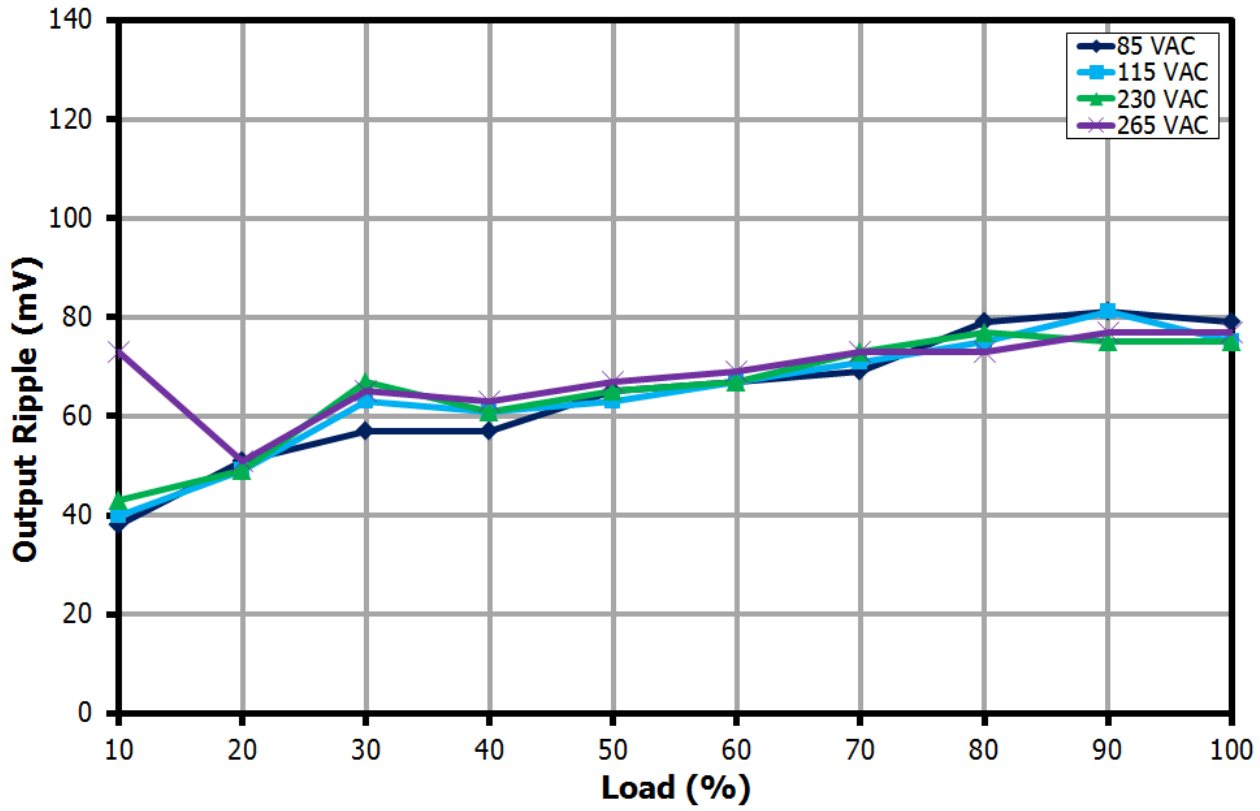


Figure 80 – 9 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

17.3.4 Output: 15 V / 3 A

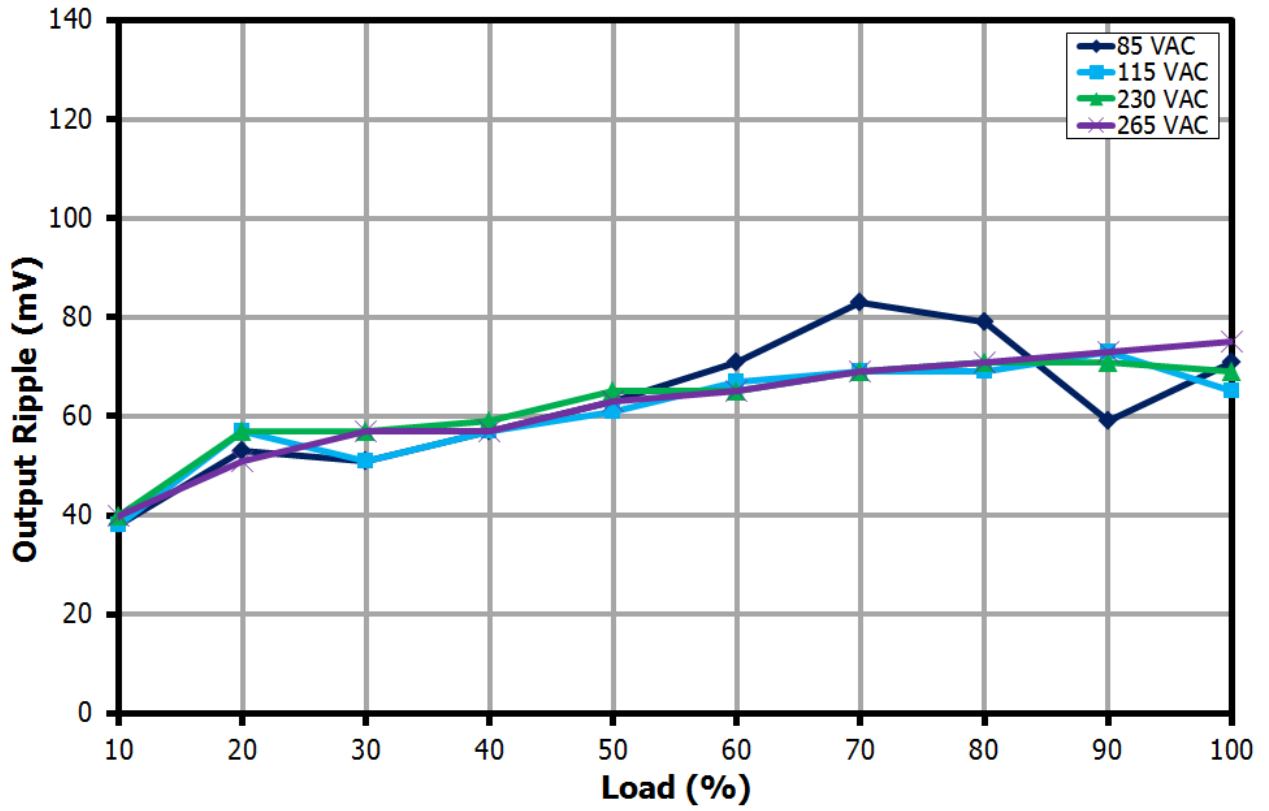


Figure 81 – 15 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.



17.3.5 Output: 16 V / 3 A

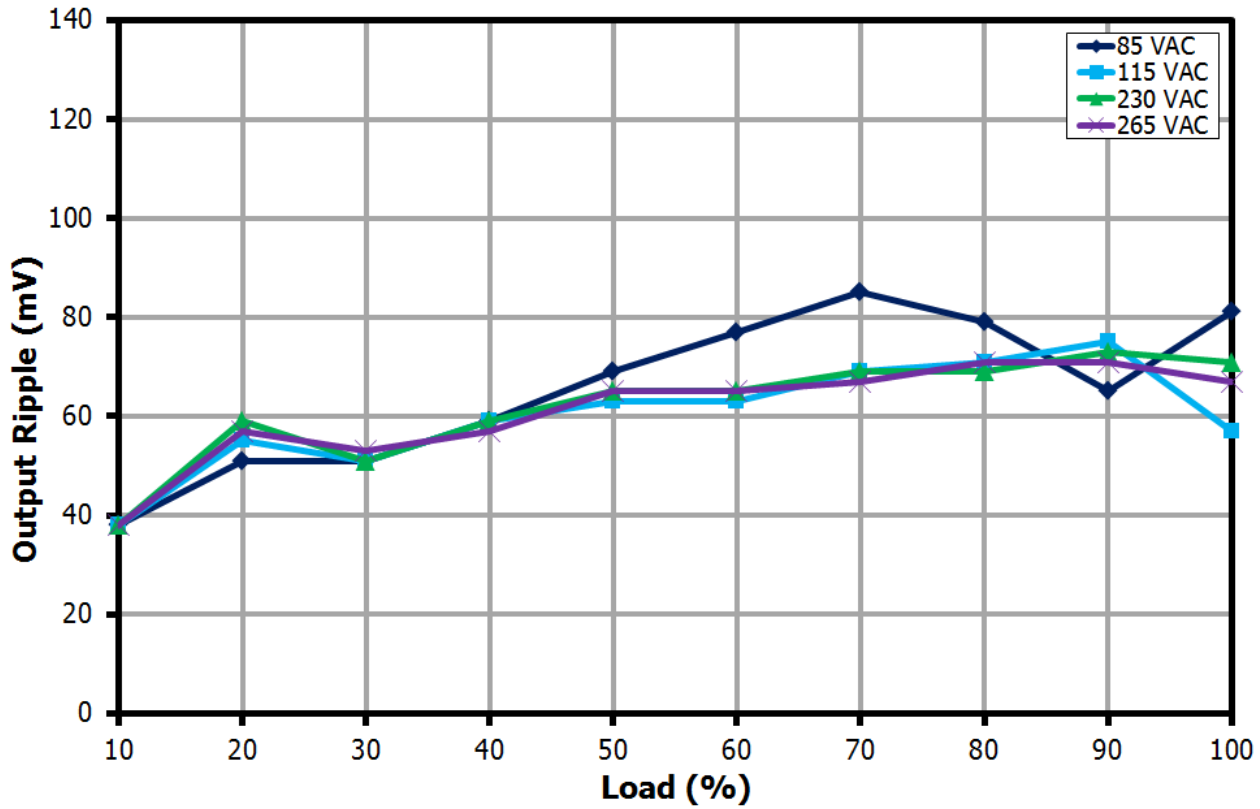


Figure 82 – 16 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

17.3.6 Output: 20 V / 2.25 A

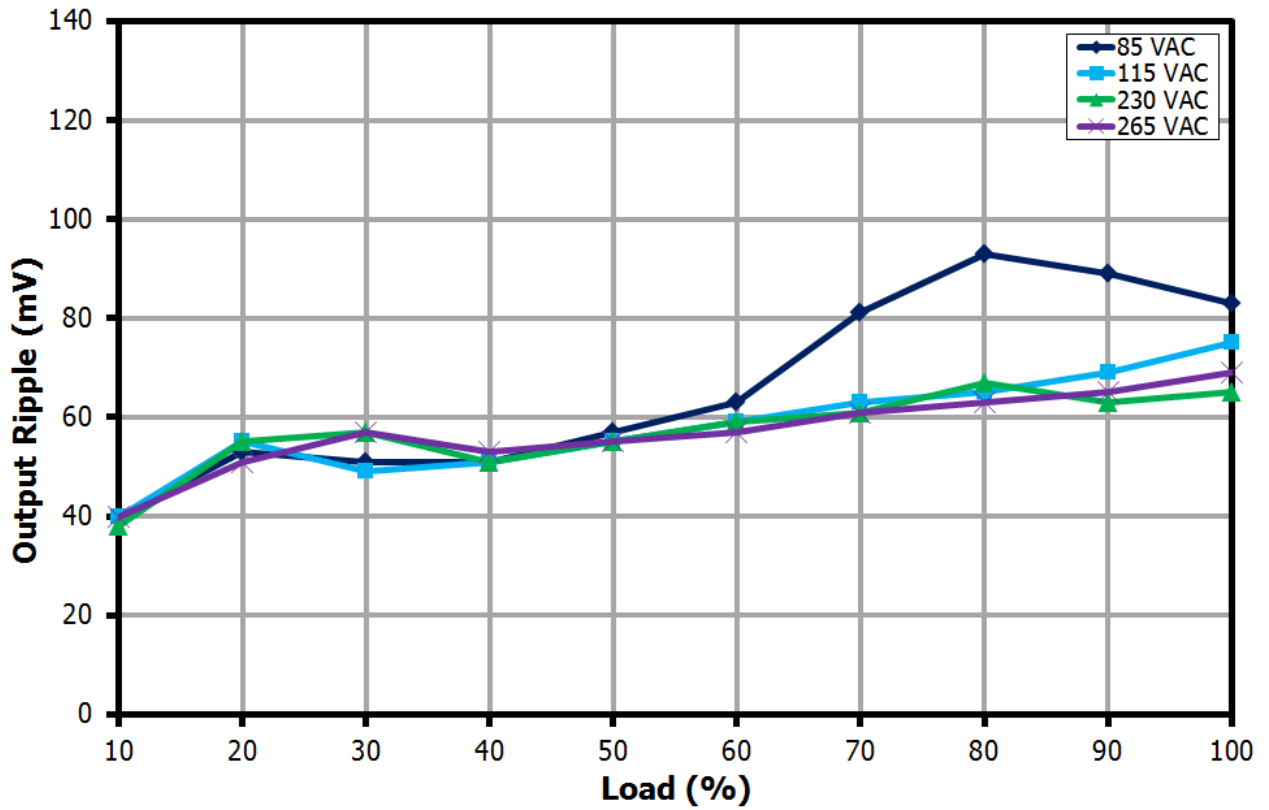


Figure 83 – 20 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.



17.3.7 Output: 21 V / 2.25 A

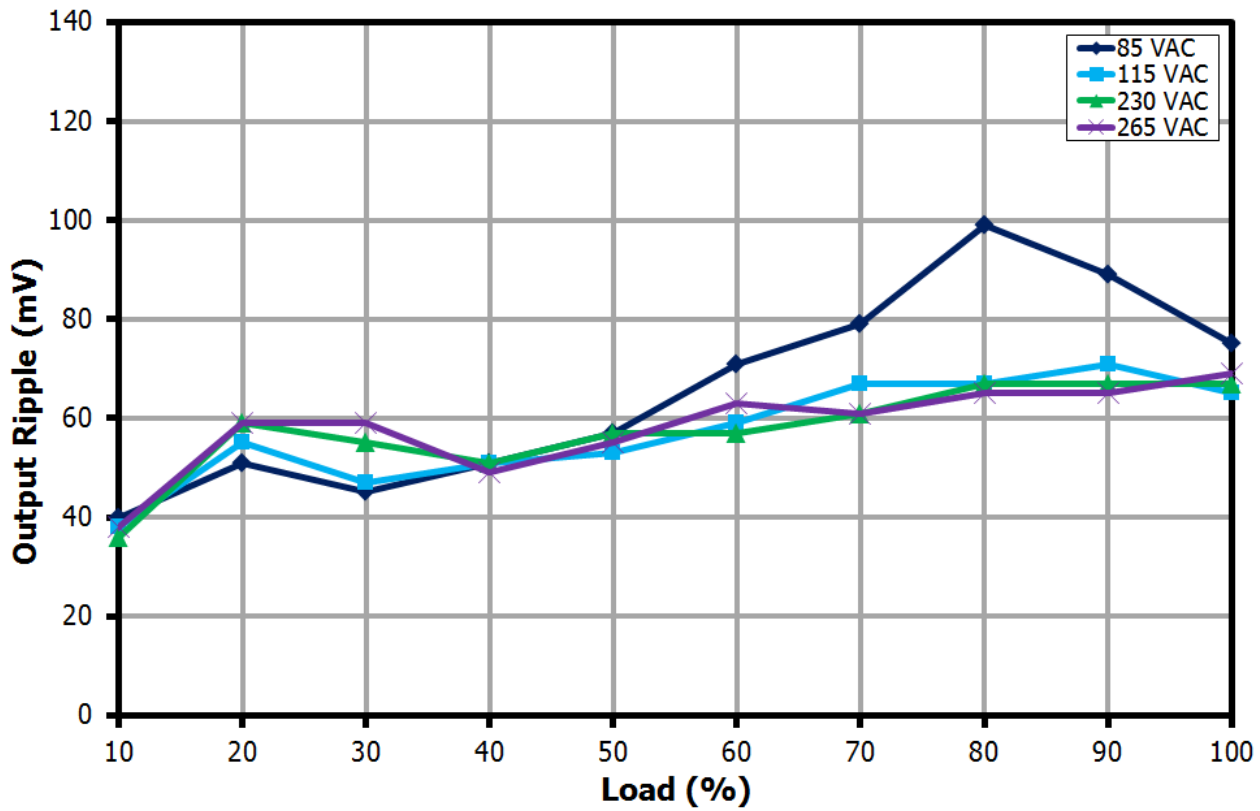


Figure 84 – 21 V Output Peak-to-Peak Ripple Amplitude vs. Percent Load.

18 Waveforms

18.1 Transient Response (On the Board)

18.1.1 Output: 3.3 V

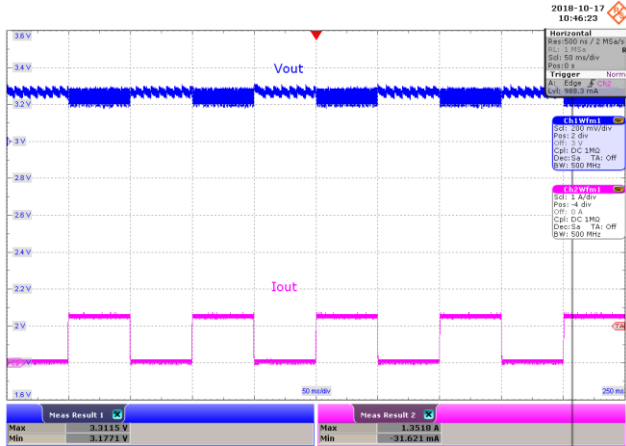


Figure 85 – Dynamic Load Response.
 85 VAC, 3.3 V, 0 – 1.25 A Load Step.
 V_{MAX} : 3.31 V, V_{MIN} : 3.17 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

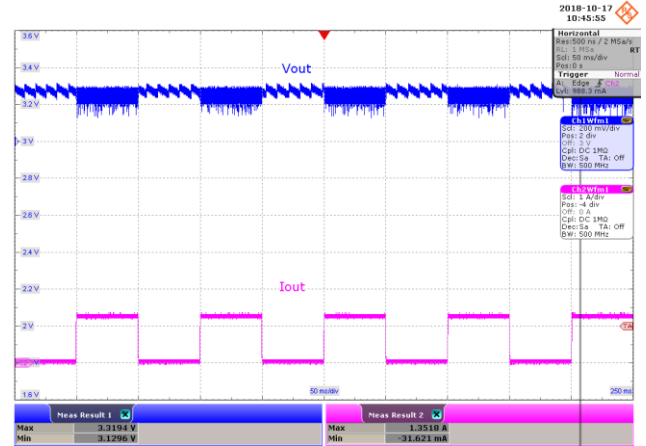


Figure 86 – Dynamic Load Response.
 265 VAC, 3.3 V, 0 – 1.25 A Load Step.
 V_{MAX} : 3.31 V, V_{MIN} : 3.12 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

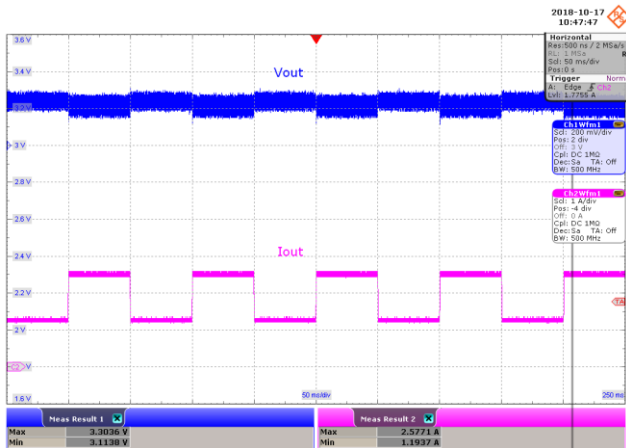


Figure 87 – Dynamic Load Response.
 85 VAC, 3.3 V, 1.25 – 2.5 A Load Step.
 V_{MAX} : 3.30 V, V_{MIN} : 3.11 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

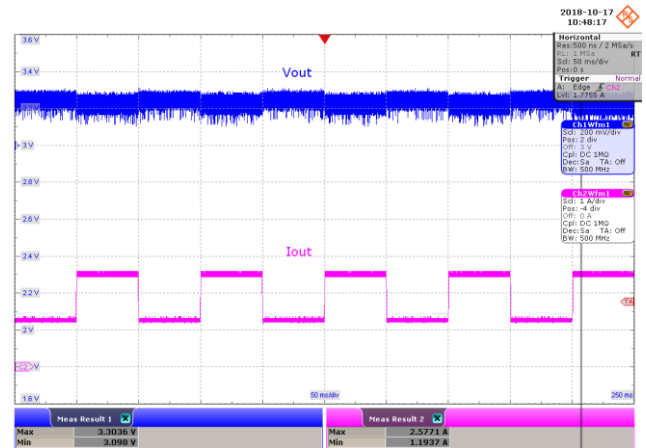


Figure 88 – Dynamic Load Response.
 265 VAC, 3.3 V, 1.25 – 2.5 A Load Step.
 V_{MAX} : 3.30 V, V_{MIN} : 3.09 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.





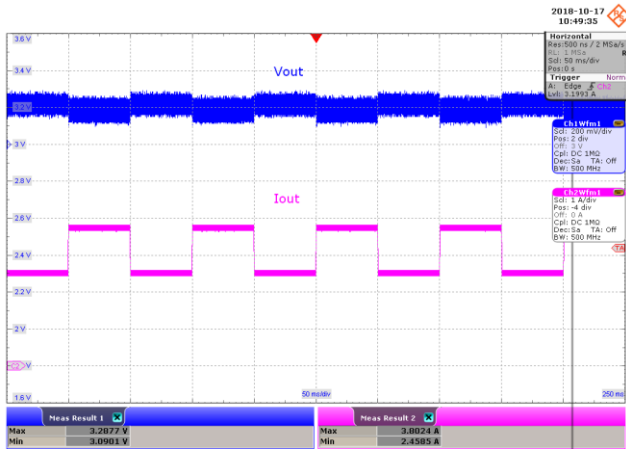


Figure 89 – Dynamic Load Response.
 85 VAC, 3.3 V, 2.5 – 3.75 A Load Step.
 V_{MAX} : 3.28 V, V_{MIN} : 3.09 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

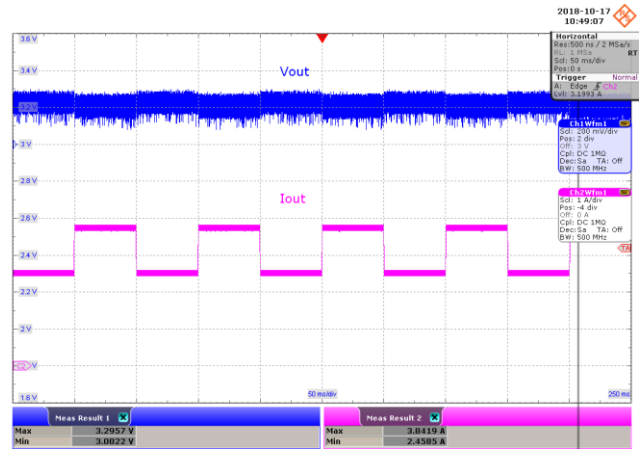


Figure 90 – Dynamic Load Response.
 265 VAC, 3.3 V, 2.5 – 3.75 A Load Step.
 V_{MAX} : 3.29 V, V_{MIN} : 3.08 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

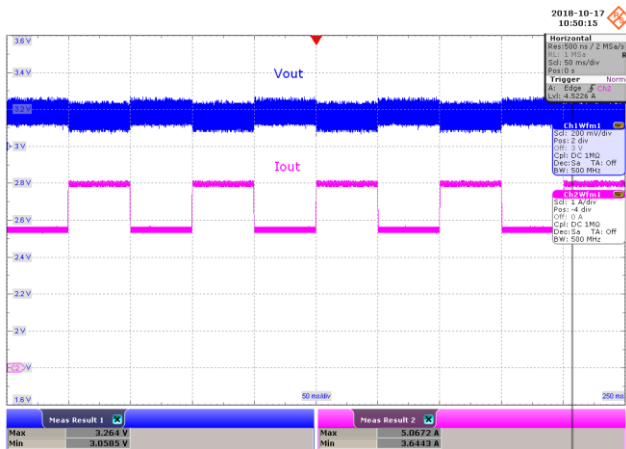


Figure 91 – Dynamic Load Response.
 85 VAC, 3.3 V, 3.75 – 5 A Load Step.
 V_{MAX} : 3.26 V, V_{MIN} : 3.05 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

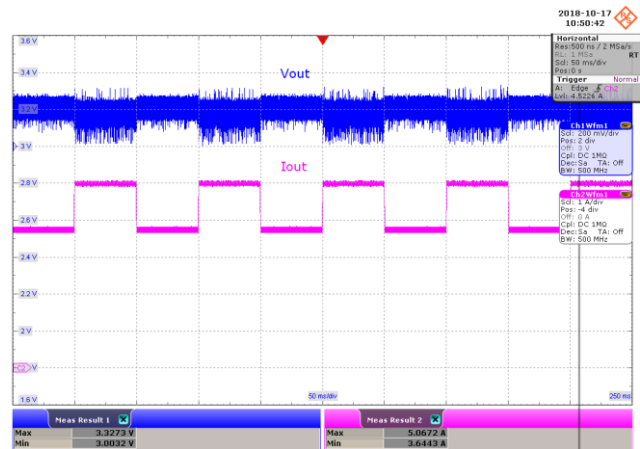


Figure 92 – Dynamic Load Response.
 265 VAC, 3.3 V, 3.75 – 5 A Load Step.
 V_{MAX} : 3.32 V, V_{MIN} : 3.00 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.



18.1.2 Output: 5 V

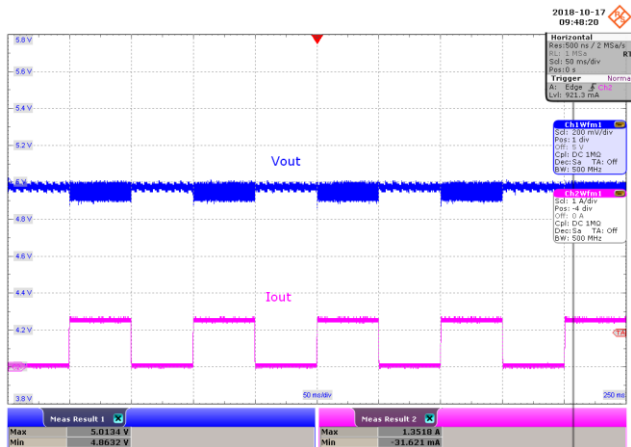


Figure 93 – Dynamic Load Response.
 85 VAC, 5 V, 0 – 1.25 A Load Step.
 V_{MAX} : 5.01 V, V_{MIN} : 4.86 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

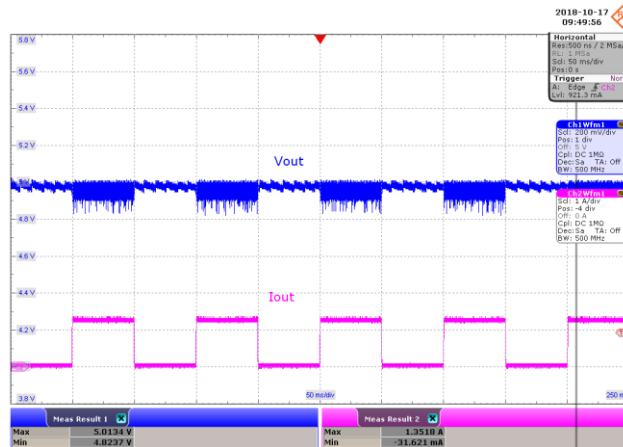


Figure 94 – Dynamic Load Response.
 265 VAC, 5 V, 0 – 1.25 A Load Step.
 V_{MAX} : 5.01 V, V_{MIN} : 4.82 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

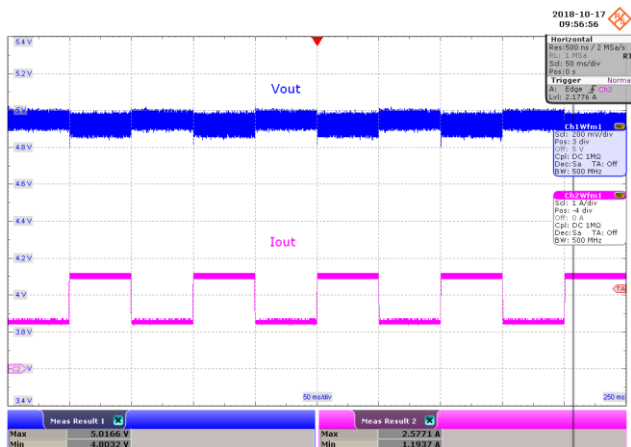


Figure 95 – Dynamic Load Response.
 85 VAC, 5 V, 1.25 – 2.5 A Load Step.
 V_{MAX} : 5.01 V, V_{MIN} : 4.80 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

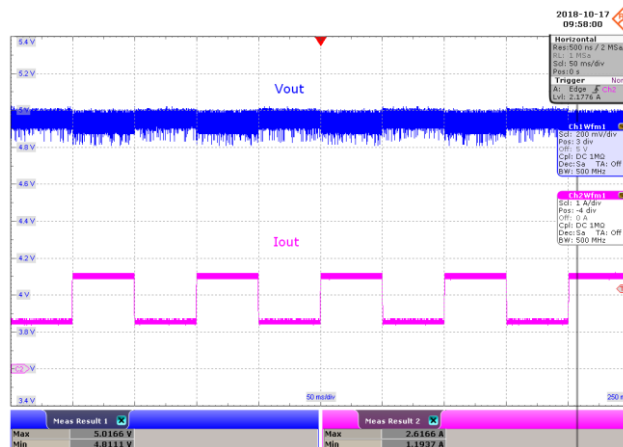


Figure 96 – Dynamic Load Response.
 265 VAC, 5 V, 1.25 – 2.5 A Load Step.
 V_{MAX} : 5.01 V, V_{MIN} : 4.81 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

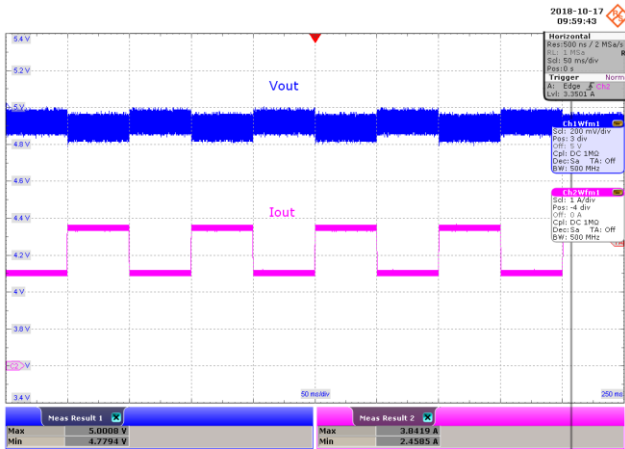


Figure 97 – Dynamic Load Response.
 85 VAC, 5 V, 2.5 – 3.75 A Load Step.
 V_{MAX} : 5.00 V, V_{MIN} : 4.77 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

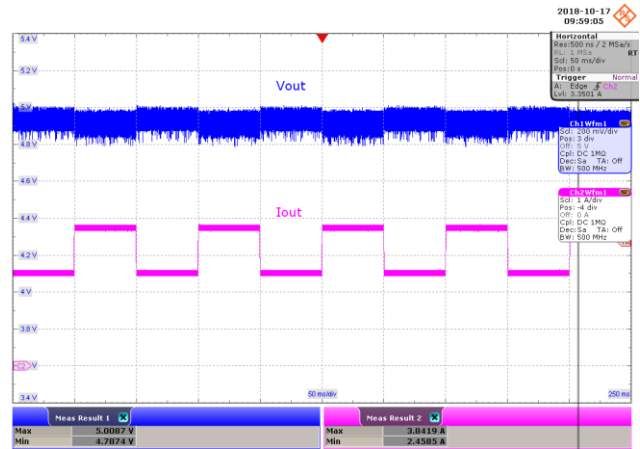


Figure 98 – Dynamic Load Response.
 265 VAC, 5 V, 2.5 – 3.75 A Load Step.
 V_{MAX} : 5.00 V, V_{MIN} : 4.78 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

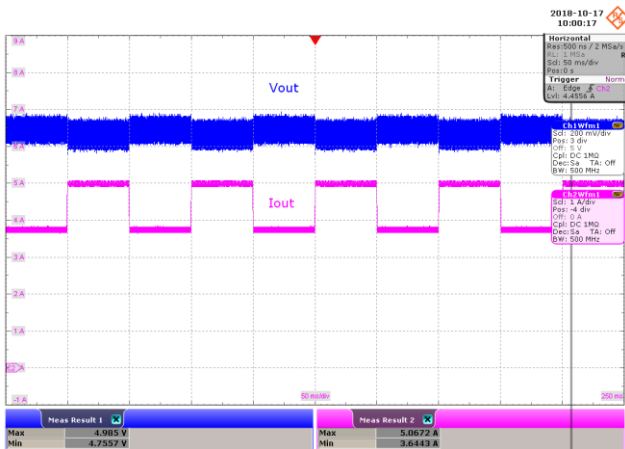


Figure 99 – Dynamic Load Response.
 85 VAC, 5 V, 3.75 – 5 A Load Step.
 V_{MAX} : 4.98 V, V_{MIN} : 4.75 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

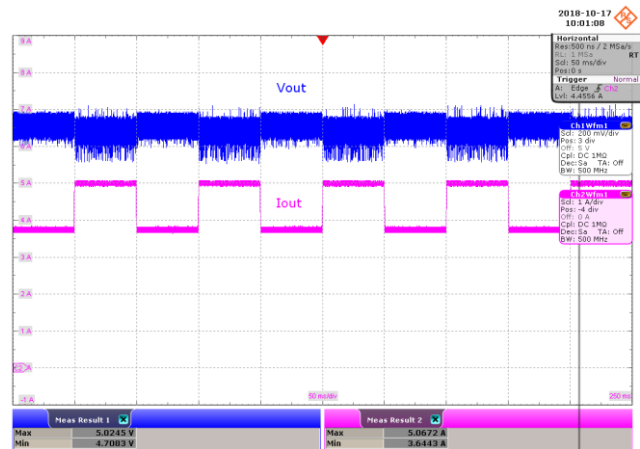


Figure 100 – Dynamic Load Response.
 265 VAC, 5 V, 3.75 – 5 A Load Step.
 V_{MAX} : 5.02 V, V_{MIN} : 4.70 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.



18.1.3 Output: 9 V

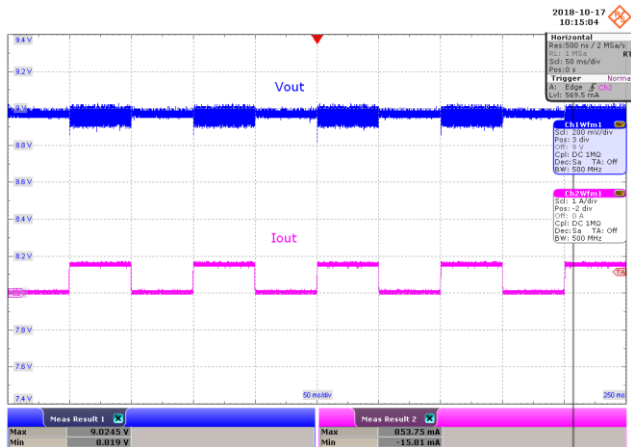


Figure 101 – Dynamic Load Response.
 85 VAC, 9 V, 0 – 0.75 A Load Step.
 V_{MAX} : 9.02 V, V_{MIN} : 8.81 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

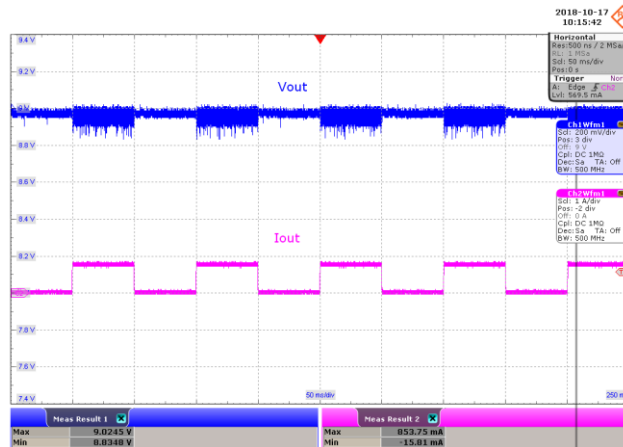


Figure 102 – Dynamic Load Response.
 265 VAC, 9 V, 0 – 0.75 A Load Step.
 V_{MAX} : 9.02 V, V_{MIN} : 8.83 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

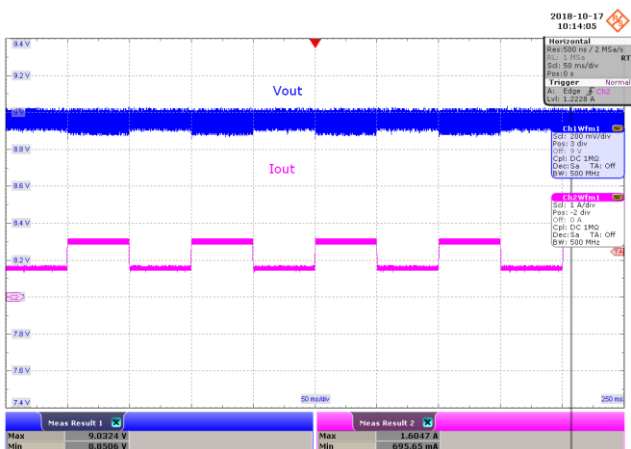


Figure 103 – Dynamic Load Response.
 85 VAC, 9 V, 0.75 – 1.5 A Load Step.
 V_{MAX} : 9.03 V, V_{MIN} : 8.85 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

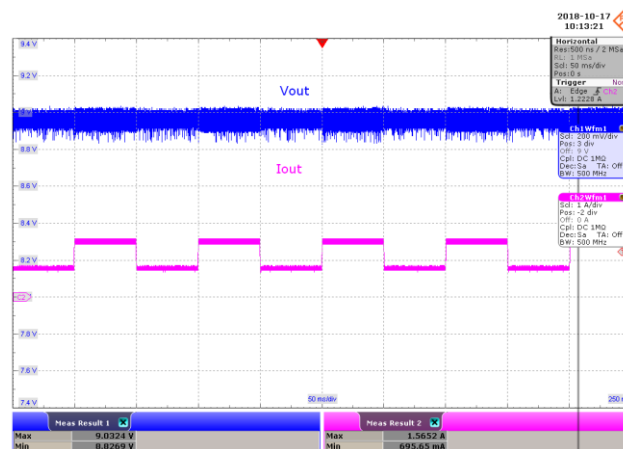


Figure 104 – Dynamic Load Response.
 265 VAC, 9 V, 0.75 – 1.5 A Load Step.
 V_{MAX} : 9.03 V, V_{MIN} : 8.82 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

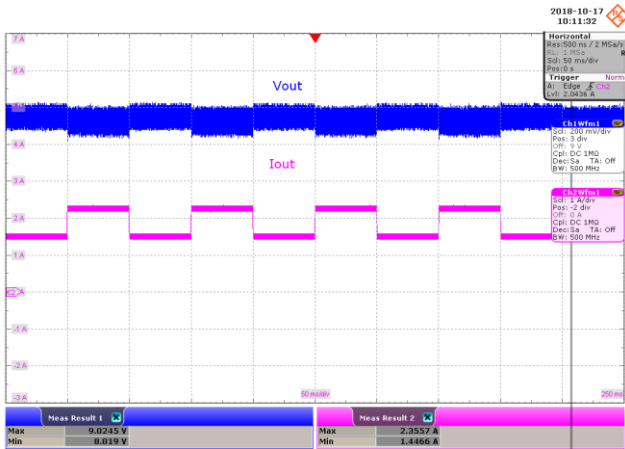


Figure 105 – Dynamic Load Response.
 85 VAC, 9 V, 1.5 – 2.25 A Load Step.
 V_{MAX} : 9.02 V, V_{MIN} : 8.81 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

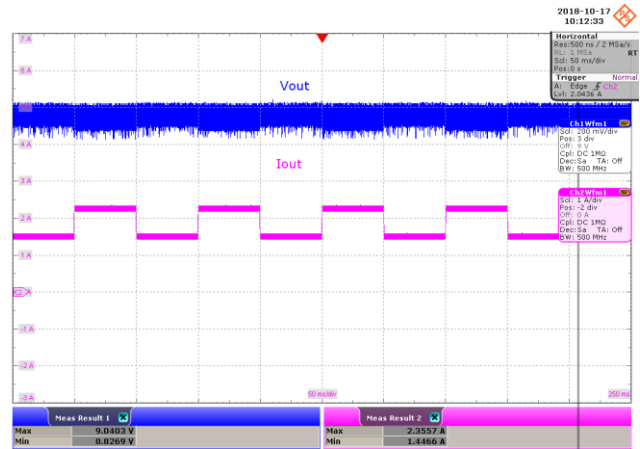


Figure 106 – Dynamic Load Response.
 265 VAC, 9 V, 1.5 – 2.25 A Load Step.
 V_{MAX} : 9.04 V, V_{MIN} : 8.82 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

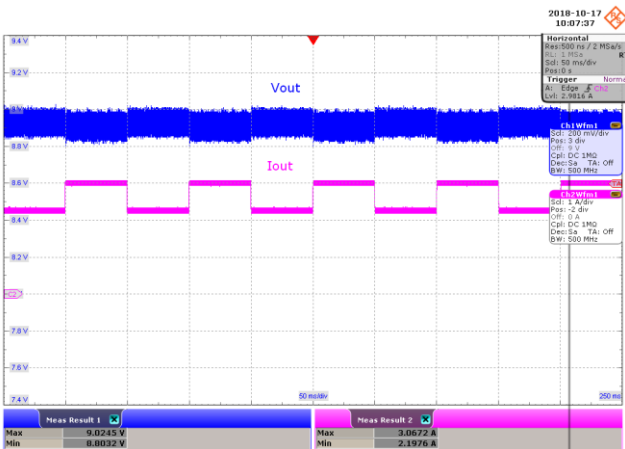


Figure 107 – Dynamic Load Response.
 85 VAC, 9 V, 2.25 – 3 A Load Step.
 V_{MAX} : 9.02 V, V_{MIN} : 8.80V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

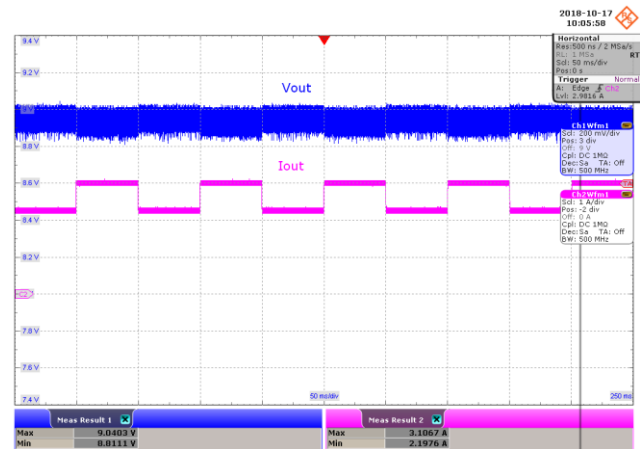


Figure 108 – Dynamic Load Response.
 265 VAC, 9 V, 2.25 – 3 A Load Step.
 V_{MAX} : 9.04 V, V_{MIN} : 8.81 V.
 Upper: V_{OUT} , 200 mV / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.



18.1.4 Output: 15 V

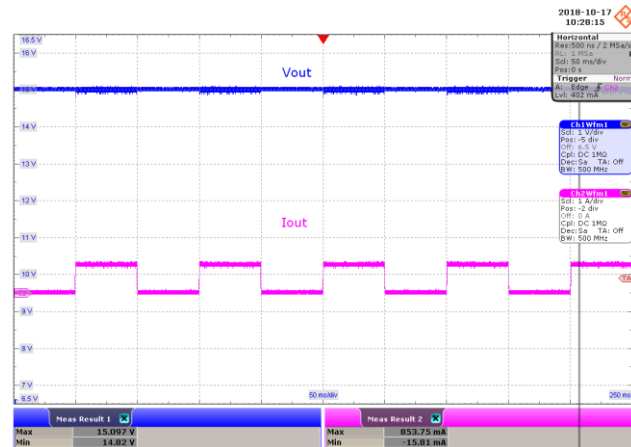
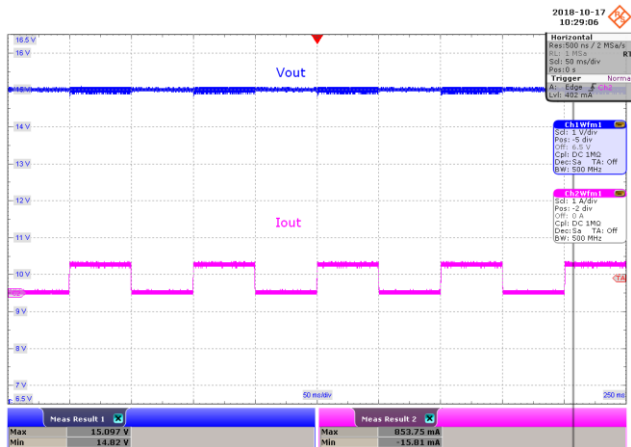


Figure 109 – Dynamic Load Response.
 85 VAC, 15 V, 0 – 0.75 A Load Step.
 V_{MAX} : 15.09 V, V_{MIN} : 14.82 V.
 Upper: V_{OUT} , 1 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

Figure 110 – Dynamic Load Response.
 265 VAC, 15 V, 0 – 0.75 A Load Step.
 V_{MAX} : 15.09V, V_{MIN} : 14.82 V.
 Upper: V_{OUT} , 1 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

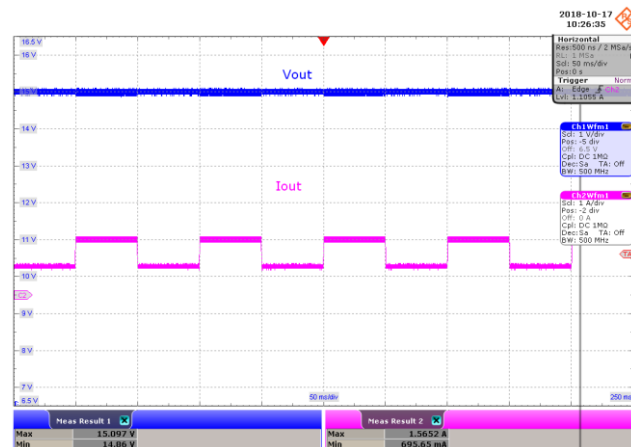
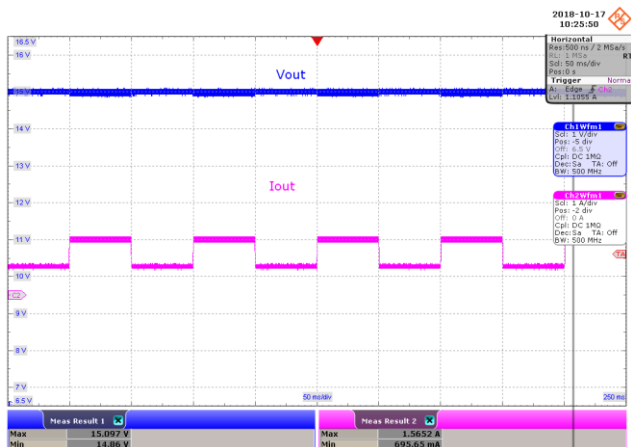


Figure 111 – Dynamic Load Response.
 85 VAC, 15 V, 0.75 – 1.5 A Load Step.
 V_{MAX} : 15.09 V, V_{MIN} : 14.86 V.
 Upper: V_{OUT} , 1 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

Figure 112 – Dynamic Load Response.
 265 VAC, 15 V, 0.75 – 1.5 A Load Step.
 V_{MAX} : 15.09 V, V_{MIN} : 14.86 V.
 Upper: V_{OUT} , 1 V / div., 50 ms / div..
 Lower: I_{LOAD} , 1 A / div.



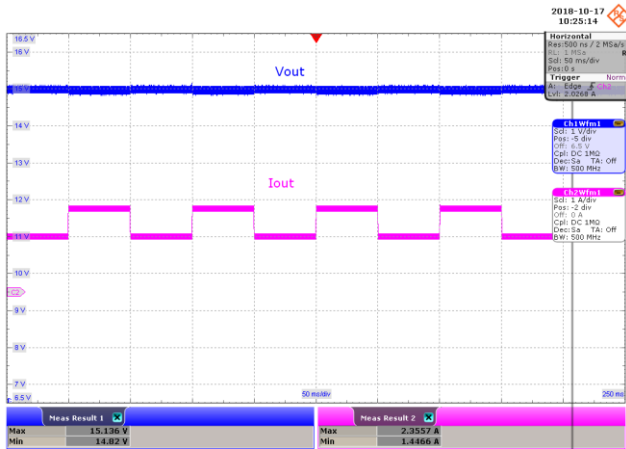


Figure 113 – Dynamic Load Response.
 85 VAC, 15 V, 1.5 – 2.25 A Load Step.
 V_{MAX} : 15.13 V, V_{MIN} : 14.82 V.
 Upper: V_{OUT} , 1 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

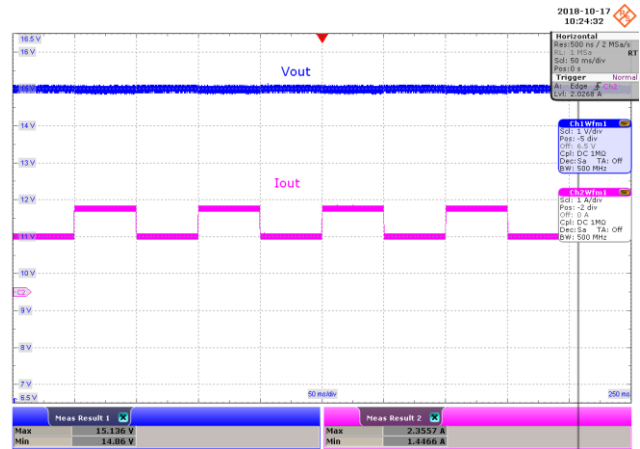


Figure 114 – Dynamic Load Response.
 265 VAC, 15 V, 1.5 – 2.25 A Load Step.
 V_{MAX} : 15.13 V, V_{MIN} : 14.86 V.
 Upper: V_{OUT} , 1 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

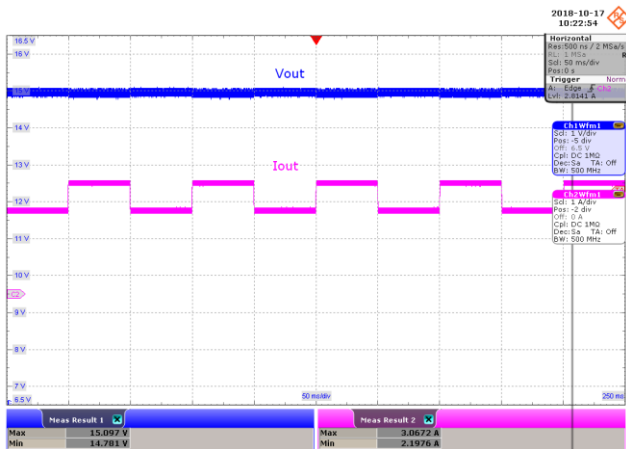


Figure 115 – Dynamic Load Response.
 85 VAC, 15 V, 2.25 – 3 A Load Step.
 V_{MAX} : 15.097 V, V_{MIN} : 14.78 V.
 Upper: V_{OUT} , 1 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

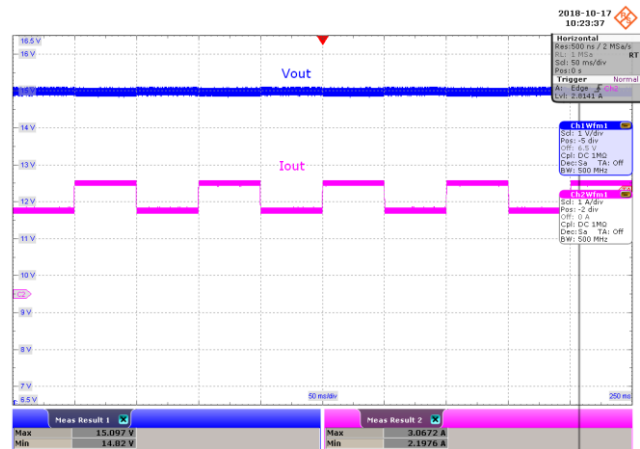


Figure 116 – Dynamic Load Response.
 265 VAC, 15 V, 2.25 – 3 A Load Step.
 V_{MAX} : 15.097 V, V_{MIN} : 14.82 V.
 Upper: V_{OUT} , 1 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.



18.1.5 Output: 20 V

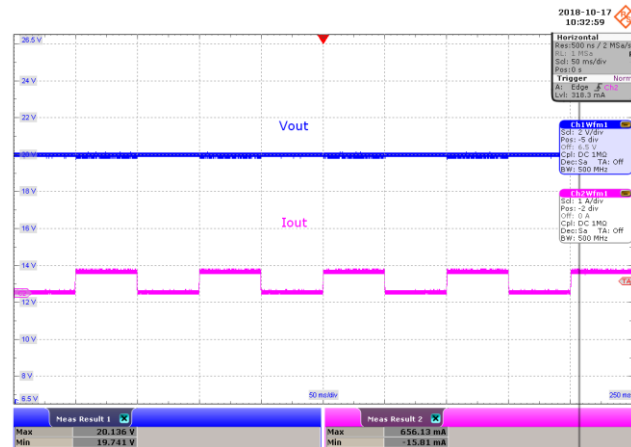
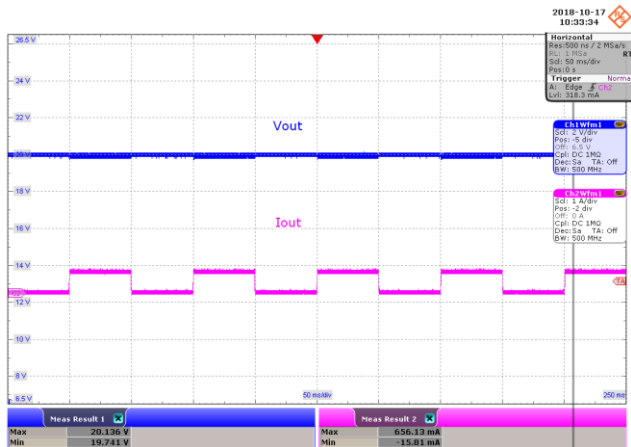


Figure 117 – Dynamic Load Response.
 85 VAC, 20 V, 0 – 0.56 A Load Step.
 V_{MAX} : 20.13 V, V_{MIN} : 19.74 V.
 Upper: V_{OUT} , 2 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

Figure 118 – Dynamic Load Response.
 265 VAC, 20 V, 0 – 0.56 A Load Step.
 V_{MAX} : 20.13 V, V_{MIN} : 19.74 V.
 Upper: V_{OUT} , 2 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

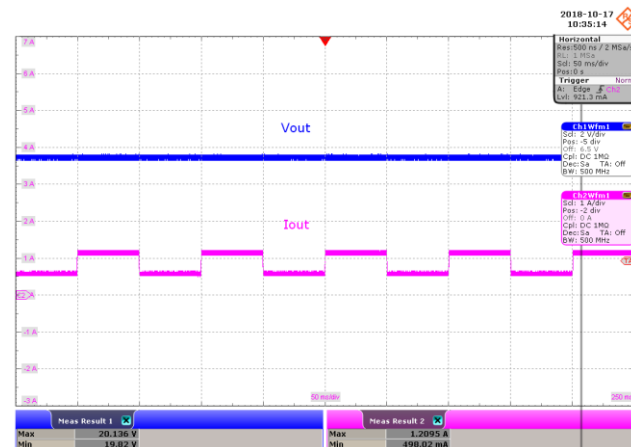


Figure 119 – Dynamic Load Response.
 85 VAC, 20 V, 0.56 – 1.125 A Load Step.
 V_{MAX} : 20.13 V, V_{MIN} : 19.74 V.
 Upper: V_{OUT} , 2 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

Figure 120 – Dynamic Load Response.
 265 VAC, 20 V, 0.56 – 1.125 A Load Step.
 V_{MAX} : 20.13 V, V_{MIN} : 19.82 V.
 Upper: V_{OUT} , 2 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

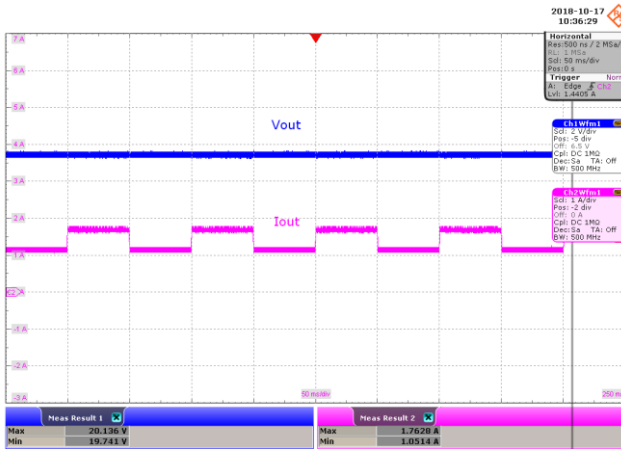


Figure 121 – Dynamic Load Response.
 85 VAC, 20 V, 1.125 – 1.68 A Load Step.
 V_{MAX} : 20.13 V, V_{MIN} : 19.74 V.
 Upper: V_{OUT} , 2 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

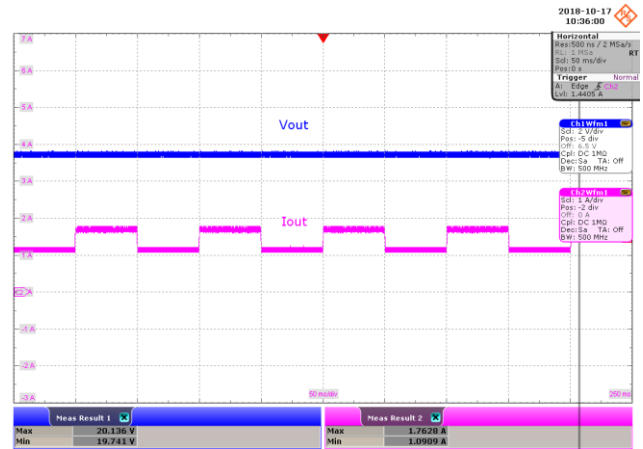


Figure 122 – Dynamic Load Response.
 265 VAC, 20 V, 1.125 – 1.68 A Load Step.
 V_{MAX} : 20.13 V, V_{MIN} : 19.74 V.
 Upper: V_{OUT} , 2 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

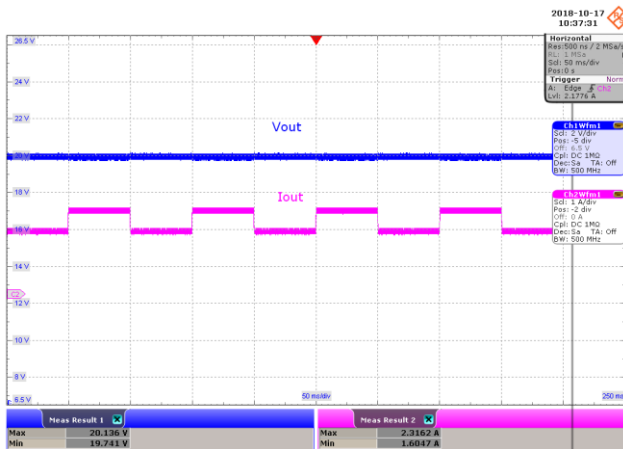


Figure 123 – Dynamic Load Response.
 85 VAC, 20 V, 1.68 – 2.25 A Load Step.
 V_{MAX} : 20.13 V, V_{MIN} : 19.74 V.
 Upper: V_{OUT} , 2 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.

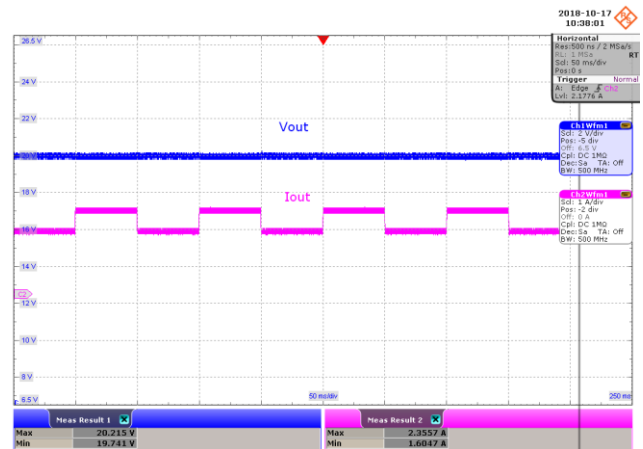


Figure 124 – Dynamic Load Response.
 265 VAC, 20 V, 1.68 – 2.25 A Load Step.
 V_{MAX} : 20.21 V, V_{MIN} : 19.74 V.
 Upper: V_{OUT} , 2 V / div., 50 ms / div.
 Lower: I_{LOAD} , 1 A / div.



18.2 Drain Voltage and Current

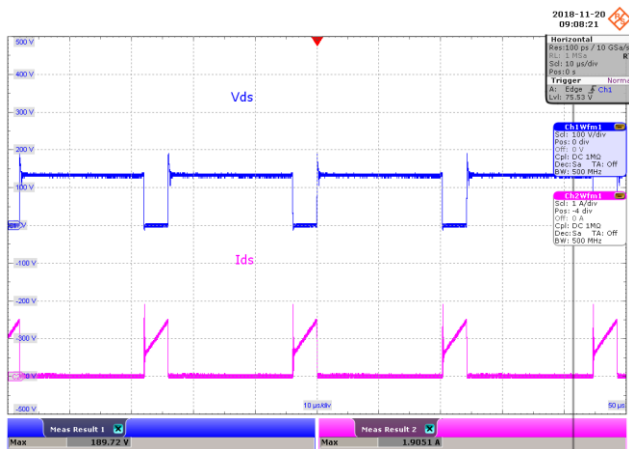


Figure 125 – Drain Voltage and Current Waveforms. 85 VAC, 3.3 V, 5 A Load (189 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div., 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.

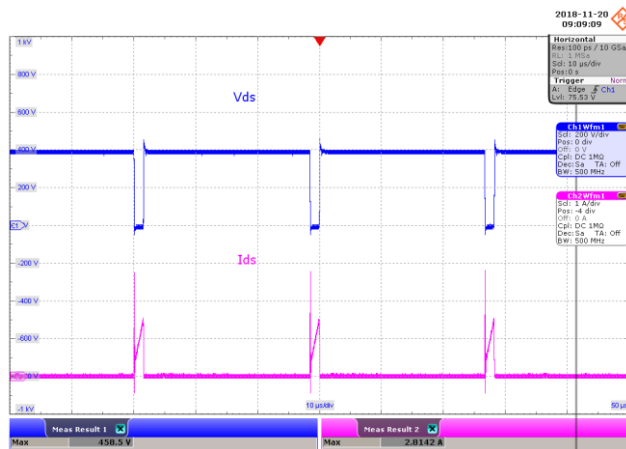


Figure 126 – Drain Voltage and Current Waveforms. 265 VAC, 3.3 V, 5 A Load (458 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.

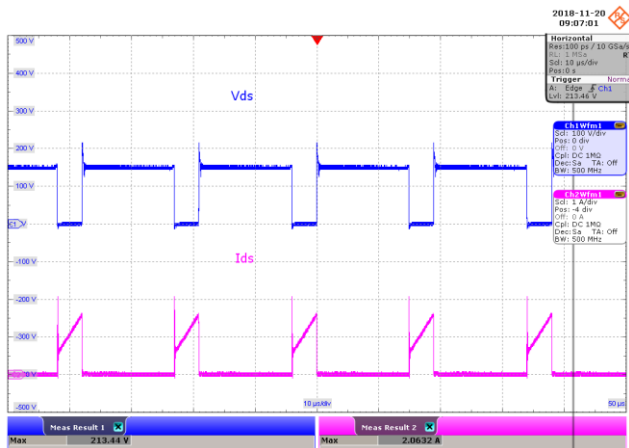


Figure 127 – Drain Voltage and Current Waveforms. 85 VAC, 5.0 V, 5 A Load (213 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div., 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.

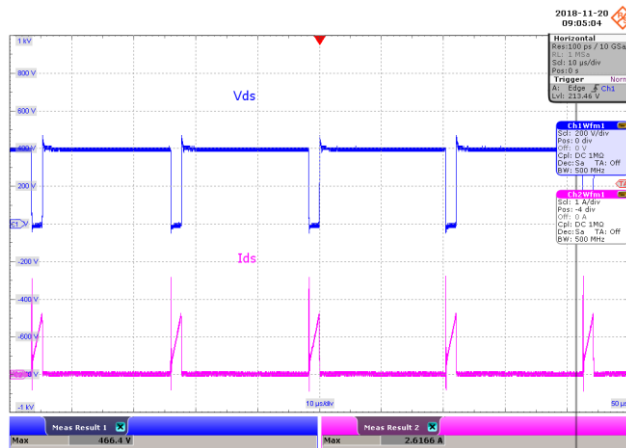


Figure 128 – Drain Voltage and Current Waveforms. 265 VAC, 5.0 V, 5 A Load (466 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 10 µs / div.
Lower: I_{DRAIN}, 1 A / div.

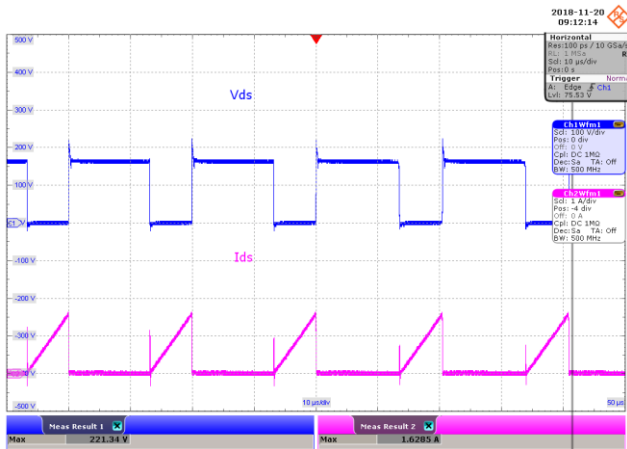


Figure 129 – Drain Voltage and Current Waveforms. 85 VAC, 9.0 V, 3 A Load (221 V_{MAX}). Upper: V_{DRAIN}, 100 V / div., 10 µs / div. Lower: I_{DRAIN}, 1 A / div.

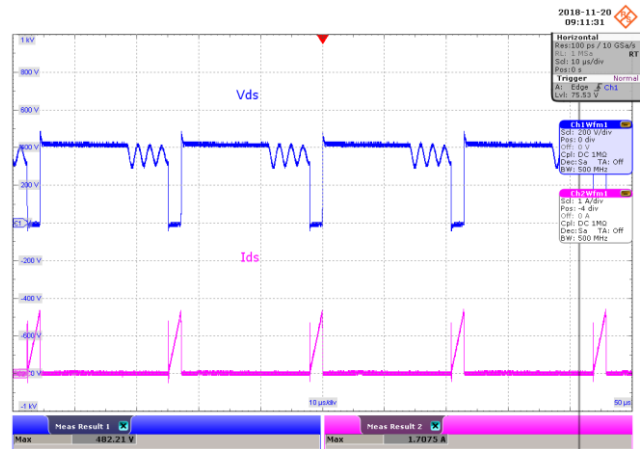


Figure 130 – Drain Voltage and Current Waveforms. 265 VAC, 9.0 V, 3 A Load (482 V_{MAX}). Upper: V_{DRAIN}, 200 V / div., 10 µs / div. Lower: I_{DRAIN}, 1 A / div.

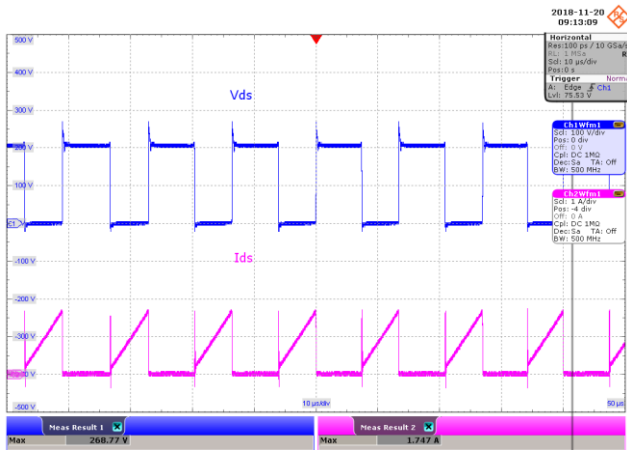


Figure 131 – Drain Voltage and Current Waveforms. 85 VAC, 15.0 V, 3 A Load (268 V_{MAX}). Upper: V_{DRAIN}, 100 V / div., 20 µs / div. Lower: I_{DRAIN}, 1 A / div.

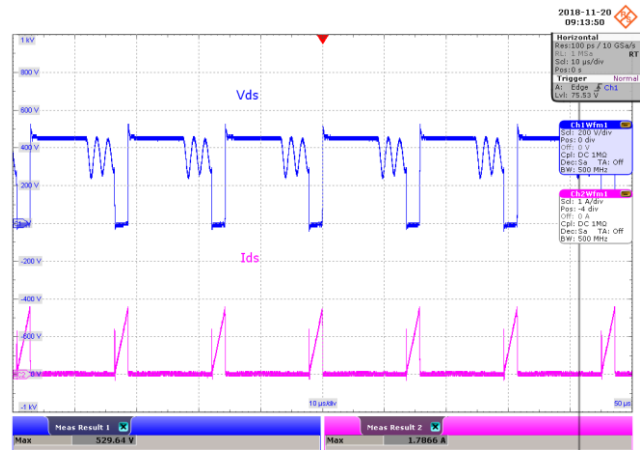


Figure 132 – Drain Voltage and Current Waveforms. 265 VAC, 15.0 V, 3 A Load (529 V_{MAX}). Upper: V_{DRAIN}, 200 V / div., 20 µs / div. Lower: I_{DRAIN}, 1 A / div.

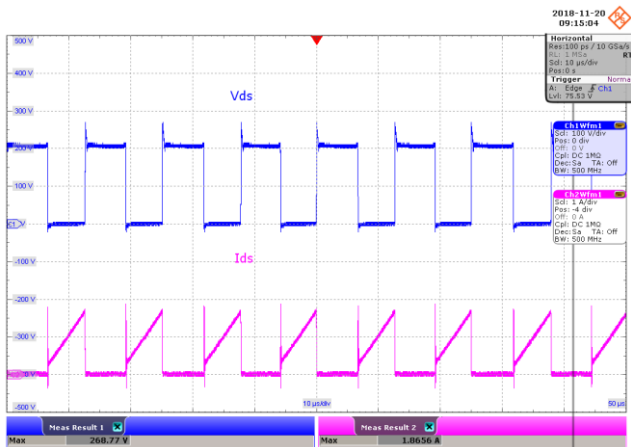


Figure 133 – Drain Voltage and Current Waveforms.
 85 VAC, 16.0 V, 3 A Load (268 V_{MAX}).
 Upper: V_{DRAIN}, 100 V / div., 20 μs / div.
 Lower: I_{DRAIN}, 1 A / div.

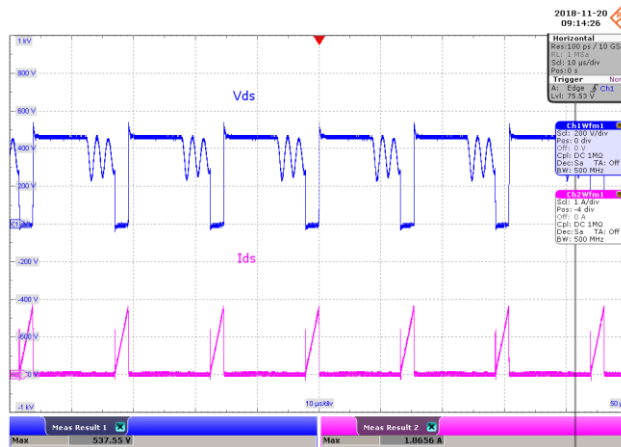


Figure 134 – Drain Voltage and Current Waveforms.
 265 VAC, 16.0 V, 3 A Load (537 V_{MAX}).
 Upper: V_{DRAIN}, 200 V / div., 20 μs / div.
 Lower: I_{DRAIN}, 1 A / div.

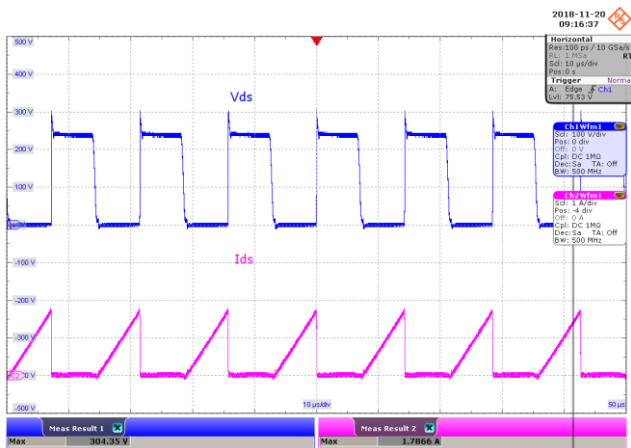


Figure 135 – Drain Voltage and Current Waveforms.
 85 VAC, 20.0 V, 2.25 A Load (304 V_{MAX}).
 Upper: V_{DRAIN}, 100 V / div., 20 μs / div.
 Lower: I_{DRAIN}, 1 A / div.

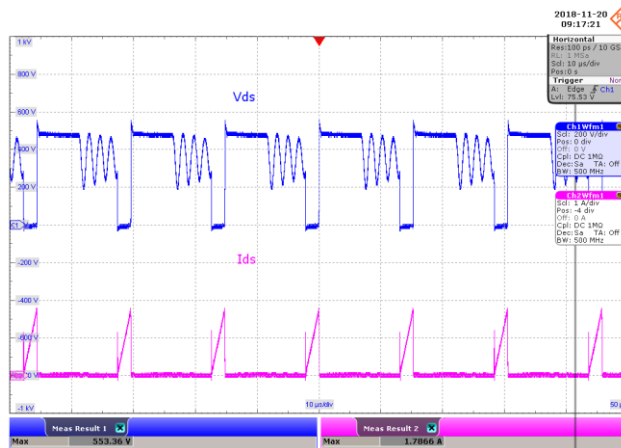


Figure 136 – Drain Voltage and Current Waveforms.
 265 VAC, 20.0 V, 2.25 A Load (553 V_{MAX}).
 Upper: V_{DRAIN}, 200 V / div., 20 μs / div.
 Lower: I_{DRAIN}, 1 A / div.

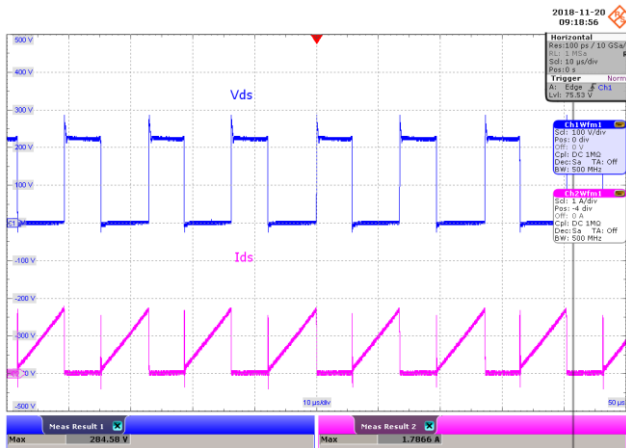


Figure 137 – Drain Voltage and Current Waveforms.
85 VAC, 21.0 V, 2.25 A Load (284 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div., 20 μs / div.
Lower: I_{DRAIN}, 1 A / div.

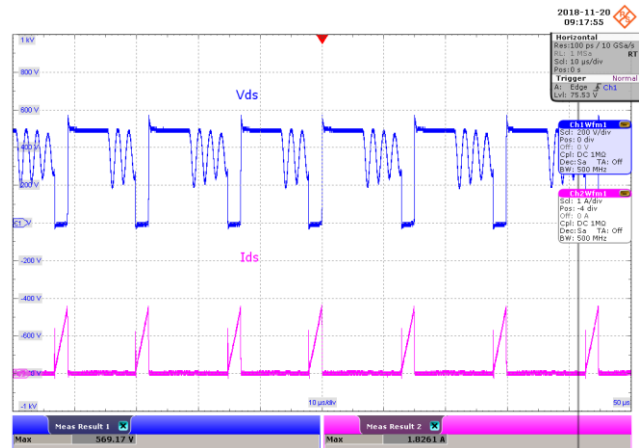


Figure 138 – Drain Voltage and Current Waveforms.
265 VAC, 21.0 V, 2.25 A Load (569 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 20 μs / div.
Lower: I_{DRAIN}, 1 A / div.

18.3 Drain Voltage and Current at Start-up

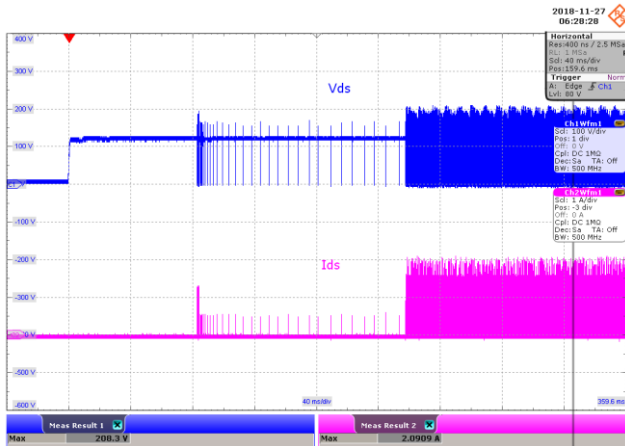


Figure 139 – Drain Voltage and Current Waveforms.
85 VAC, 5.0 V, 5.0 A Load (208 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div., 40 ms / div.
Lower: I_{DRAIN}, 1 A / div.

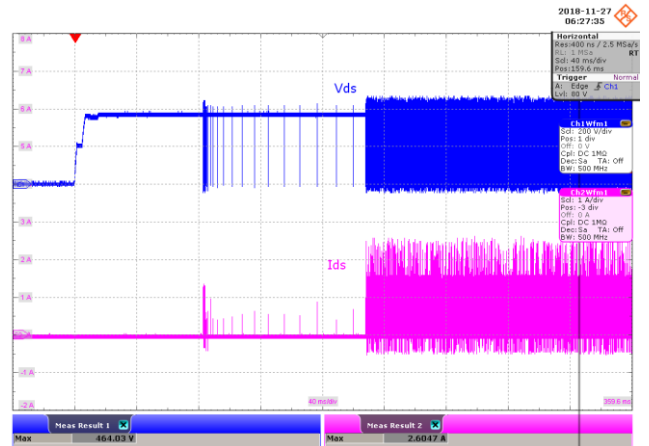


Figure 140 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 5.0 A Load (464 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div., 40 ms / div.
Lower: I_{DRAIN}, 1 A / div.



18.4 SR FET Voltage

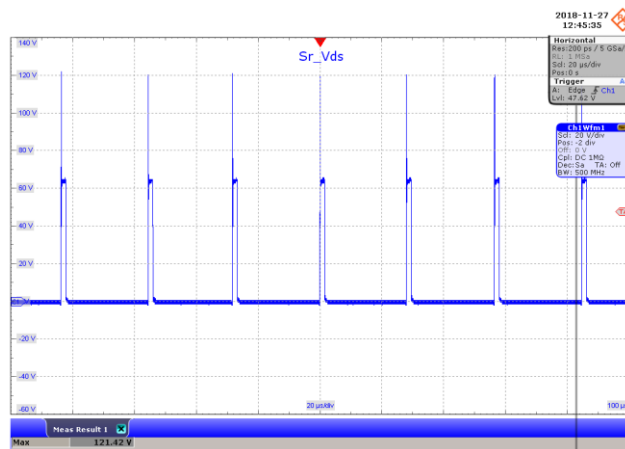
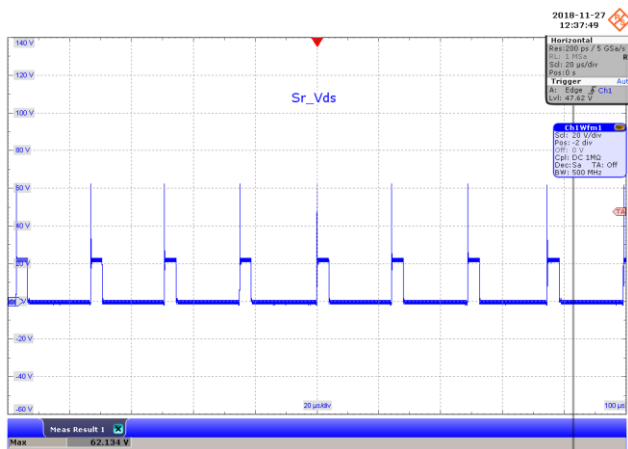


Figure 141 – SR FET Voltage Waveform.
85 VAC, 3.3 V, 5 A Load (62 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 μs / div.

Figure 142 – SR FET Voltage Waveform.
265 VAC, 3.3 V, 5 A Load (121 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 μs / div.

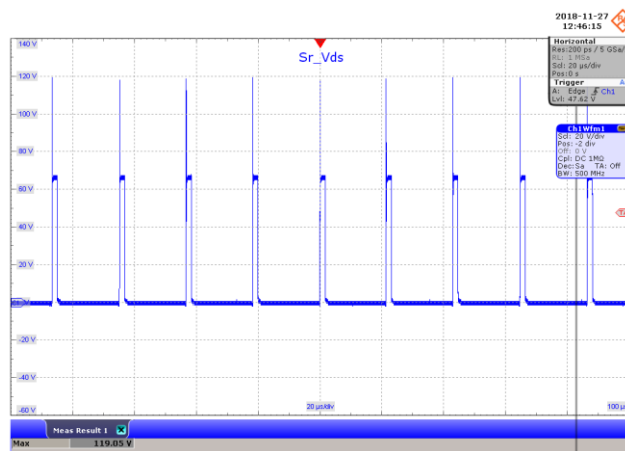
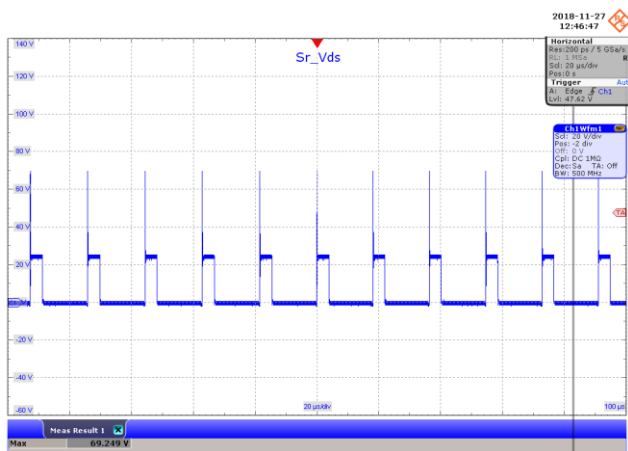


Figure 143 – SR FET Voltage Waveform.
85 VAC, 5.0 V, 5 A Load (69 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 μs / div.

Figure 144 – SR FET Voltage Waveform.
265 VAC, 5.0 V, 5 A Load (119 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 μs / div.

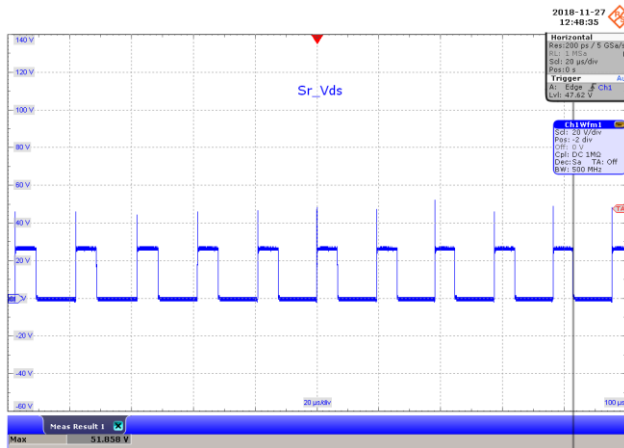


Figure 145 – SR FET Voltage Waveform.
85 VAC, 9.0 V, 3 A Load (51 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 μs / div.

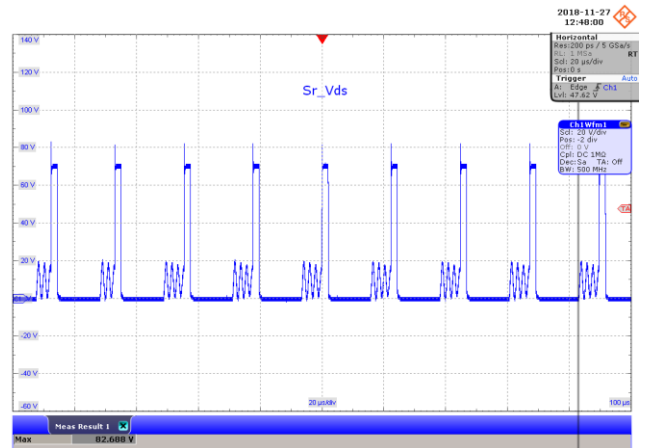


Figure 146 – SR FET Voltage Waveform.
265 VAC, 9.0 V, 3 A Load (82 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 0 μs / div.

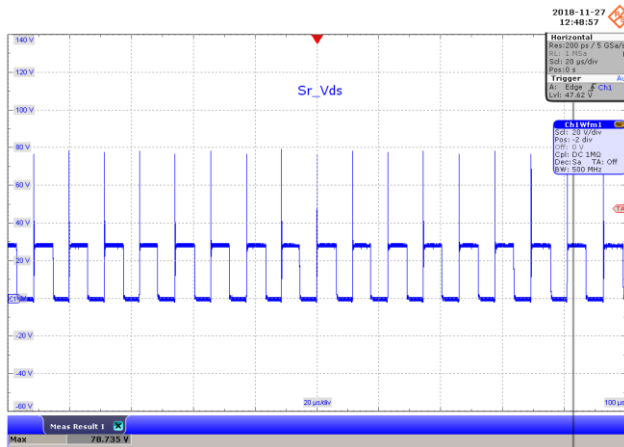


Figure 147 – SR FET Voltage Waveform.
85 VAC, 15.0 V, 3 A Load (78 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 μs / div.

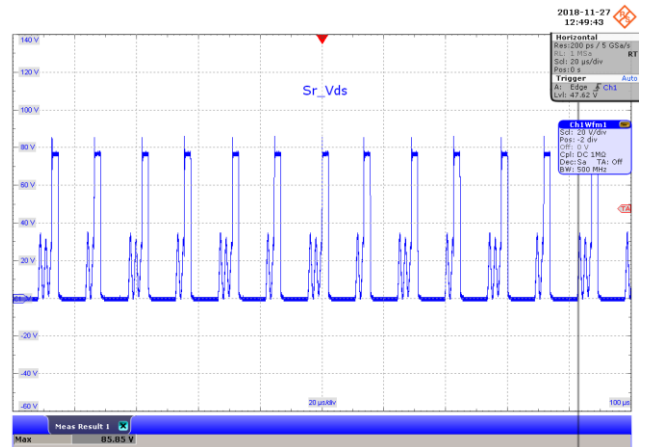


Figure 148 – SR FET Voltage Waveform.
265 VAC, 15.0 V, 3 A Load (85 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 μs / div.



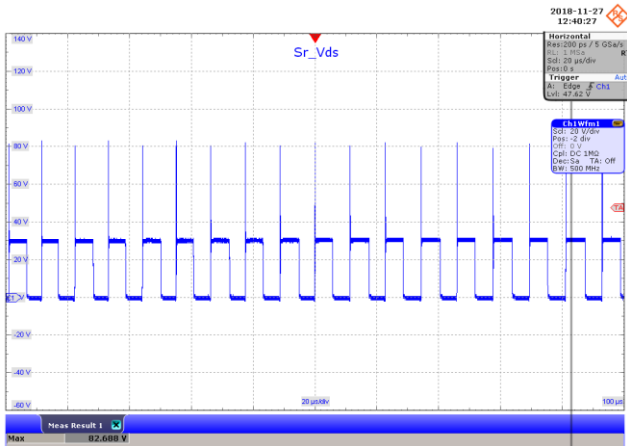


Figure 149 – SR FET Voltage Waveform.
85 VAC, 16.0 V, 3 A Load (82 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 µs / div.

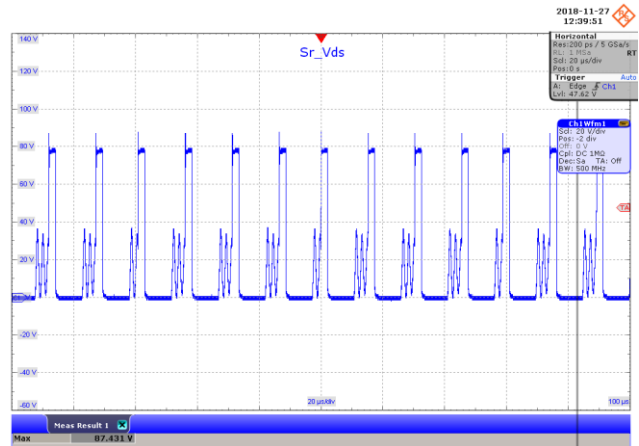


Figure 150 – SR FET Voltage Waveform.
265 VAC, 16.0 V, 3 A Load (87 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 µs / div.

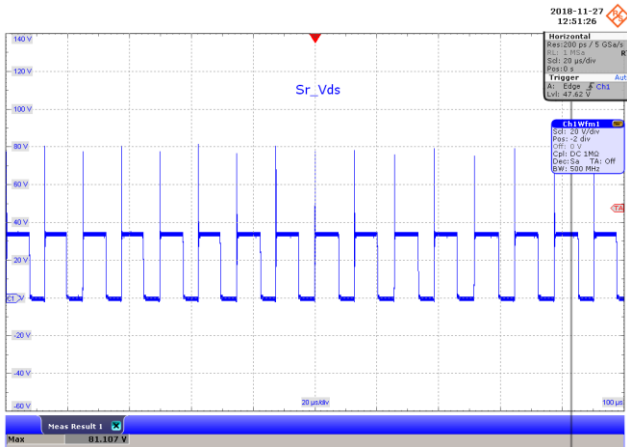


Figure 151 – SR FET Voltage Waveform.
85 VAC, 20.0 V, 2.25 A Load (81 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 µs / div.

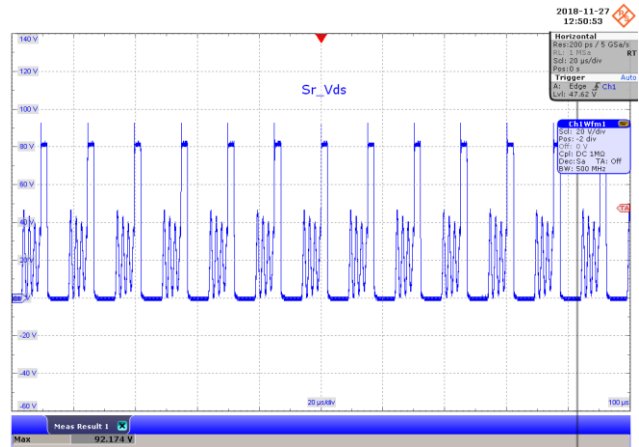


Figure 152 – SR FET Voltage Waveform.
265 VAC, 20.0 V, 2.25 A Load (92 V_{MAX}).
SR_V_{DRAIN}, 20 V / div., 20 µs / div.

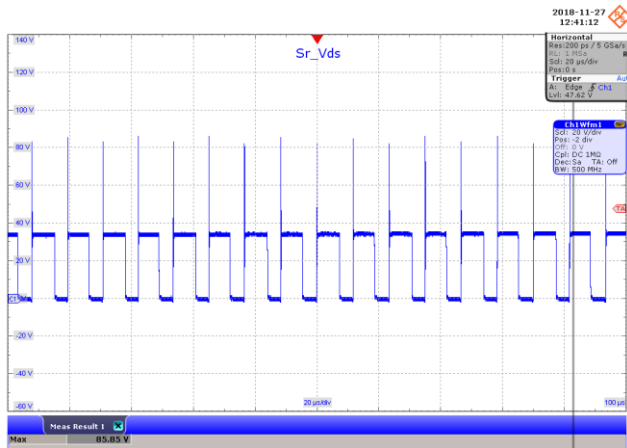


Figure 153 – SR FET Voltage Waveform.
 85 VAC, 21.0 V, 2.25 A Load (85 V_{MAX}).
 SR_V_{DRAIN}, 20 V / div., 20 μs / div.

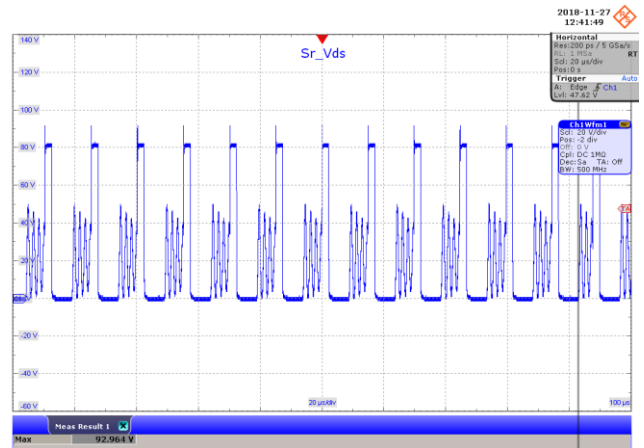


Figure 154 – SR FET Voltage Waveform.
 265 VAC, 21.0 V, 2.25 A Load (92 V_{MAX}).
 SR_V_{DRAIN}, 20 V / div., 20 μs / div.

18.5 Output Voltage and Current at Start-up (On the Board)

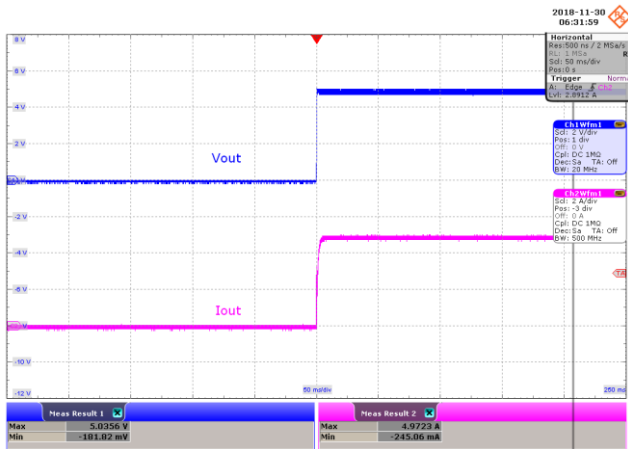


Figure 155 – Output Voltage and Current Waveforms.
 85 VAC, 5 V, 5 A Load.
 Upper: V_{OUT} , 2 V / div.
 Lower: I_{OUT} , 2 A / div., 50 ms / div.

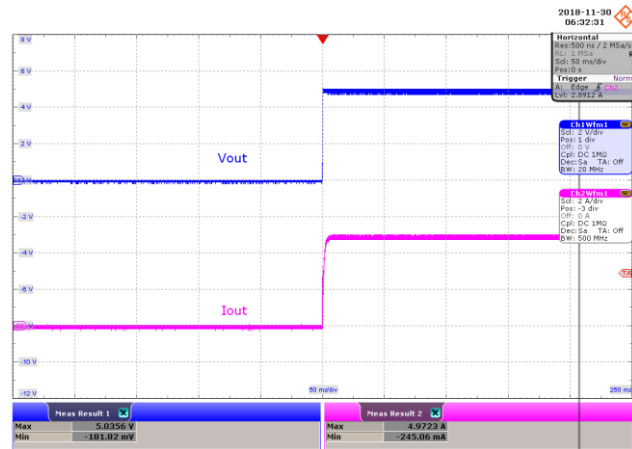


Figure 156 – Output Voltage and Current Waveforms.
 265 VAC, 5 V, 5 A Load.
 Upper: V_{OUT} , 2 V / div.
 Lower: I_{OUT} , 1 A / div., 50 ms / div.

19 Voltage and Current Step Test using Quadramax and Total Phase Analyzer

19.1 Voltage Step Test (VST)

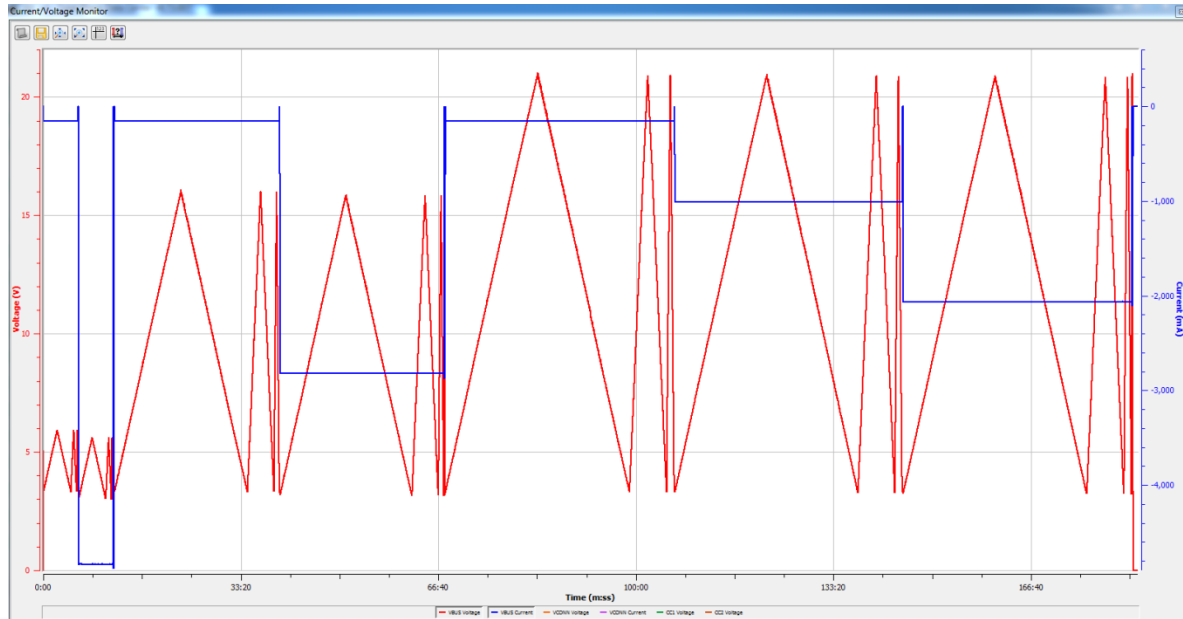


Figure 157 – Plot of SPT.6 VST from Total Phase Analyzer.

19.2 Current Limit Test (CLT)

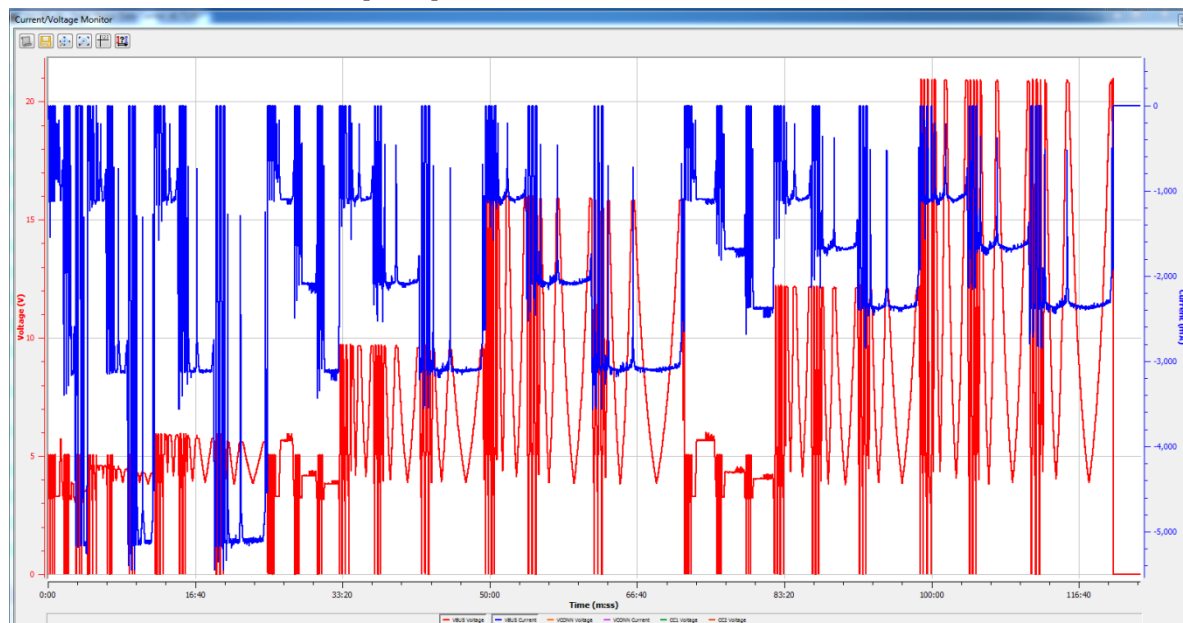


Figure 158 – Plot of SPT.7 CLT from Total Phase Analyzer.

20 Conducted EMI

20.1 Floating Output

20.1.1 Output: 5 V / 5 A

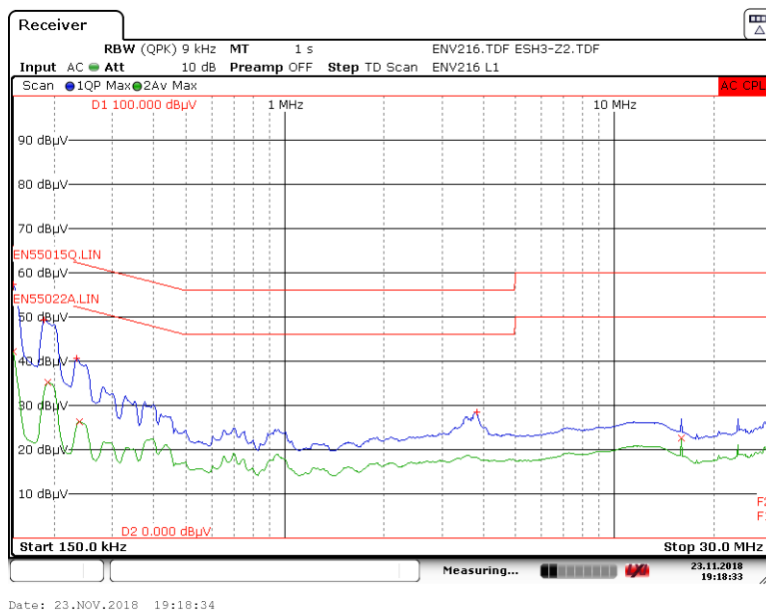


Figure 159 – Floating Ground EMI, 5 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

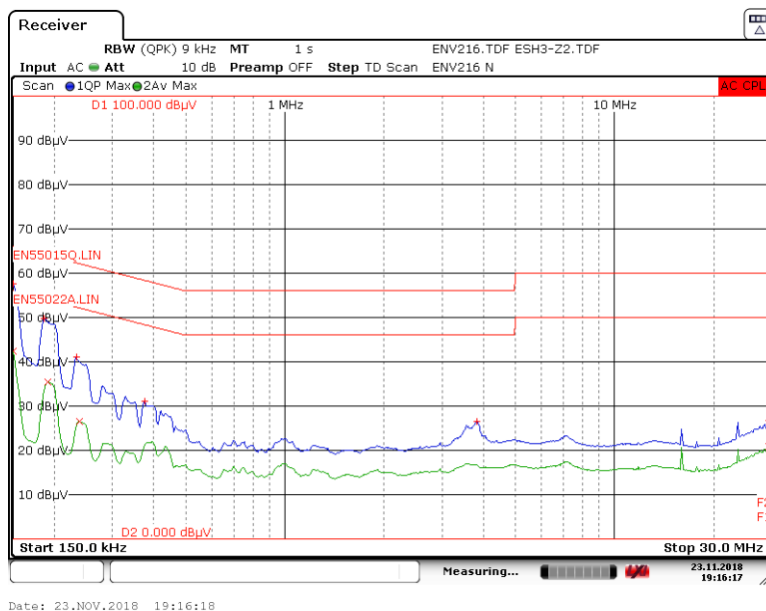


Figure 160 – Floating Ground EMI, 5 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).



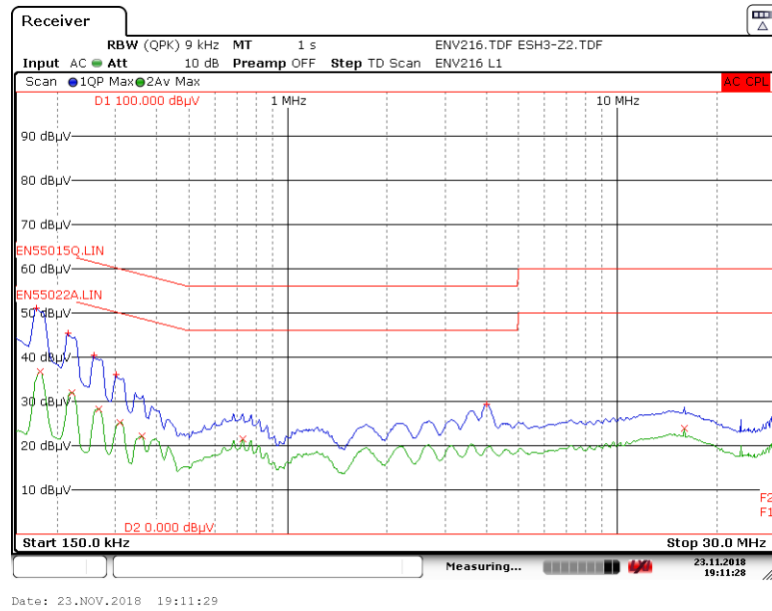


Figure 161 – Floating Ground EMI, 5 V / 5 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

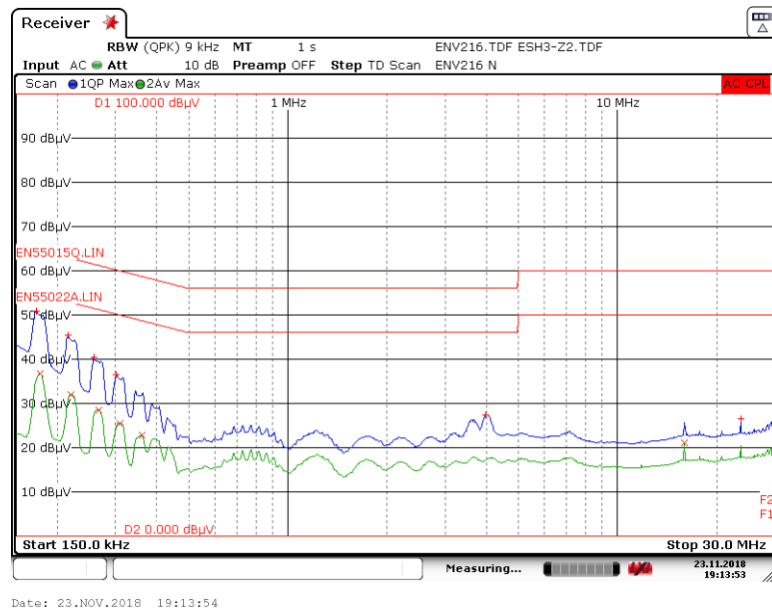


Figure 162 – Floating Ground EMI, 5 V / 5 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.1.2 Output: 9 V / 3 A

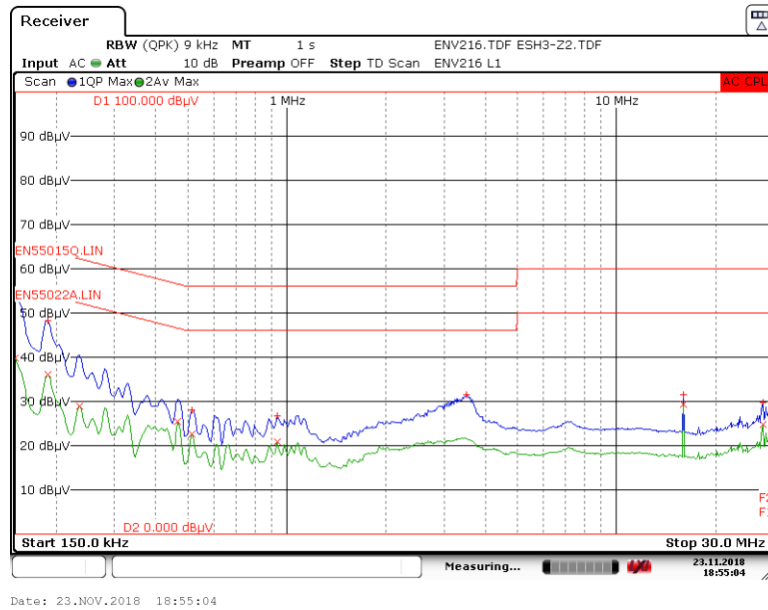


Figure 163 – Floating Ground EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

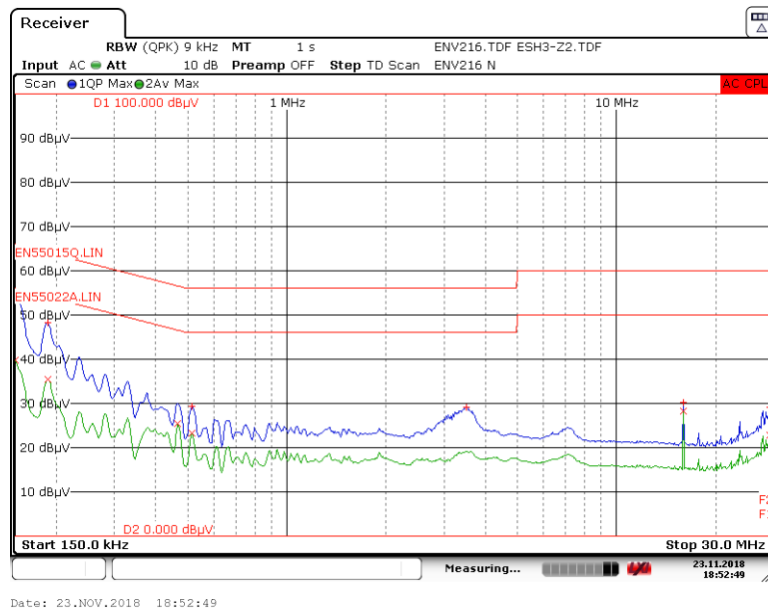


Figure 164 – Floating Ground EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

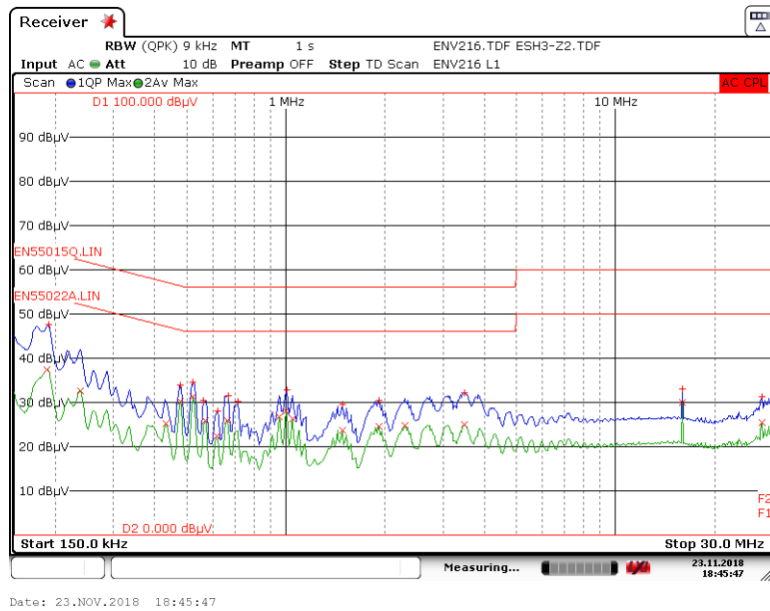


Figure 165 – Floating Ground EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

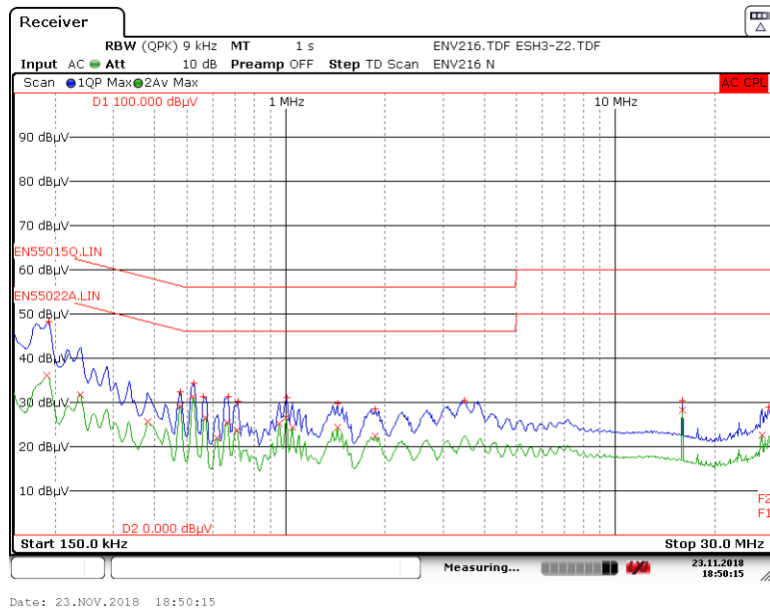


Figure 166 – Floating Ground EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.1.3 Output: 15 V / 3 A

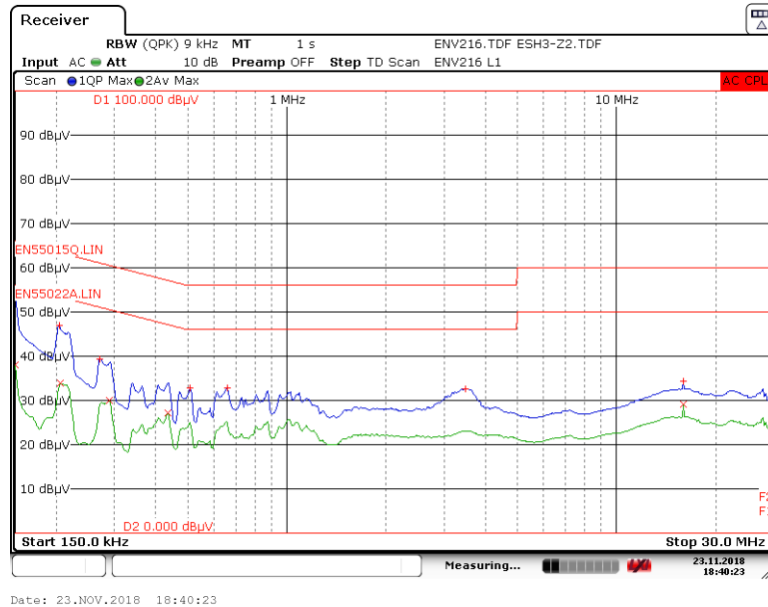


Figure 167 – Floating Ground EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

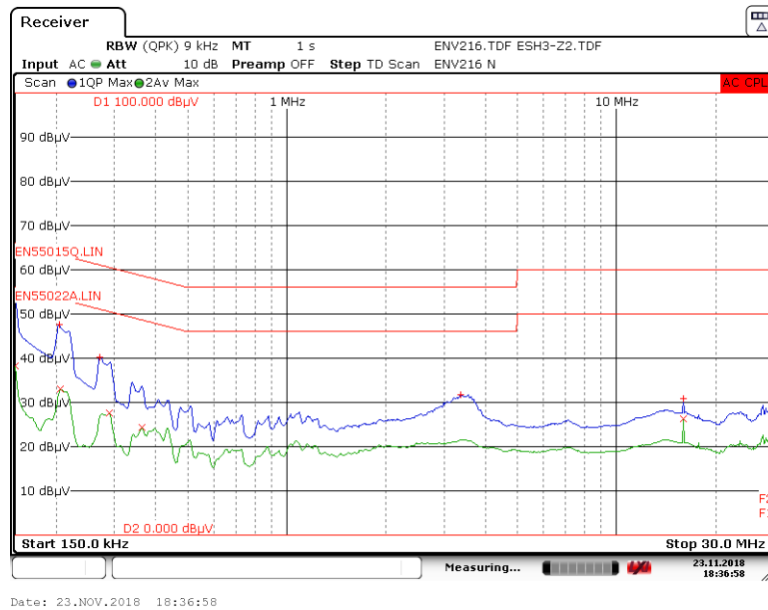


Figure 168 – Floating Ground EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

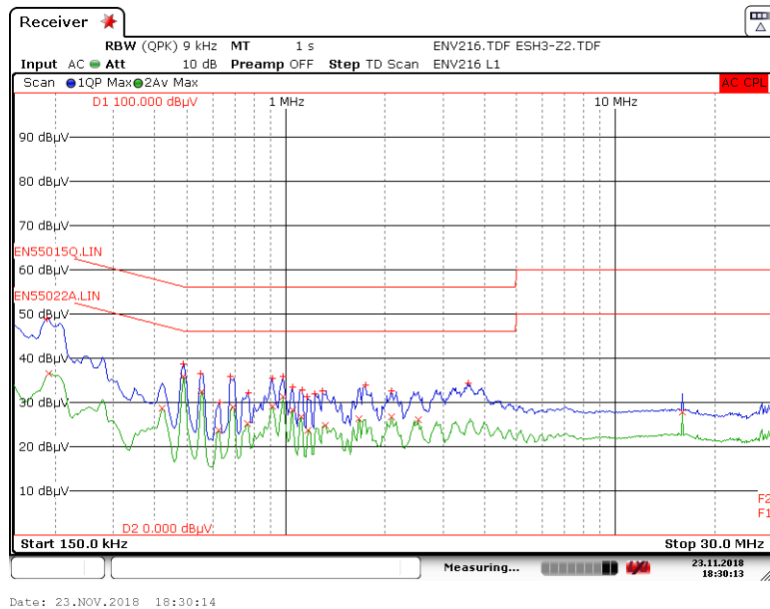


Figure 169 – Floating Ground EMI, 15 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

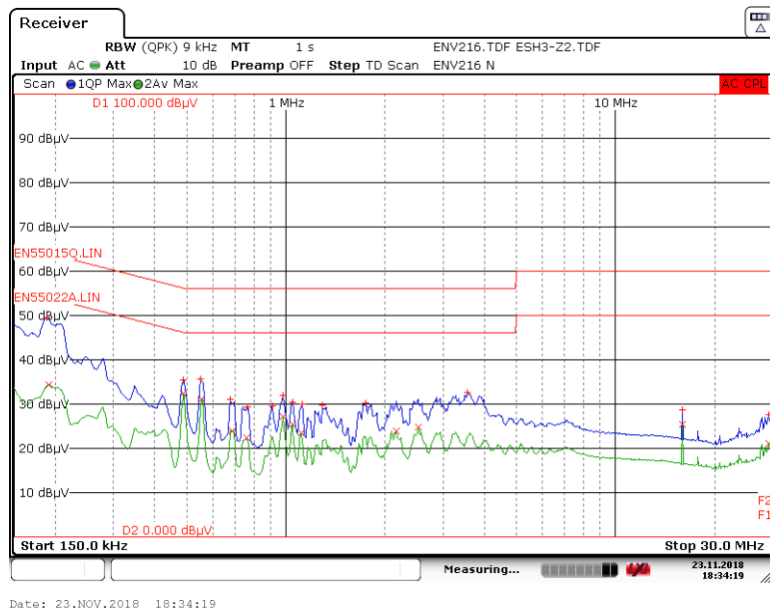


Figure 170 – Floating Ground EMI, 15 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.1.4 Output: 20 V / 2.25 A

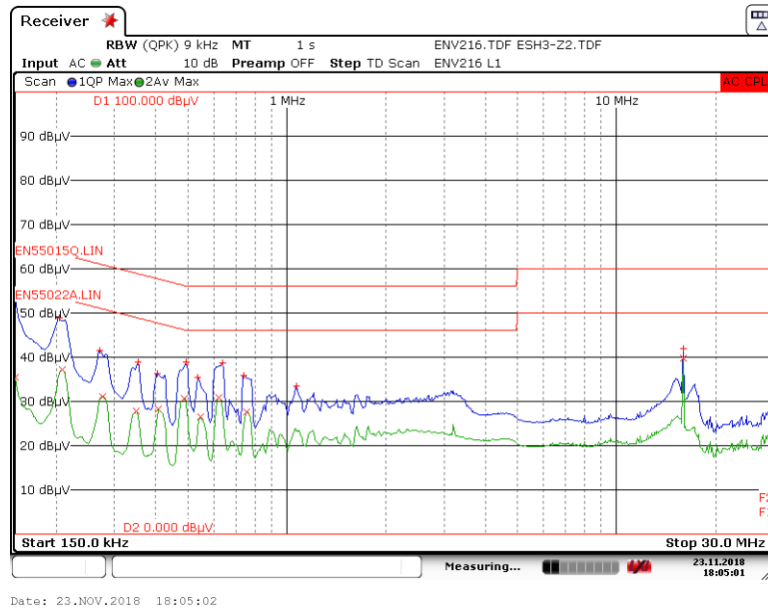


Figure 171 – Floating Ground EMI, 20 V / 2.25 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

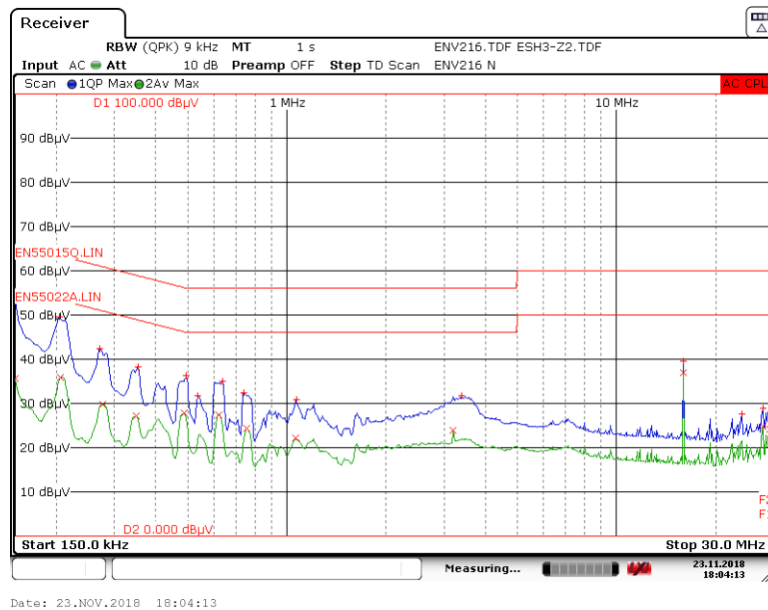


Figure 172 – Floating Ground EMI, 20 V / 2.25 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

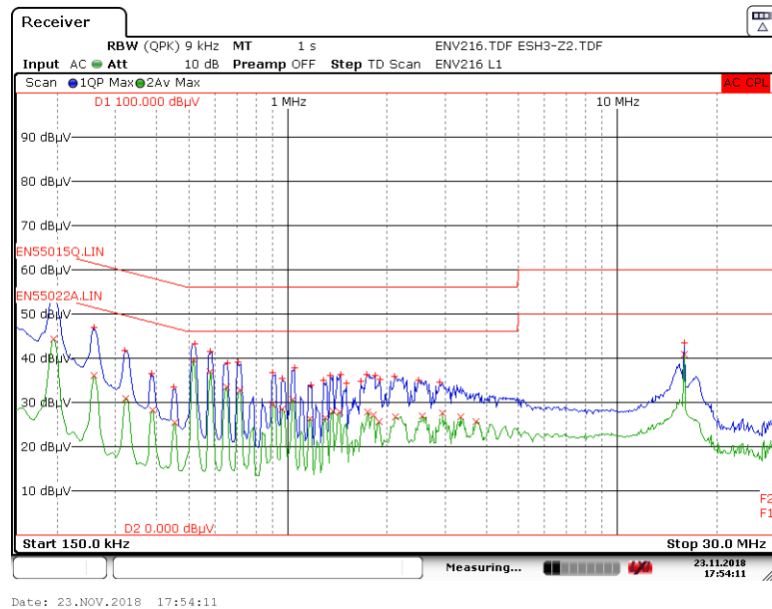


Figure 173 – Floating Ground EMI, 20 V / 2.25 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

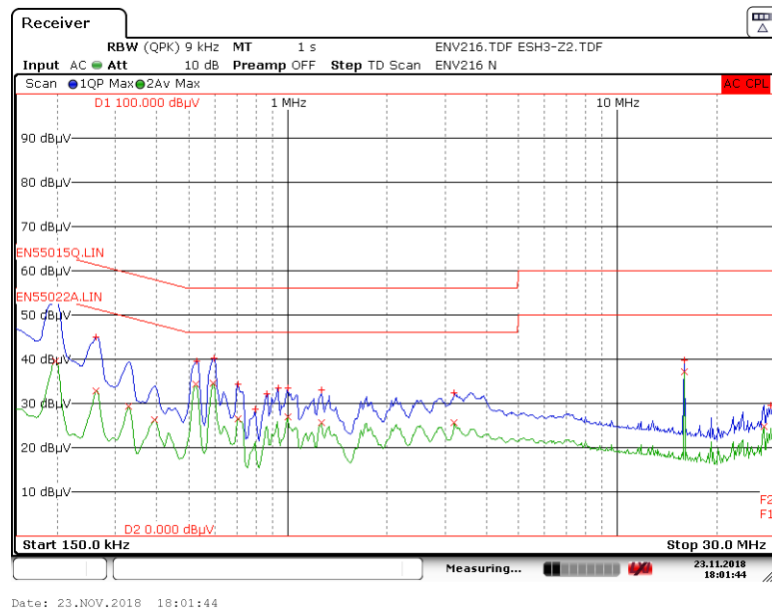


Figure 174 – Floating Ground EMI, 20 V / 2.25 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

20.2 Artificial Hand

20.2.1 Output: 5 V / 5 A

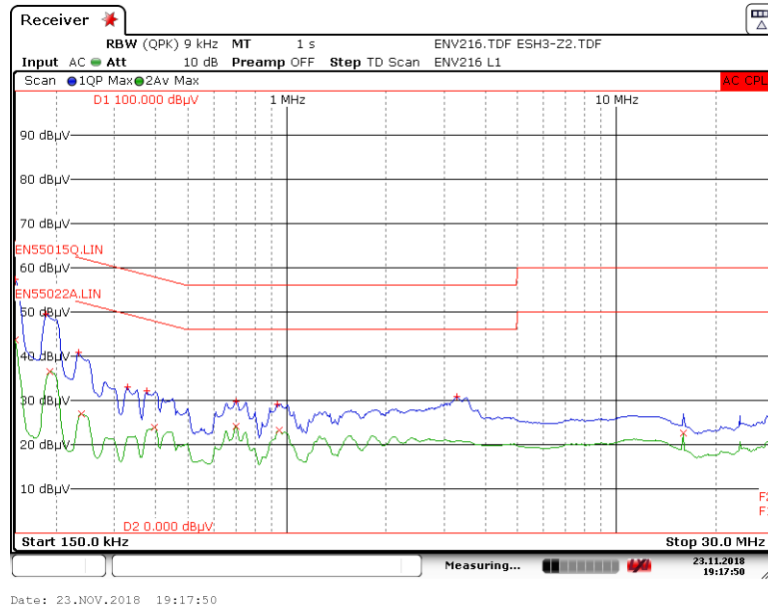


Figure 175 – Artificial Hand EMI, 5 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

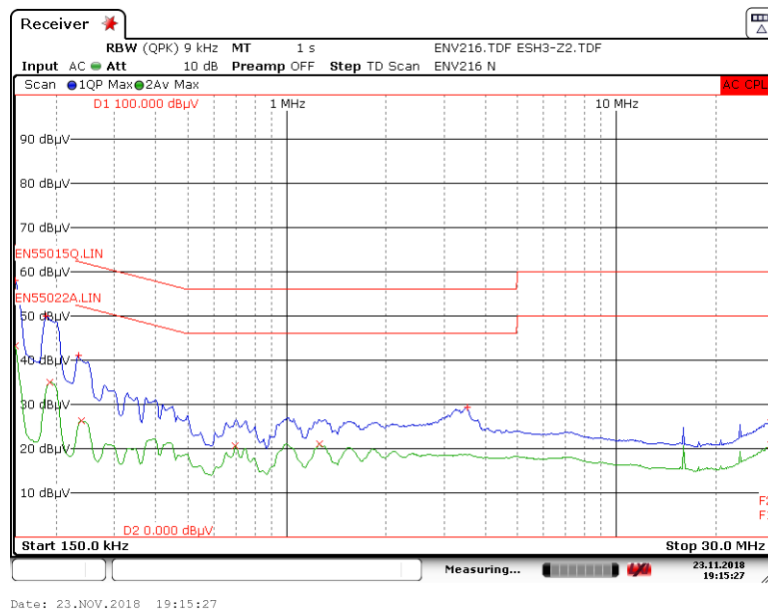


Figure 176 – Artificial Hand EMI, 5 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

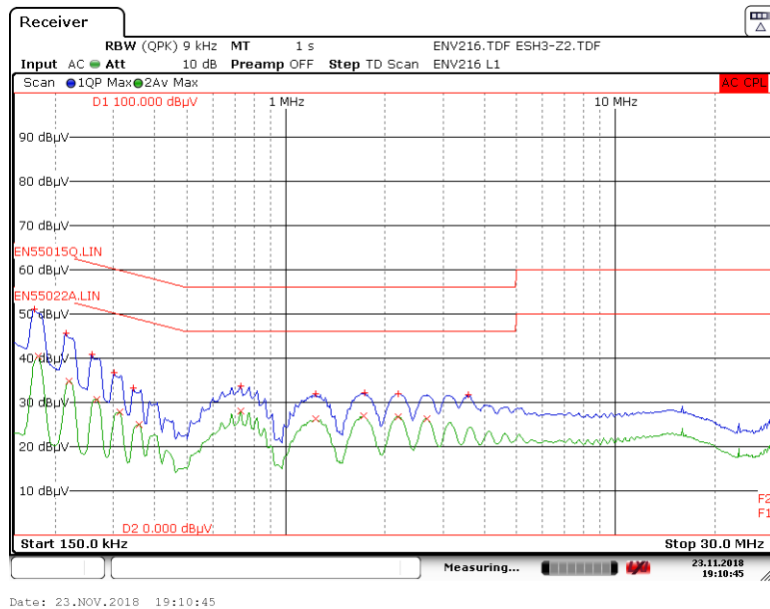


Figure 177 – Artificial Hand EMI, 5 V / 5 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

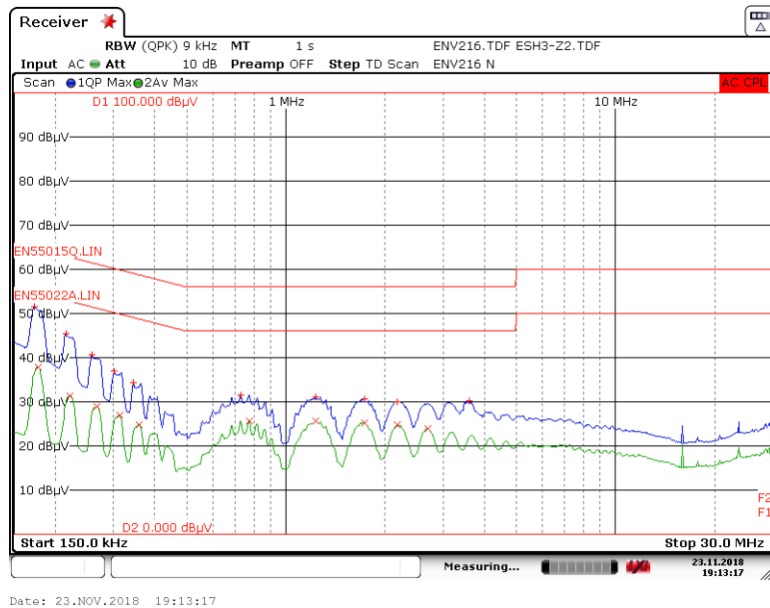


Figure 178 – Artificial Hand EMI, 5 V / 5 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.2.2 Output: 9 V / 3 A

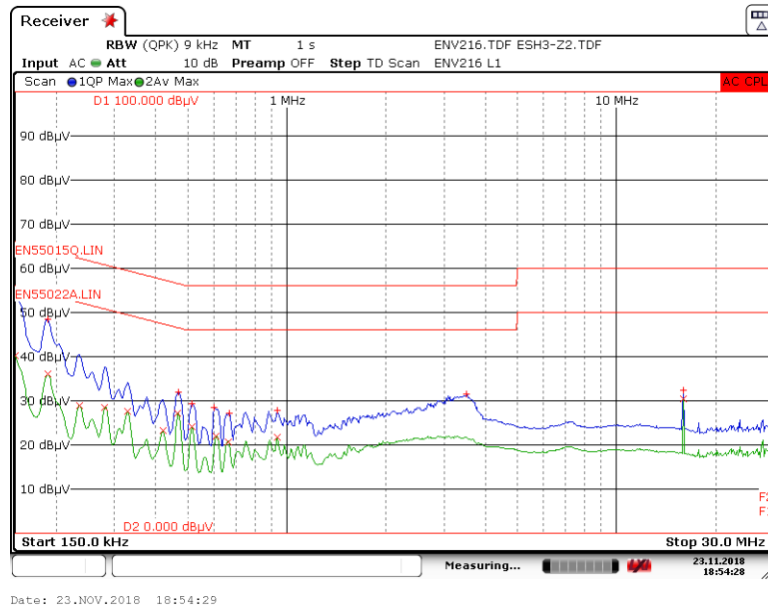


Figure 179 – Artificial Hand EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

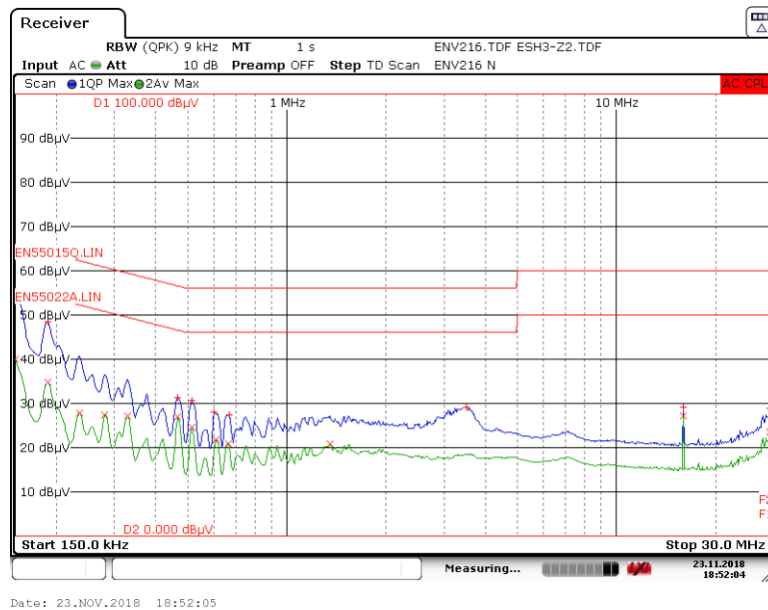


Figure 180 – Artificial Hand EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

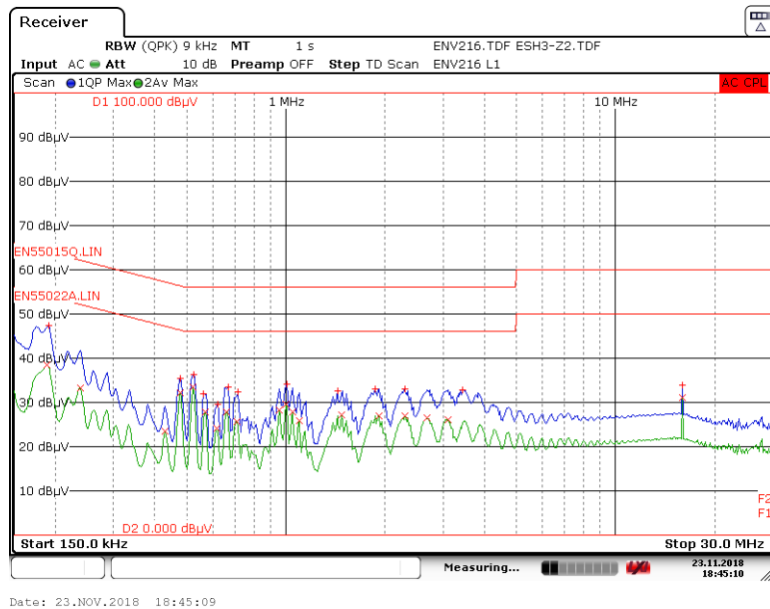


Figure 181 – Artificial Hand EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

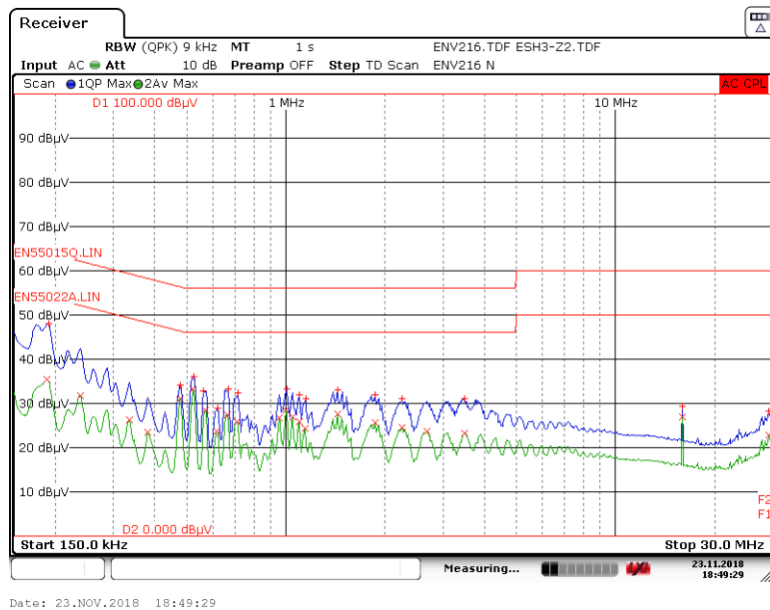


Figure 182 – Artificial Hand EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.2.3 Output: 15 V / 3 A

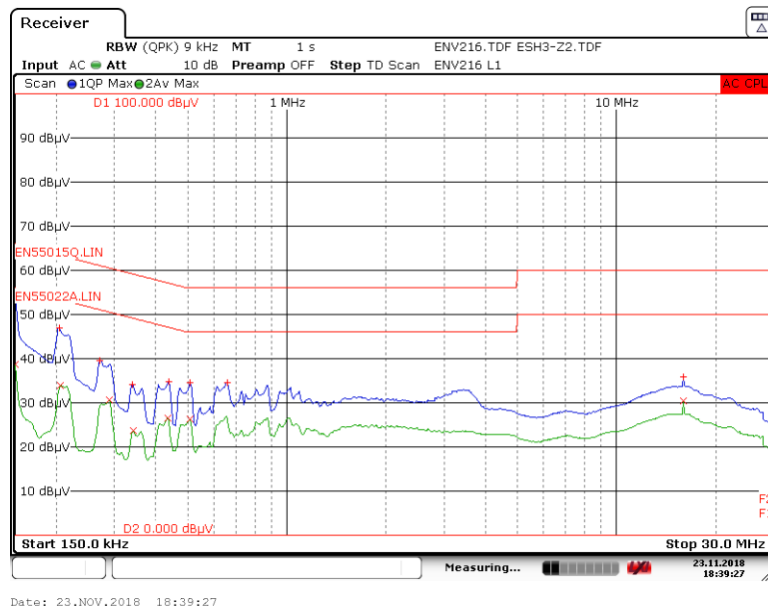


Figure 183 – Artificial Hand EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

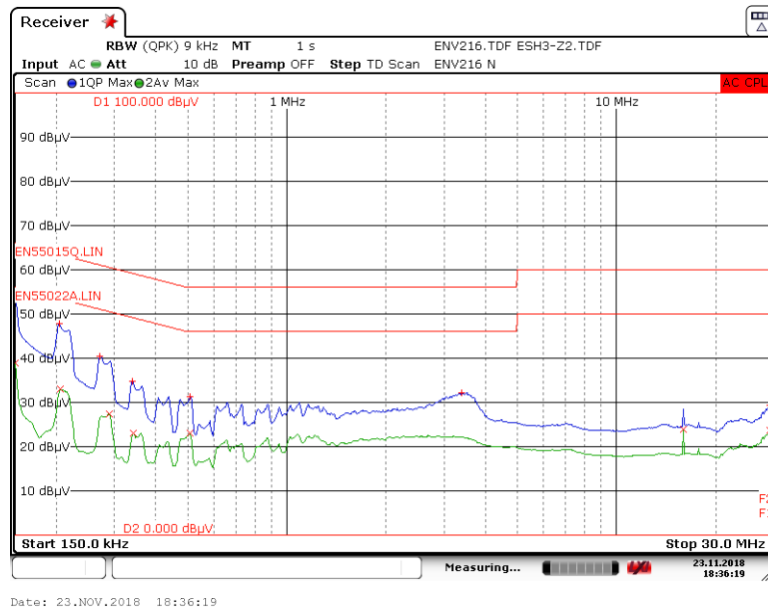


Figure 184 – Artificial Hand EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).



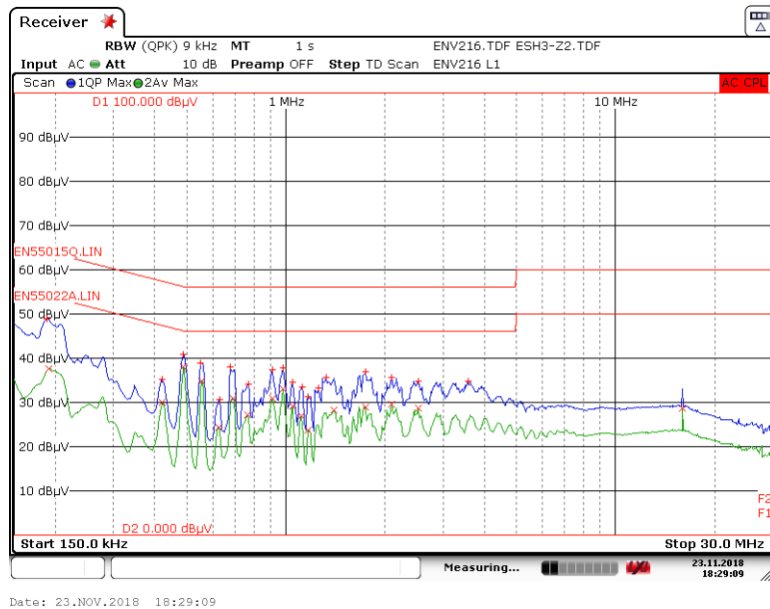


Figure 185 – Artificial Hand EMI, 15 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

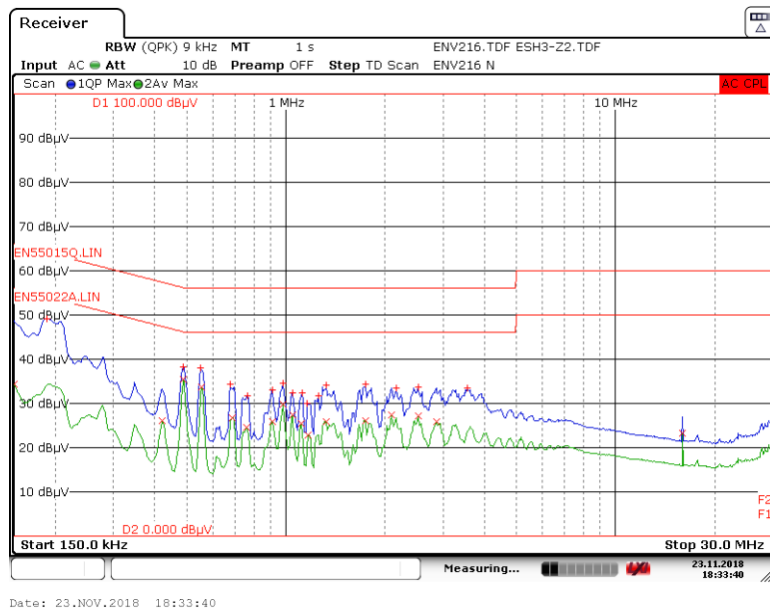


Figure 186 – Artificial Hand EMI, 15 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.2.4 Output: 20 V / 2.25 A

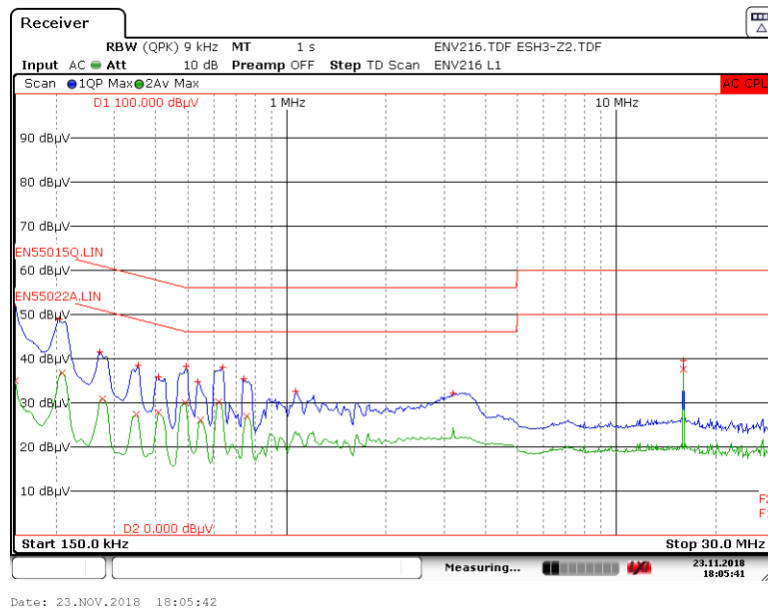


Figure 187 – Artificial Hand EMI, 20 V / 2.25 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

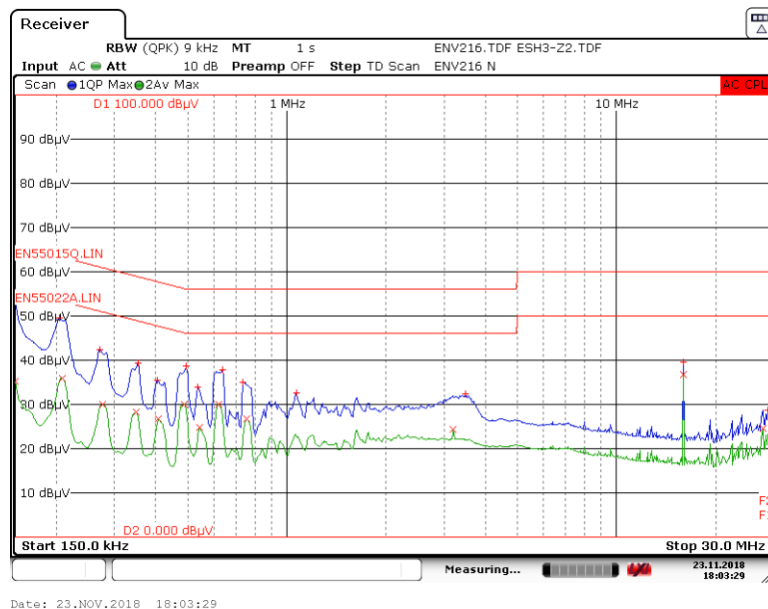


Figure 188 – Artificial Hand EMI, 20 V / 2.25 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).



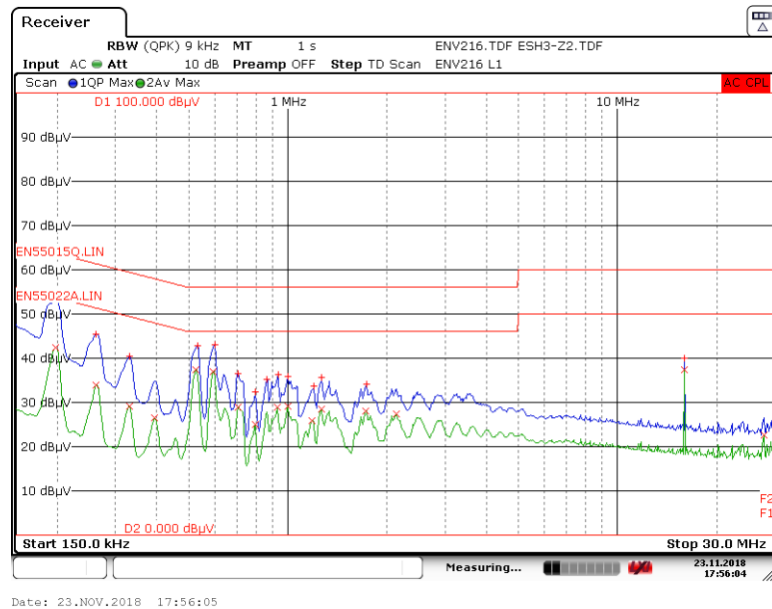


Figure 189 – Artificial Hand EMI, 20 V / 2.25 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

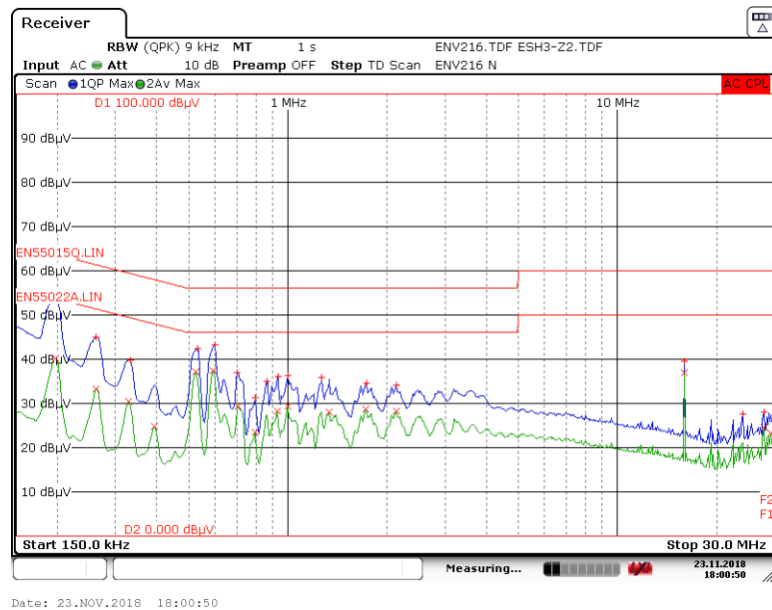


Figure 190 – Artificial Hand EMI, 20 V / 2.25 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.3 Earth Ground

20.3.1 Output: 5 V / 5 A

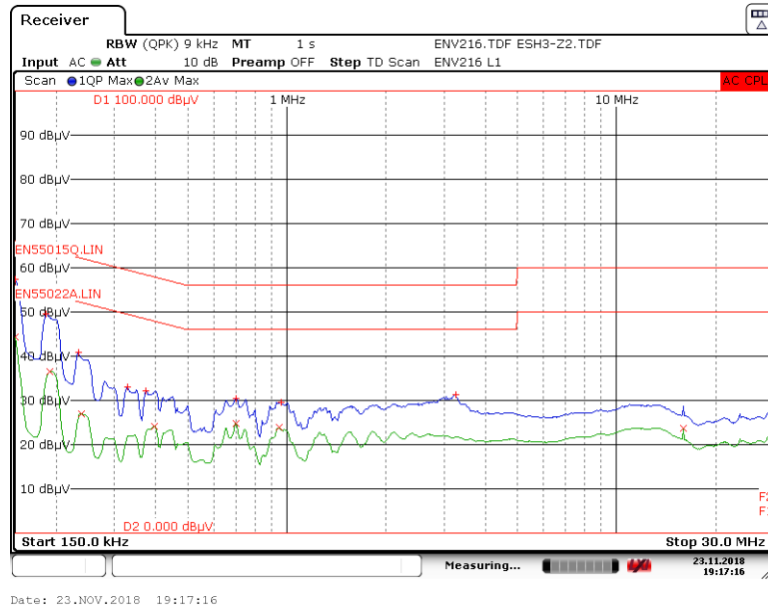


Figure 191 – Earth Ground EMI, 5 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

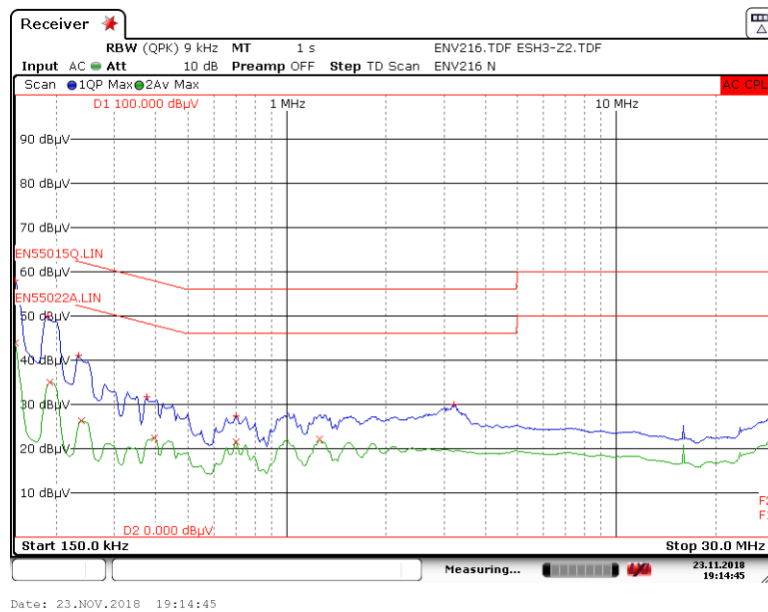


Figure 192 – Earth Ground EMI, 5 V / 5 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

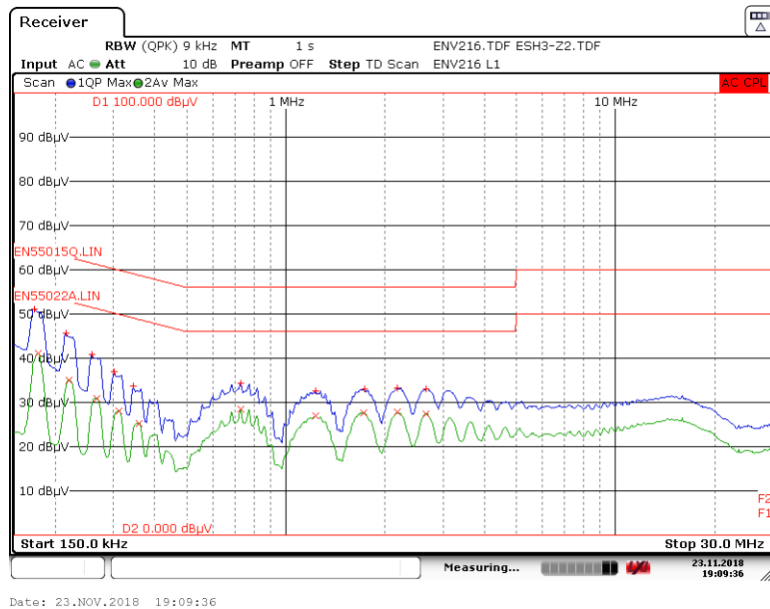


Figure 193 – Earth Ground EMI, 5 V / 5 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

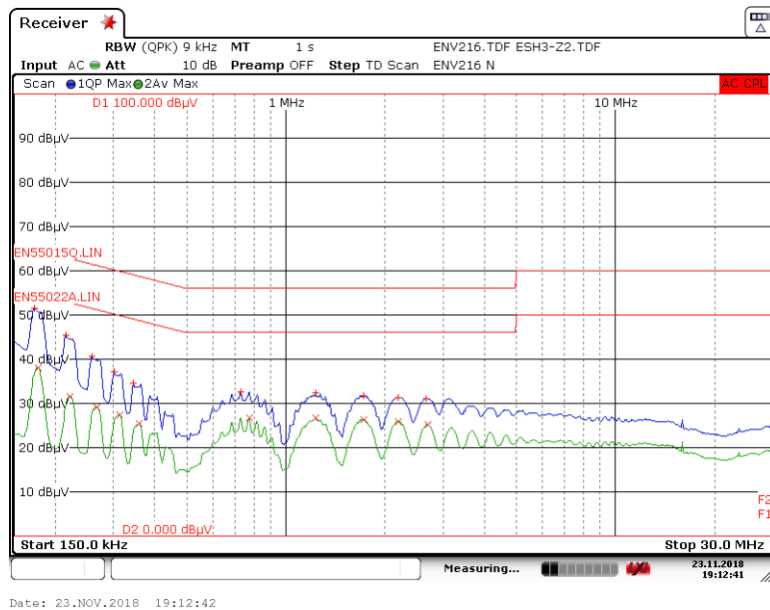


Figure 194 – Earth Ground EMI, 5 V / 5 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.3.2 Output: 9 V / 3 A

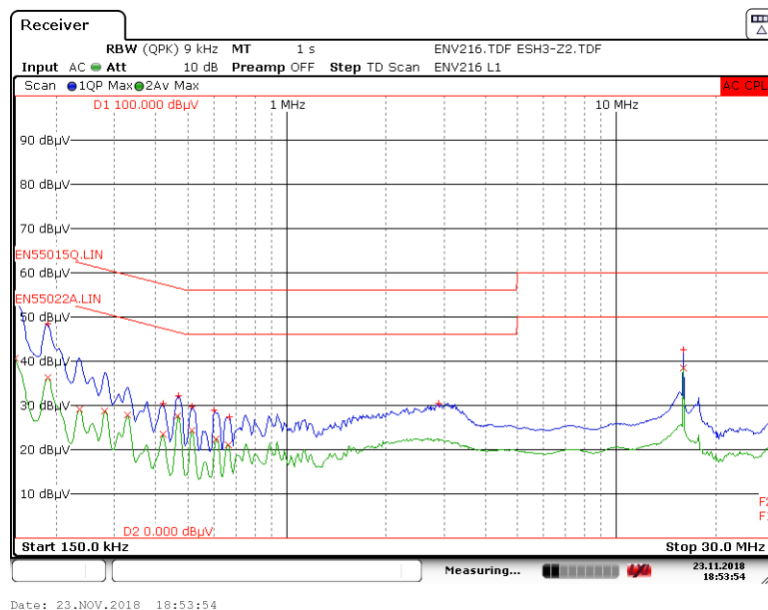


Figure 195 – Earth Ground EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

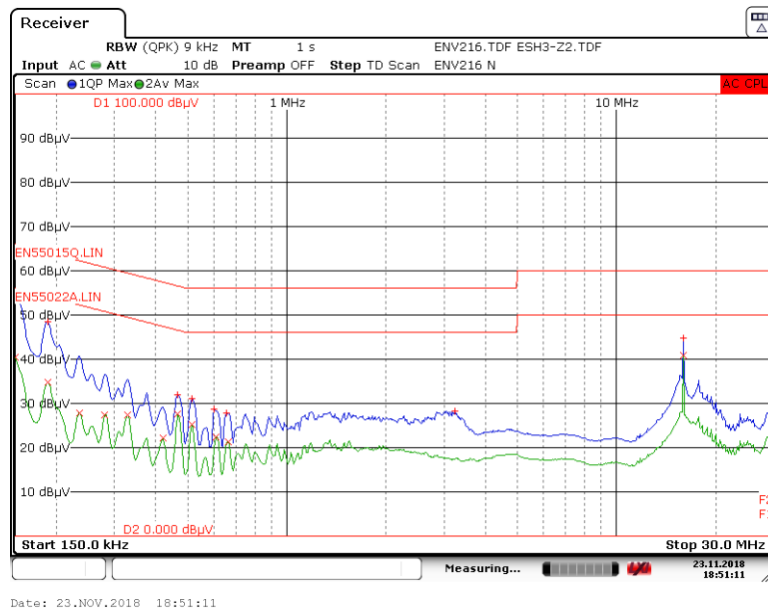


Figure 196 – Earth Ground EMI, 9 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).

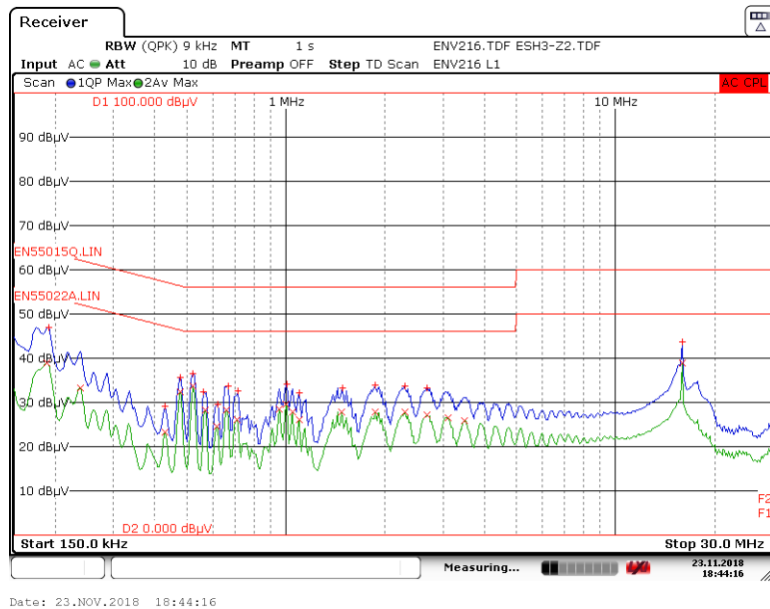


Figure 197 – Earth Ground EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

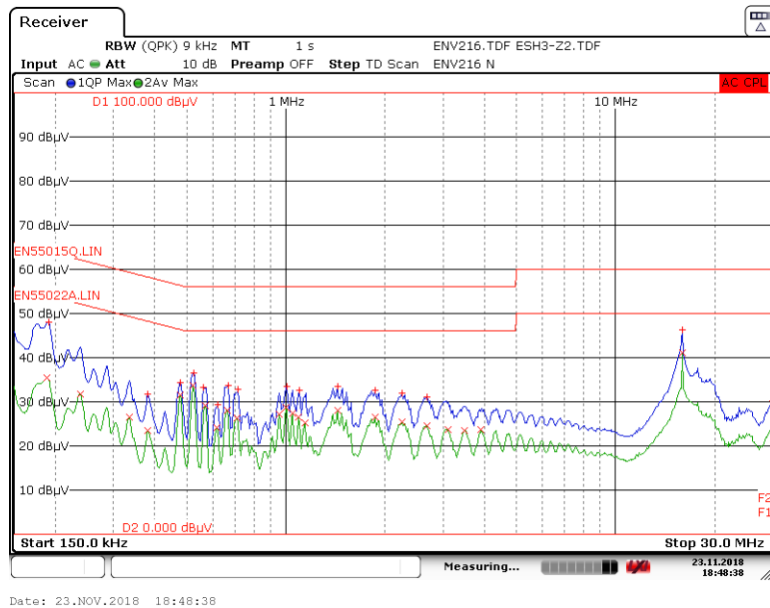


Figure 198 – Earth Ground EMI, 9 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

20.3.3 Output: 15 V / 3 A

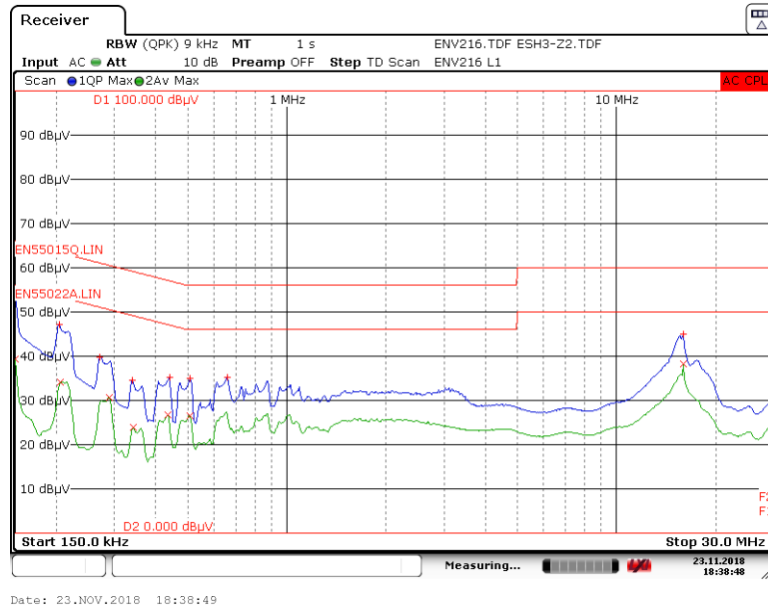


Figure 199 – Earth Ground EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

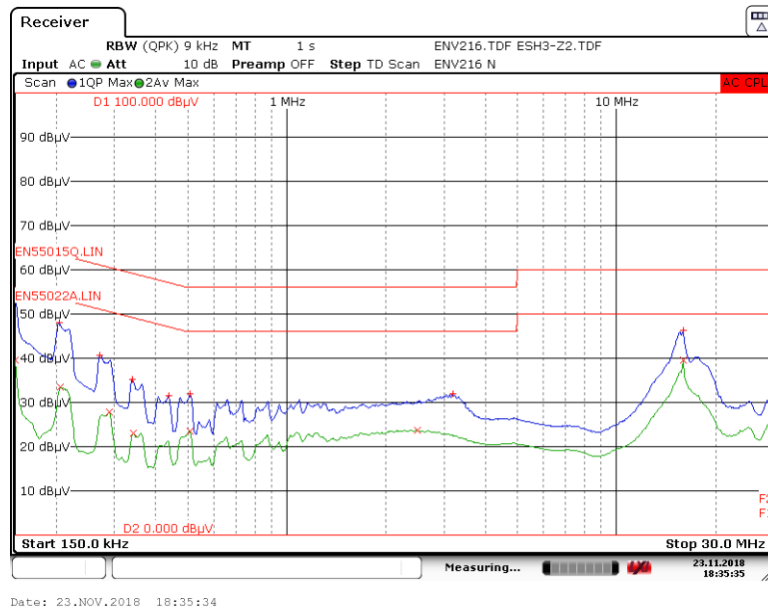


Figure 200 – Earth Ground EMI, 15 V / 3 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).



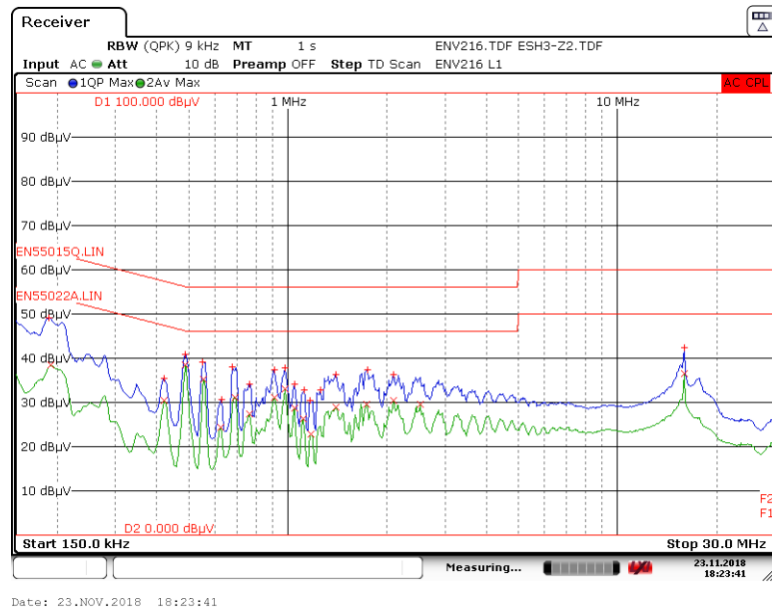


Figure 201 – Earth Ground EMI, 15 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

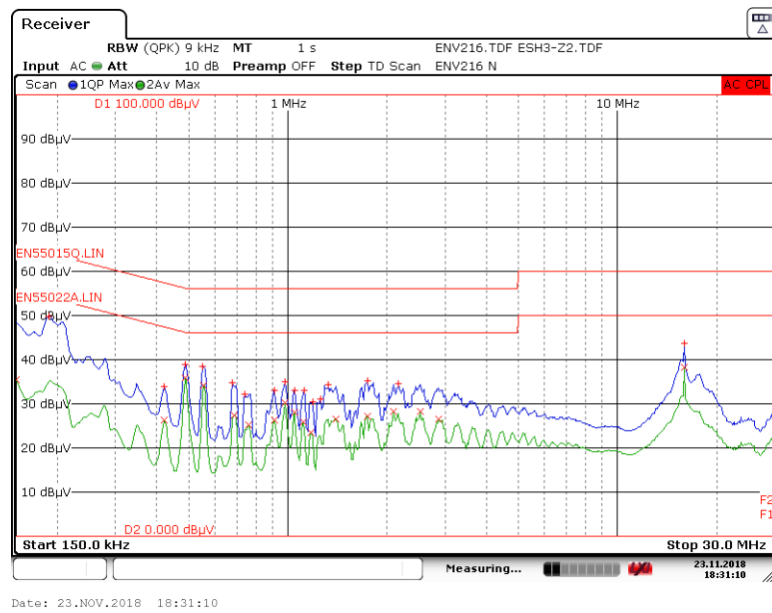


Figure 202 – Earth Ground EMI, 15 V / 3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



20.3.4 Output: 20 V / 2.25 A

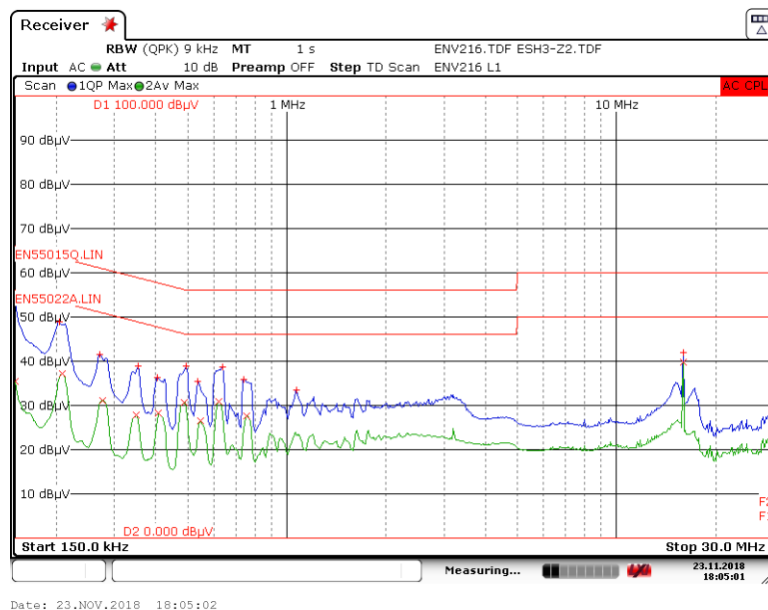


Figure 203 – Earth Ground EMI, 20 V / 2.25 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Line).

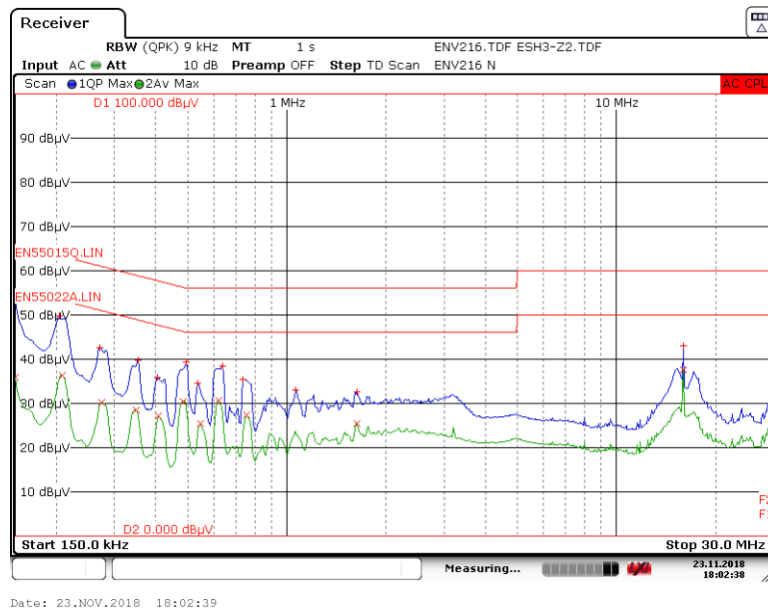
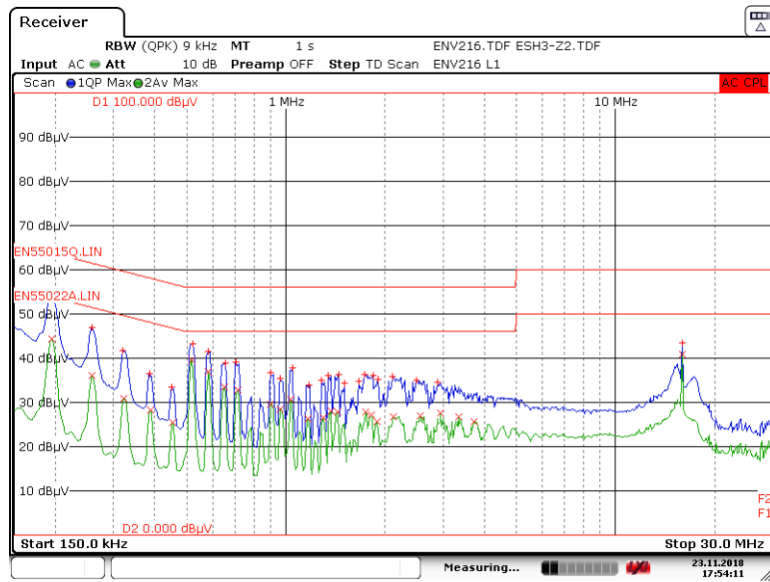
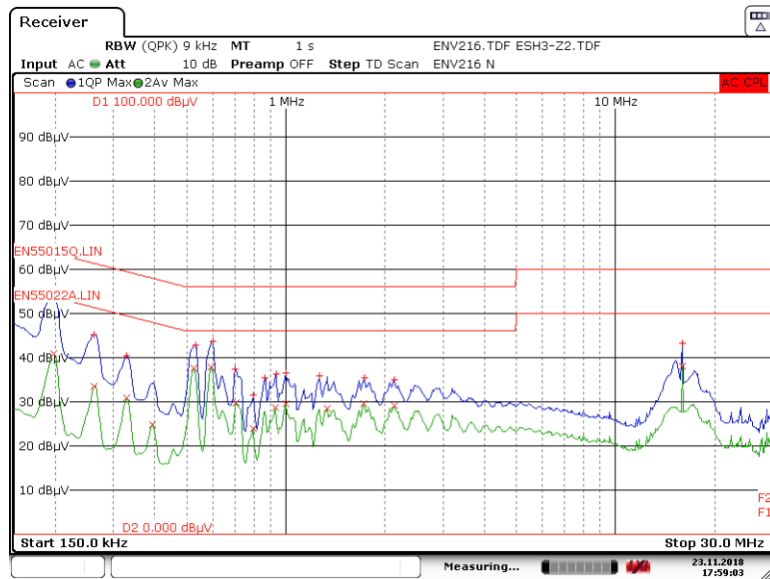


Figure 204 – Earth Ground EMI, 20 V / 2.25 A Load 115 VAC, 60 Hz, and EN55022 B Limits (Neutral).



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Figure 205 – Earth Ground EMI, 20 V / 2.25 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).



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Figure 206 – Earth Ground EMI, 20 V / 2.25 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).



21 Line Surge

The unit was subjected to ± 2000 V common mode surge and differential surge with 10 strikes for each condition. A test failure was defined as a temporary interruption of output, even if it is self-recoverable or needs operator intervention to recover, or a complete loss of function which is not recoverable.

21.1 Differential Surge

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result 5 V / 5 A (Pass/Fail)	Test Result 20 V / 2.25 A (Pass/Fail)
+2000	230	L1 to L2	0	PASS	PASS
-2000	230	L1 to L2	0	PASS	PASS
+2000	230	L1 to L2	90	PASS	PASS
-2000	230	L1 to L2	90	PASS	PASS
+2000	230	L1 to L2	180	PASS	PASS
-2000	230	L1 to L2	180	PASS	PASS
+2000	230	L1 to L2	270	PASS	PASS
-2000	230	L1 to L2	270	PASS	PASS

21.2 Common Mode Surge

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result 5 V / 5 A (Pass/Fail)	Test Result 20 V / 2.25 A (Pass/Fail)
+2000	230	L1 to PE	0	PASS	PASS
-2000	230	L1 to PE	0	PASS	PASS
+2000	230	L1 to PE	90	PASS	PASS
-2000	230	L1 to PE	90	PASS	PASS
+2000	230	L1 to PE	180	PASS	PASS
-2000	230	L1 to PE	180	PASS	PASS
+2000	230	L1 to PE	270	PASS	PASS
-2000	230	L1 to PE	270	PASS	PASS

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result 5 V / 5 A (Pass/Fail)	Test Result 20 V / 2.25 A (Pass/Fail)
+2000	230	L2 to PE	0	PASS	PASS
-2000	230	L2 to PE	0	PASS	PASS
+2000	230	L2 to PE	90	PASS	PASS
-2000	230	L2 to PE	90	PASS	PASS
+2000	230	L2 to PE	180	PASS	PASS
-2000	230	L2 to PE	180	PASS	PASS
+2000	230	L2 to PE	270	PASS	PASS
-2000	230	L2 to PE	270	PASS	PASS



22 Electrostatic Discharge

The unit was tested with ± 8 kV to ± 14 kV air discharge at the end of the USB Type-C cable and ± 8 kV to ± 12 kV at the USB receptacle with 20 strikes for each condition. Contact discharge was tested at ± 8 kV. After each strike, the discharge location is discharged to Earth with two 470 k Ω resistors in series. A test failure was defined as a temporary interruption of output, even if it is self-recoverable or needs operator intervention to recover, or a complete loss of function which is not recoverable.

22.1 Air Discharge: End of Cable

Input Voltage (VAC)	Discharge Voltage (kV)	Number Of Strikes	Discharge Location	Test Result 20 V / 2.25 A (Pass/Fail)
230	+8	20	End of cable	PASS
230	- 8	20	End of cable	PASS
230	+10	20	End of cable	PASS
230	- 10	20	End of cable	PASS
230	+12	20	End of cable	PASS
230	- 12	20	End of cable	PASS
230	+14	20	End of cable	PASS
230	- 14	20	End of cable	PASS

22.2 Air Discharge: On-board USB Receptacle

Input Voltage (VAC)	Discharge Voltage (kV)	Number Of Strikes	Discharge Location	Test Result 20 V / 2.25 A (Pass/Fail)
230	+8	20	On-board receptacle	PASS
230	- 8	20	On-board receptacle	PASS
230	+10	20	On-board receptacle	PASS
230	- 10	20	On-board receptacle	PASS
230	+12	20	On-board receptacle	PASS
230	- 12	20	On-board receptacle	PASS

22.3 Contact Discharge: End of Cable

Input Voltage (VAC)	Discharge Voltage (kV)	Number Of Strikes	Discharge Location	Test Result 20 V / 2.25 A (Pass/Fail)
230	+8	20	End of cable	PASS
230	- 8	20	End of cable	PASS

23 Revision History

Date	Author	Revision	Description & Changes	Reviewed
10-Jan-19	CS	1.0	Initial Release.	Apps & Mktg
3-Apr-19	CS	1.1	Updated Construction Material of CMC L1	Apps & Mktg
27-Apr-19	CS	1.2	Updated Winding Instructions and Illustrations of Transformer T1.	Apps & Mktg



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