Design Example Report

Title	***4.5 W Non-Isolated Buck Power Supply Using LinkSwitch™-TN2 LNK3206GQ***
Specification	60 VDC – 550 VDC Input; 15.0 V / 300 mA Outputs
Application	Automotive Application
Author	Applications Engineering Department
Document Number	DER-844Q
Date	May 29, 2020
Revision	1.1

Summary and Features

- Automotive graded BOM
- 750 V MOSFET rating for excellent surge withstand
- Highly integrated solution
- Lowest possible component count
- No optocoupler required for regulation
- <50 mW no-load consumption
- >74% efficiency at full load
- <±5% load regulation
- 85 ºC ambient temperature operation

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved.

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1 Introduction

This engineering report describes a buck converter designed to provide a non-isolated nominal output voltage of 15 V at 300 mA load from a wide input voltage range of 60 VDC to 550 VDC for automotive application. This power supply utilizes the LNK3206GQ from the LinkSwitch-TN2 family for Automotive of ICs.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

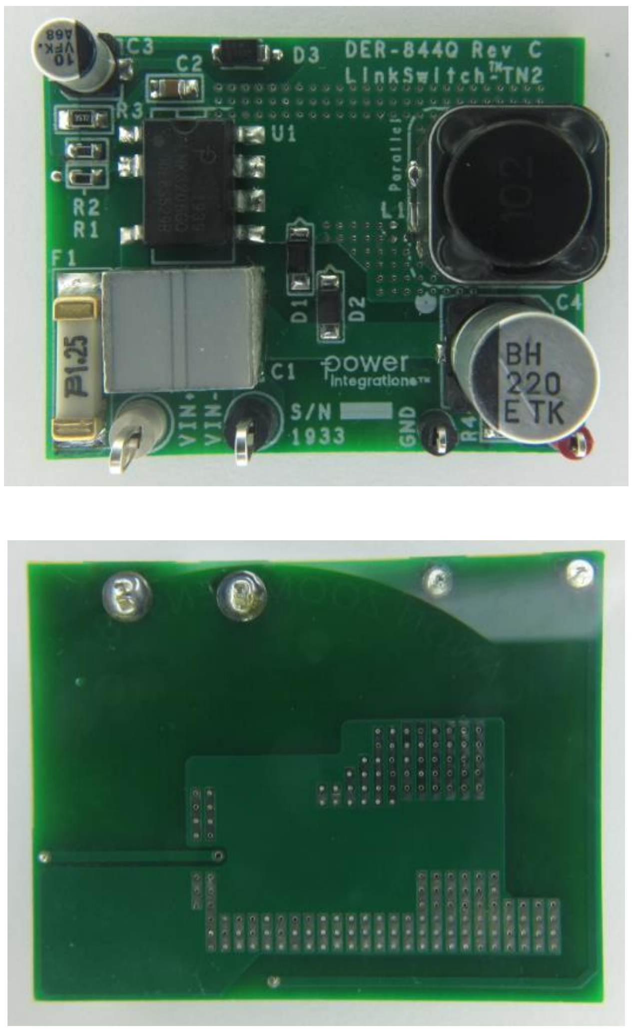

Figure 1 – Populated Circuit Board.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	60		550	VDC	
No-load Input Power (400 VDC)				50	mW	
Output1						
Output Voltage	V_{OUT}	14.25	15	15.75	V	± 5% @ 5% to 100% Load.
No Load Output Voltage	V_{OUT}			16	V	Regulation at No-load.
Output Ripple Voltage	V_{RIPPLE}			150	mV	20 MHz Bandwidth.
Output Current	I_{OUT}			300	mA	
Total Output Power						
Continuous Output Power	P_{OUT}			4.5	W	
Transient Response						
Output Voltage during transient	V_{OUT}	13.8		16.2	V	± 8%
Efficiency						
Full Load Efficiency	η	74			%	Measured at P_{OUT} 25 °C.
Environmental						
Ambient Temperature	T_{AMB}	0		85	°C	Free Convection, Sea Level.

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3 Schematic

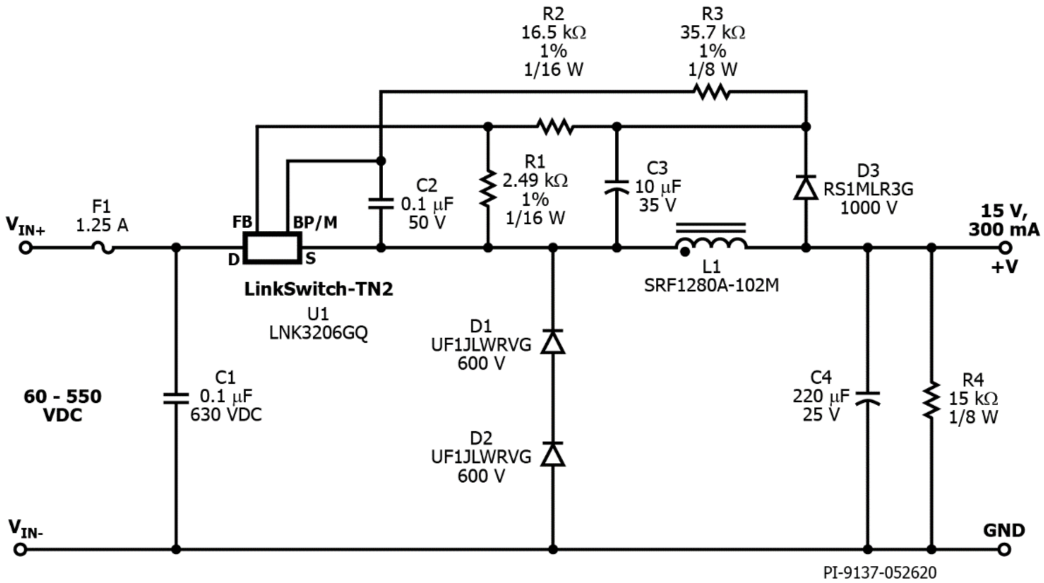

Figure 2 – Schematic.

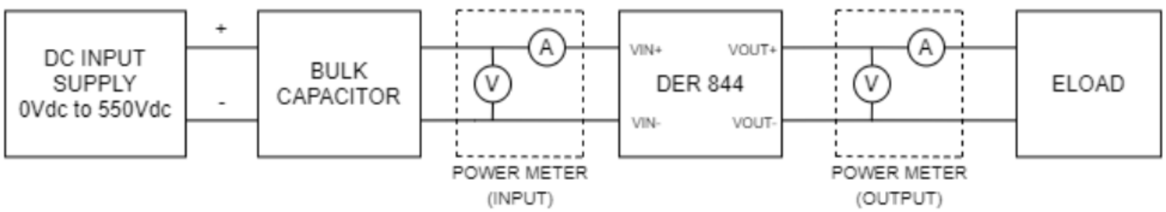

Figure 3 – Test Set-up.

4 Circuit Description

The schematic in Figure 2 shows a buck converter using LNK3206GQ. The circuit provides a non-isolated 15 V, 300 mA continuous output. In this design, automotive battery will be the intended input source of the buck circuit. To simulate battery stiff voltage source, bulk capacitors was added in the test setup during the test as shown in Figure 3.

The LinkSwitch™-TN2 family of ICs for automotive power supplies provide significant reduction in component count compared to traditional discrete solutions. Regulation is achieved using a low cost resistor divider feedback network. The switching frequency jitter feature of the LinkSwitch-TN2 family and the 66 kHz switching frequency of operation helps reduce EMI. Each device incorporates a 750 V power MOSFET, oscillator, On/Off control, a high-voltage switched current source for self-biasing, frequency jittering, fast (cycle-by-cycle) current limit, hysteretic thermal shutdown, and output and overvoltage protection circuitry onto a monolithic IC. LinkSwitch-TN2 ICs consume very little current in standby resulting in power supply designs that meet <50 mW no-load input at 400 VDC input. A full suite of protection features enable safe and reliable power supplies protecting the device and the system against input and output overvoltage faults, device over-temperature faults, lost regulation, and power supply output overload or short-circuit faults.

Due to automotive application, all component selected are AEC compliant.

4.1 *Input Filter*

Fuse F1 isolates the circuit and provides protection from component failure. A bypass capacitor C1 is added to provide a local instantaneous charge and a stable DC bus to the buck converter.

4.2 *Power Stage*

The device is self-starting from the DRAIN (D) pin with local supply decoupling provided by a small 100 nF capacitor C2 connected to the BYPASS (BP/M) pin when input is first applied. During normal operation the device is powered from output via a current limiting resistor R3. Here, the device LNK3206GQ is used in a high side driven buck converter. The supply is designed to operate in continuous conduction mode (CCM), with the peak L1 inductor current set by the LNK3206GQ internal current limit. The control scheme used is similar to the ON/OFF control used in TinySwitchTM. The on-time for each switching cycle is set by the inductance value of L1, LinkSwitch-TN2 Auto current limit and the high-voltage DC input bus across C1. Output regulation is accomplished by skipping switching cycles in response to an ON/OFF feedback signal applied to the FEEDBACK (FB) pin. This differs significantly from traditional PWM schemes that control the duty factor (duty cycle) of each switching cycle. Unlike TinySwitch, the logic of the FB pin has been inverted in LinkSwitch-TN. This allows a very simple feedback scheme to be used when the device is used in the buck converter configuration. Current into the FB pin greater than 49 ųA will inhibit the switching of the internal MOSFET, while current below this allows switching cycles to occur.

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4.3 *Output Rectification*

During the ON time of U1, current ramps in L1 and is simultaneously delivered to the load. During the OFF time, the inductor current ramps down via free-wheeling diode D1 and D2 into C4 and is delivered to the load. Diode D1 and D2 should be selected as an ultrafast diode (t_{RR} of 35 ns or better is recommended) due to CCM and high ambient temperature operation. High-voltage with low t_{RR} diode are not common. To meet 80% diode voltage derating requirement, two freewheeling diode in series was implemented.

Capacitor C4 should be selected to have an adequate ripple current rating (very low ESR type). Please see the spreadsheet output capacitor section.

4.4 *Output Feedback*

The voltage across L1 is rectified and smoothed by D3 and C3 during the off-time of U1. To provide a feedback signal, the voltage developed across C3 is divided by R1 and R2 and connected to U1's FB pin. The values of R1 and R2 are selected such that at the nominal output voltage, the voltage on the FB pin is 2 V. R1 and R2 can be optimized for better output voltage regulation and efficiency. This voltage is specified for U1 at an FB pin current of 49 μA. This allows simple feedback to meet the required overall output tolerance of ±5% at rated output current.

4.5 *PCB*

Printed Circuit Board (PCB) should be rigid enough to survive the harsh environment of automotive application. FR-4 High Tg PCB material was used in the design.

5 PCB Layout

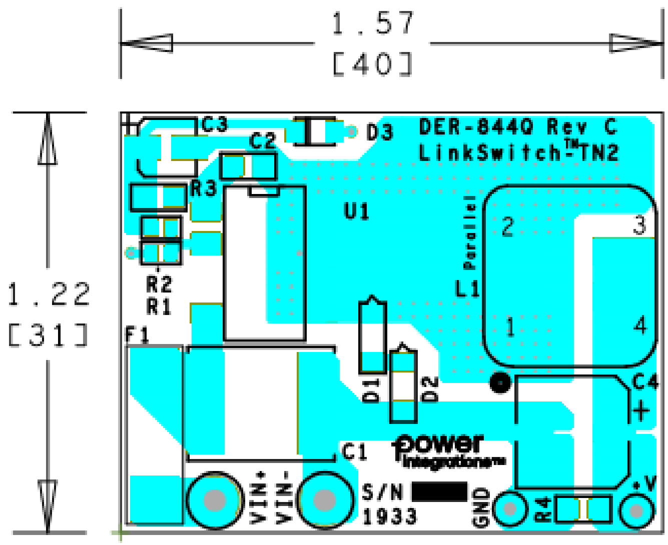

Figure 4 – Printed Circuit Board, Top View.

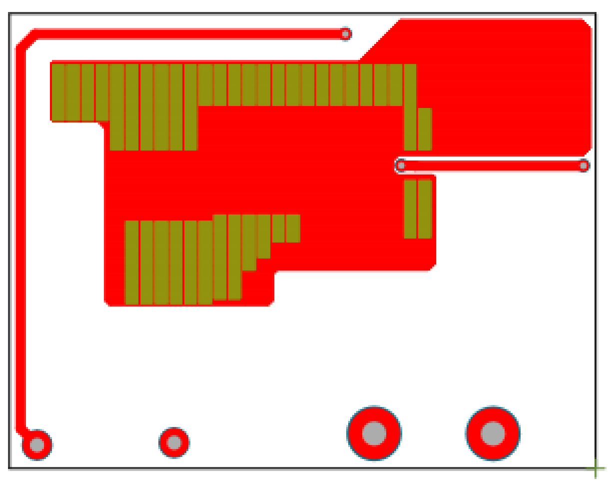

Figure 5 – Printed Circuit Board, Bottom View.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	0.1 μF, ±10%, 630 VDC, 200 VAC,Film, Stacked, 4030, -55°C ~ 125°C	LDEPF3100KA0N00	KEMET
2	1	C2	0.1 μF ±10% 50 V Ceramic X7R 0805	CL21B104KBC5PNL	Samsung
3	1	C3	10 μF, 20%, 35 V, Electrolytic, (4.30mm x 4.30mm), SMD	EEE-FK1V100UR	Panasonic
4	1	C4	220 μF, 20%, 25 V, Electrolytic, (8.30mm x 8.30mm), SMD	25TKV220M8X10.5	Rubycon
5	1	D1	Diode Standard 600 V 1 A SMT SOD123W	UF1JLW RVG	Taiwan Semi
6	1	D2	Diode Standard 600 V 1 A SMT SOD123W	UF1JLW RVG	Taiwan Semi
7	1	D3	1000 V, 800 mA, General Purpose, Fast Recovery =<500 ns, >200 mA (Io), DO-219AB, Sub SMA	RS1ML R3G	Taiwan Semi
8	1	F1	FUSE, 1.25 A, 600 VAC, SLOW, 2SMD	SF-3812TM125T-2	Bourns
9	1	L1	Shielded 2 Coil Inductor Array, 4 mH (Series), 1 mH (Parallel), 1.992 Ω Max DC Resistance (DCR), Parallel 610 mA, Automotive AEC-Q200,	SRF1280A-102M	Bourns
10	1	R1	RES, 2.49 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2491V	Panasonic
11	1	R2	RES, 16.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1652V	Panasonic
12	1	R3	RES, 35.7 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3572V	Panasonic
13	1	R4	RES, 15 Ωk, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
14	1	U1	LinkSwitch-TN2, SMD-8C	LNK3206GQ	Power Integrations

Miscellaneous

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	+V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
2	1	GND	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
3	1	VIN+	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
4	1	VIN-	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone

7 Design Spreadsheet

ACDC_LinkSwitchTN2-Buck_032720; Rev.1.3; Copyright Power Integrations 2020	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitchTN2 Buck
APPLICATION VARIABLES					
LINE VOLTAGE RANGE			Custom		AC line voltage range
VACMIN	71.00		71.00	V	Minimum AC line voltage
VACTYP			115.00	V	Typical AC line voltage
VACMAX	390.00	Info	390.00	V	The maximum AC line voltage is too high
fL			60.00	Hz	AC mains frequency
LINE RECTIFICATION TYPE	F		F		Select 'F'ull wave rectification or 'H'alf wave rectification
VOUT	15.00		15.00	V	Output voltage
IOUT	0.300		0.300	A	Average output current
EFFICIENCY_ESTIMATED			0.80		Efficiency estimate at output terminals
EFFICIENCY_CALCULATED			0.75		Calculated efficiency based on real components and operating point
POUT			4.50	W	Continuous Output Power
CIN			10.00	uF	Input capacitor
VMIN			60.1	V	Valley of the rectified input voltage
VMAX			551.5	V	Peak of the rectified maximum input AC voltage
T_AMBIENT	85		85	degC	Operating ambient temperature in degrees celcius
INPUT STAGE RESISTANCE			10	Ohms	Input stage resistance in ohms (includes fuse, thermistor, filtering components)
PLOSS_INPUTSTAGE			0.063	W	Input stage losses estimate
LINKSWITCH-TN2 VARIABLES					
OPERATION MODE			MCM		Mostly continuous mode of operation
CURRENT LIMIT MODE	STD		STD		Choose 'RED' for reduced current limit or 'STD' for standard current limit
PACKAGE	DIP-8C		DIP-8C		Select the device package
DEVICE SERIES	LNK32X6		LNK32X6		Generic LinkSwitch-TN2 device
DEVICE CODE			LNK3206		Required LinkSwitch-TN2 device
ILIMITMIN			0.450	A	Minimum current limit of the device
ILIMITTYP			0.482	A	Typical current limit of the device
ILIMITMAX			0.515	A	Maximum current limit of the device
RDSON			12.90	ohms	MOSFET's on-time drain to source resistance at 100degC
FSMIN			62000	Hz	Minimum switching frequency
FSTYP			66000	Hz	Typical switching frequency
FSMAX			70000	Hz	Maximum switching frequency
VDSON			2.00	V	MOSFET on-time drain to source voltage estimate
DUTY			0.28		Maximum duty cycle
TIME_ON			4.467	us	MOSFET conduction time at the minimum line voltage
TIME_ON_MIN			0.833	us	MOSFET conduction time at the maximum line voltage
KP_TRANSIENT		Info	0.157		KP under condition of a transient
IRMS_MOSFET			0.164	A	MOSFET RMS current
PLOSS_MOSFET			0.727	W	Primary MOSFET loss estimate
BUCK INDUCTOR PARAMETERS					
INDUCTANCE_MIN			900	uH	Minimum design inductance required for power delivery
INDUCTANCE_TYP	1000		1000	uH	Typical design inductance required for power delivery
INDUCTANCE_MAX			1100	uH	Maximum design inductance required for power delivery
TOLERANCE_INDUCTANCE			10	%	Tolerance of the design inductance
DC RESISTANCE OF INDUCTOR			2.0	ohms	DC resistance of the buck inductor
FACTOR_LOSS			0.900		Factor that accounts for "off-state" power loss to be supplied by inductor
IRMS_INDUCTOR			0.312	A	Inductor RMS current

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PLOSS_INDUCTOR			0.195	W	Inductor losses
FREEWHEELING DIODE PARAMETERS					
VF_FREEWHEELING	1.50		1.50	V	Forward voltage drop of the freewheeling diode
PIV		Warning	689	V	Peak inverse voltage of the freewheeling diode
IRMS_DIODE			0.266	A	Diode RMS current
TRR			30	ns	Required reverse recovery time of the selected diode
PLOSS_DIODE			0.535	W	Freewheeling diode losses
RECOMMENDED DIODE			BYV26C	W	Recommended freewheeling diode
BIAS/FEEDBACK PARAMETERS					
VF_BIAS			0.70	V	Forward voltage drop of the bias diode
RBIAS			2490	Ohms	Bias resistor
CBP			0.1	uF	BP pin capacitor
RFB			16200	Ohms	Feedback resistor
CFB			10	uF	Feedback capacitor
C_SOFTSTART			1-10	uF	If the output voltage is greater than 12 V or total output and system capacitance is greater than 100 uF, a soft start capacitor between 1uF and 10 uF is recommended
PLOSS_FEEDBACK			0.012	W	Feedback section losses
OUTPUT CAPACITOR					
OUTPUT VOLTAGE RIPPLE			300	mV	Desired output voltage ripple
IRIPPLE_COUT			0.300	A	Output capacitor ripple current
ESR_COUT			1000	mOhms	Maximum ESR of the output capacitor

Note: Freewheeling diode PIV warning was addressed by using two diodes in series. The design requires a low t_{RR} diode but high-voltage with low t_{RR} diode is not common. To meet the diode's PIV and low t_{RR} requirement, two freewheeling diodes in series was implemented.

8 Performance Data

8.1 *Efficiency*

8.1.1 Line Efficiency

Test Condition: Soak for 10 minutes for each line and 2 minutes integration time.

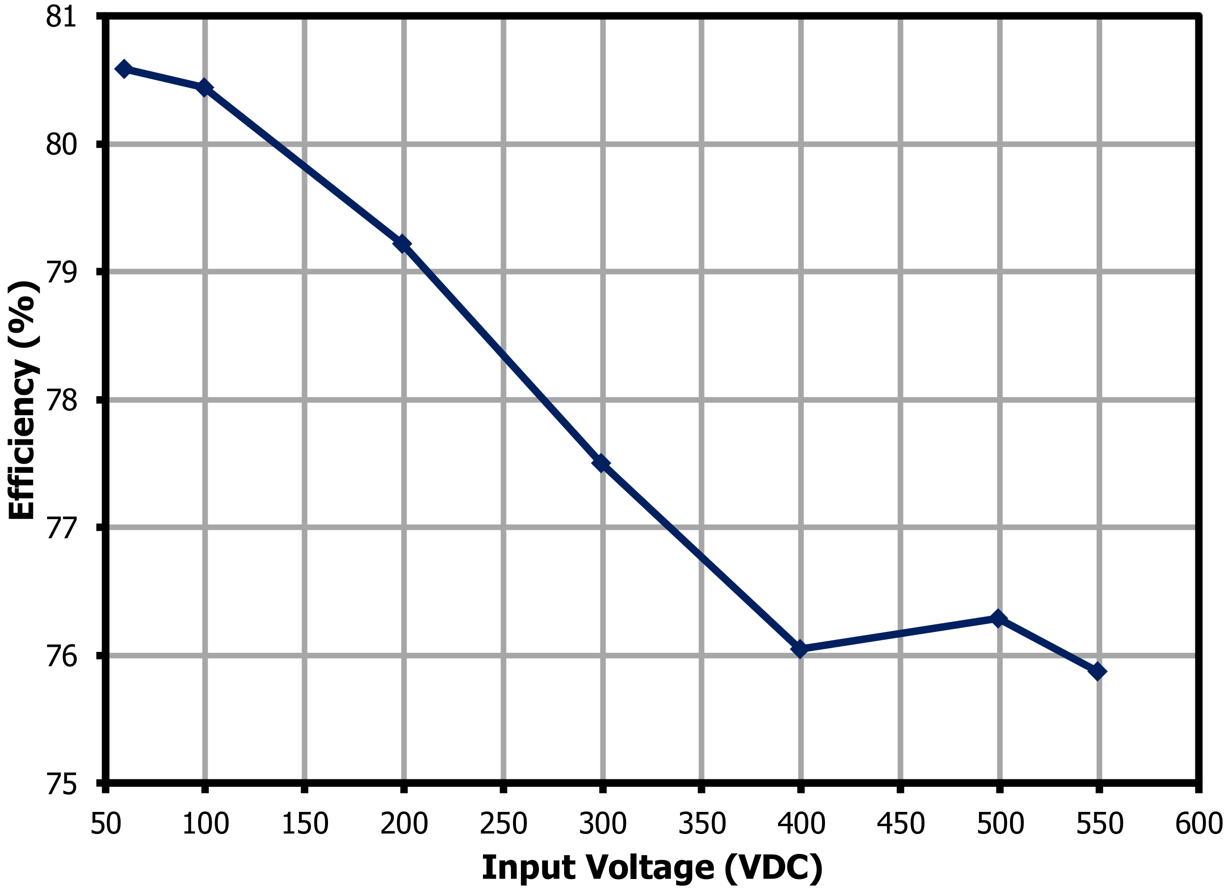

Figure 6 – Efficiency vs. Input Voltage.

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8.1.2 Load Efficiency

Test Condition: Soak for 10 minutes, 5 minutes delay per each line, 10 sec. delay for each load, and 2 minutes integration time.

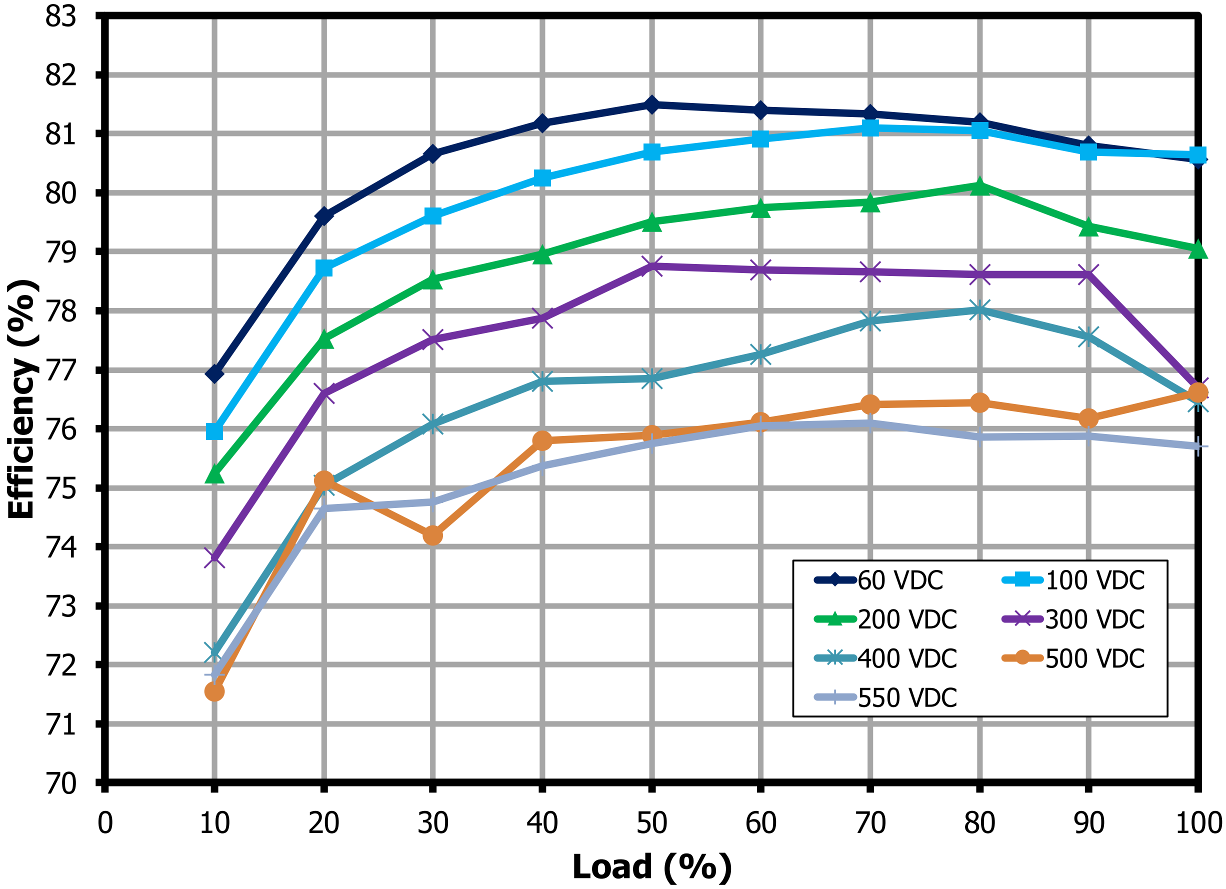

Figure 7 – Efficiency vs. Percentage Load.

8.2 ***No-Load Input Power***

Test Condition: Soak for 15 minutes each line and 1 minute integration time.

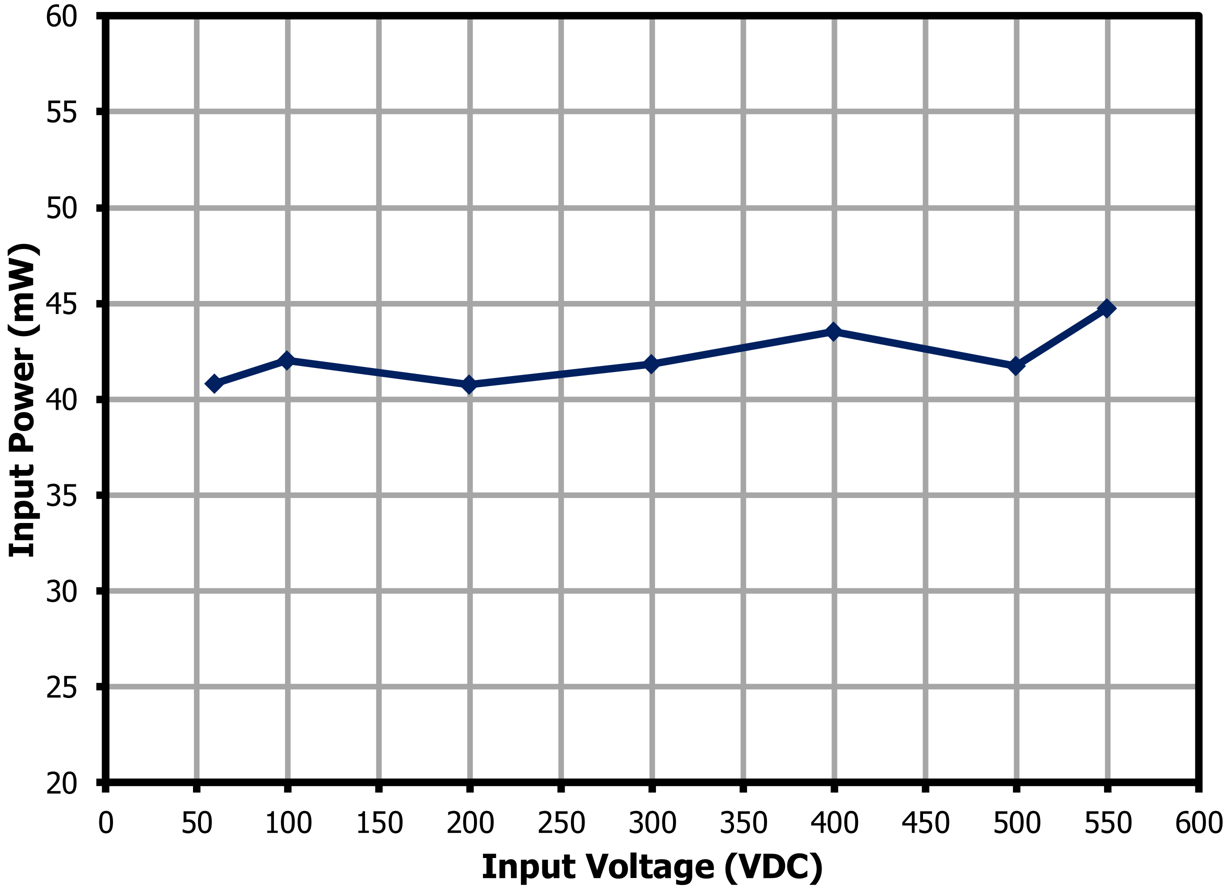

Figure 8 – No-Load Input Power vs. Line at Room Temperature.

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8.3 *Line Regulation*

Test Condition: Soak for 10 minutes for each line and 2 minutes integration time.

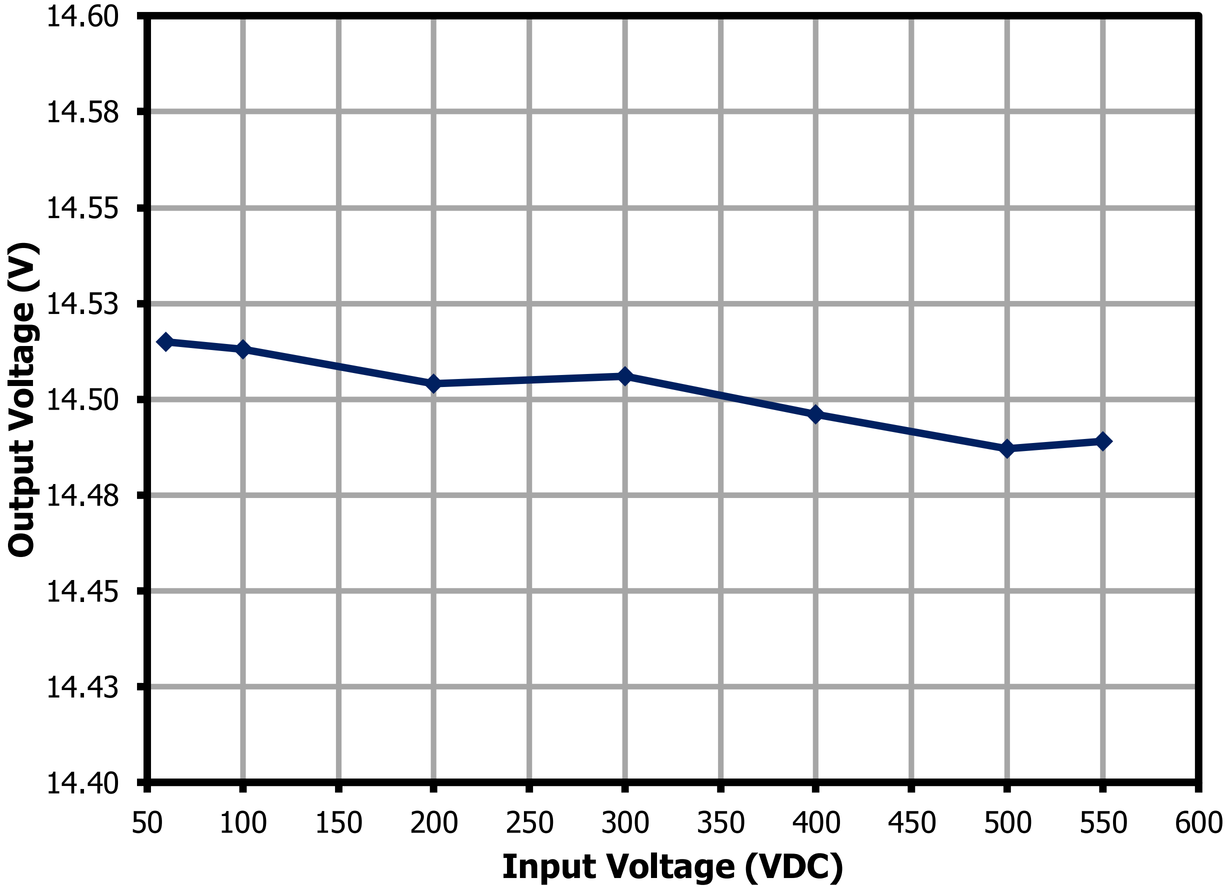

Figure 9 – Output Voltage vs. Line Voltage.

8.4 *Load Regulation*

Test Condition: Soak for 10 minutes, 5 minutes delay per each line, 10 sec. delay for each load, and 2 minutes integration time.

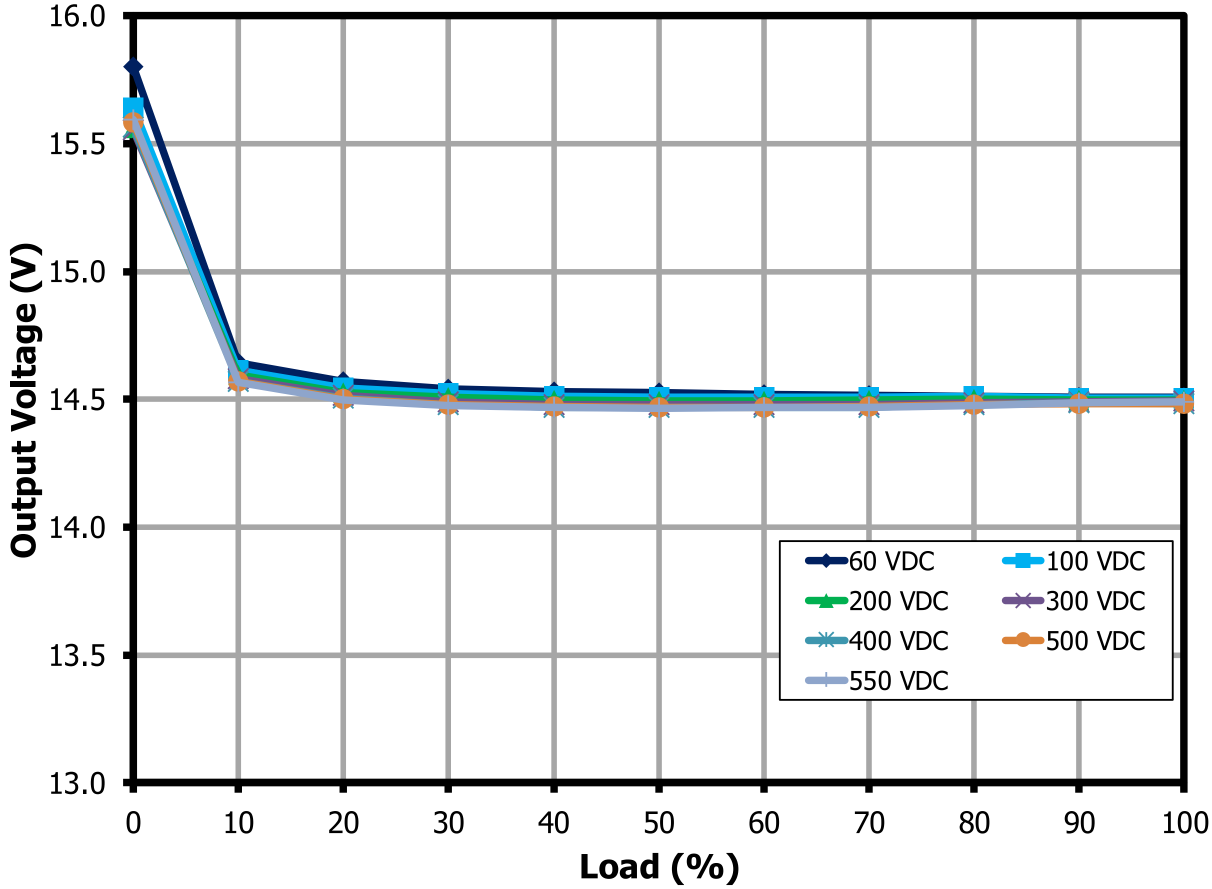

Figure 10 – Output Voltage vs. Percent Load.

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9 Waveforms

9.1 *Load Transient Response*

Test Condition: Dynamic load frequency = 100 Hz, Duty cycle = 50 %
Slew Rate = 0.5 A / µs

9.1.1 15 V Transient 0% - 100% Load Change

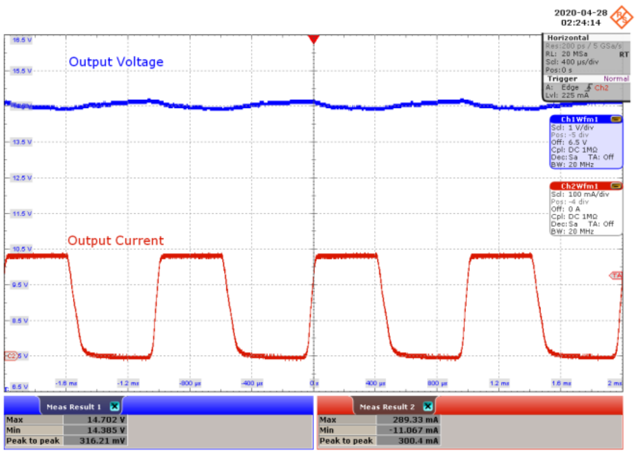

Figure 11 – 60 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.702 V, $V_{OUT(MIN)}$ = 14.385 V.

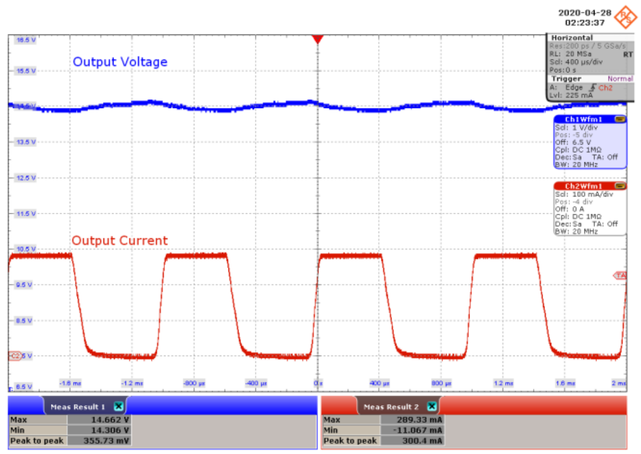

Figure 12 – 200 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.662 V, $V_{OUT(MIN)}$ = 14.306 V.

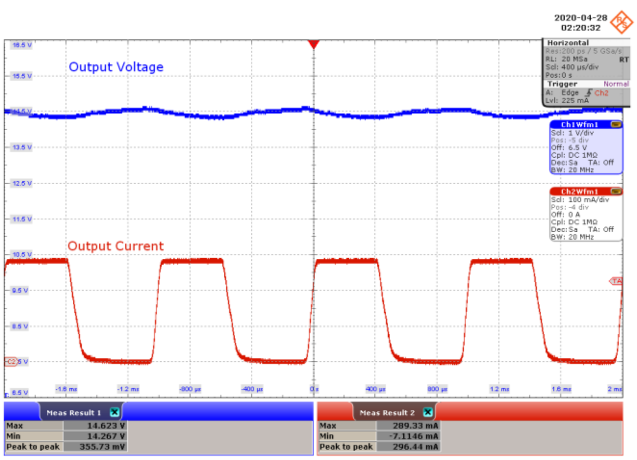

Figure 13 – 400 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.623 V, $V_{OUT(MIN)}$ = 14.267 V.

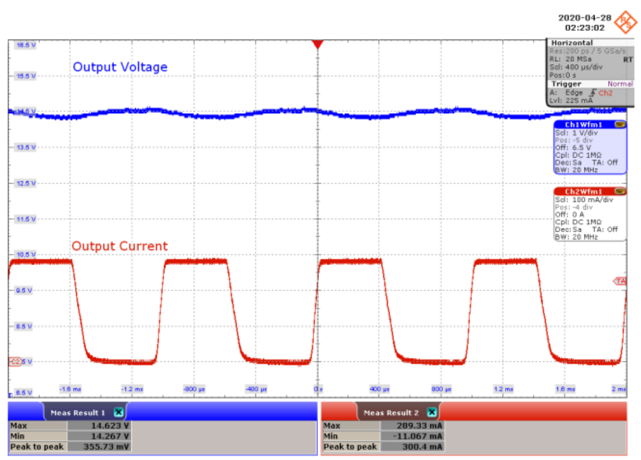

Figure 14 – 550 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.623 V, $V_{OUT(MIN)}$ = 14.267 V.

9.1.2 15 V Transient 10% - 100% Load Change

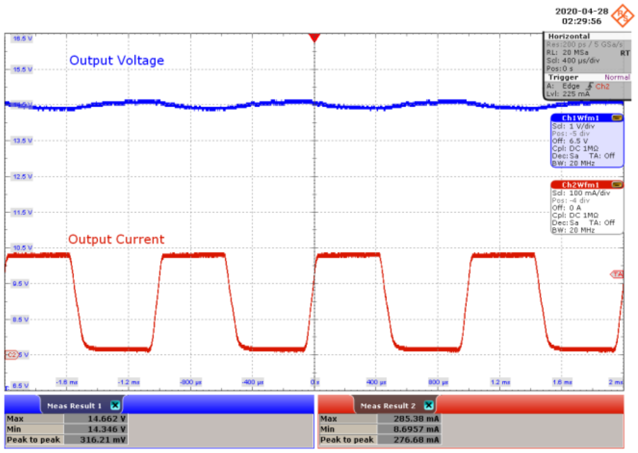

Figure 15 – 60 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.662 V, $V_{OUT(MIN)}$ = 14.346 V.

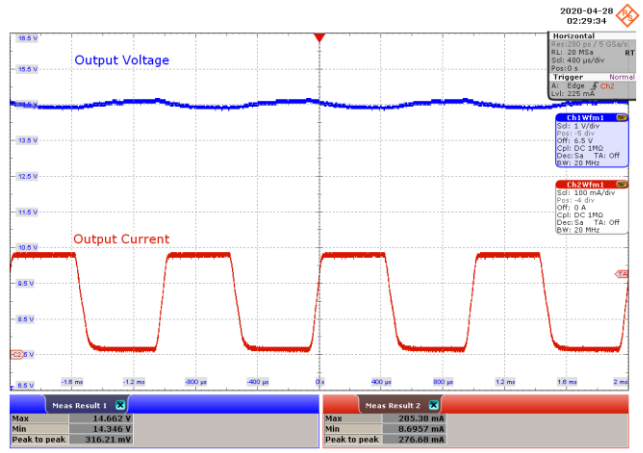

Figure 16 – 200 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.662 V, $V_{OUT(MIN)}$ = 14.346 V.

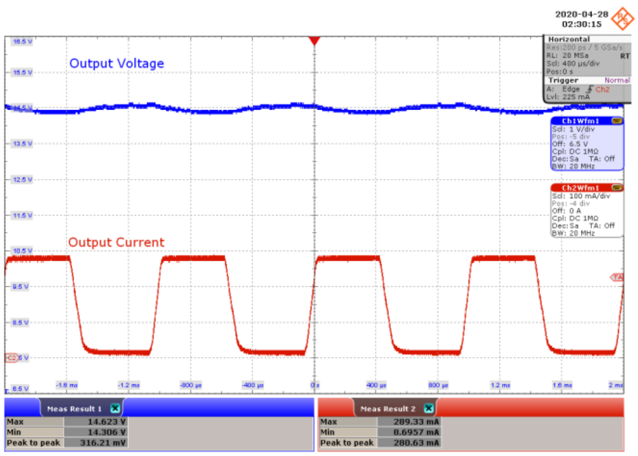

Figure 17 – 400 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.623 V, $V_{OUT(MIN)}$ = 14.306 V.

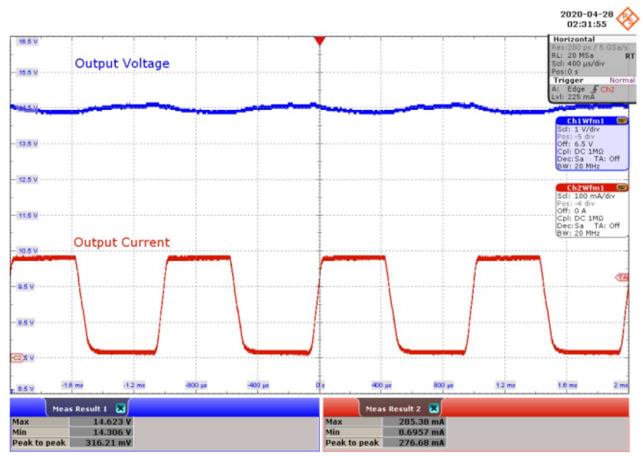

Figure 18 – 550 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.623 V, $V_{OUT(MIN)}$ = 14.306 V.

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9.1.3 15 V Transient 50% - 100% Load Change

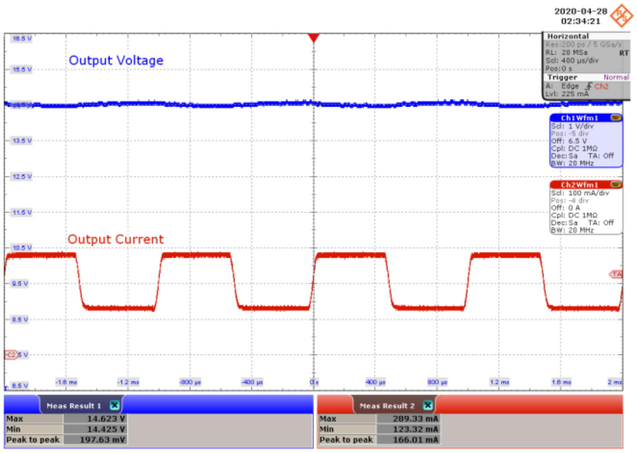

Figure 19 – 60 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.623 V, $V_{OUT(MIN)}$ = 14.425 V.

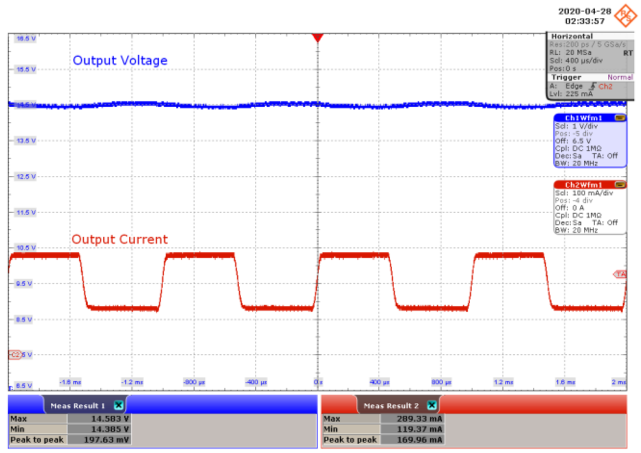

Figure 20 – 200 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.583 V, $V_{OUT(MIN)}$ = 14.385 V.

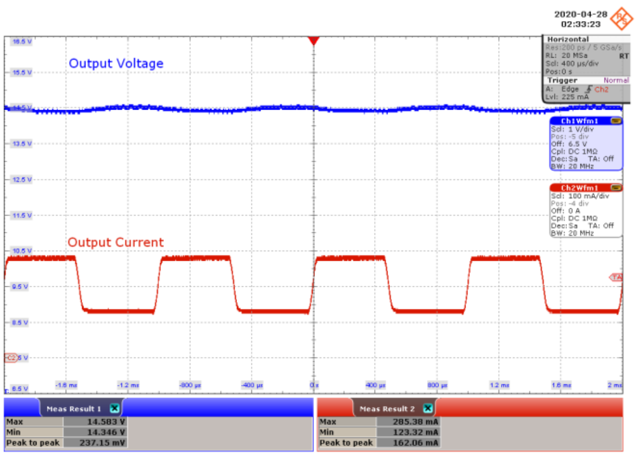

Figure 21 – 400 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.583 V, $V_{OUT(MIN)}$ = 14.346 V.

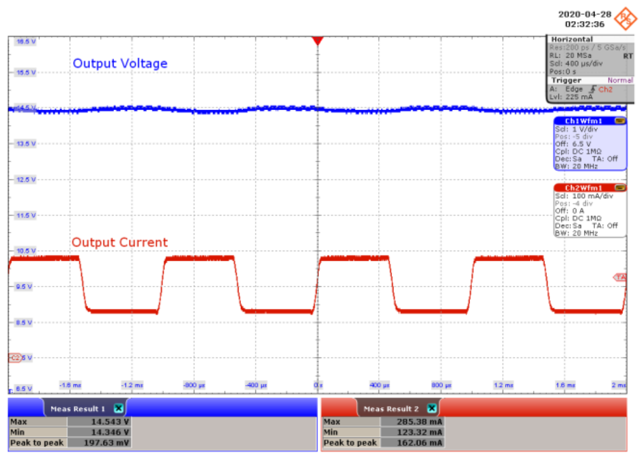

Figure 22 – 550 VDC Input.
CH1: V_{OUT}, 1 V / div., 400 µs / div.
CH2: I_{OUT}, 100 mA / div., 400 µs / div.
$V_{OUT(MAX)}$ = 14.543 V, $V_{OUT(MIN)}$ = 14.346 V.

9.2 ***Switching Waveforms***

9.2.1 Primary MOSFET Drain-Source Voltage and Current at Normal Operation

9.2.1.1 100% Load CC

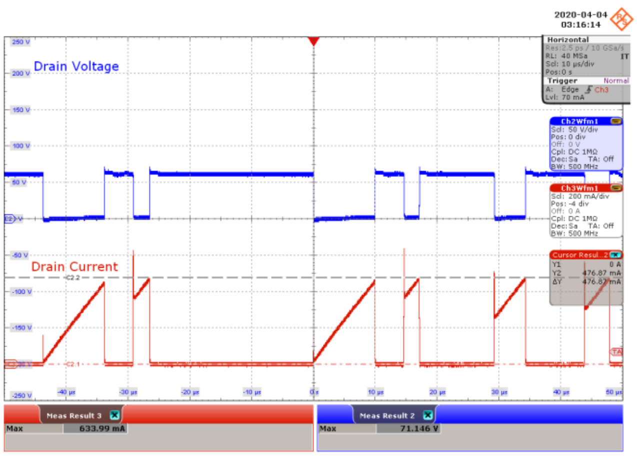

Figure 23 – 60 VDC Input.
CH2: V_{DS}, 50 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 71.146 V, $I_{DS(MAX)}$ = 633.99 mA.

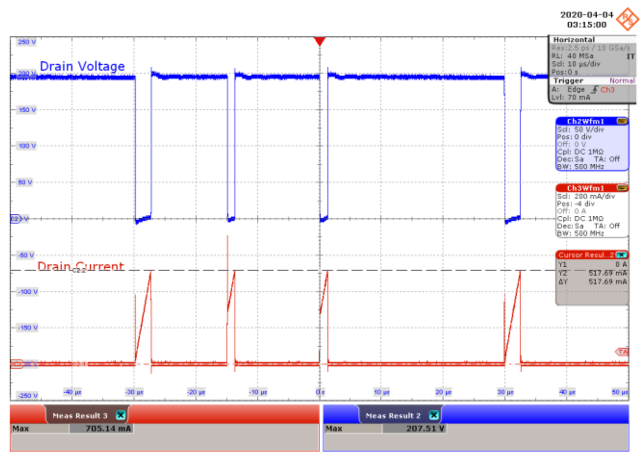

Figure 24 – 200 VDC Input.
CH2: V_{DS}, 50 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 207.51 V, $I_{DS(MAX)}$ = 705.14 mA.

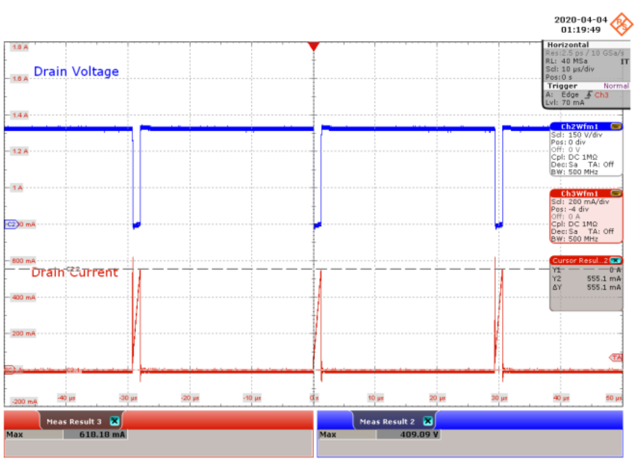

Figure 25 – 400 VDC Input.
CH2: V_{DS}, 150 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 409.09 V, $I_{DS(MAX)}$ = 618.18 mA.

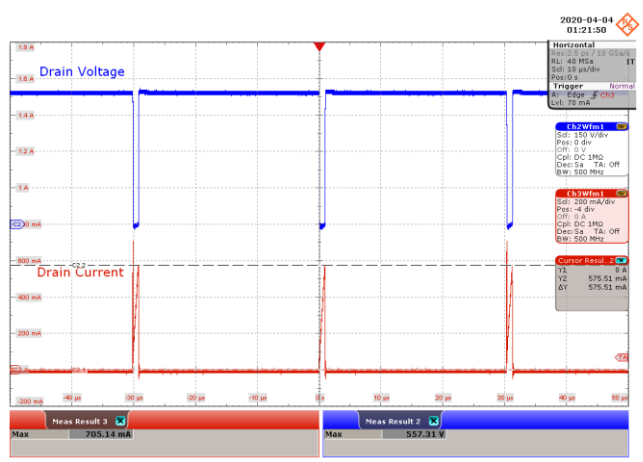

Figure 26 – 550 VDC Input.
CH2: V_{DS}, 150 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 557.31 V, $I_{DS(MAX)}$ = 705.14 mA.

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9.2.1.2 100% Load CR

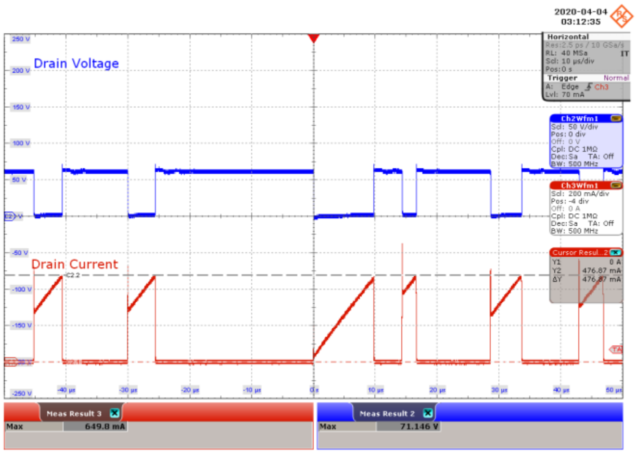

Figure 27 – 60 VDC Input.
CH2: $V_{DS,}$ 50 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 71.146 V, $I_{DS(MAX)}$ = 649.8 mA.

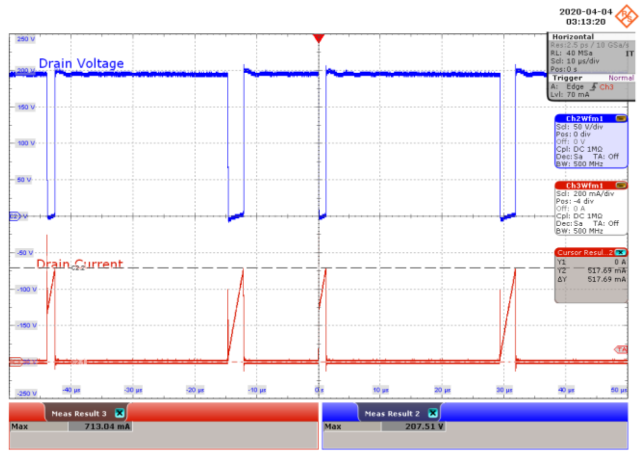

Figure 28 – 200 VDC Input.
CH2: $V_{DS,}$ 50 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 207.51 V, $I_{DS(MAX)}$ = 713.04 mA.

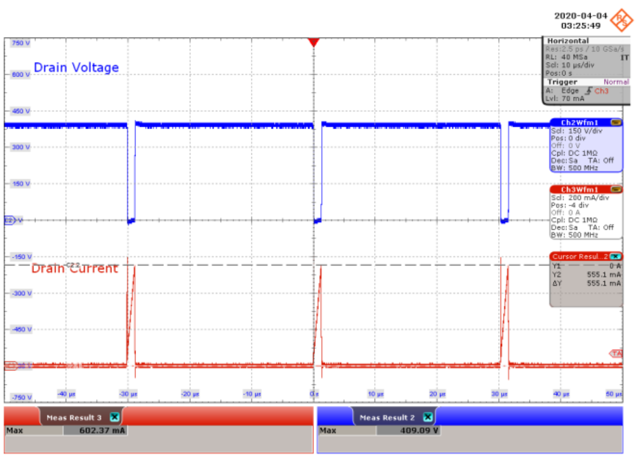

Figure 29 – 400 VDC Input.
CH2: $V_{DS,}$ 150 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 409.09 V, $I_{DS(MAX)}$ = 602.37 mA.

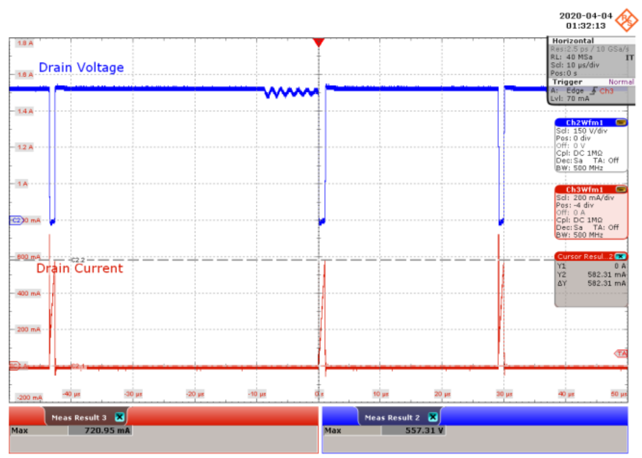

Figure 30 – 550 VDC Input.
CH2: $V_{DS,}$ 150 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 557.31 V, $I_{DS(MAX)}$ = 720.95 mA.

9.2.1.3 0% Load CC

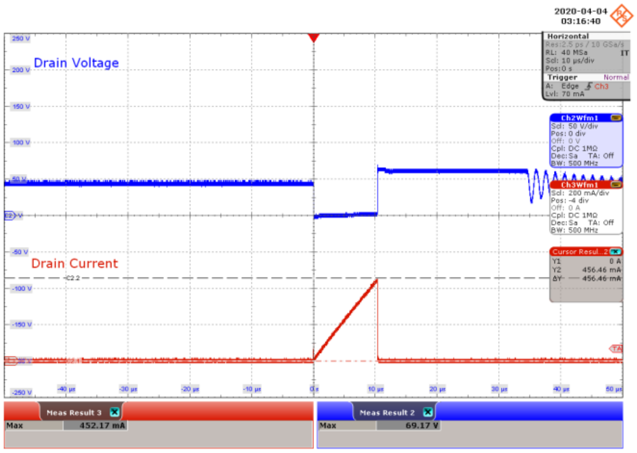

Figure 31 – 60 VDC Input.
CH2: V_{DS}, 50 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 69.17 V, $I_{DS(MAX)}$ = 452.17 mA.

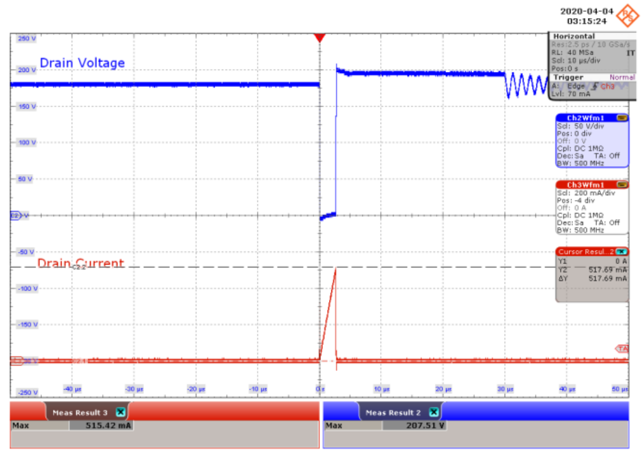

Figure 32 – 200 VDC Input.
CH2: V_{DS}, 50 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 207.51 V, $I_{DS(MAX)}$ = 515.42 mA.

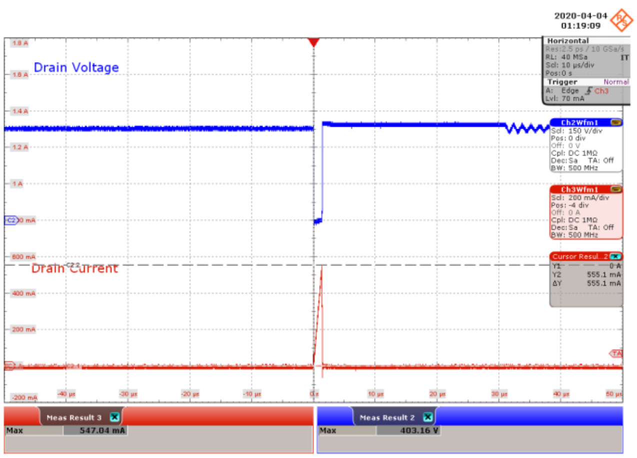

Figure 33 – 400 VDC Input.
CH2: V_{DS}, 150 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 403.16 V, $I_{DS(MAX)}$ = 547.04 mA.

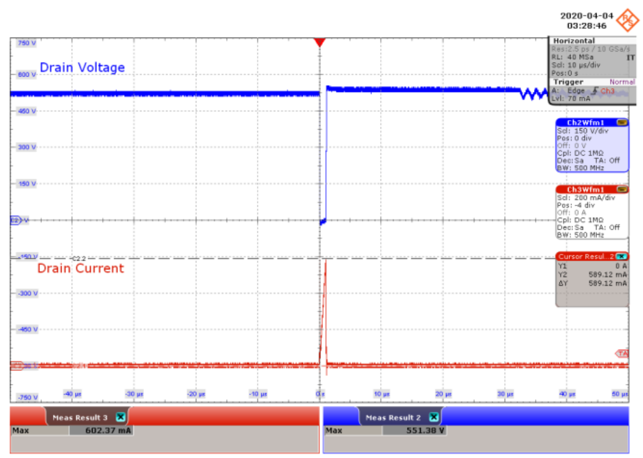

Figure 34 – 550 VDC Input.
CH2: V_{DS}, 150 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 551.38 V, $I_{DS(MAX)}$ = 602.37 mA.

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9.2.1.4 0% Load CR

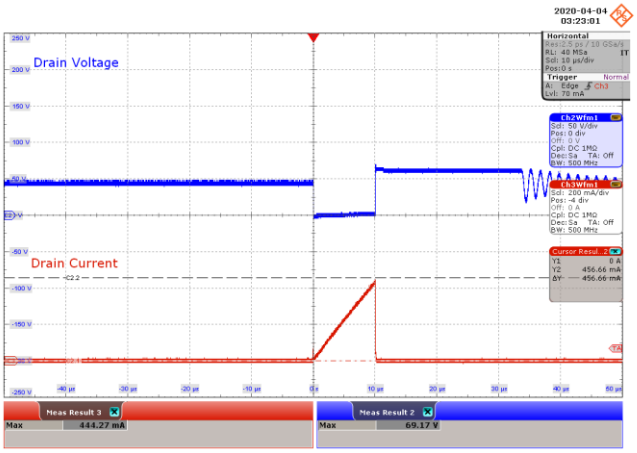

Figure 35 – 60 VDC Input.
CH2: V_{DS}, 50 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 69.17 V, $I_{DS(MAX)}$ = 444.27 mA.

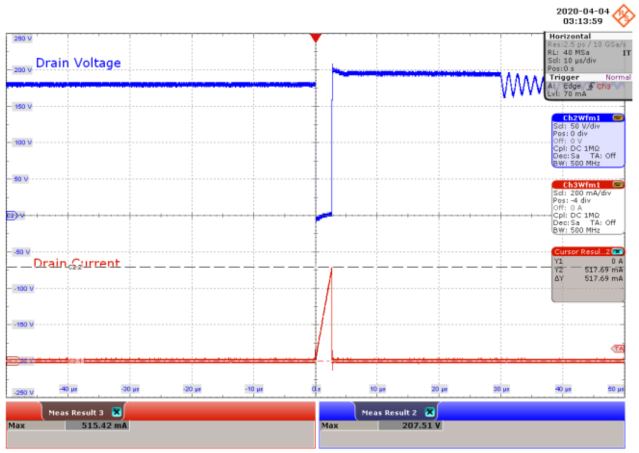

Figure 36 – 200 VDC Input.
CH2: V_{DS}, 50 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 207.51 V, $I_{DS(MAX)}$ = 515.42 mA.

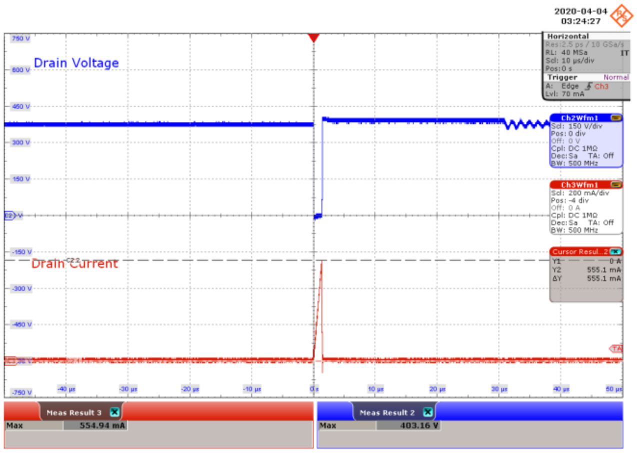

Figure 37 – 400 VDC Input.
CH2: V_{DS}, 150 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 403.16 V, $I_{DS(MAX)}$ = 554.94 mA.

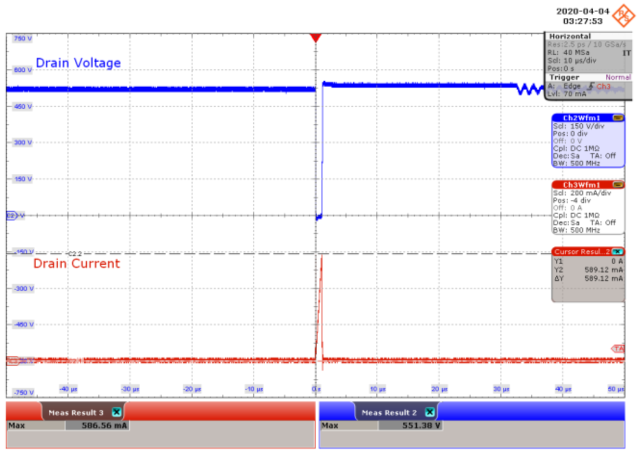

Figure 38 – 550 VDC Input.
CH2: V_{DS}, 150 V / div., 10 µs / div.
CH3: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$ = 551.38 V, $I_{DS(MAX)}$ = 586.56 mA.

9.2.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

9.2.2.1 100% Load CC

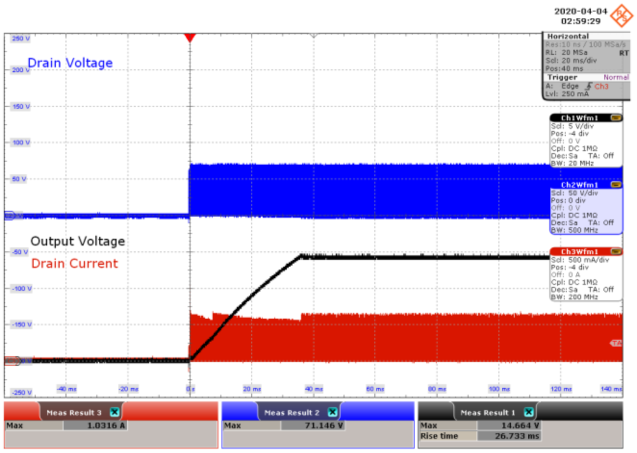

Figure 39 – 60 VDC Input.
CH1: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH2: $V_{DS,}$ 50 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 71.146 V, $I_{DS(MAX)}$ = 1.0316 A.
$V_{OUT(MAX)}$ = 14.664 V.

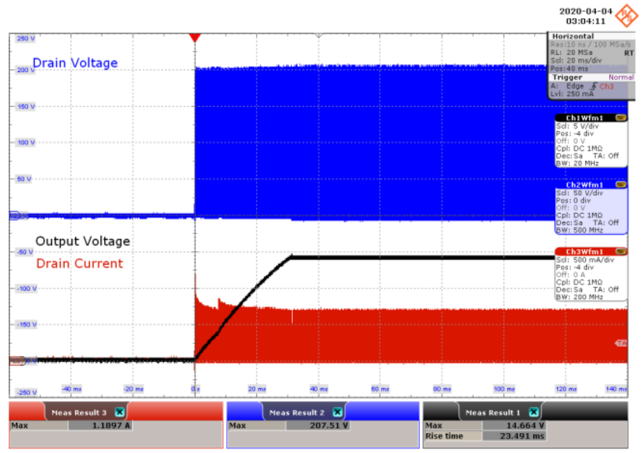

Figure 40 – 200 VDC Input.
CH1: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH2: $V_{DS,}$ 50 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 207.51 V, $I_{DS(MAX)}$ = 1.1897 A.
$V_{OUT(MAX)}$ = 14.664 V.

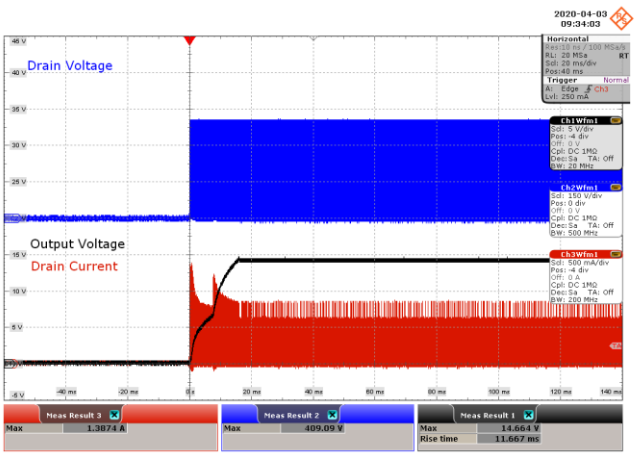

Figure 41 – 400 VDC Input.
CH1: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH2: $V_{DS,}$ 150 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 409.09 V, $I_{DS(MAX)}$ = 1.3874 A.
$V_{OUT(MAX)}$ = 14.664 V.

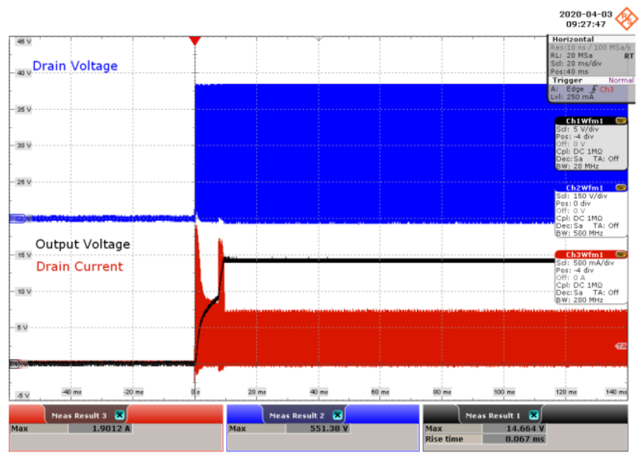

Figure 42 – 550 VDC Input.
CH1: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH2: $V_{DS,}$ 150 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 551.38 V, $I_{DS(MAX)}$ = 1.9012 A.
$V_{OUT(MAX)}$ = 14.664 V.

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9.2.2.2 100% Load CR

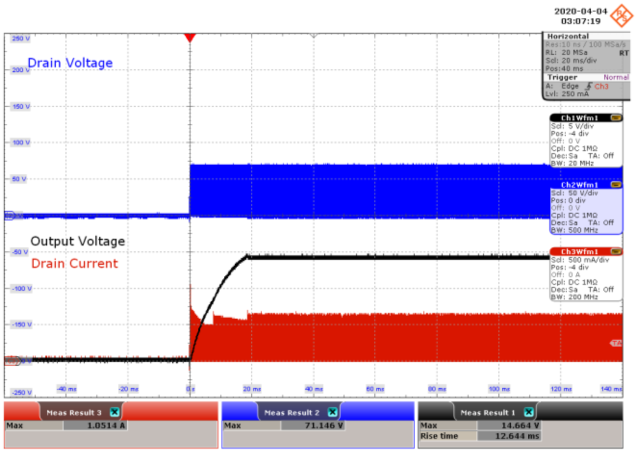

Figure 43 – 60 VDC Input.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{DS}, 50 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 71.146 V, $I_{DS(MAX)}$ = 1.0514 A.
$V_{OUT(MAX)}$ = 14.664 V.

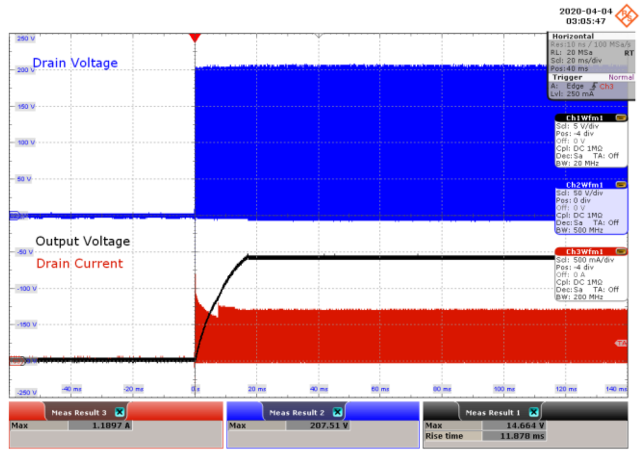

Figure 44 – 200 VDC Input.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{DS}, 50 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 207.51 V, $I_{DS(MAX)}$ = 1.1897 A.
$V_{OUT(MAX)}$ = 14.664 V.

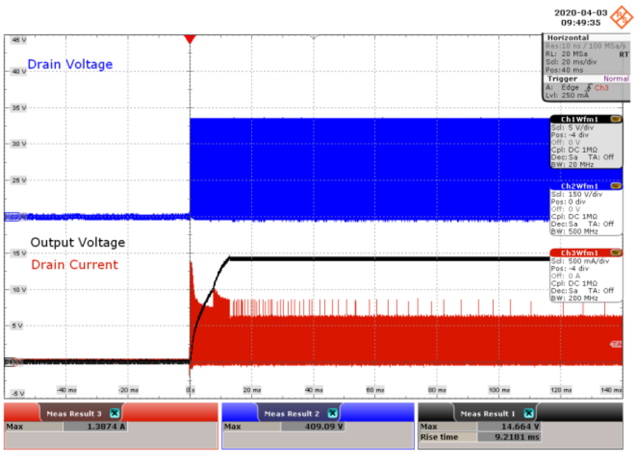

Figure 45 – 400 VDC Input.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{DS}, 150 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 409.09 V, $I_{DS(MAX)}$ = 1.3874 A.
$V_{OUT(MAX)}$ = 14.664 V.

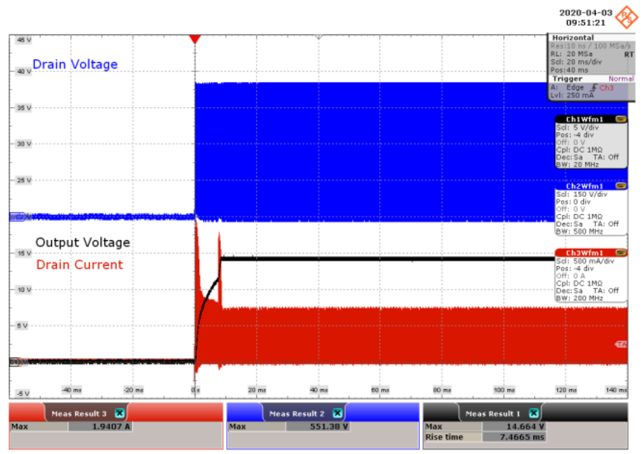

Figure 46 – 550 VDC Input.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{DS}, 150 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 551.38 V, $I_{DS(MAX)}$ = 1.9407 A.
$V_{OUT(MAX)}$ = 14.664 V.

9.2.2.3 0% Load CC

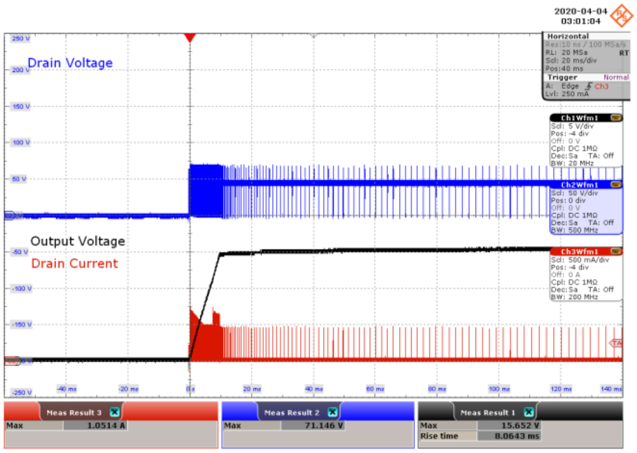

Figure 47 – 60 VDC Input.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{DS}, 50 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 71.146 V, $I_{DS(MAX)}$ = 1.0514 A.
$V_{OUT(MAX)}$ = 15.652 V.

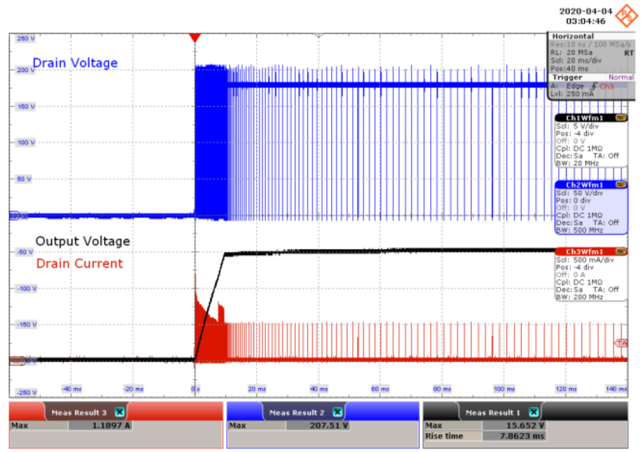

Figure 48 – 200 VDC Input.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{DS}, 50 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 207.51 V, $I_{DS(MAX)}$ = 1.1897 A.
$V_{OUT(MAX)}$ = 15.652 V.

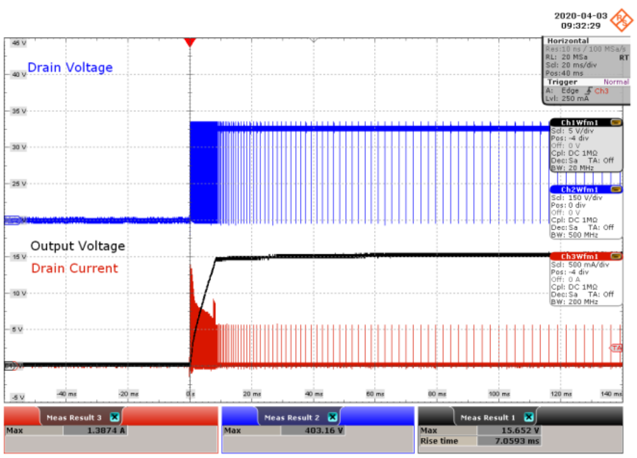

Figure 49 – 400 VDC Input.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{DS}, 150 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 403.16 V, $I_{DS(MAX)}$ = 1.3874 A.
$V_{OUT(MAX)}$ = 15.652 V.

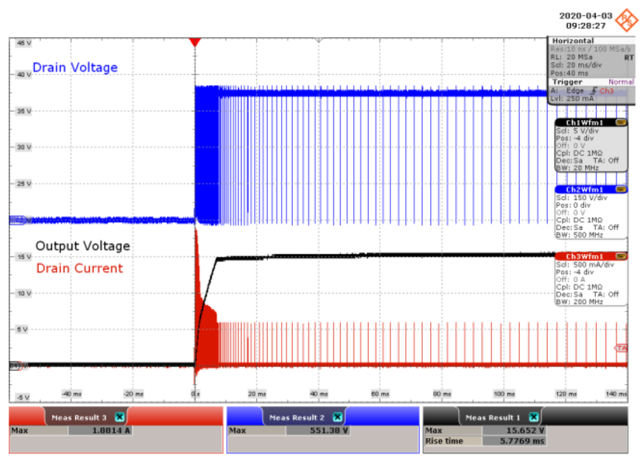

Figure 50 – 550 VDC Input.
CH1: V_{OUT}, 5 V / div., 20 ms / div.
CH2: V_{DS}, 150 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 551.38 V, $I_{DS(MAX)}$ = 1.8814 A.
$V_{OUT(MAX)}$ = 15.652 V.

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9.2.2.4 0% Load CR

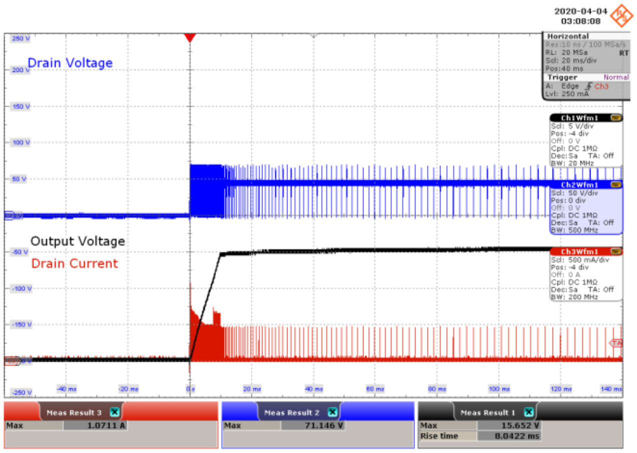

Figure 51 – 60 VDC Input.
CH1: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH2: $V_{DS,}$ 50 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 71.146 V, $I_{DS(MAX)}$ = 1.0711 A.
$V_{OUT(MAX)}$ = 15.652 V.

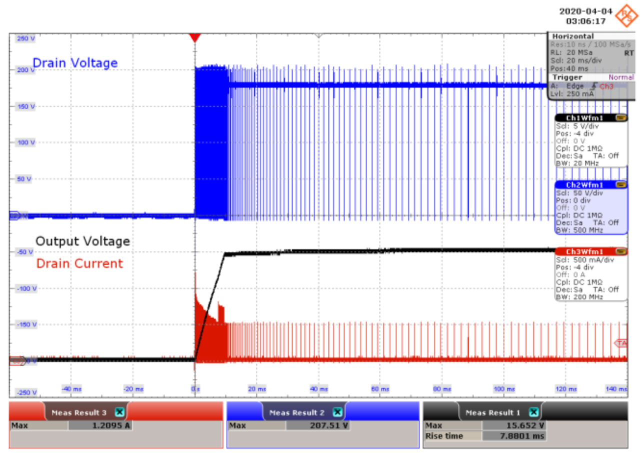

Figure 52 – 200 VDC Input.
CH1: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH2: $V_{DS,}$ 50 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 207.51 V, $I_{DS(MAX)}$ = 1.2095 A.
$V_{OUT(MAX)}$ = 15.652 V.

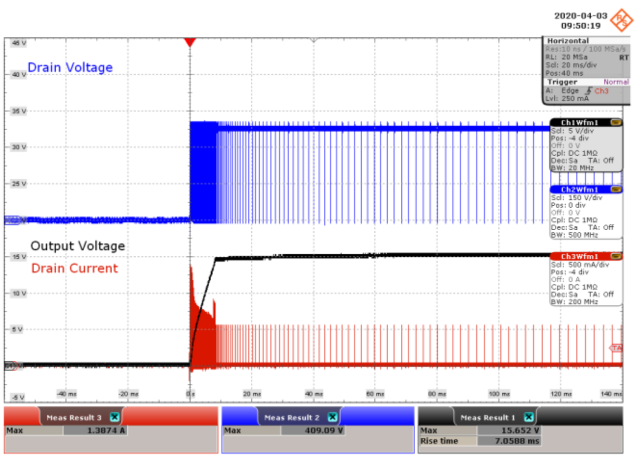

Figure 53 – 400 VDC Input.
CH1: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH2: $V_{DS,}$ 150 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 409.09 V, $I_{DS(MAX)}$ = 1.3874 A.
$V_{OUT(MAX)}$ = 15.652 V.

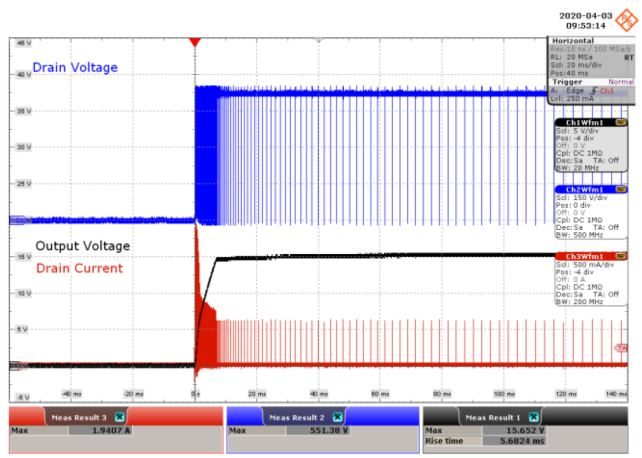

Figure 54 – 550 VDC Input.
CH1: $V_{OUT,}$ 5 V / div., 20 ms / div.
CH2: $V_{DS,}$ 150 V / div., 20 ms / div.
CH3: I_{DS}, 500 mA / div., 20 ms / div.
$V_{DS(MAX)}$ = 551.38 V, $I_{DS(MAX)}$ = 1.9407 A.
$V_{OUT(MAX)}$ = 15.652 V.

9.2.3 Free Wheeling Diode Voltage at Normal Operation

9.2.3.1 100% Load CC

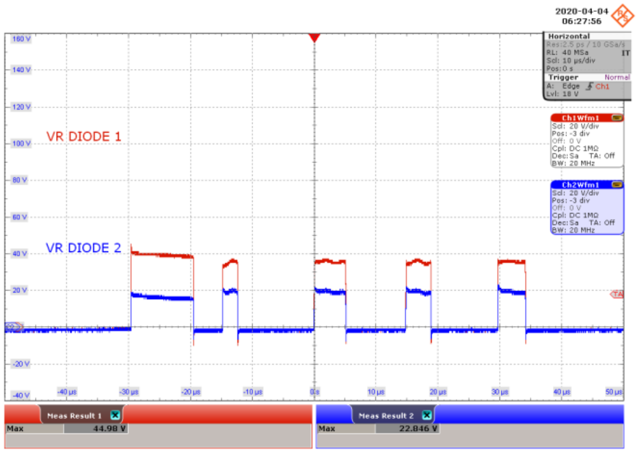

Figure 55 – 60 VDC Input.
CH1: $V_{R,DIODE1}$, 20 V / div., 10 µs / div.
CH2: $V_{R,DIODE2}$, 20 V / div., 10 µs / div.
PIV_1 = 44.98 V, PIV_2 = 22.846 V.

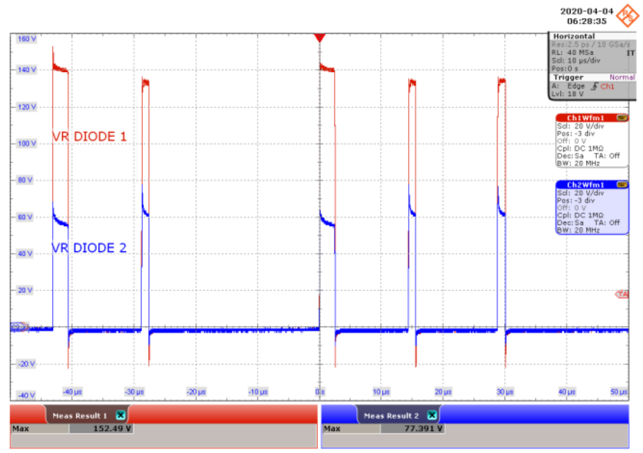

Figure 56 – 200 VDC Input.
CH1: $V_{R,DIODE1}$, 20 V / div., 10 µs / div.
CH2: $V_{R,DIODE2}$, 20 V / div., 10 µs / div.
PIV_1 = 152.49 V, PIV_2 = 77.391 V.

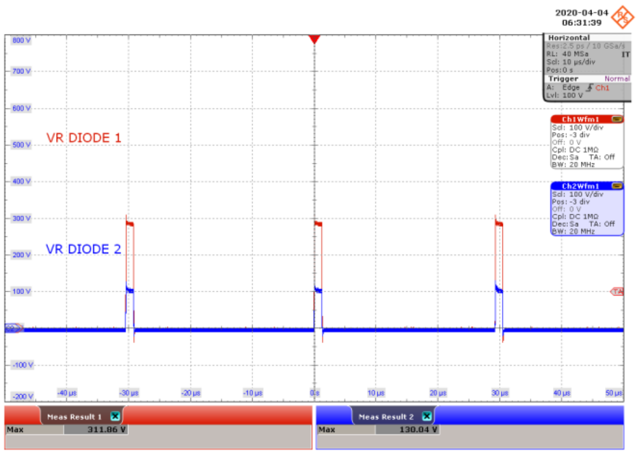

Figure 57 – 400 VDC Input.
CH1: $V_{R,DIODE1}$, 100 V / div., 10 µs / div.
CH2: $V_{R,DIODE2}$, 100 V / div., 10 µs / div.
PIV_1 = 311.86 V, PIV_2 = 130.04 V.

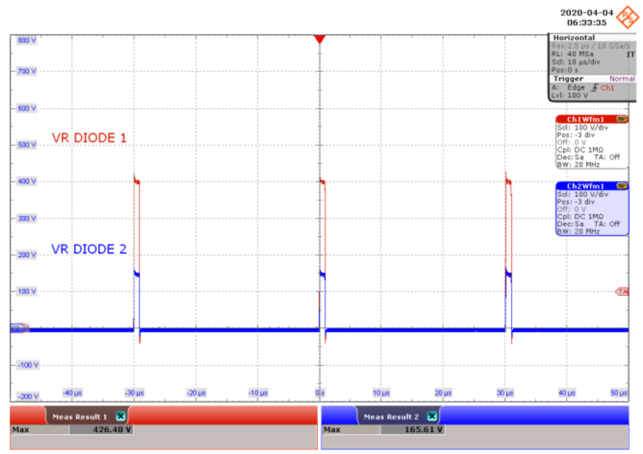

Figure 58 – 550 VDC Input.
CH1: $V_{R,DIODE1}$, 100 V / div., 10 µs / div.
CH2: $V_{R,DIODE2}$, 100 V / div., 10 µs / div.
PIV_1 = 426.48 V, PIV_2 = 165.61 V.

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9.2.3.2 0% Load CC

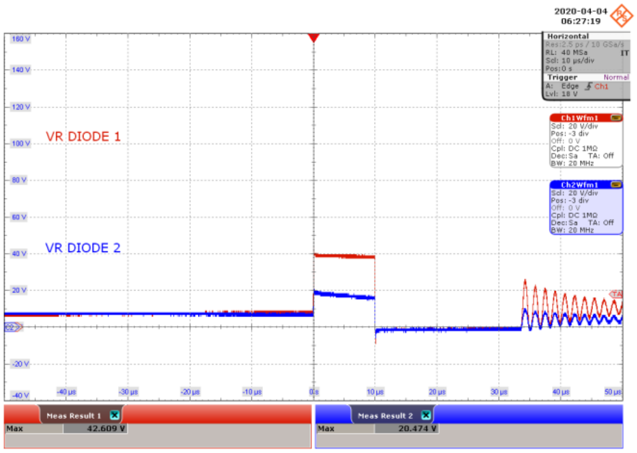

Figure 59 – 60 VDC Input.
CH1: $V_{R,DIODE1}$, 20 V / div., 10 μs / div.
CH2: $V_{R,DIODE2}$, 20 V / div., 10 μs / div.
PIV_1 = 42.609 V, PIV_2 = 20.474 V.

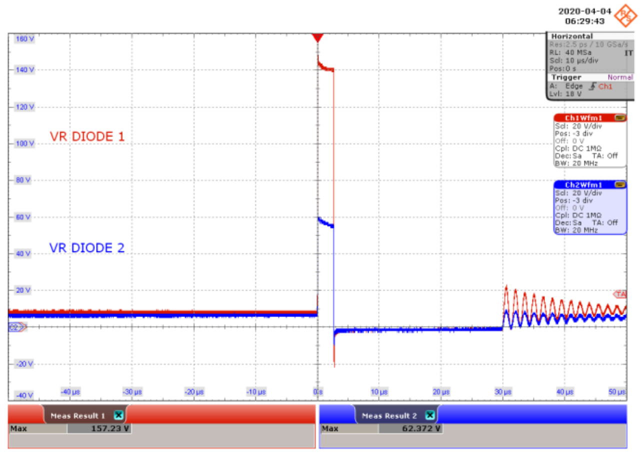

Figure 60 – 200 VDC Input.
CH1: $V_{R,DIODE1}$, 20 V / div., 10 μs / div.
CH2: $V_{R,DIODE2}$, 20 V / div., 10 μs / div.
PIV_1 = 157.23 V, PIV_2 = 62.372 V.

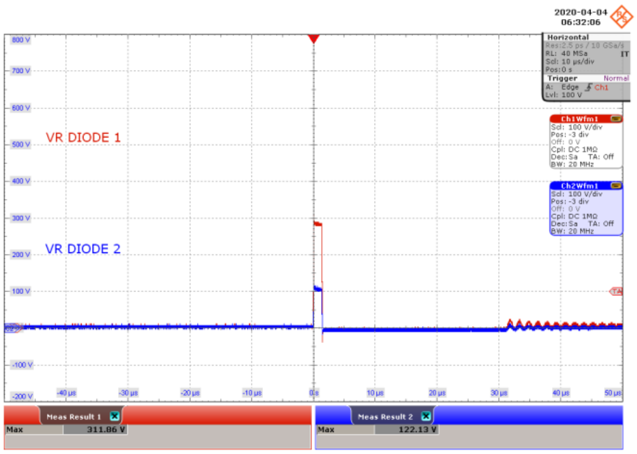

Figure 61 – 400 VDC Input.
CH1: $V_{R,DIODE1}$, 100 V / div., 10 μs / div.
CH2: $V_{R,DIODE2}$, 100 V / div., 10 μs / div.
PIV_1 = 311.86 V, PIV_2 = 122.13 V.

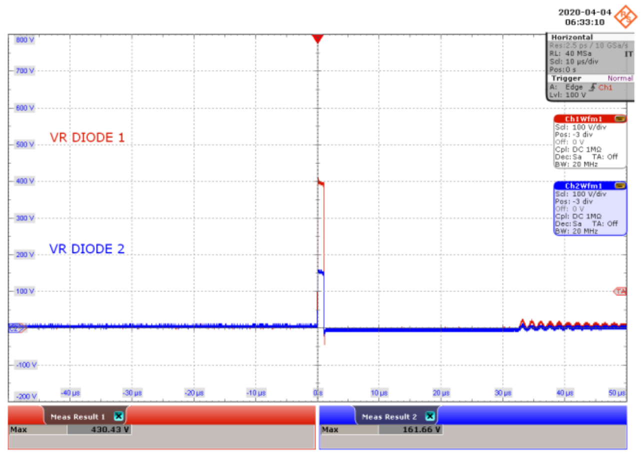

Figure 62 – 550 VDC Input.
CH1: $V_{R,DIODE1}$, 100 V / div., 10 μs / div.
CH2: $V_{R,DIODE2}$, 100 V / div., 10 μs / div.
PIV_1 = 430.43 V, PIV_2 = 161.66 V.

9.3 *Fault Conditions*

9.3.1 15 V Output Short-Circuit

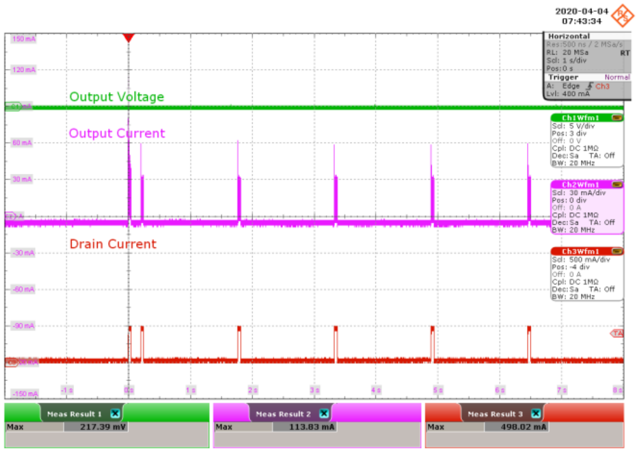

Figure 63 – 60 VDC Input. Output Short.
CH1: V_{OUT}, 5 V / div., 1 s / div.
CH2: I_{OUT}, 30 mA / div., 1 s / div.
CH3: I_{DS}, 500 mA / div., 1 s / div.
$V_{OUT(MAX)}$ = 217.39 mV.
$I_{OUT(MAX)}$ = 113.83 mA.
$I_{DS(MAX)}$ = 498.02 mA.

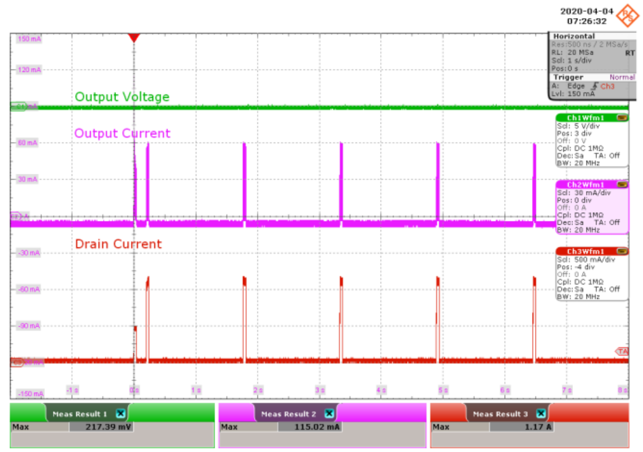

Figure 64 – 200 VDC Input. Output Short.
CH1: V_{OUT}, 5 V / div., 1 s / div.
CH2: I_{OUT}, 30 mA / div., 1 s / div.
CH3: I_{DS}, 500 mA / div., 1 s / div.
$V_{OUT(MAX)}$ = 217.39 mV.
$I_{OUT(MAX)}$ = 115.02 mA.
$I_{DS(MAX)}$ = 1.17 A.

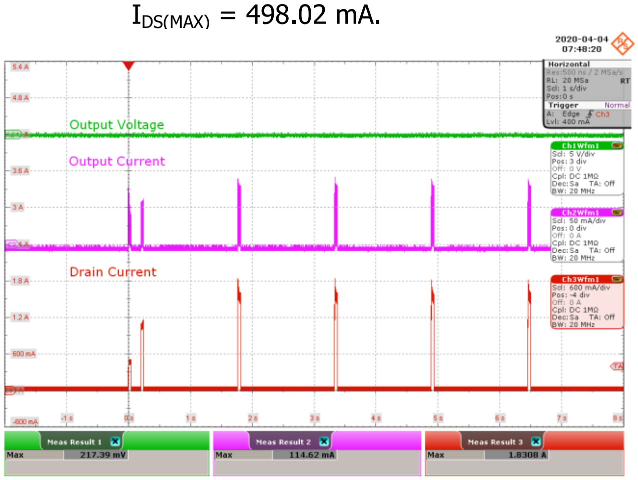

Figure 65 – 400 VDC Input. Output Short.
CH1: V_{OUT}, 5 V / div., 1 s / div.
CH2: I_{OUT}, 50 mA / div., 1 s / div.
CH3: I_{DS}, 600 mA / div., 1 s / div.
$V_{OUT(MAX)}$ = 217.39 mV.
$I_{OUT(MAX)}$ = 114.62 mA.
$I_{DS(MAX)}$ = 1.8308 A.

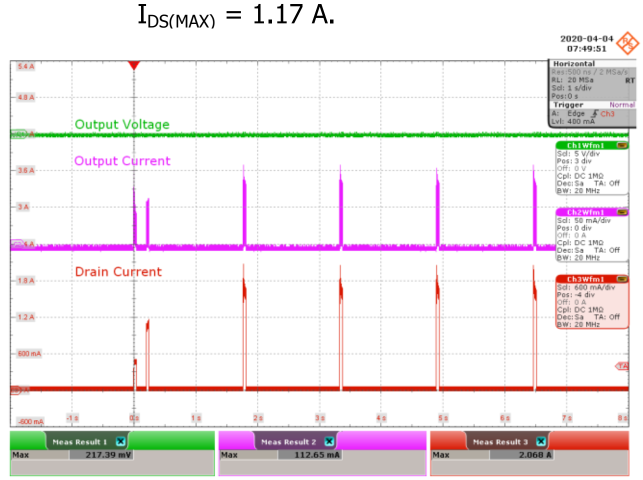

Figure 66 – 550 VDC Input. Output Short.
CH1: V_{OUT}, 5 V / div., 1 s / div.
CH2: I_{OUT}, 50 mA / div., 1 s / div.
CH3: I_{DS}, 600 mA / div., 1 s / div.
$V_{OUT(MAX)}$ = 217.39 mV.
$I_{OUT(MAX)}$ = 112.65 mA.
$I_{DS(MAX)}$ = 2.068 A.

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9.4 ***Output Voltage Ripple***

9.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

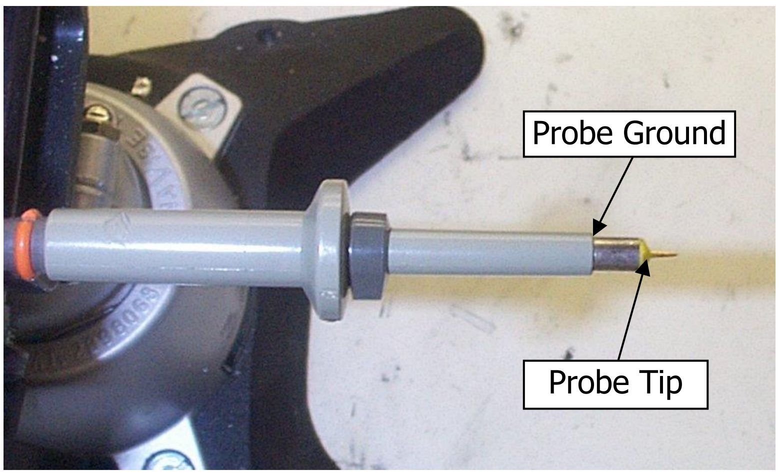

Figure 67 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

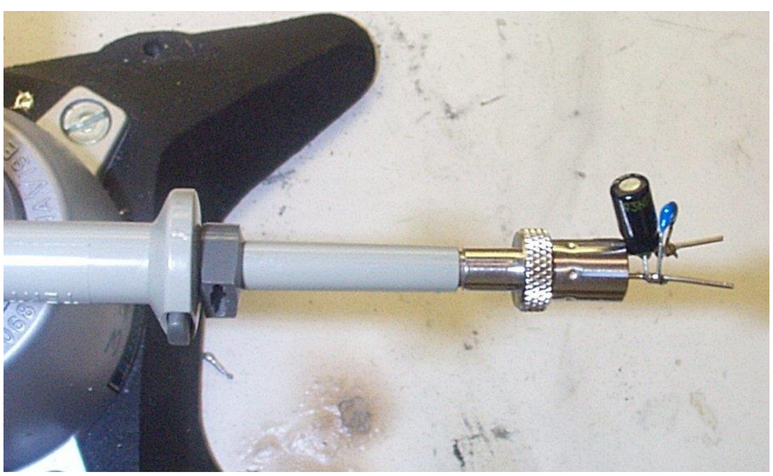

Figure 68 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

9.4.2 Measurement Results

Note: All ripple measurements were taken at PCB end.

9.4.2.1 100% Load Condition

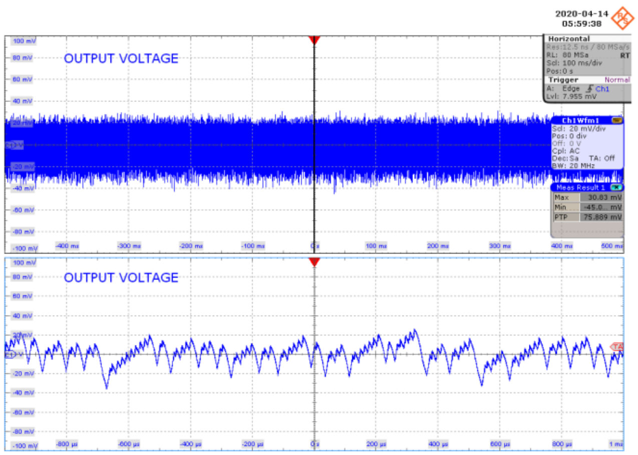

Figure 69 – 60 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 75.889 mV.

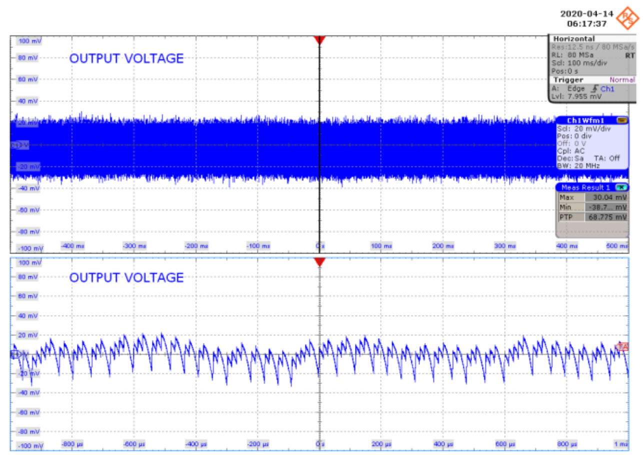

Figure 70 – 200 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 68.775 mV.

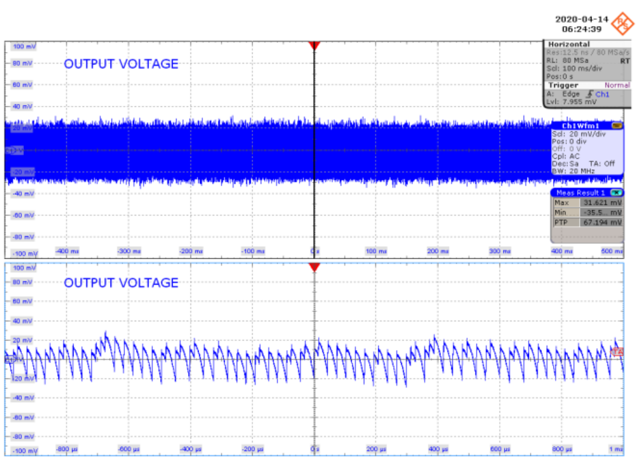

Figure 71 – 400 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 67.194 mV.

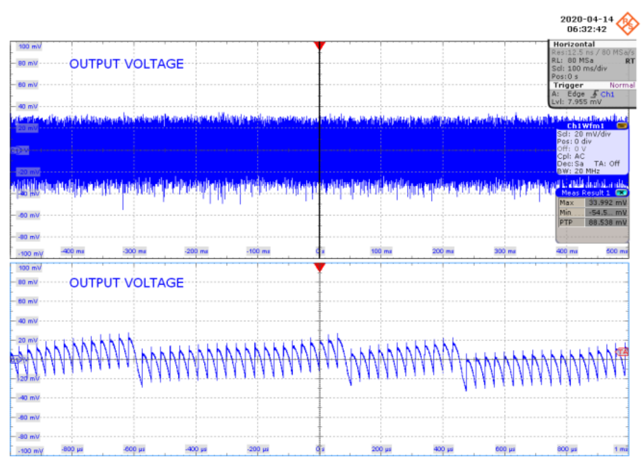

Figure 72 – 550 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 88.538 mV.

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9.4.2.2 90% Load Condition

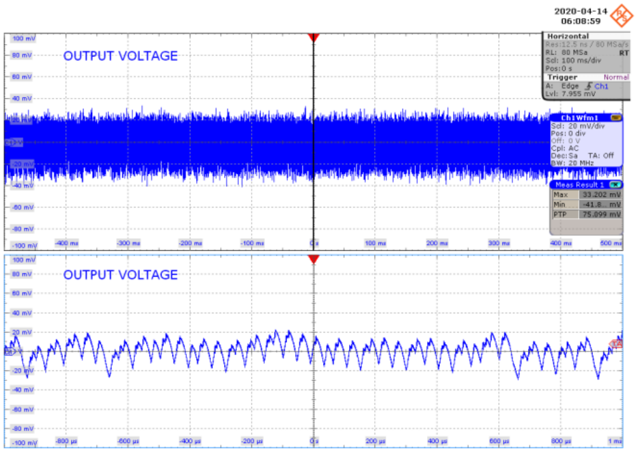

Figure 73 – 60 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 75.099 mV.

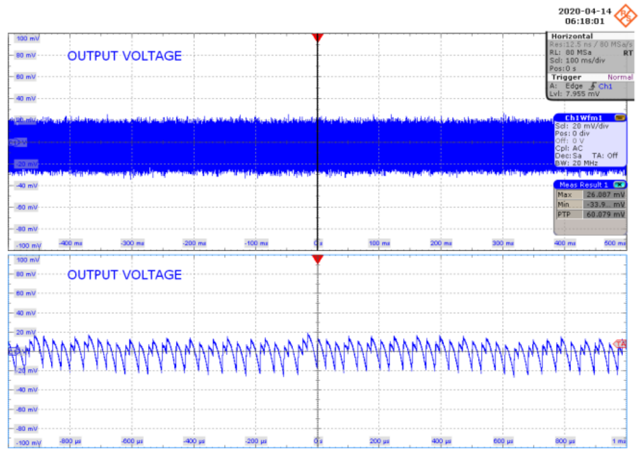

Figure 74 – 200 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 60.079 mV.

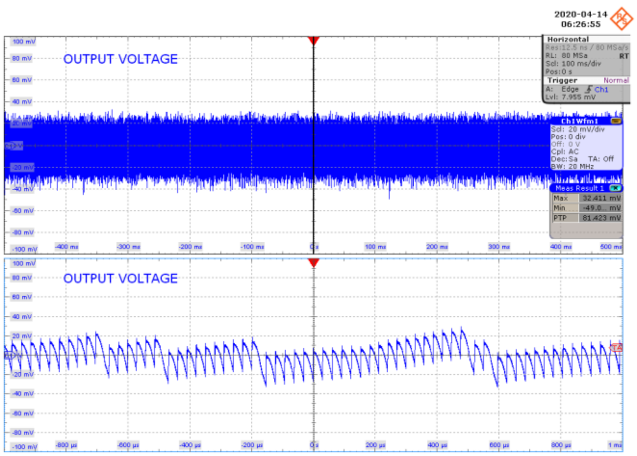

Figure 75 – 400 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 81.423 mV.

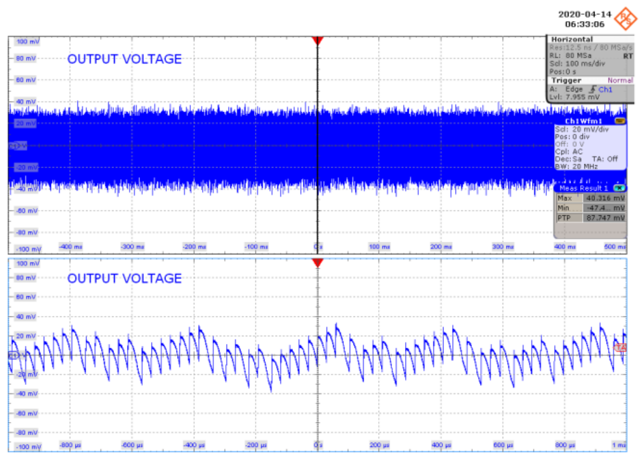

Figure 76 – 550 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 87.747 mV.

9.4.2.3 80% Load Condition

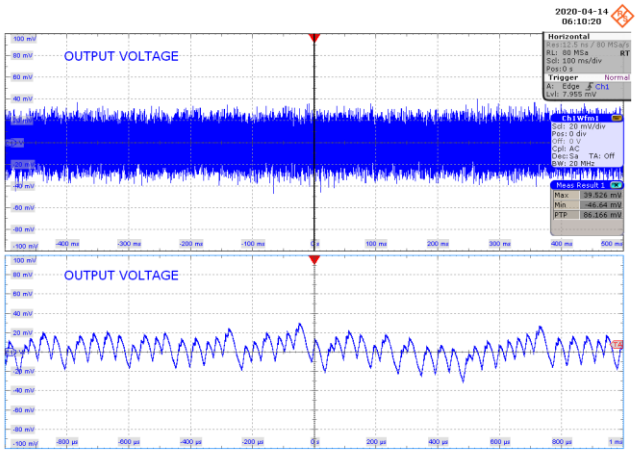

Figure 77 – 60 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 86.166 mV.

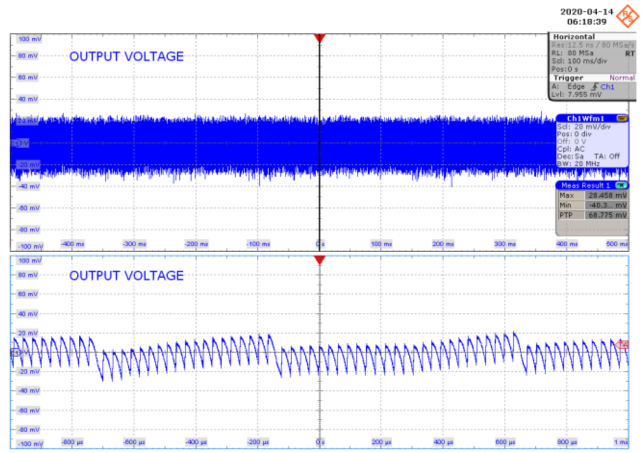

Figure 78 – 200 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 68.775 mV.

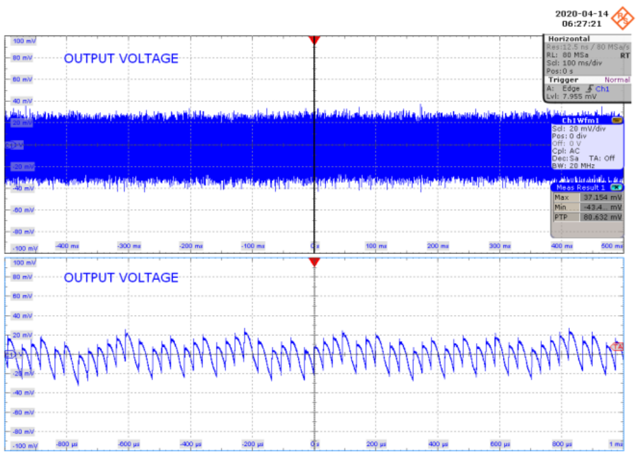

Figure 79 – 400 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 80.632 mV.

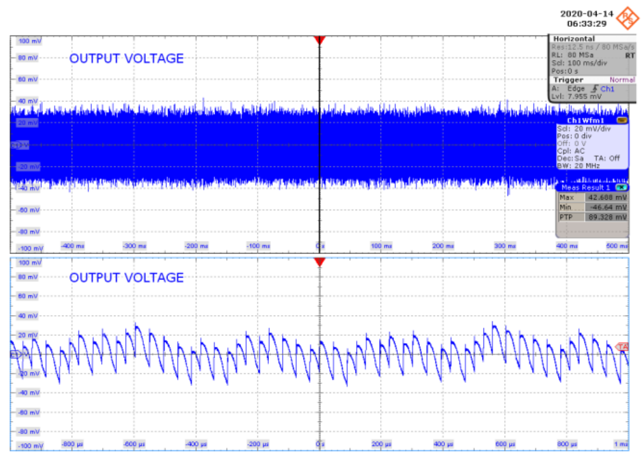

Figure 80 – 550 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 89.328 mV.

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9.4.2.4 70% Load Condition

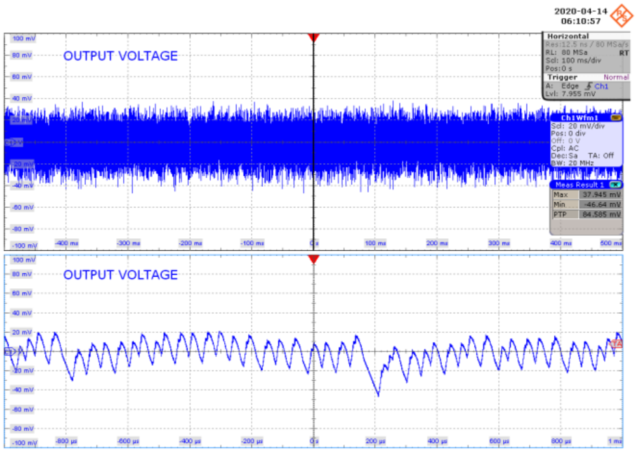

Figure 81 – 60 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 84.585 mV.

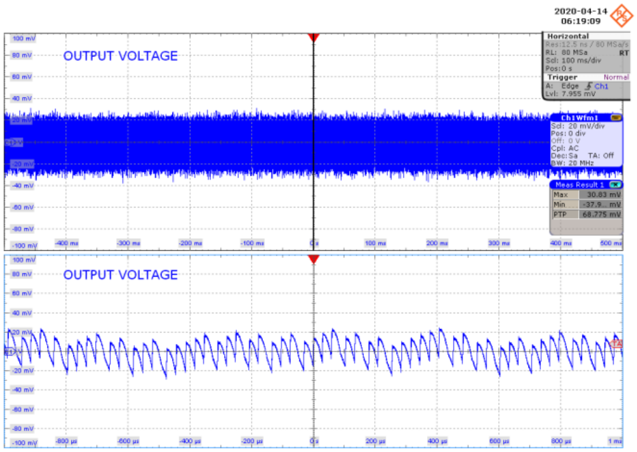

Figure 82 – 200 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 68.775 mV.

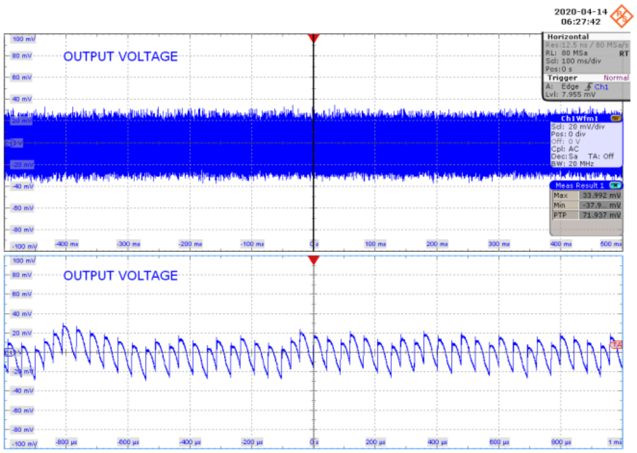

Figure 83 – 400 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 71.937 mV.

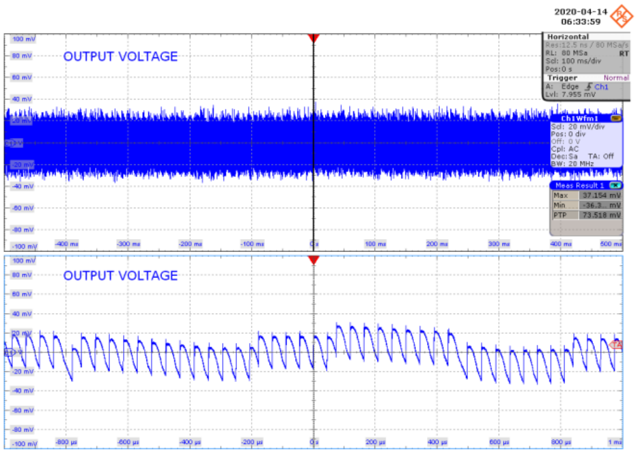

Figure 84 – 550 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 73.518 mV.

9.4.2.5 60% Load Condition

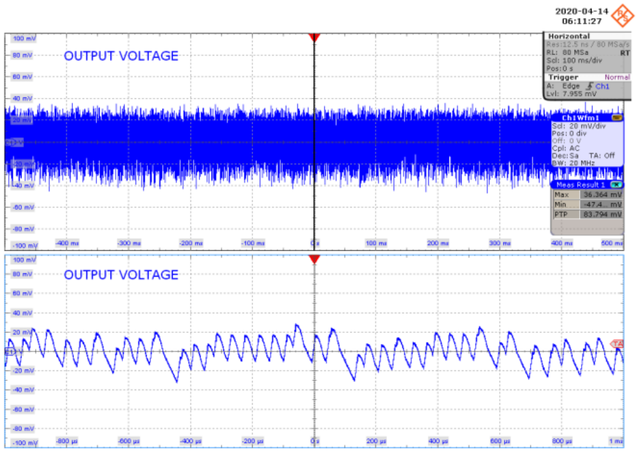

Figure 85 – 60 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 83.794 mV.

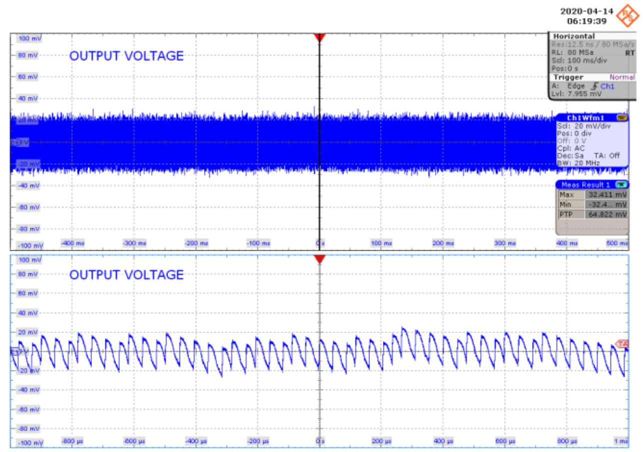

Figure 86 – 200 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 64.822 mV.

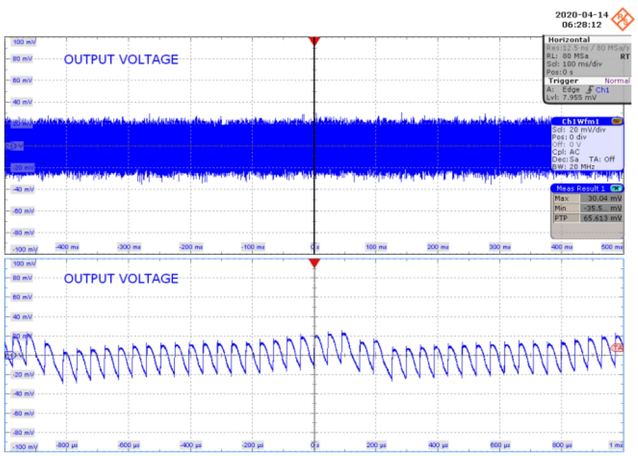

Figure 87 – 400 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 65.613 mV.

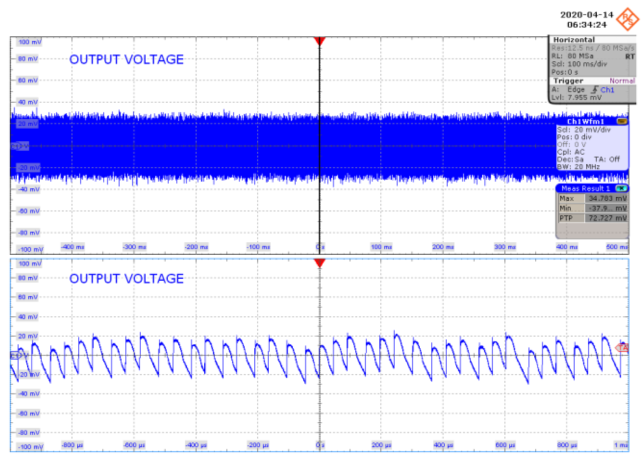

Figure 88 – 550 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 72.727 mV.

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9.4.2.6 50% Load Condition

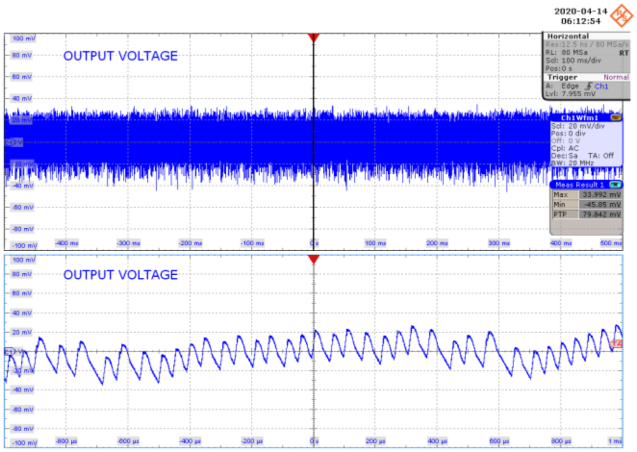

Figure 89 – 60 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 79.842 mV.

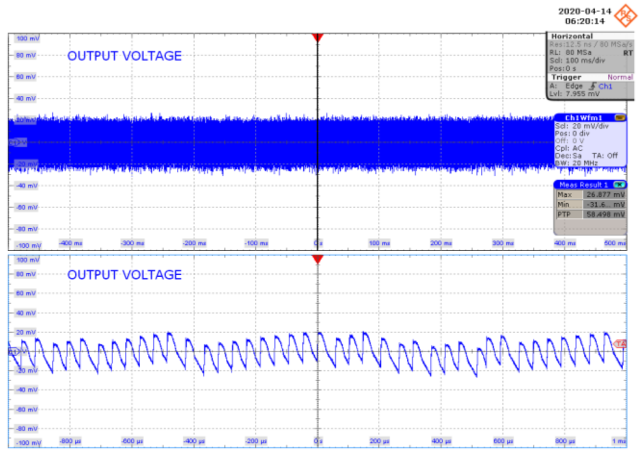

Figure 90 – 200 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 58.498 mV.

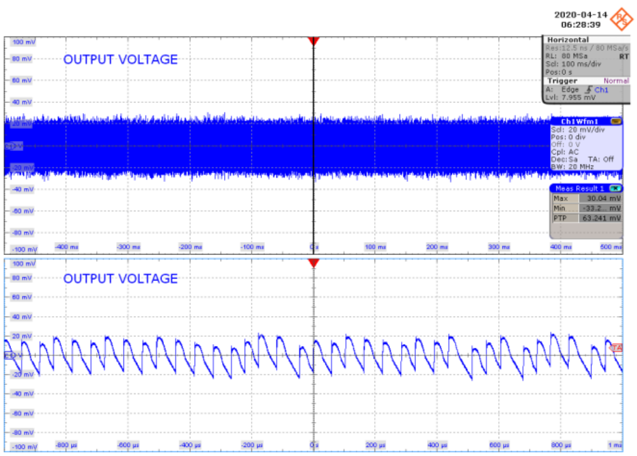

Figure 91 – 400 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 63.241 mV.

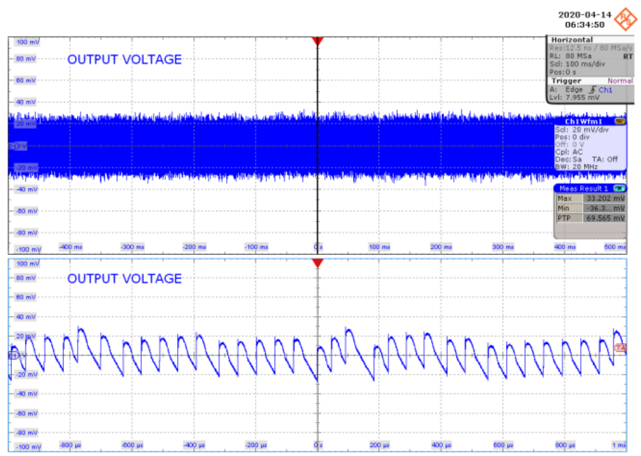

Figure 92 – 550 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 69.565 mV.

9.4.2.7 40% Load Condition

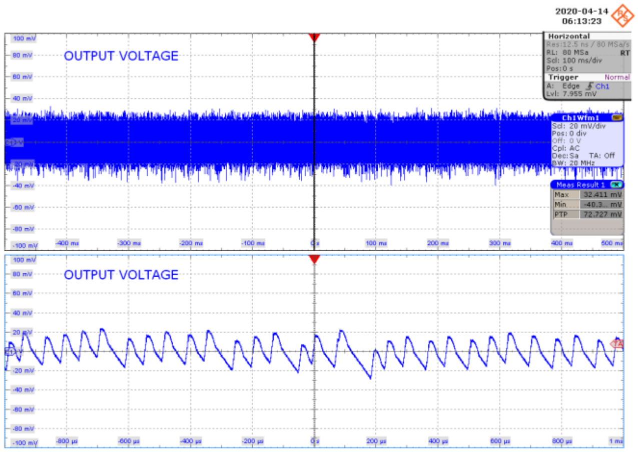

Figure 93 – 60 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 72.727 mV.

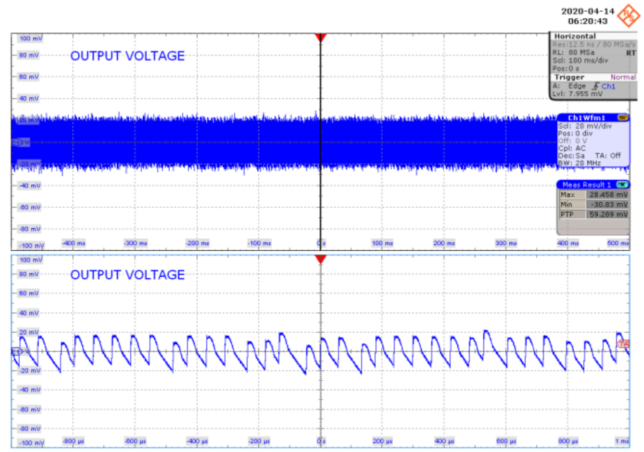

Figure 94 – 200 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 59.289 mV.

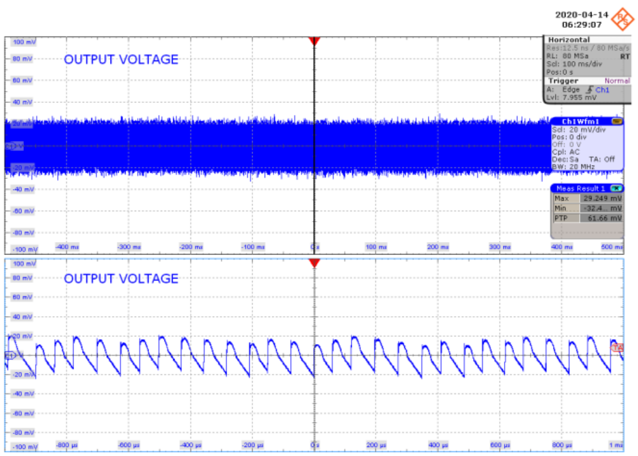

Figure 95 – 400 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 61.66 mV.

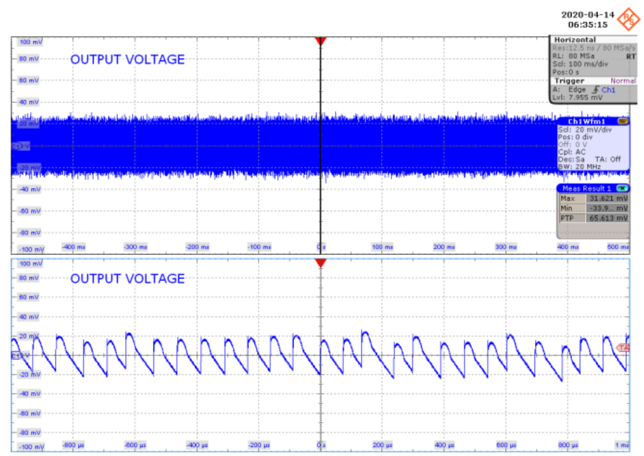

Figure 96 – 550 VDC Input.
CH1: $V_{OUT,}$ 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 65.613 mV.

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9.4.2.8 30% Load Condition

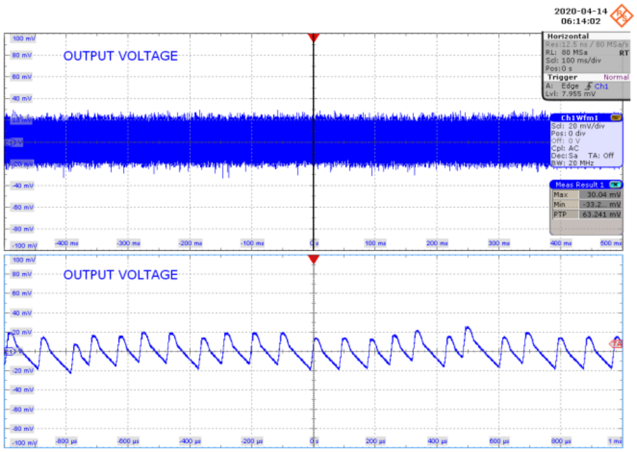

Figure 97 – 60 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 63.241 mV.

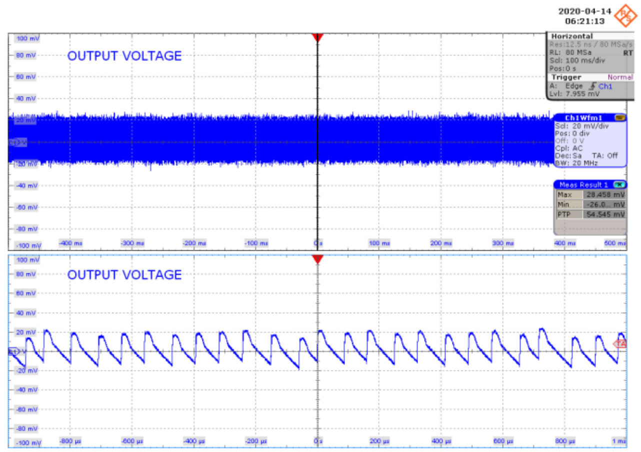

Figure 98 – 200 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 54.545 mV.

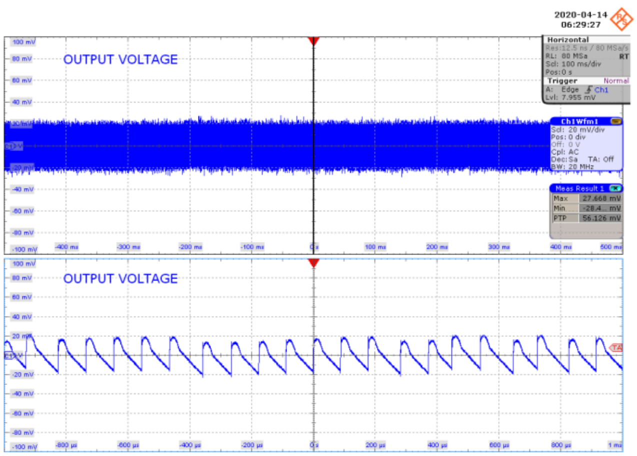

Figure 99 – 400 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 56.126 mV.

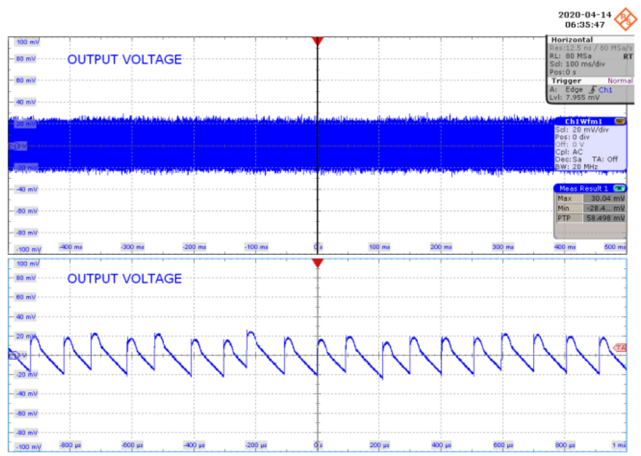

Figure 100 – 550 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 58.498 mV.

9.4.2.9 20% Load Condition

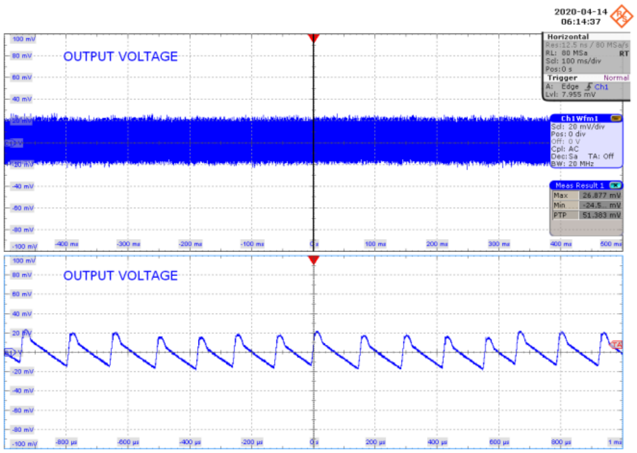

Figure 101 – 60 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 51.383 mV.

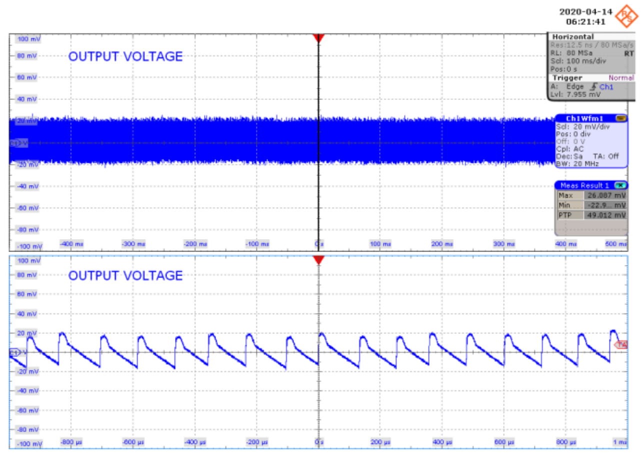

Figure 102 – 200 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 49.012 mV.

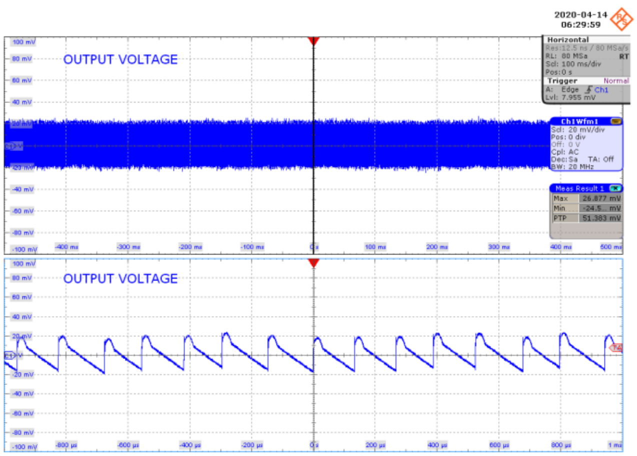

Figure 103 – 400 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 51.383 mV.

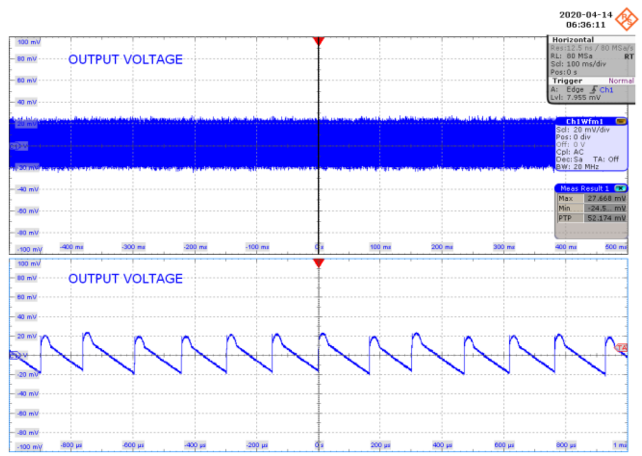

Figure 104 – 550 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 52.174 mV.

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9.4.2.10 10% Load Condition

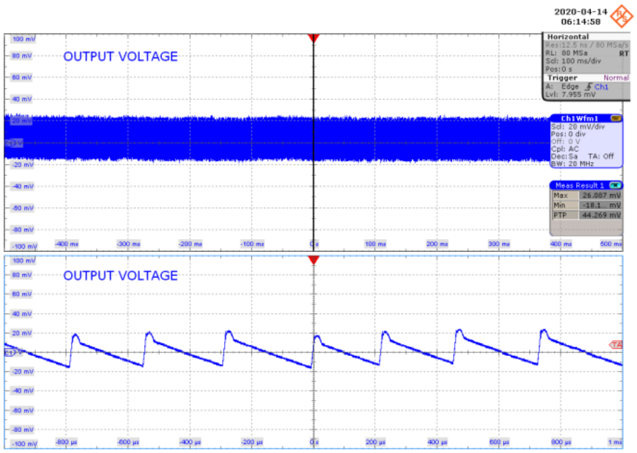

Figure 105 – 60 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 44.269 mV.

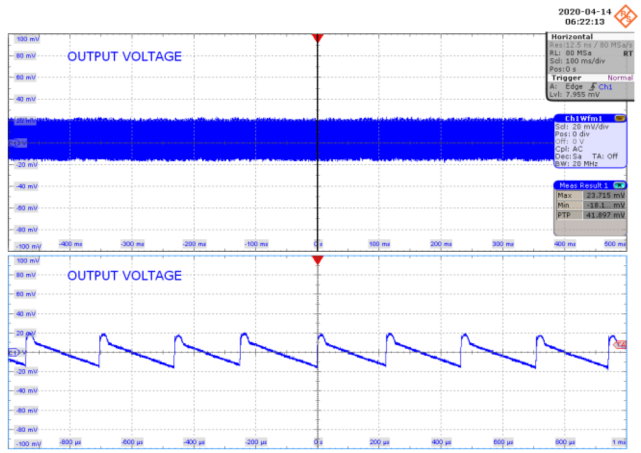

Figure 106 – 200 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 41.897 mV.

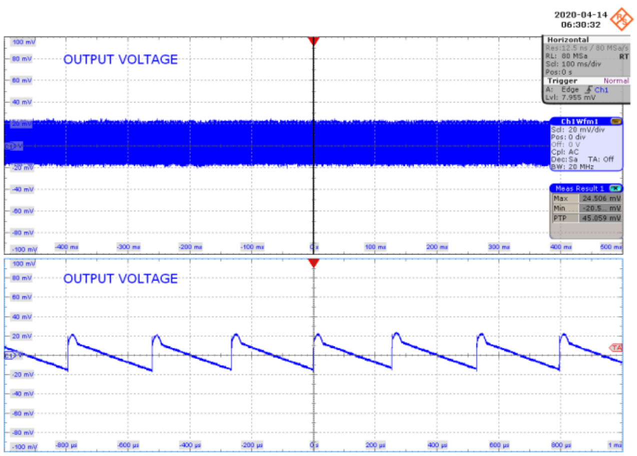

Figure 107 – 400 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 45.059 mV.

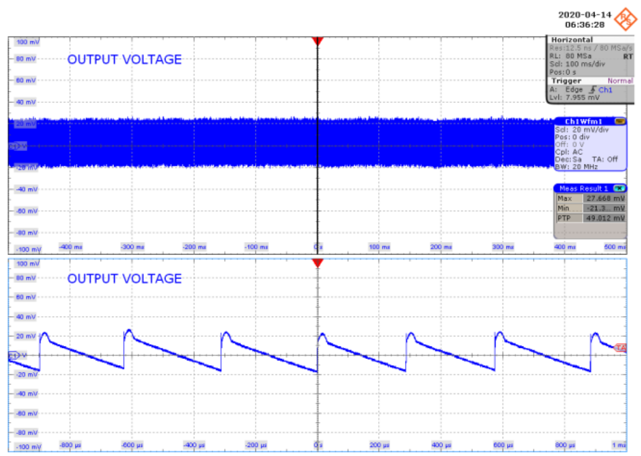

Figure 108 – 550 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 µs / div.
15 V Output Ripple = 49.012 mV.

9.4.2.11 0% Load Condition

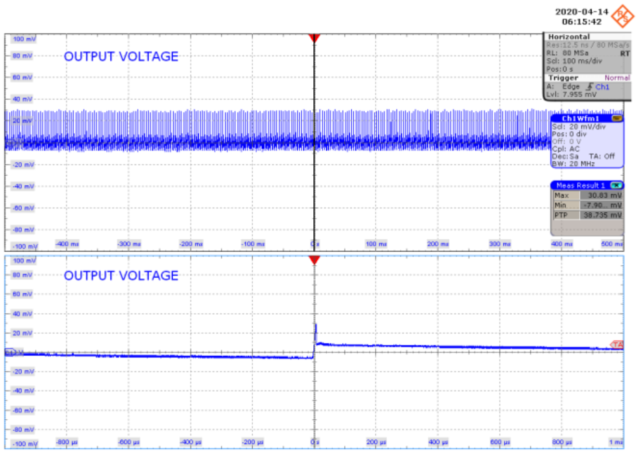

Figure 109 – 60 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 38.735 mV.

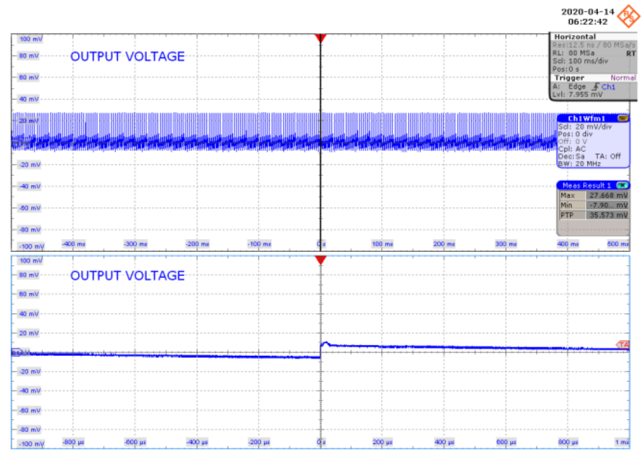

Figure 110 – 200 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 35.573 mV.

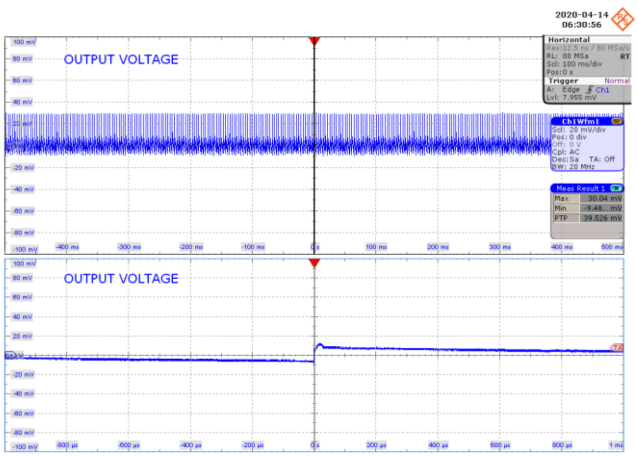

Figure 111 – 400 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 39.526 mV.

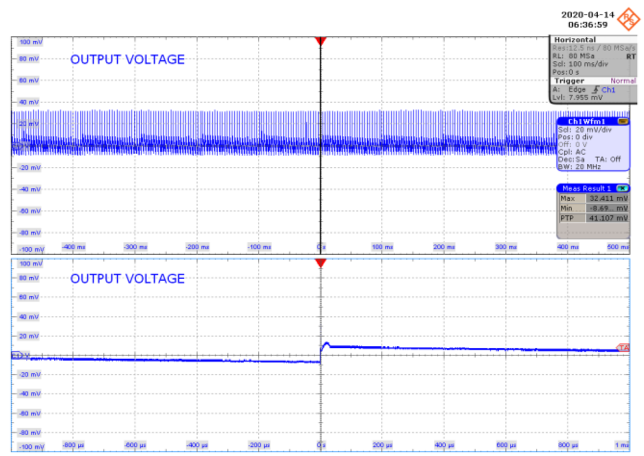

Figure 112 – 550 VDC Input.
CH1: V_{OUT}, 20 mV / div., 100 ms / div.
Zoom: 200 μs / div.
15 V Output Ripple = 41.107 mV.

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9.4.3 15 V Output Ripple Voltage Graph from 0% - 100% with 10% increment

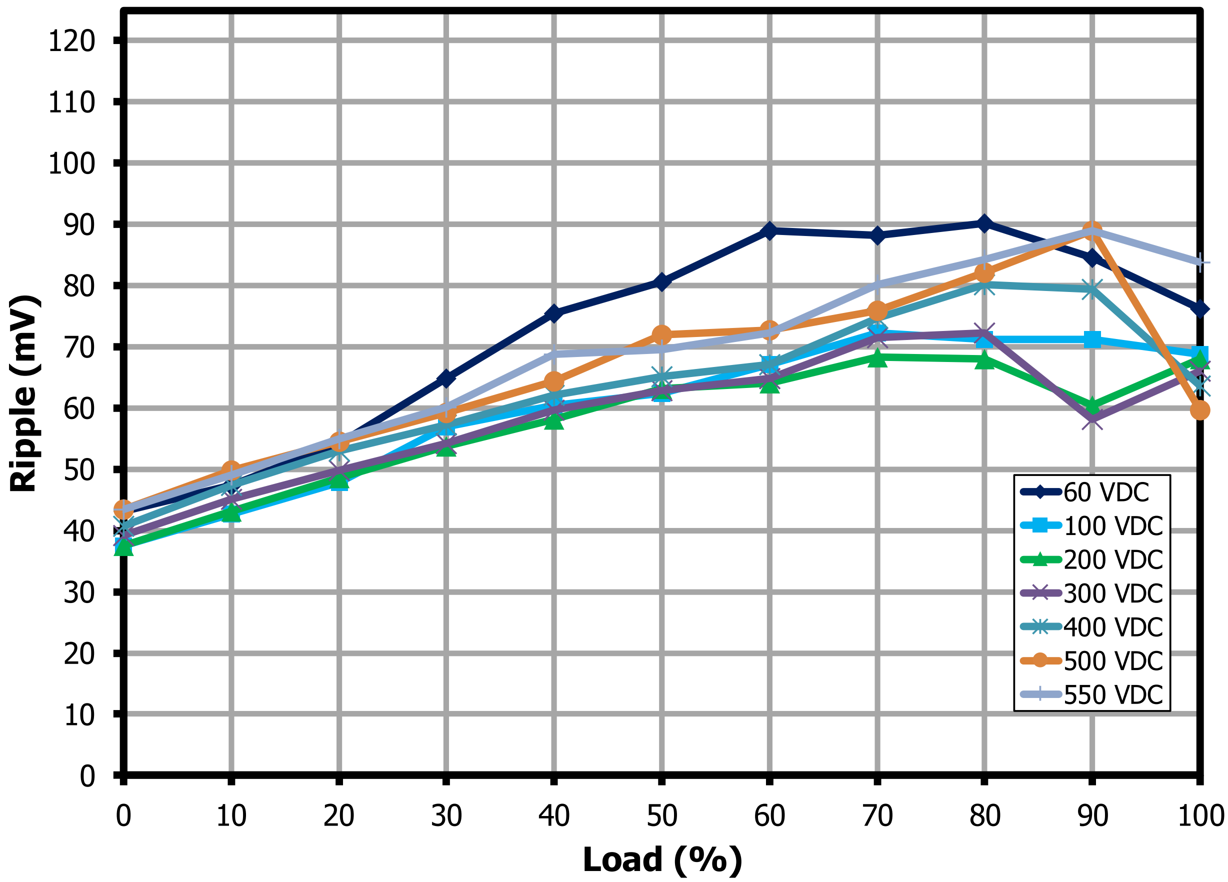

Figure 113 – 15 V Voltage Ripple (Measured at PCB End at Room Temperature).

9.5 *Brown-in and Brown-out*

Test Condition: 0-200Vdc and 200-0Vdc; 0.222Vdc/sec; CR mode

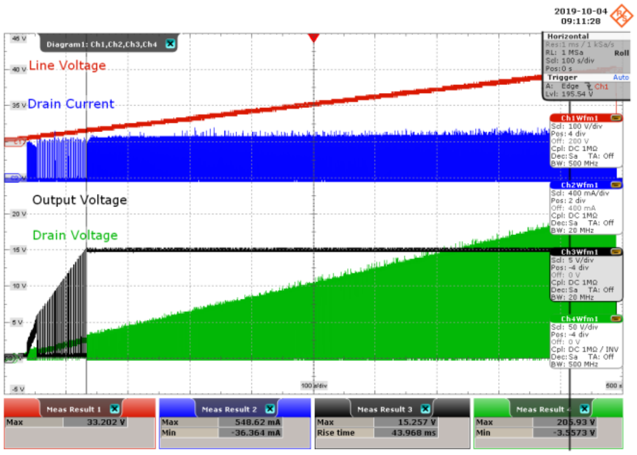

Figure 114 – Brown-In, Full Load.
CH1: $V_{LINE,}$ 100 V / div., 100 s / div.
CH2: $I_{DS,}$ 400 mA / div., 100 s / div.
CH3: $V_{OUT,}$ 5 V / div., 100 s / div.
CH4: $V_{DS,}$ 50 V / div., 100 s / div.
$V_{IN,UV}$ = 33.202 V.

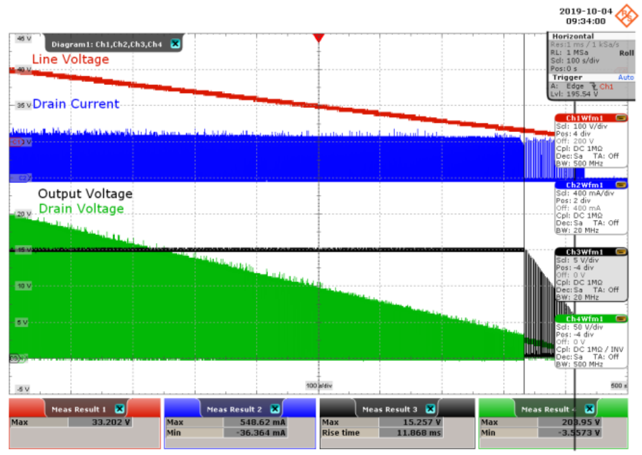

Figure 115 – Brown-Out, Full Load.
CH1: $V_{LINE,}$ 100 V / div., 100 s / div.
CH2: $I_{DS,}$ 400 mA / div., 100 s / div.
CH3: $V_{OUT,}$ 5 V / div., 100 s / div.
CH4: $V_{DS,}$ 50 V / div., 100 s / div.
$V_{IN,UV}$ = 33.202 V.

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10 Thermal Performance

10.1 *Thermal Performance at Room Temperature*

10.1.1 60 VDC at Room Temperature

Test Condition: 22°C ambient, soak time = 120 minutes, full load

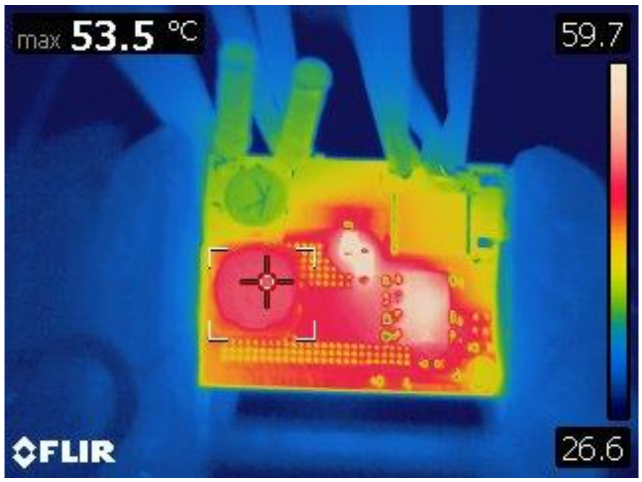

Figure 116 – Thermal Performance at 60 VDC Input.
L1 = 53.5 °C.

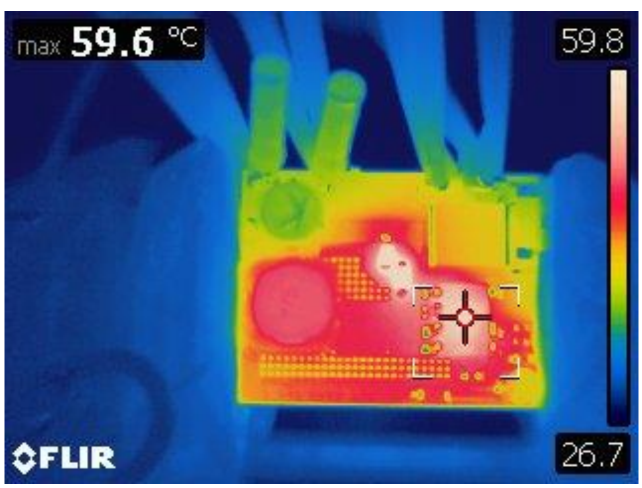

Figure 117 – Thermal Performance at 60 VDC Input.
U1 = 59.6 °C.

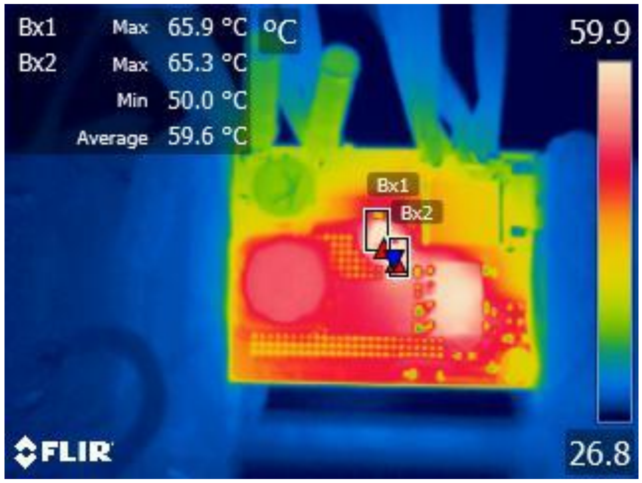

Figure 118 – Thermal Performance at 60 VDC Input.
D1 = 65.9 °C, D2 = 65.3 °C

Component	Temperature (°C)
Ambient	26
Inductor (L1)	53.5
LNK3206G (U1)	59.6
Freewheeling Diode (D1)	65.9
Freewheeling Diode (D2)	65.3

10.1.2 550 VDC at Room Temperature

Test Condition: 22°C ambient, soak time = 120 minutes, full load

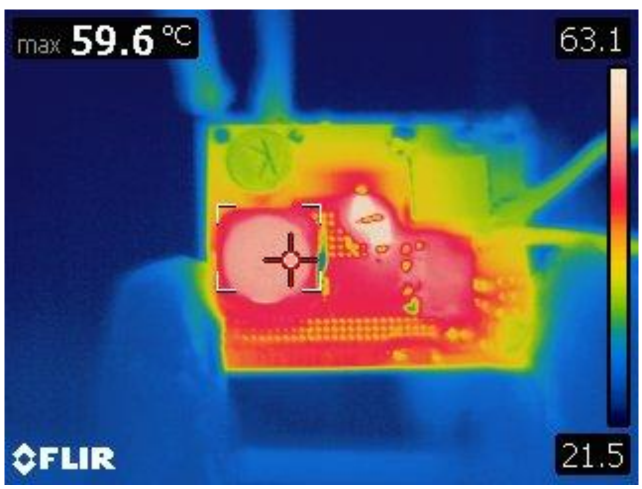

Figure 119 – Thermal Performance at 550 VDC Input.
L1 = 59.6 °C

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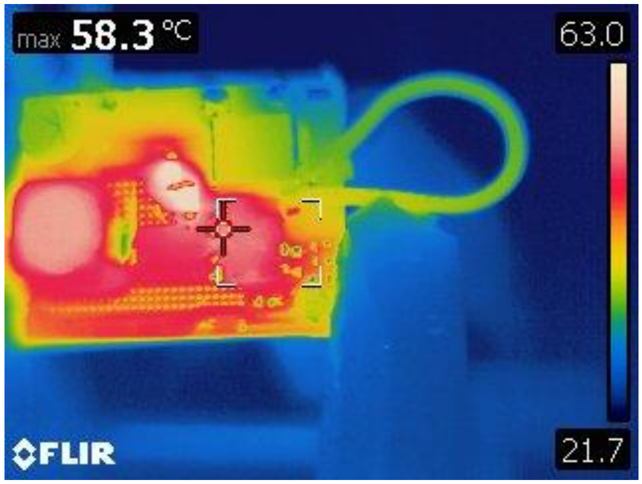

Figure 120 – Thermal Performance at 550 VDC Input.
U1 = 58.3 °C

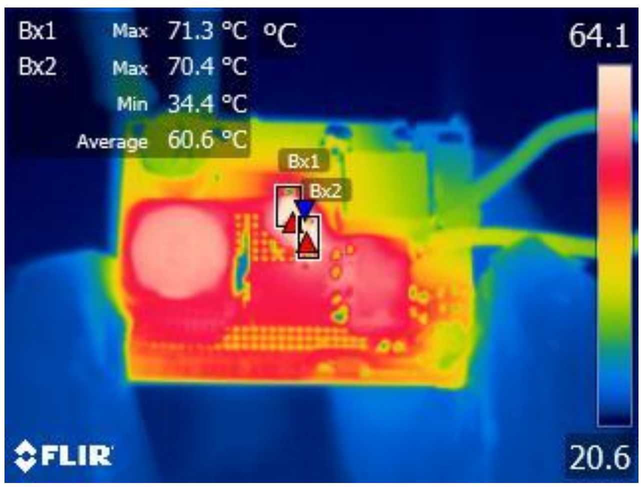

Figure 121 – Thermal Performance at 550 VDC Input.
D1 = 71.3 °C, D2 = 70.4 °C

Component	Temperature (°C)
Ambient	22
Inductor (L1)	59.6
LNK3206G (U1)	58.3
Freewheeling Diode (D1)	71.3
Freewheeling Diode (D2)	70.4

10.2 *Thermal Performance at 85°C*

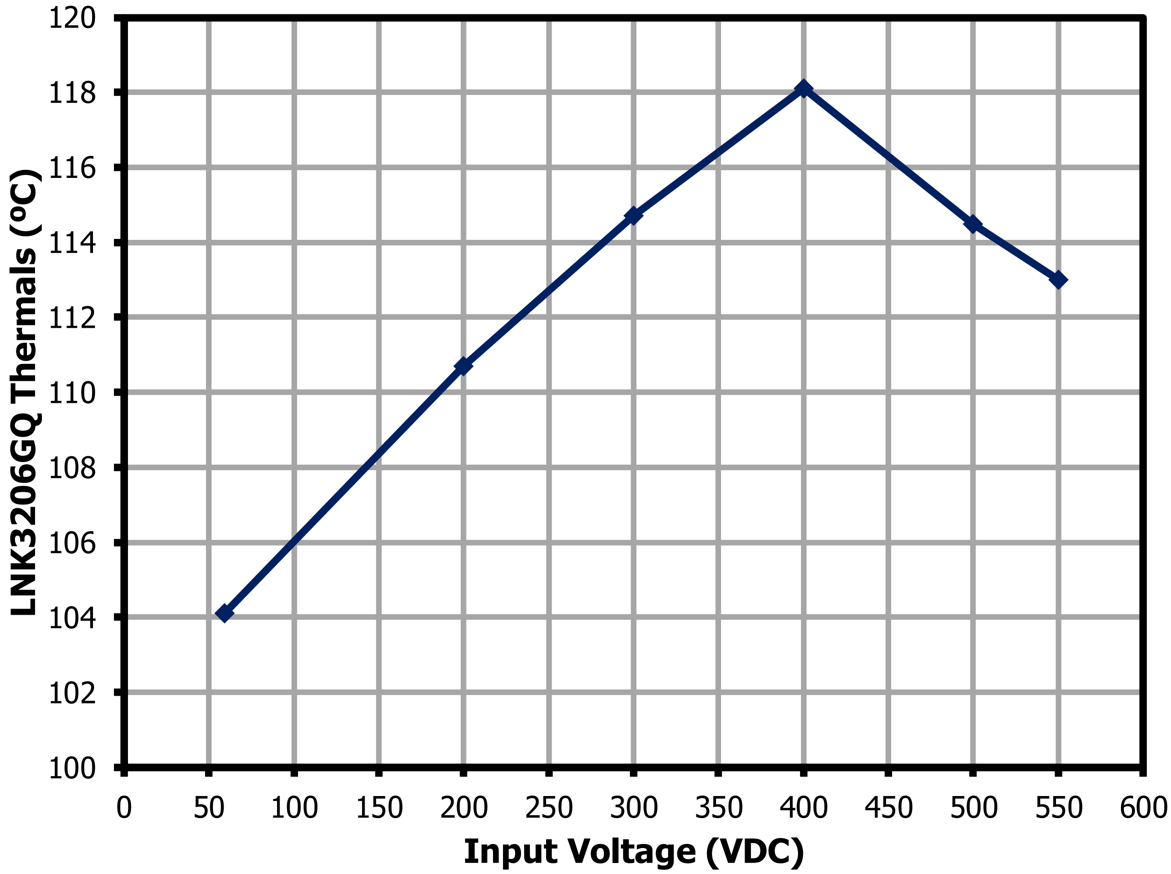

Figure 122 – Thermal Performance at 85°C.

Input Measurement			Output 1 Measurement				Temperature		
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Efficiency (%)	Ambient (Measured) (ºC)	IC @ Ambient (Measured) (ºC)	IC Temp at 85 ºC (Computed)
59.18	226.05	5.594	14.68	298.87	4.39	78.44	88.50	107.60	104.10
199.99	231.21	5.701	14.824	299.58	4.44	77.90	86.30	112	110.7
299.99	201.81	5.843	14.821	299.58	4.44	75.99	86.30	116.00	114.70
399.97	172.69	5.985	14.823	299.60	4.44	74.20	86.70	119.80	118.10
499.96	156.98	5.874	14.792	299.60	4.43	75.45	86.20	115.70	114.50
549.99	106.20	5.827	14.787	299.61	4.43	76.03	86.50	114.50	113.00

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11 Revision History

Date	Author	Revision	Description and Changes	Reviewed
29-APR-20	CMC/MAM	1.0	Initial Release.	Apps & Mktg
29-MAY-20	MAM	1.1	Board picture, F1 component and schematic change, Thermal measurements	Apps & Mktg

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